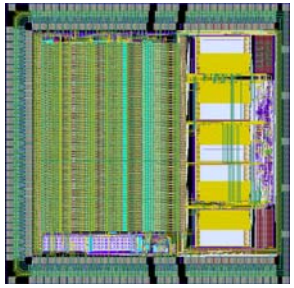
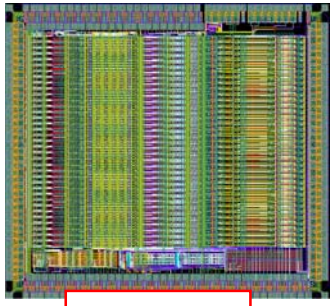
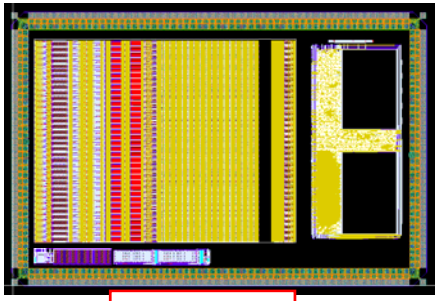


HaRDROC



SKIROC



SPIROC

Second generation Front-End ASICs for CALICE

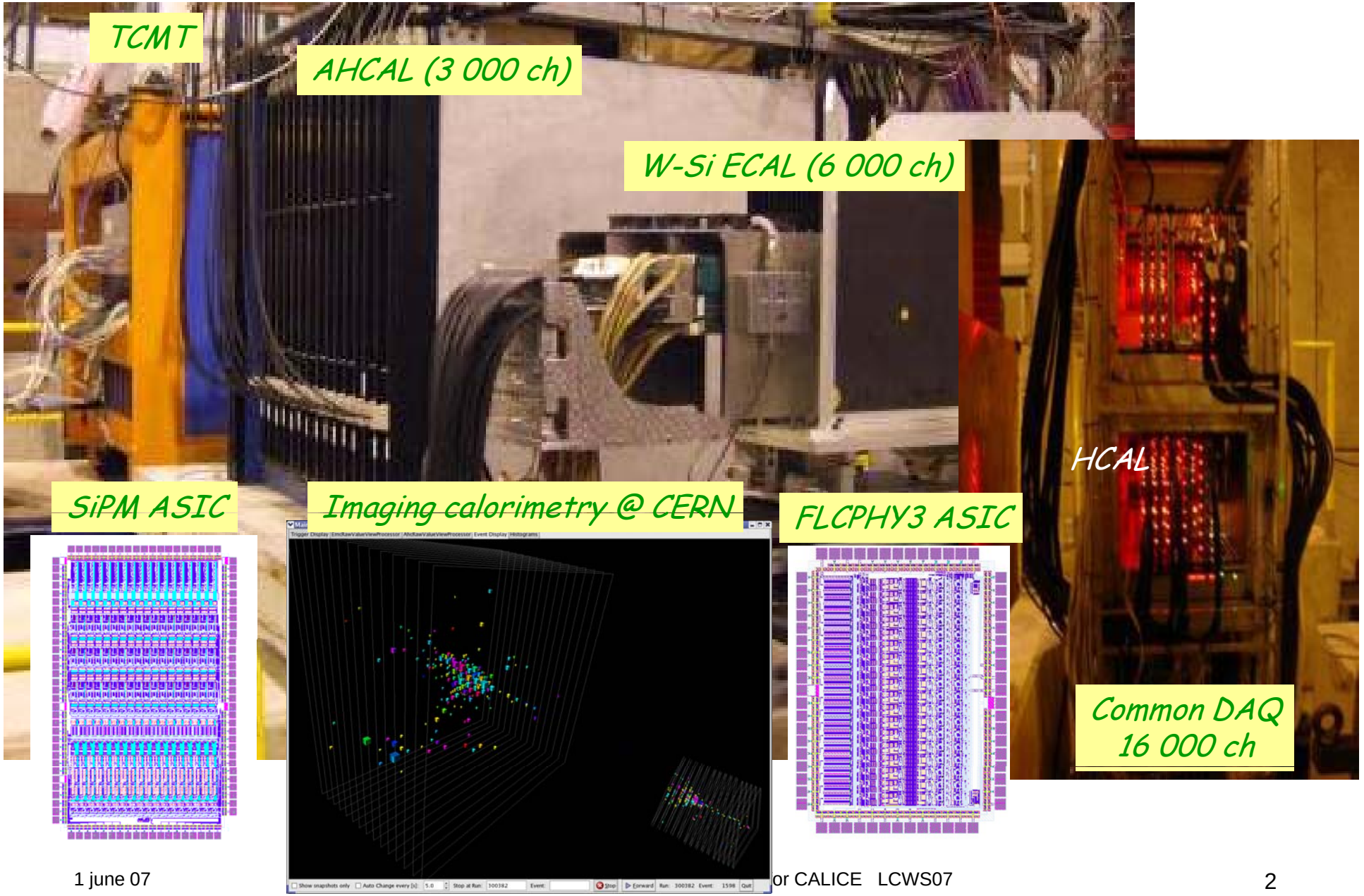
LCWS07 Hamburg

C. de La Taille

IN2P3/LAL Orsay

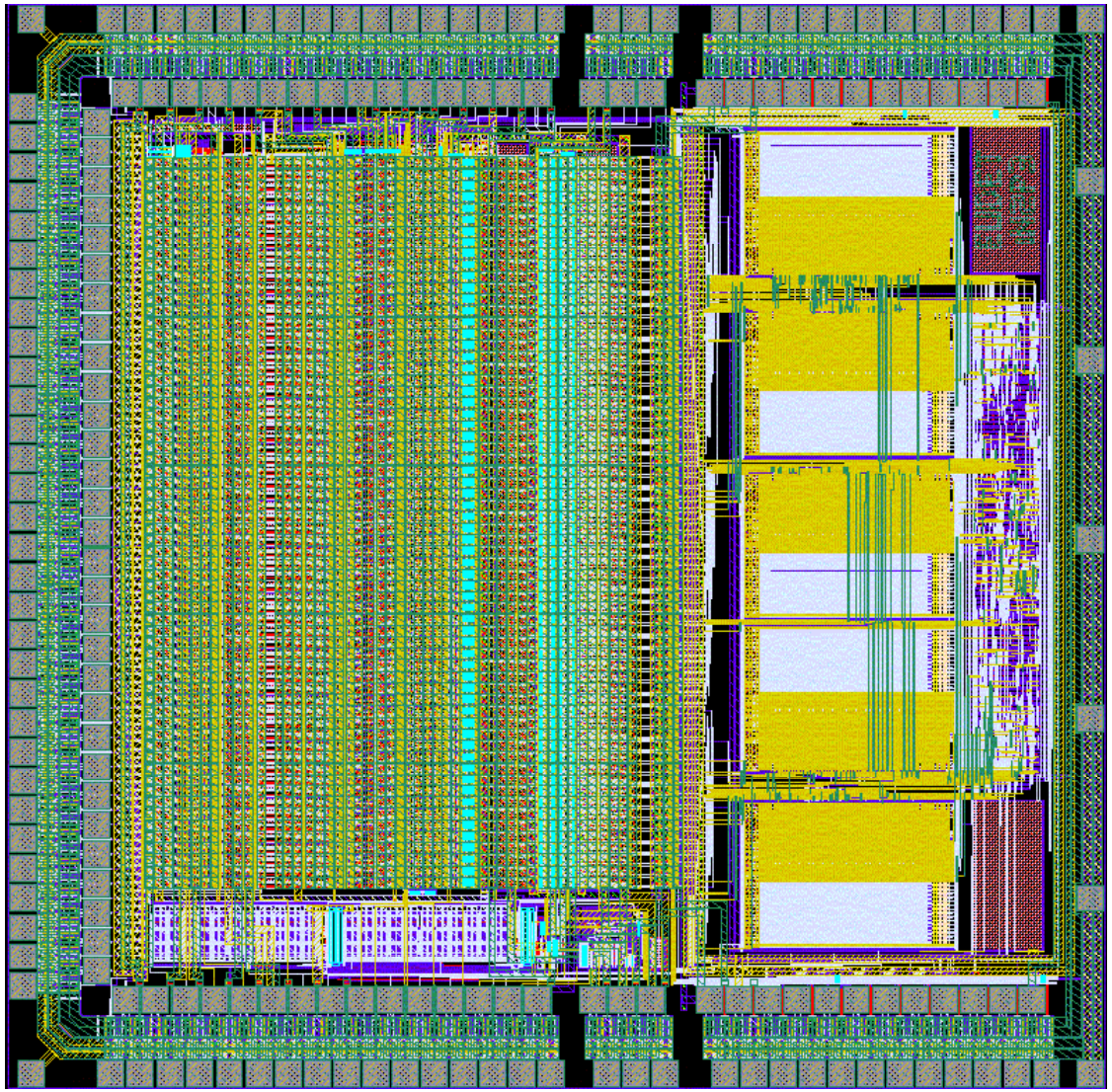
On behalf of the CALICE collaboration

CALICE Testbeam at CERN SPS

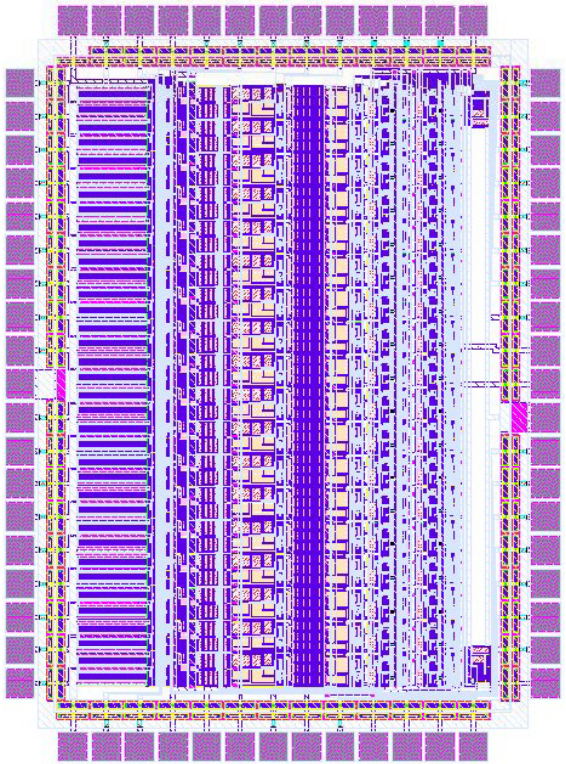


Next steps

HaRD_ROC (2006)

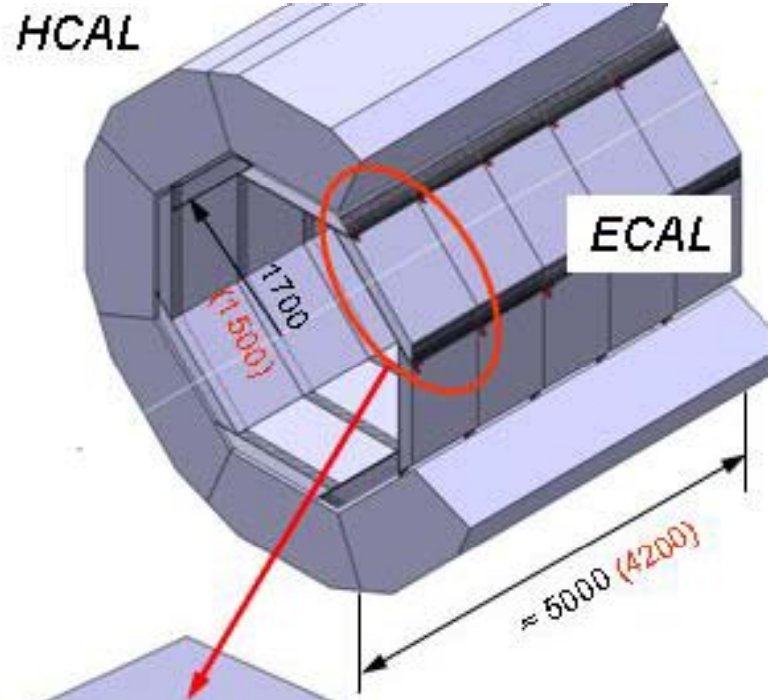


FLC_PHY3 (2003)

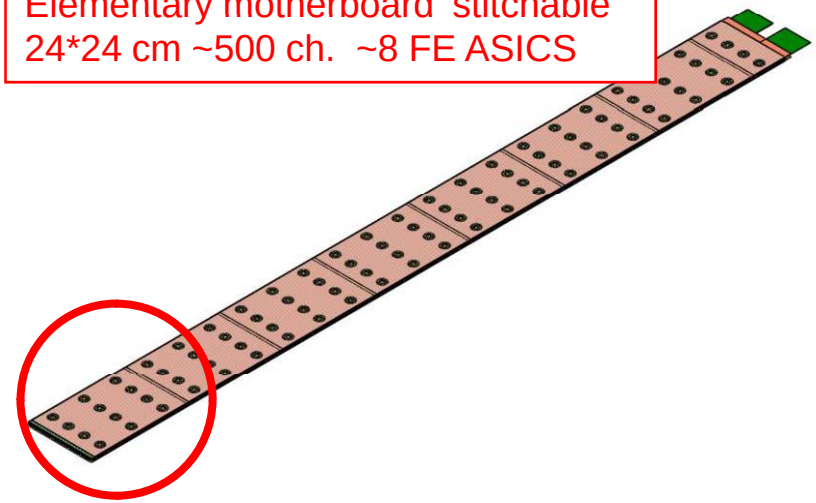


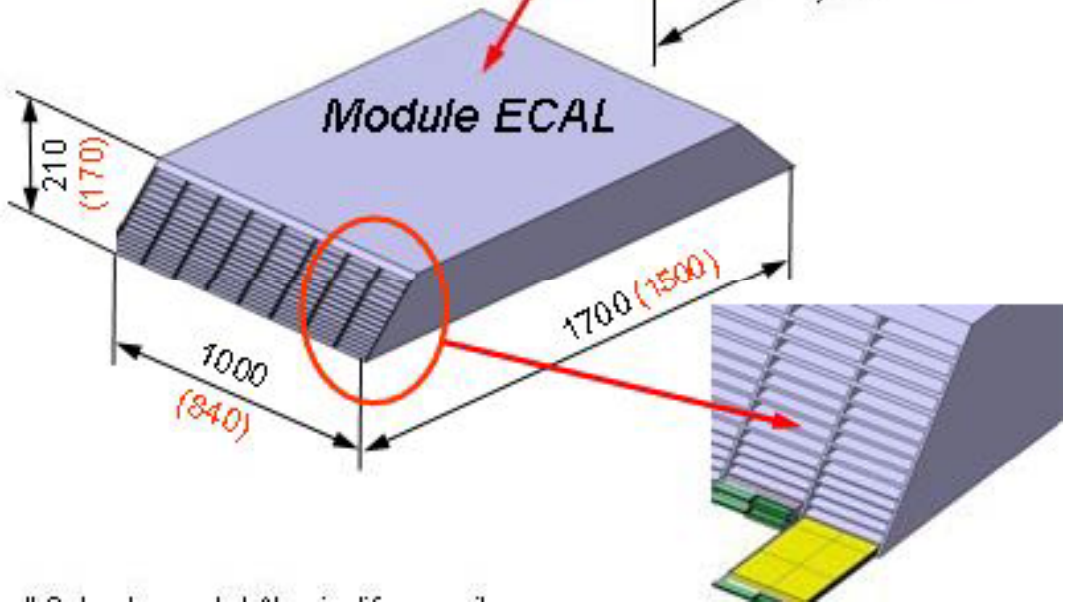
Technological prototype : "EUDET module"

- **Front-end ASICs embedded in detector**
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - Target 0.35 µm SiGe technology
- **All communications via edge**
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- **« Stitchable motherboards »**
  - Minimal conncections between boards



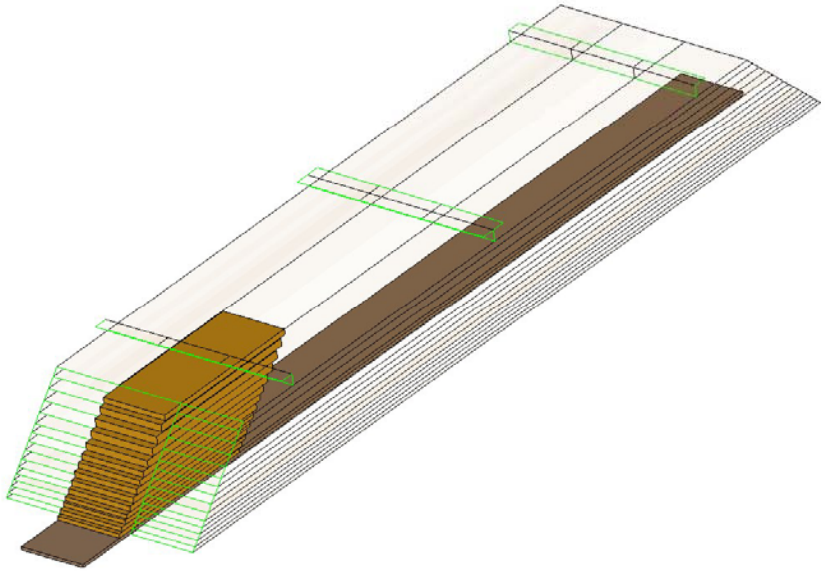
Elementary motherboard 'stitchable'
24*24 cm ~500 ch. ~8 FE ASICS

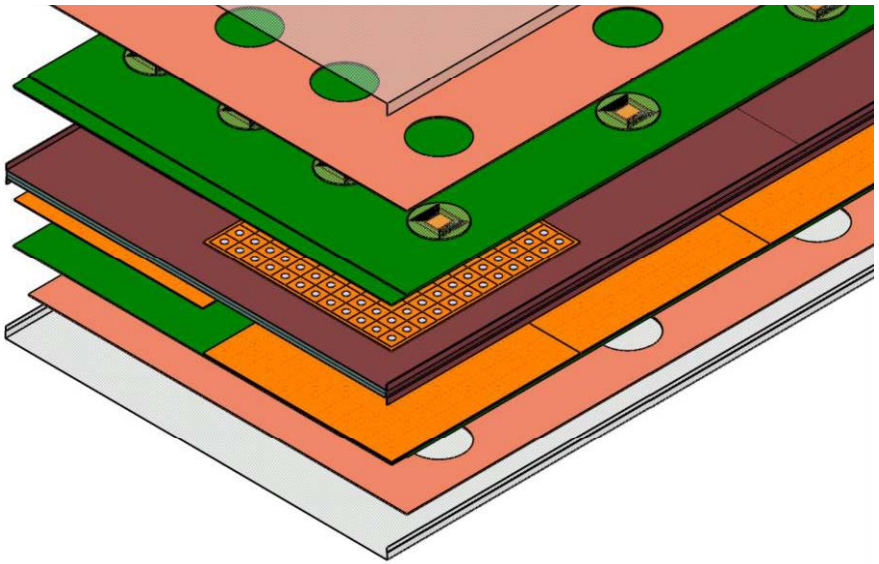




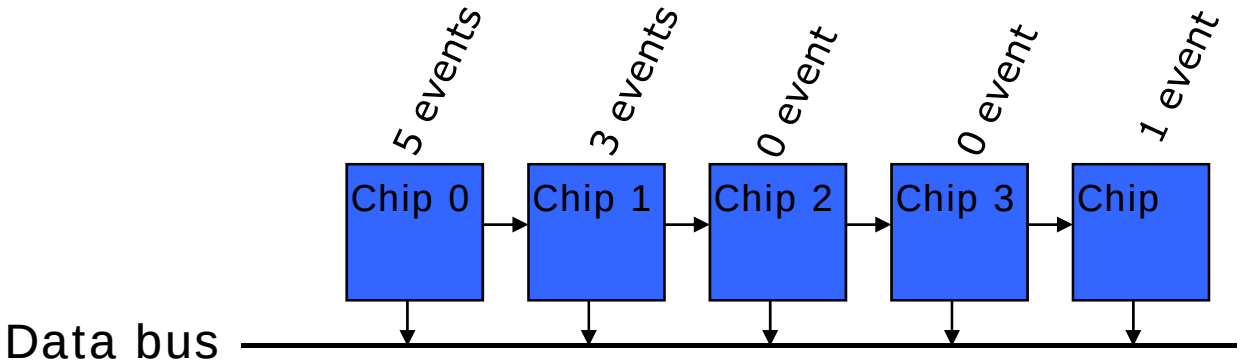
EUDET module FEE : main issues

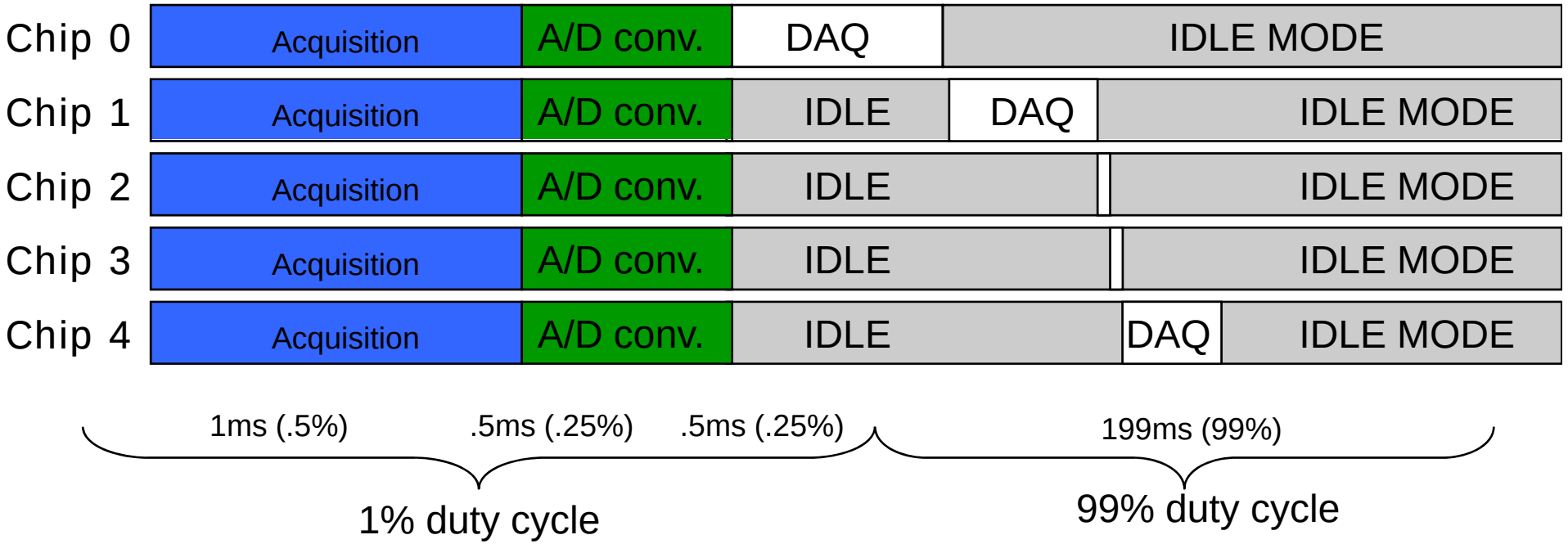
- **Mixed signal issues**
  - Digital activity with sensistive analog front-end
- **Pulsed power issues**
  - Electronics stability
  - Thermal effects
  - To be tested in beam a.s.a.p.
- **No external components**
  - Reduce PCB thickness to < 800μm
  - Internal supplies decoupling
- **Low Cost and industrialization are the major goal**





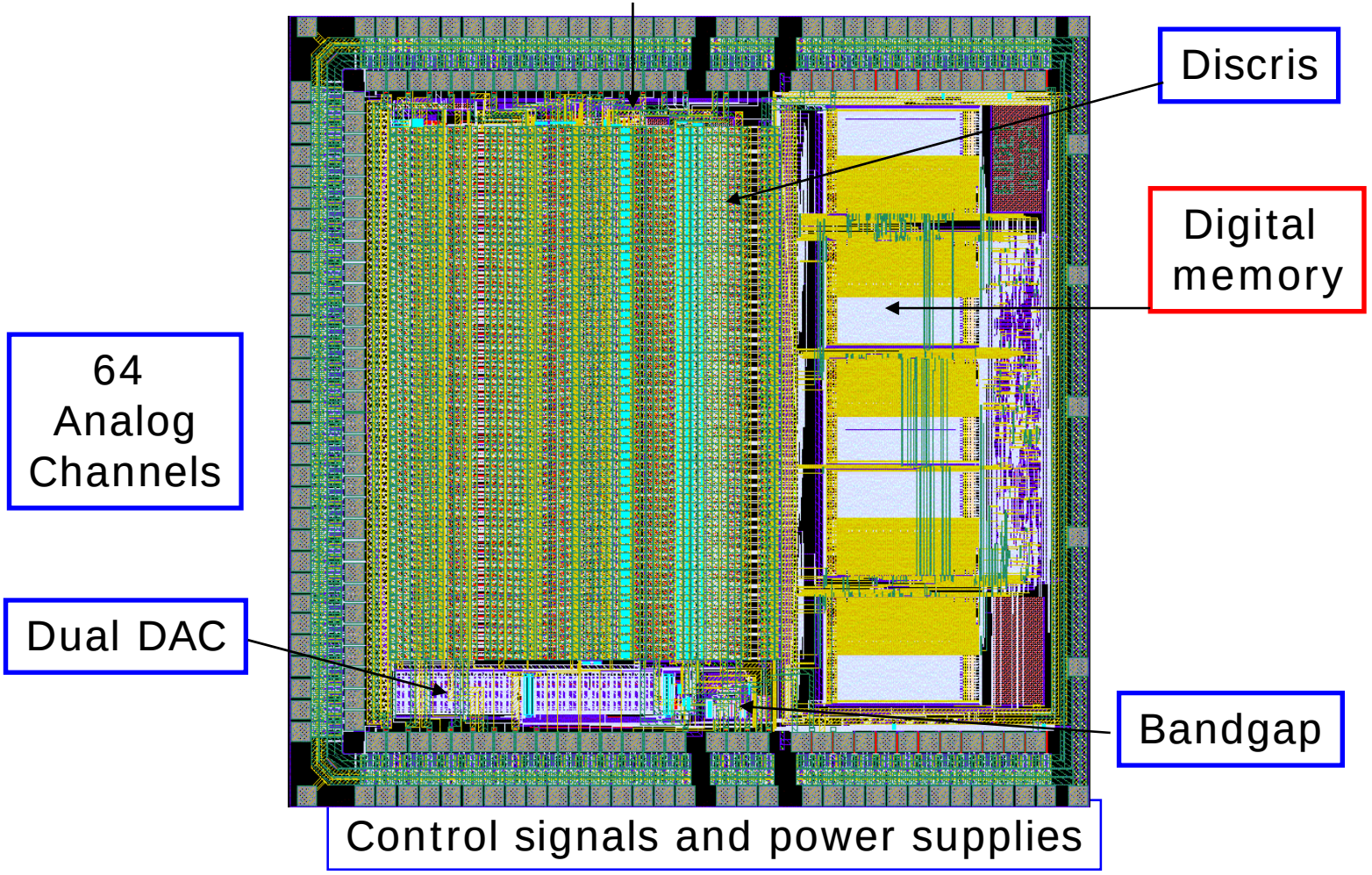
Read out : token ring





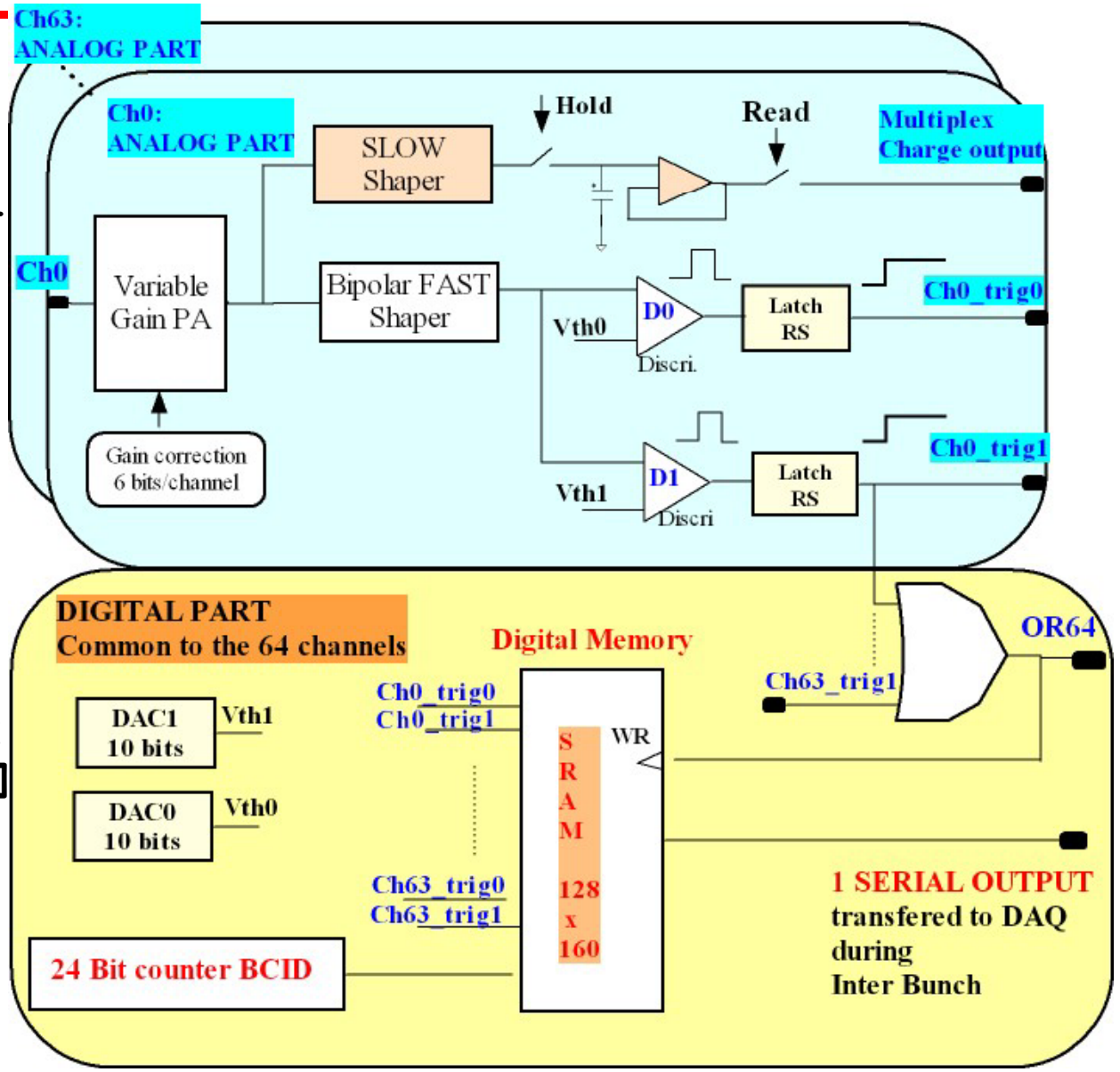
HaRDROC chip for DHCAL [LAL,IPNL]

- **Hadronic Rpc Detector Read Out Chip (Sept 06)**
  - 64 inputs, preamp + shaper+ 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ : only 1 digital data output



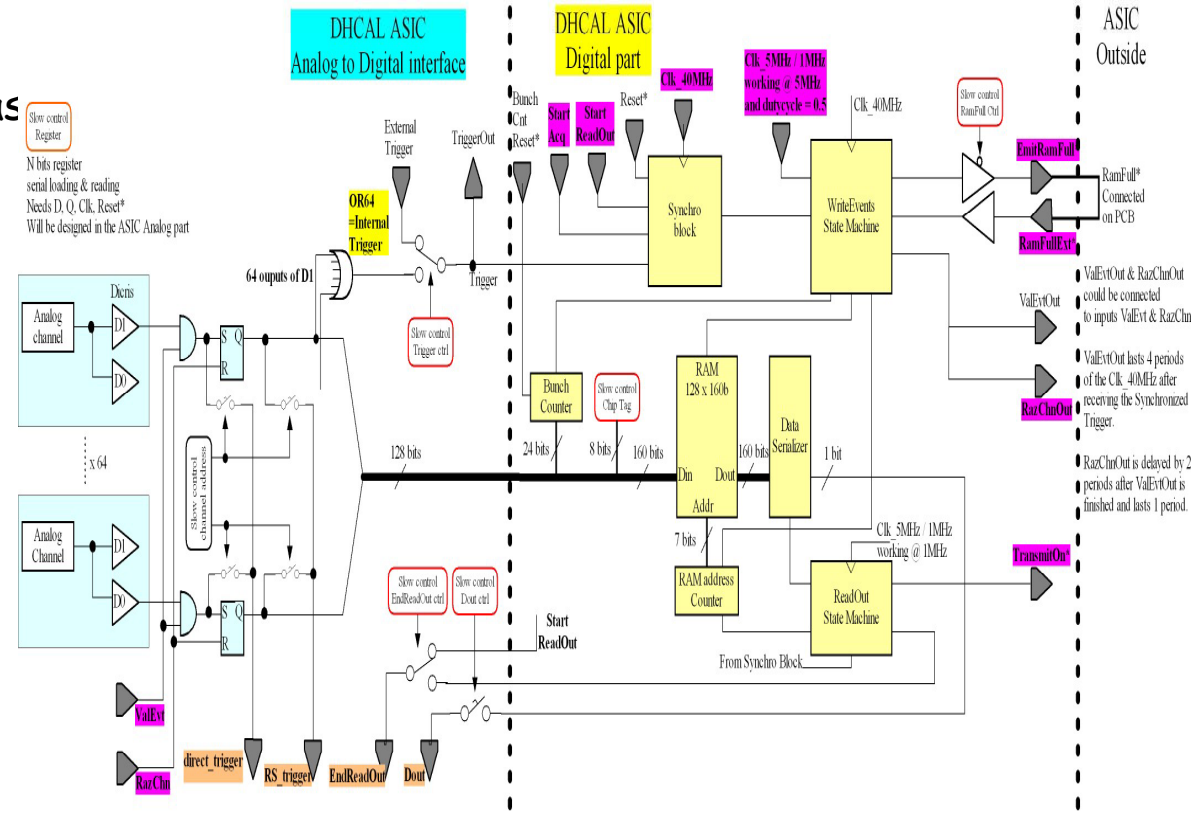
HaRDROC architecture

- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output @ 1 or 5MHz or more
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- Based on MAROC ASIC, but several design changes

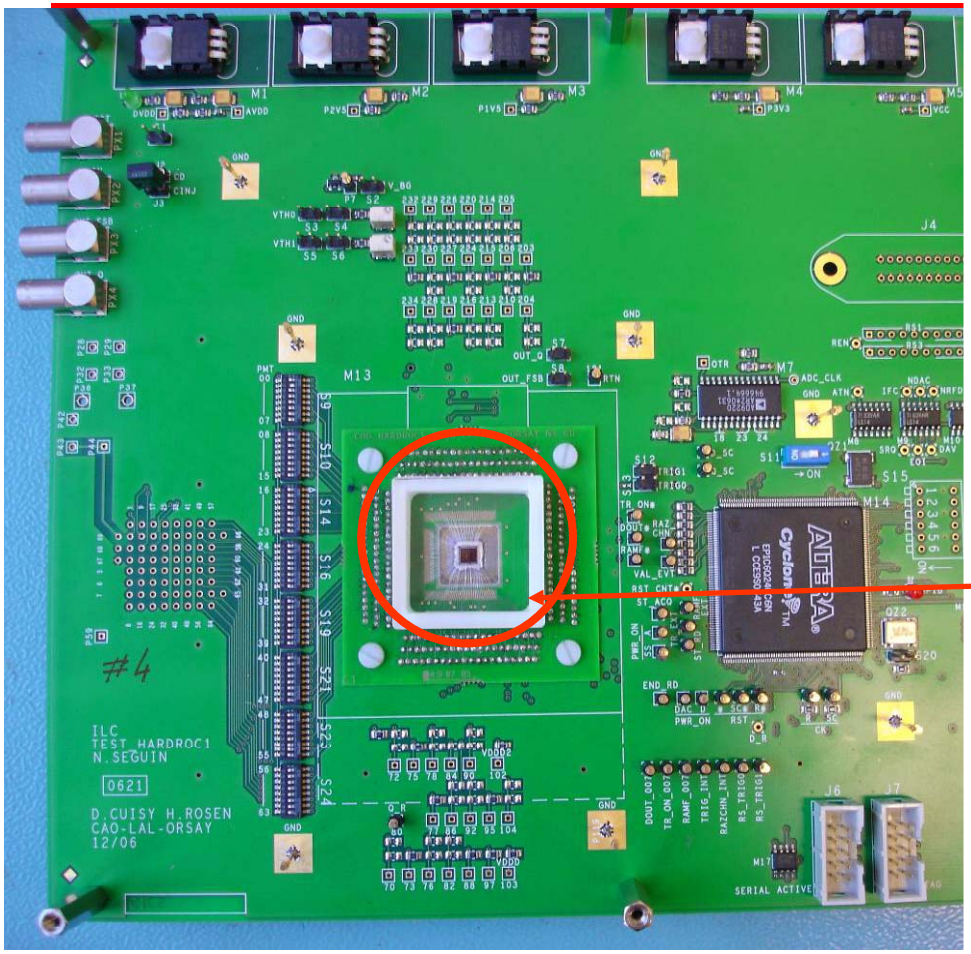


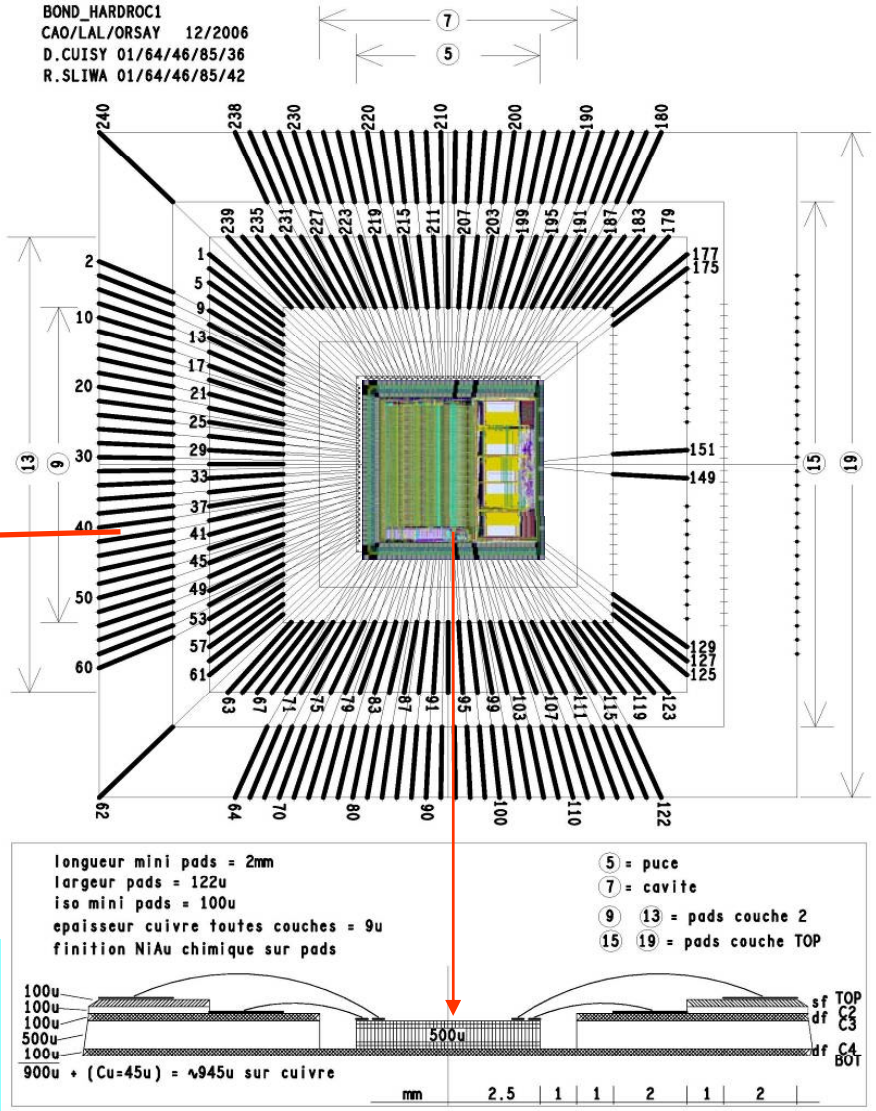
Digital part

- **Full daisy-chain readout**
  - Internal or external Trigger
  - OR36 output
  - Discriminator Validation fas input
  - 4kbyte RAM
  - « Open collector » output signals
  - LVDS clocks
  - Start conversion
  - Start/end readout



HARDROC1: TESTBOARD with Chip On Board





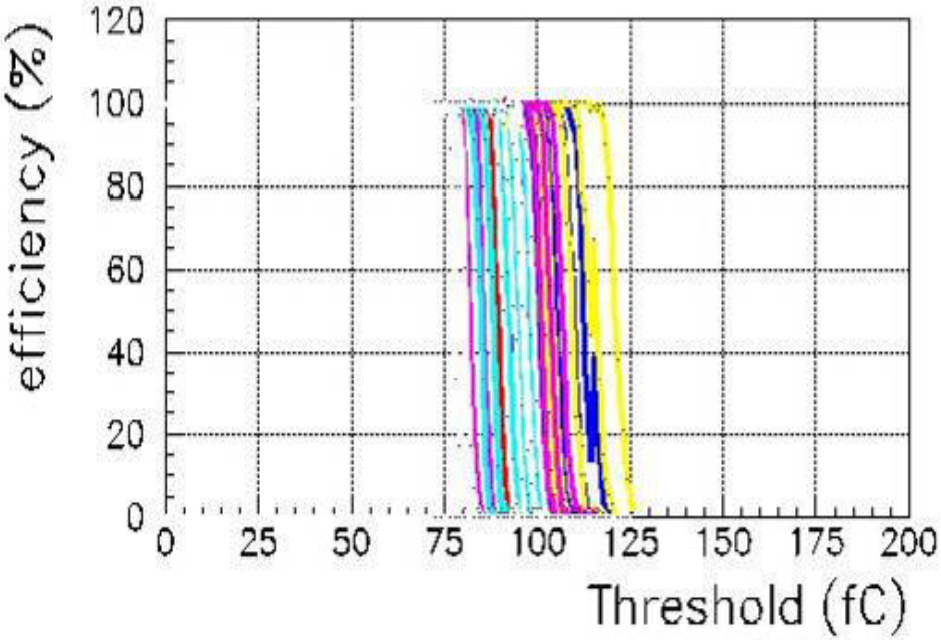
PCB for COB: to estimate feasability (ECAL)

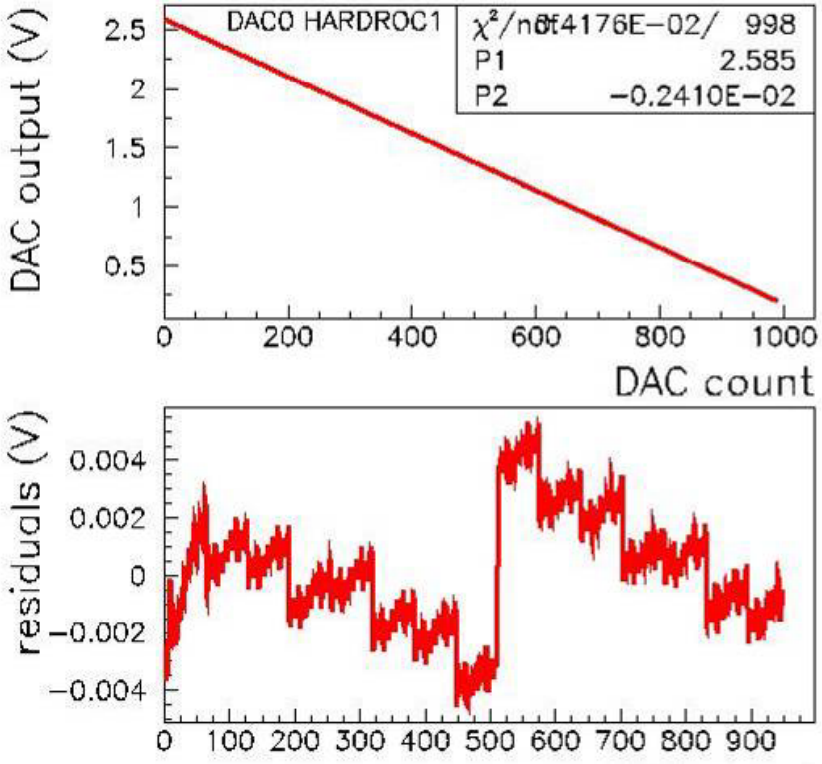
6 layers, COB on Layer 5

2 steps to facilitate the bonding

Performance

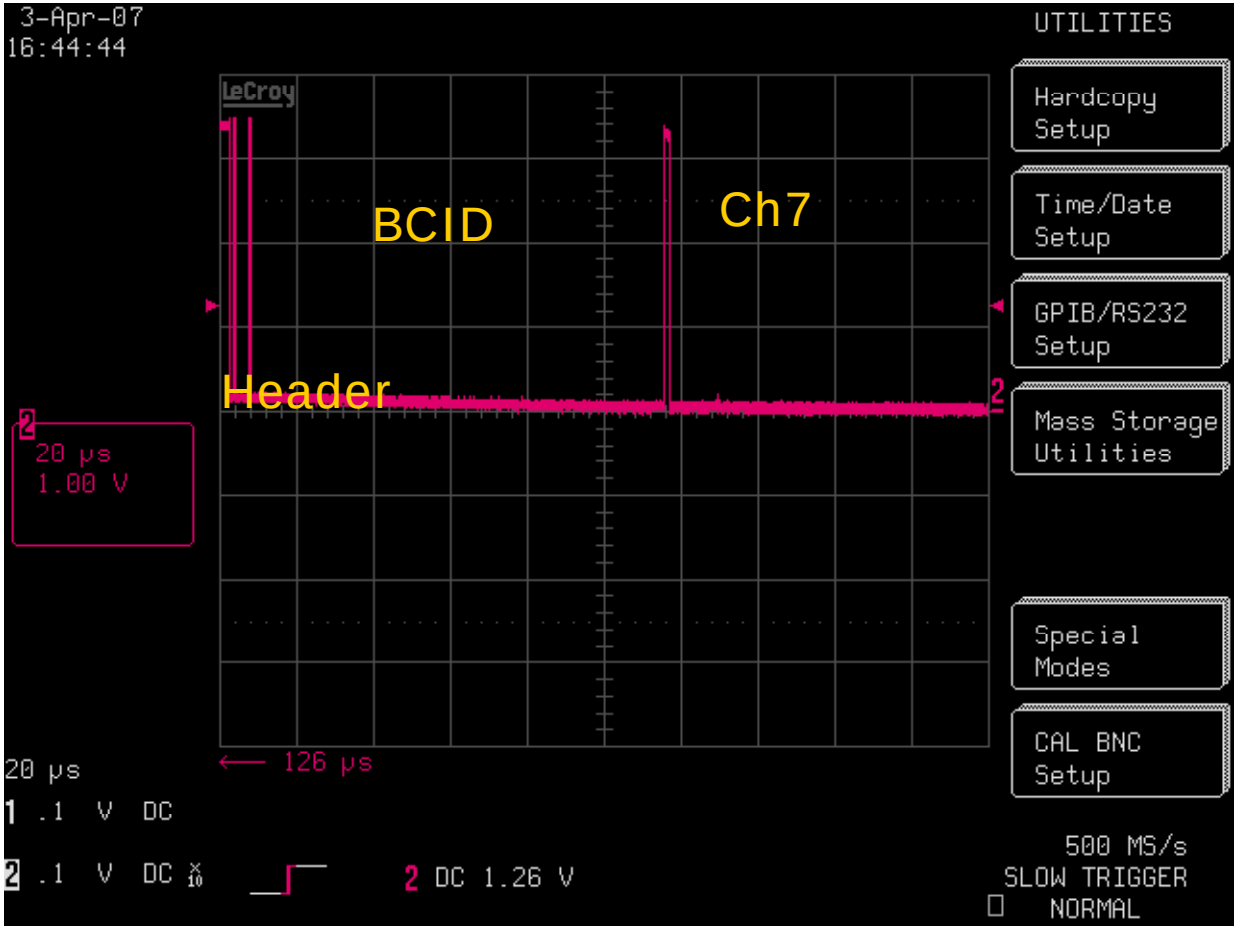
- **Good performance**
- **Power dissipation : 1.4mW/channel (unpulsed)**
  - Power pulsing tests starting. Anticipate 7-15 μW/channel (or cm2)
- **S-curves**
  - Good sensitivity to 100fC. Can go down to 10fC





MEMORY FRAMES: Auto trigger mode

Auto trigger with 10fC:
Qinj=10fC in Ch7
DAC0 and DAC1=255 (~5fC)

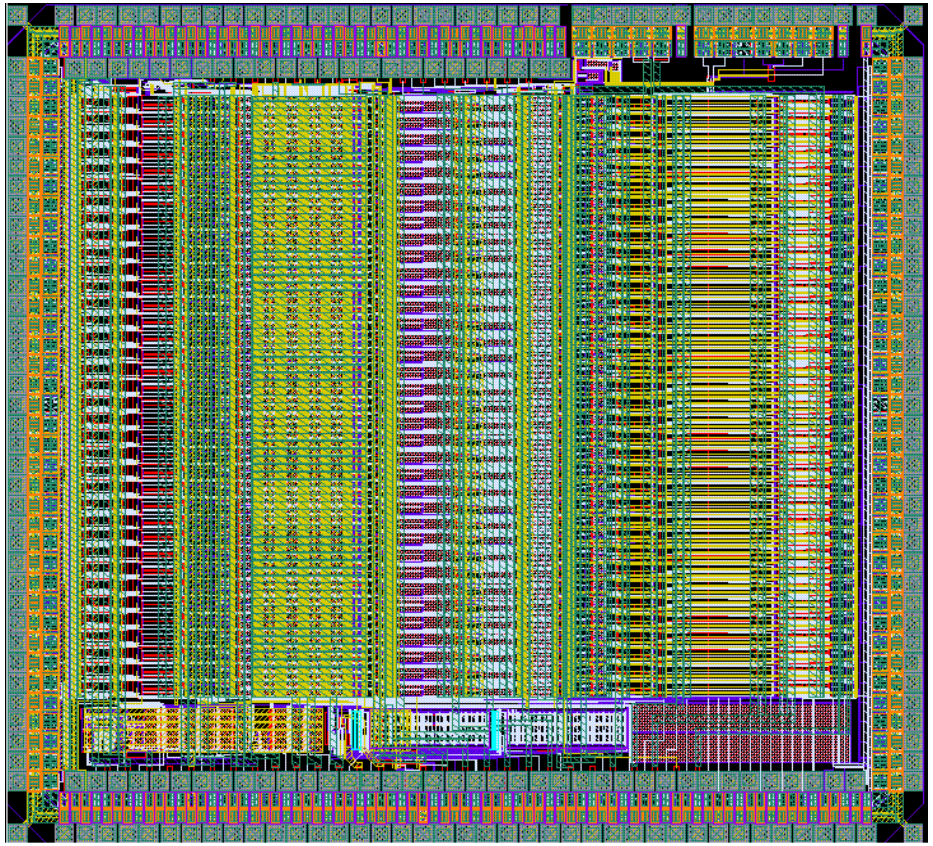


HARDROC1 PERFORMANCE SUMMARY

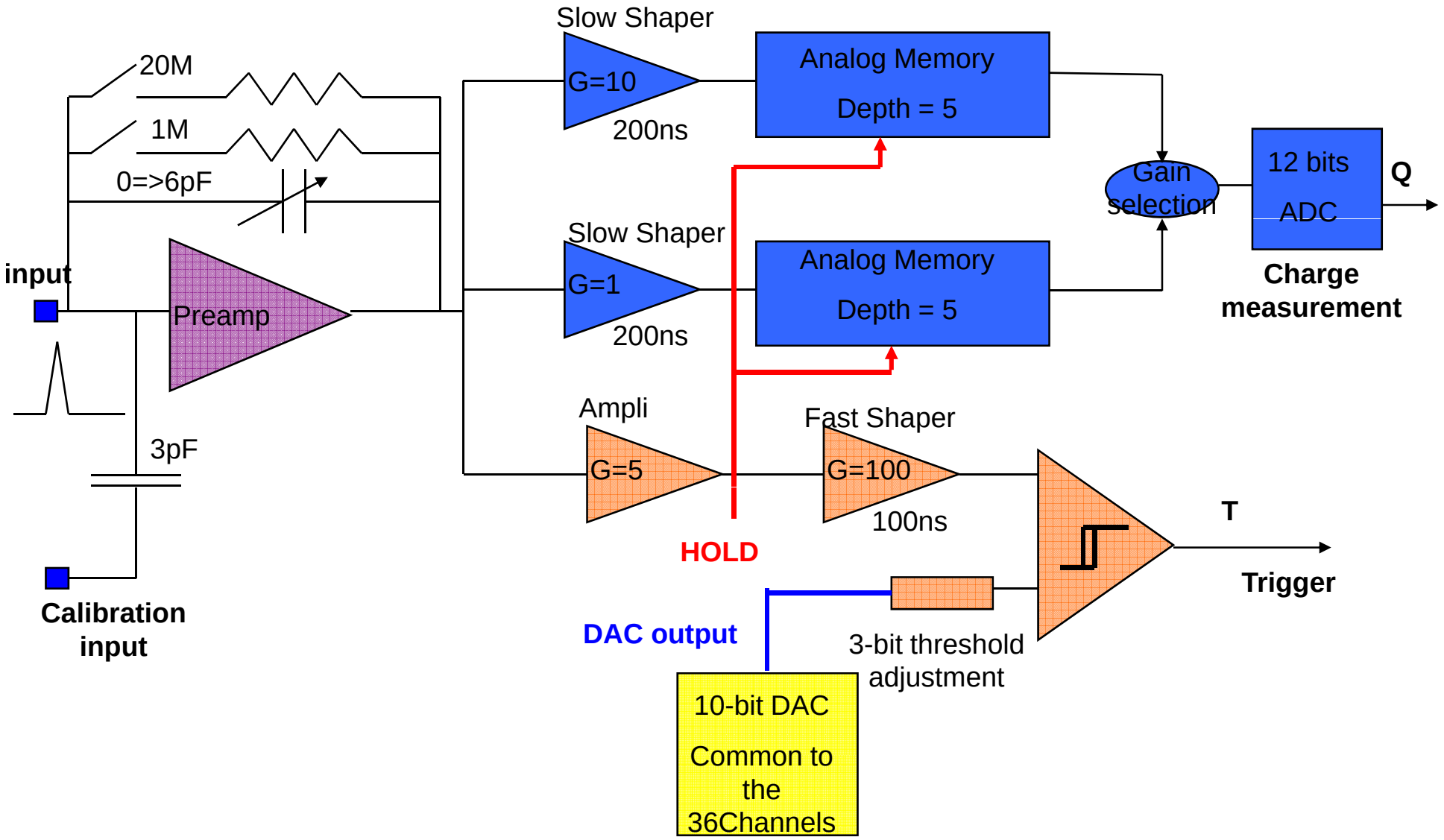
Number of inputs/outputs	64 inputs, 1 serial output
Input Impedance	50-70Ω
Gain Adjustment	0 to 4, 6bits, accuracy 6%
Bipolar Fast Shaper	≈3.5 mV/fC tp=15ns
10 bit-DAC	2.5 mV/fC, INL=0.2%
Trigger sensitivity	Down to 10fC
Slow Shaper (analog readout)	≈50 mV/pC, 5fC to 15pC , tp= 50ns to 150ns
Analog Xtk	2%
Analog Readout speed	5 MHz
Memory depth	128 (20kbits)
Digital readout speed	5MHz or more
Power dissipation (not pulsed)	100 mW (64 channels)

SKIROC for W-Si ECAL

- **Silicon Kalorimeter Integrated Read Out Chip (Nov 06)**
  - 36 channels with 16 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07, tests starting

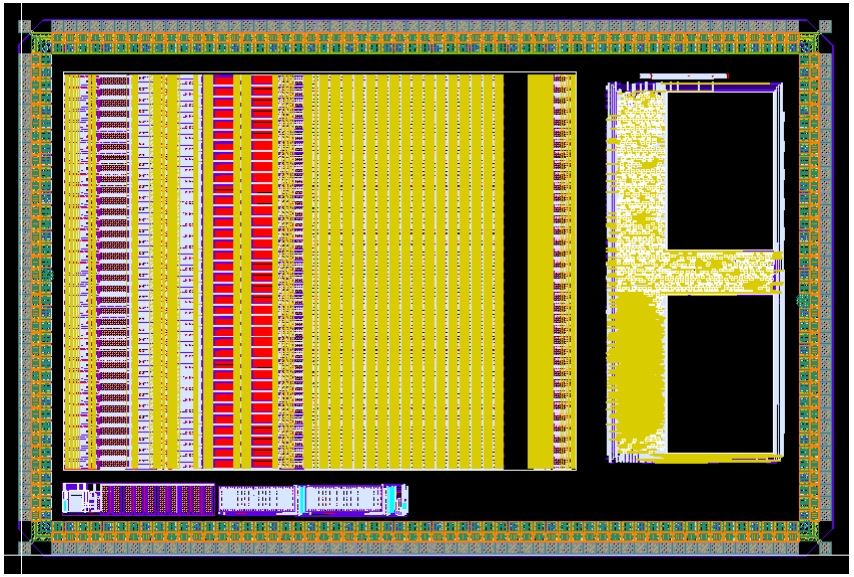


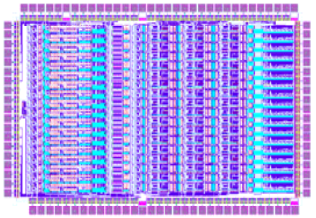
One channel


Slow Shaper
20M
G=10
Analog Memory
Depth = 5
1M
200ns
0=>6pF
Gain selection
12 bits
ADC
Q
Slow Shaper
input
G=1
Analog Memory
Depth = 5
Charge measurement
Preamp
200ns
Ampli
Fast Shaper
3pF
G=5
G=100
T
100ns
HOLD
Trigger
DAC output
3-bit threshold adjustment
10-bit DAC
Common to the 36Channels
Calibration input

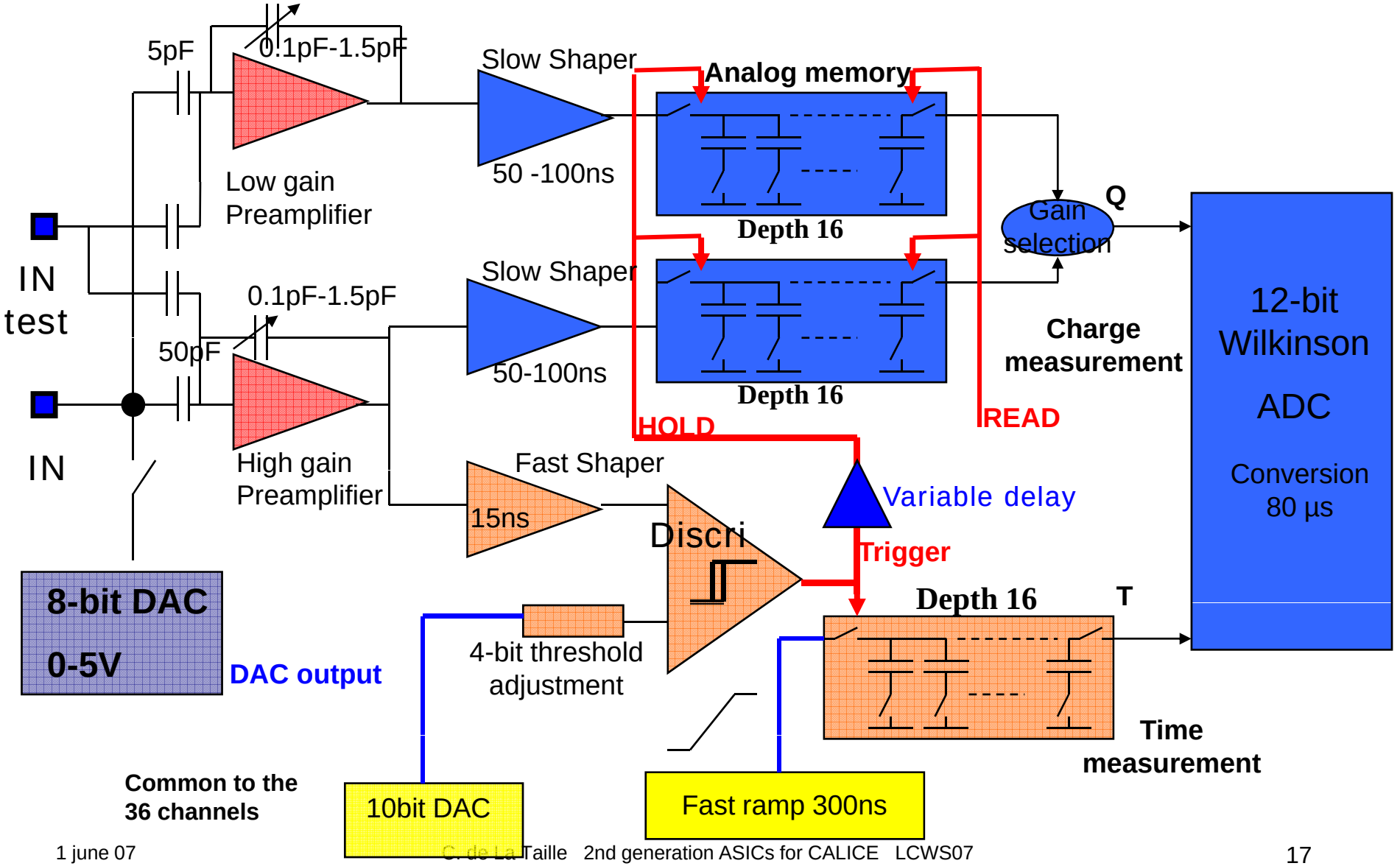
SPIROC overview

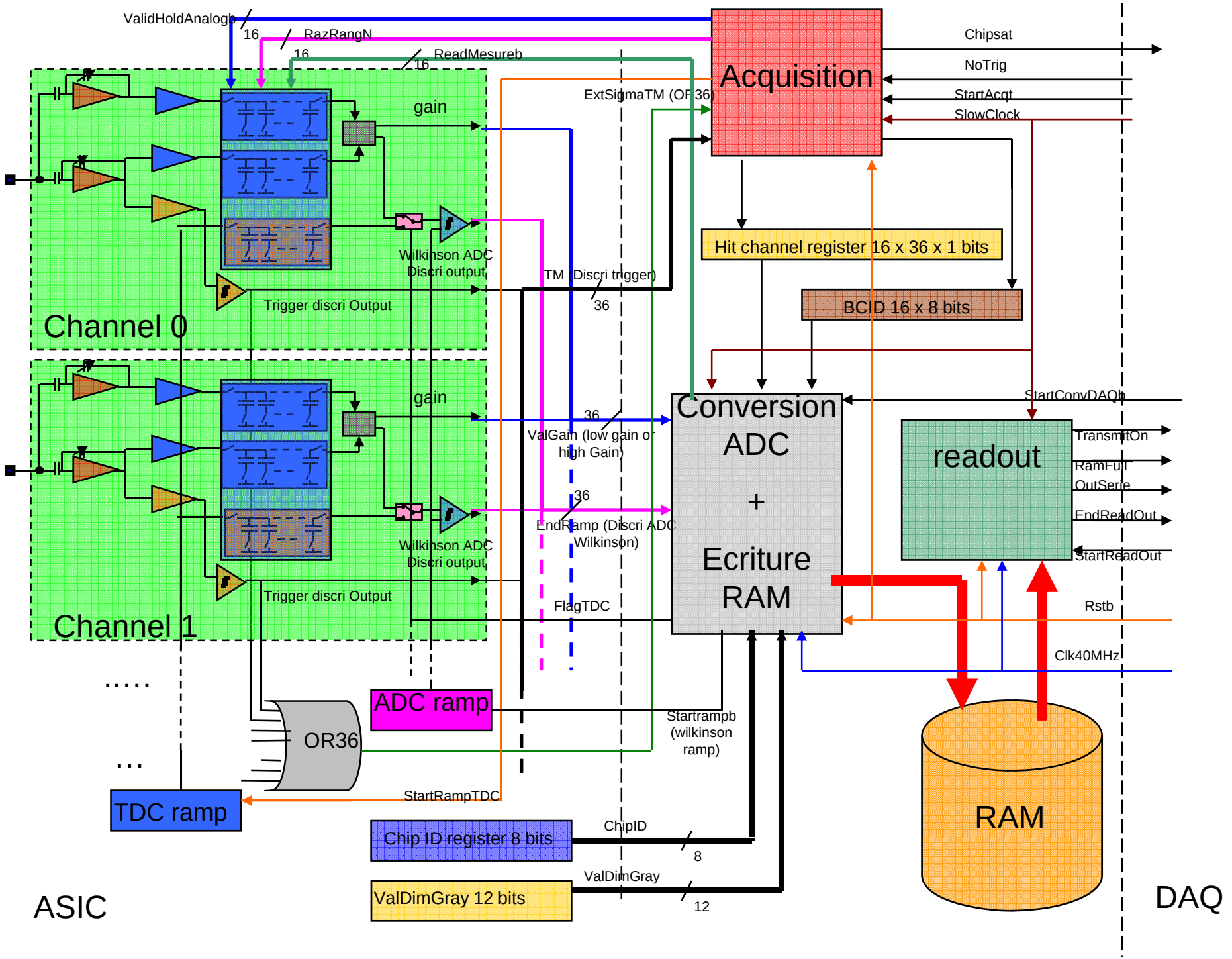
- Silicon Photomultiplier Integrated Read Out Chip
  - A-HCAL read out
- Silicon PM detector
  - G = 3 E5 to 1 E6
  - Same biasing scheme as TB
- 36 channels
  - Charge measurement (15bits)
  - Time measurement (< 1ns)
- Compatible with old & new DAQ
- Many SKIROC, HARDROC, and MAROC features re-used
- Submission foreseen june 11th



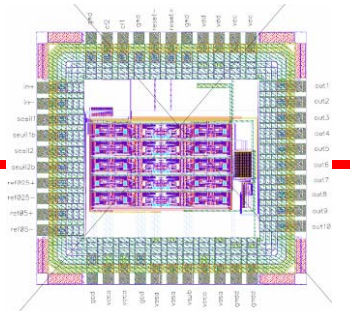


SPIROC: One channel schematic




ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

On-going R&D : ADCs

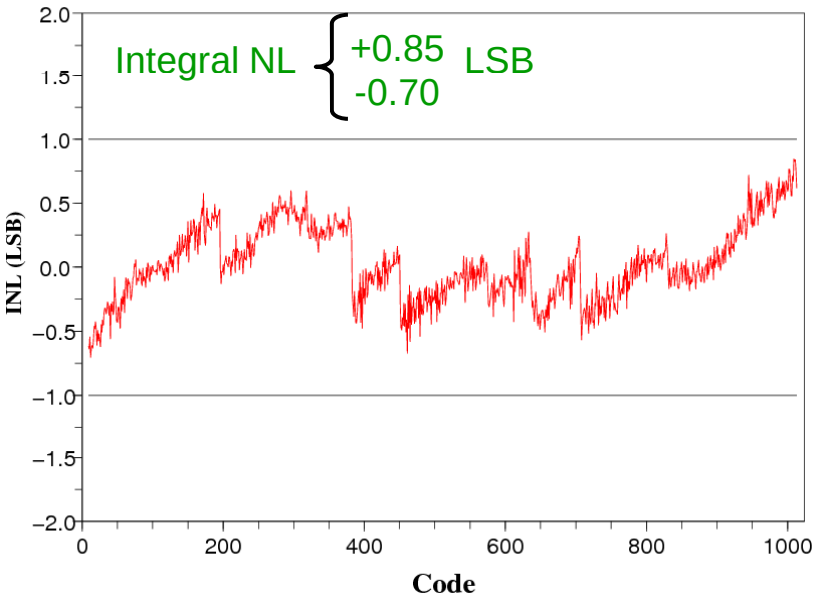


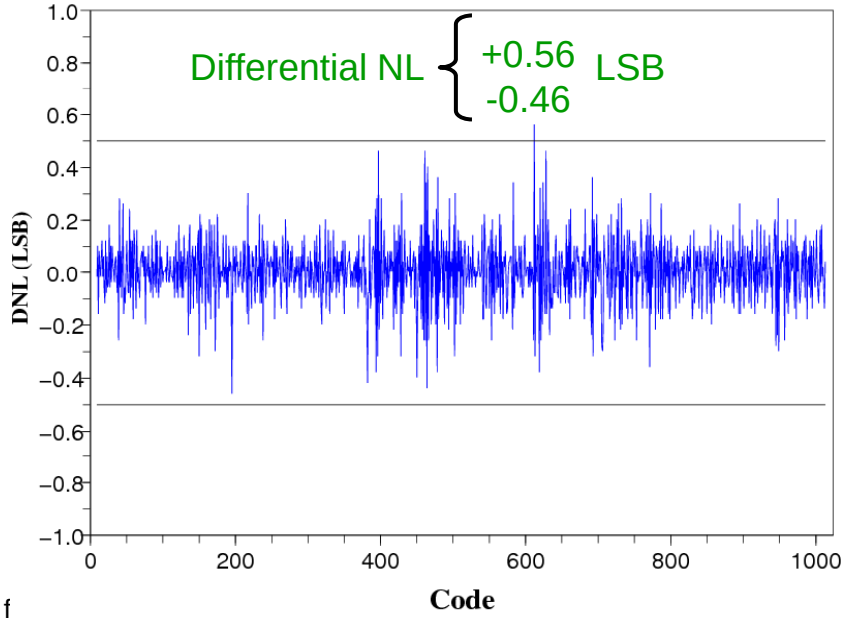
- See talk by L. Royer (2/6)

- **Characteristics:**
  - Technology: CMOS SiGe 0.35µm
  - Power supply: 5V (digital: 2.5V)
  - Clock frequency: 40 MHz
  - Differential architecture
  - 10 stages - 1.5 bit/stage
  - Die area: 1.2 mm^2

- **Performance (measured):**
  - Resolution: 10 bits
  - Consumption: 35 mW
  - Conversion time: 0.25 µs (@ 40MHz)
  - Integrated cons.: (35mW * 0.25µs)/200ms= .044µW

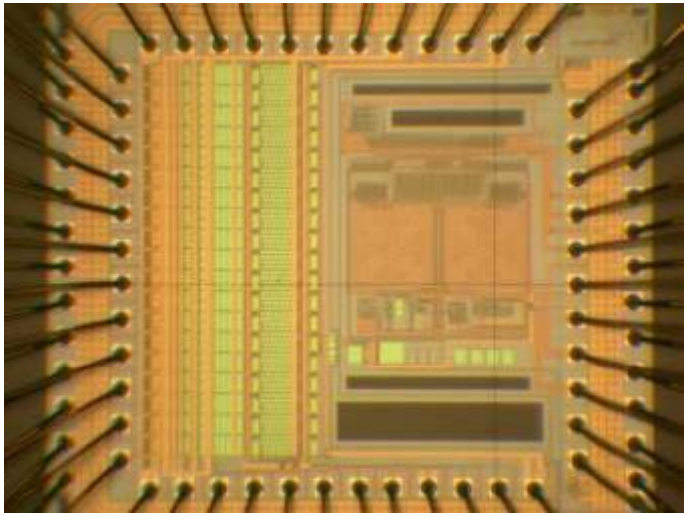
Noise (measured):
< 0.47 LSB @ 68% C.L.



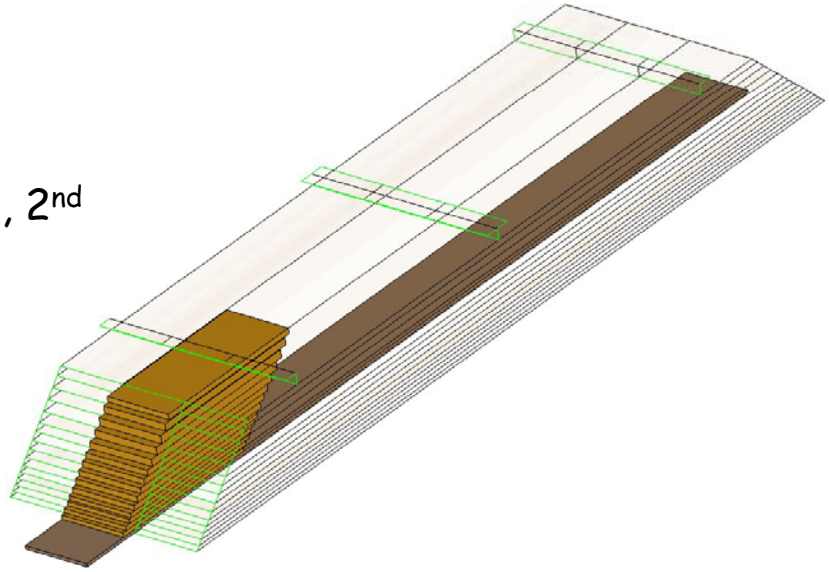


Conclusion

- **Several large dynamic range ASICs developped for CALICE physics prototypes**
  - ECAL W-Si calorimeter : FLC_PHY3 = 10^4 channels in beam, dynamic range 0.1-600 MIPS
  - AHCAL Tile-SiPM calorimeter : FLC_SiPM = 10^3 channels installed, beam in summer 06
  - DHCAL GEM/RPC

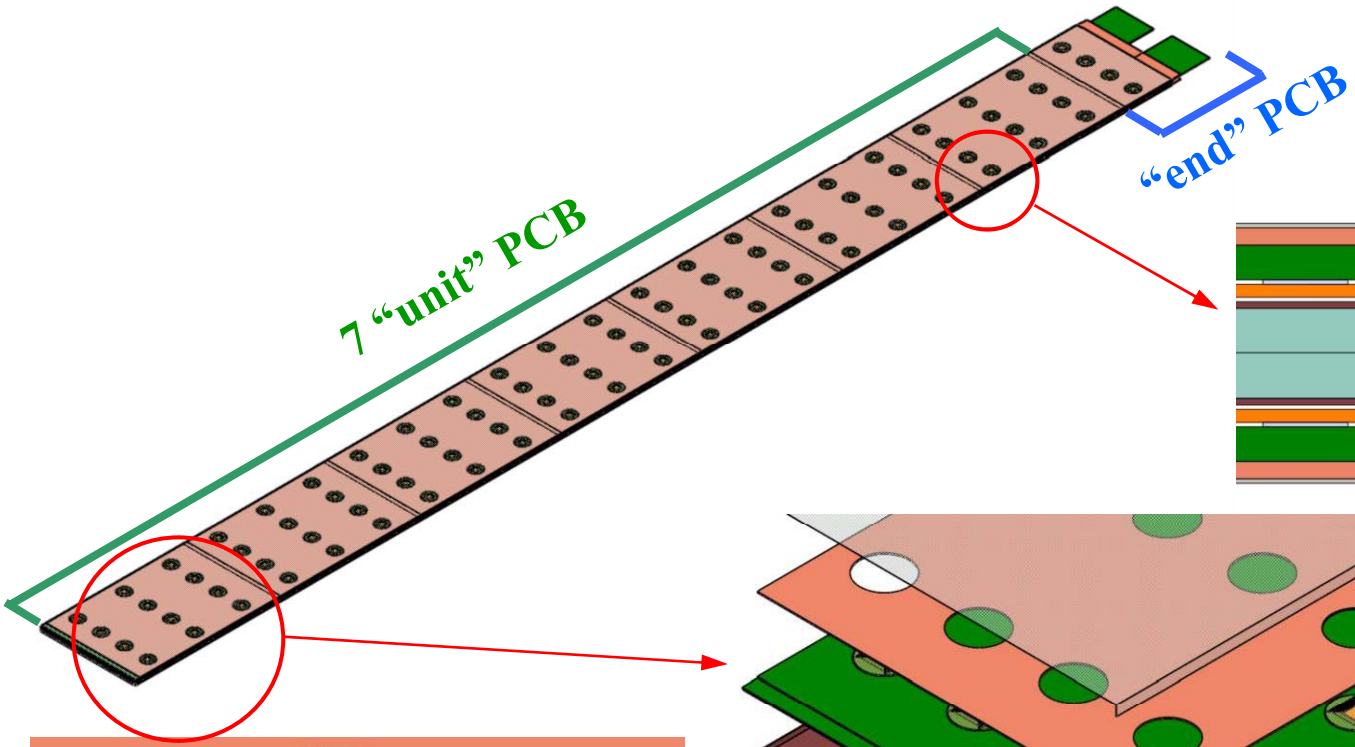


- **3 major second generation ASICs for technological prototypes submitted**
  - HARdROC submitted for DHCAL RPCs
  - SKIROC submitted for ECAL Si-W
  - SPIROC for AHCAL SiPM
  - Power pulsing, Zero-suppress, Auto-trigger, 2nd generation DAQ…

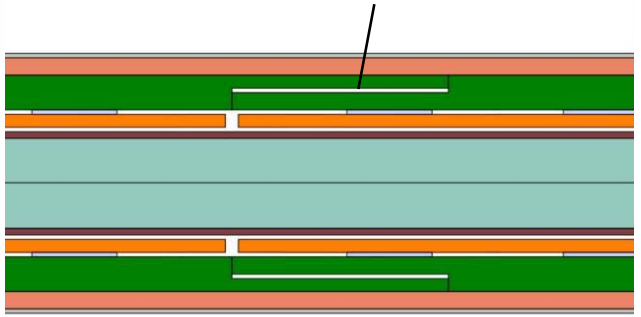


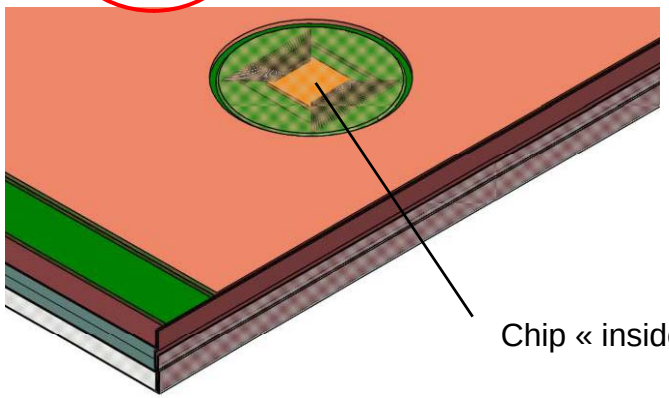
- **System aspects not to be forgotten**
  - Power supplies ! Mechanics, reliability…

EUDET - Detector slab (2)

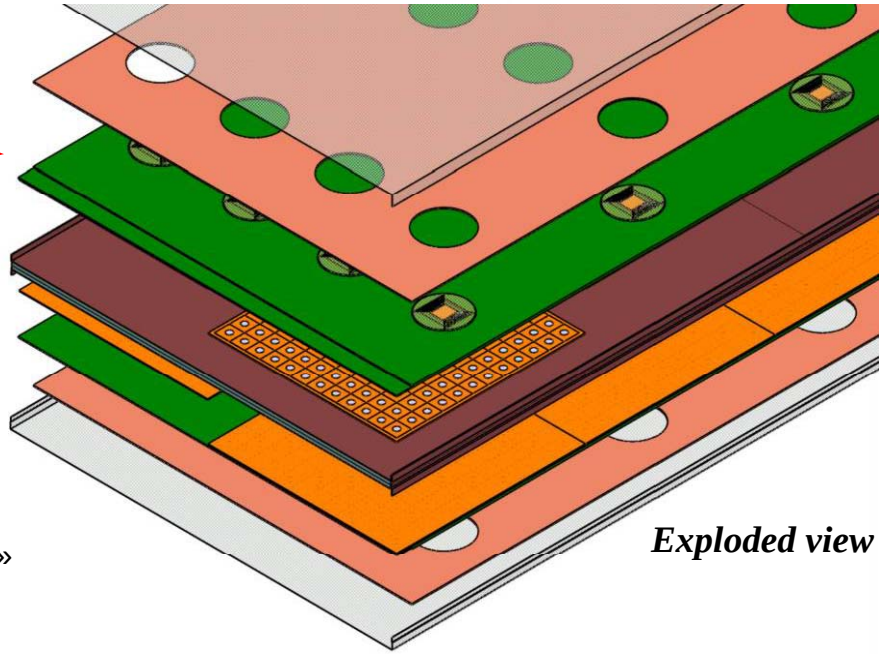


Connection between 2 PCB



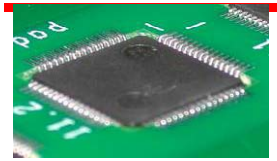


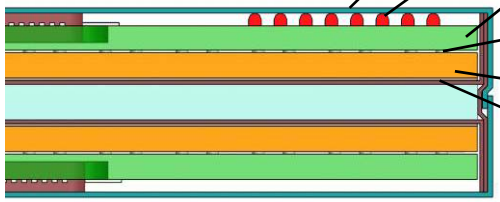
Chip « inside »



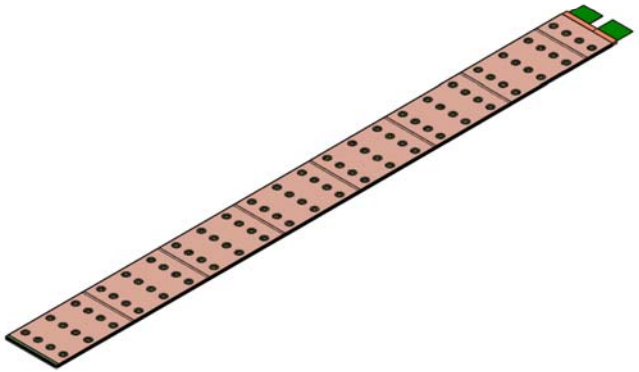
Exploded view

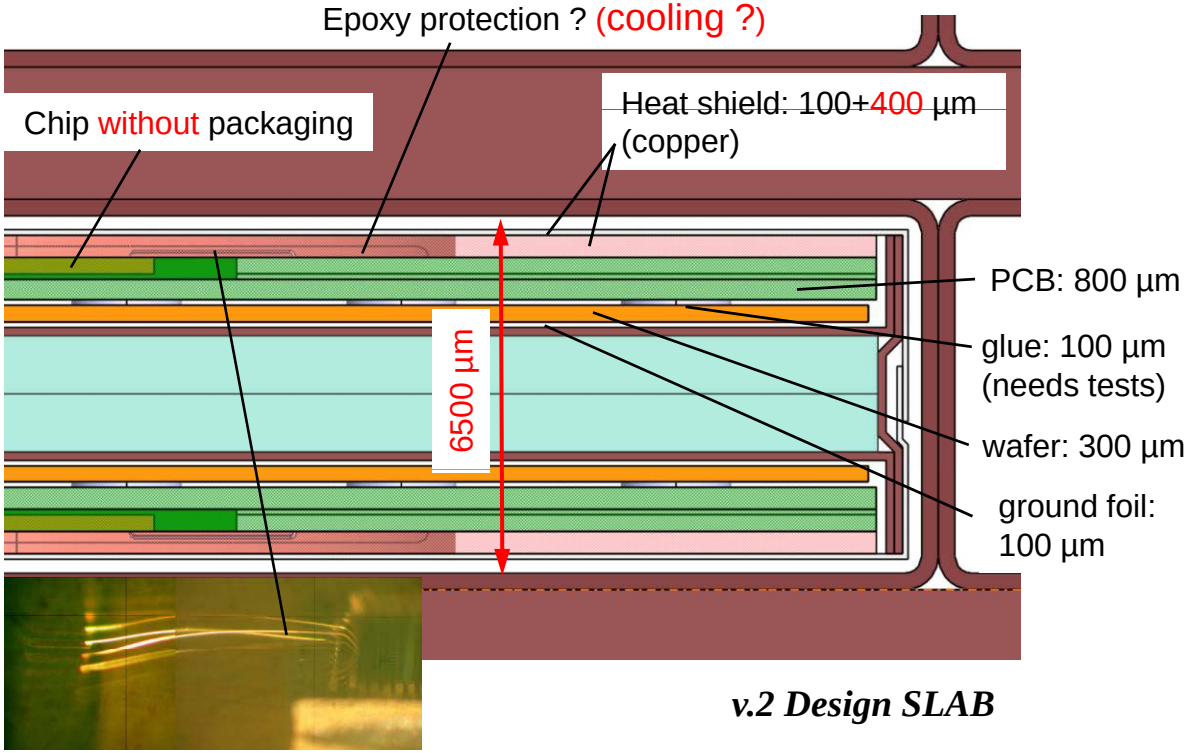
EUDET - Detector slab (1)





v.1 Design SLAB





v.2 Design SLAB

Main ISSUES :

Front End chips inside :

- ⇨ **Thermal dissipation (cooling ?)**
- ⇨ **Chip behaviour in an electron shower**

■ **Long structure :**

- ⇨ **Design and fabrication problems (composite with segmentation of W plates, mechanical behaviour ...)**
- ⇨ **Segmentation of PCB (design of an interconnection)**

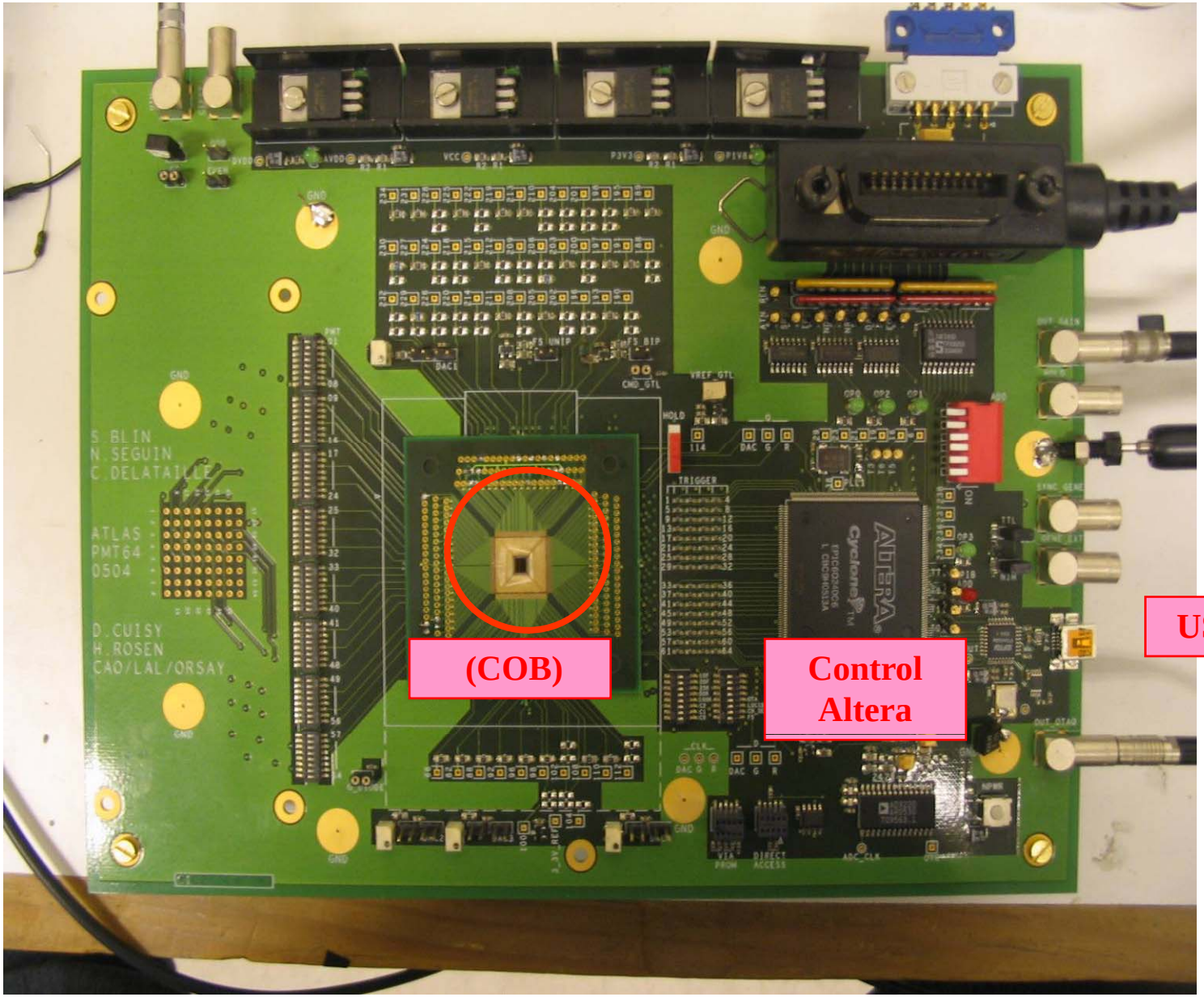
■ **Diminution of the pads size**

- ⇨ **Increases of the number of channels (thermal cooling ?)**
- ⇨ **Size of glue dots**

SPIROC main features

- **36-channel readout chip**
- **Internal input 8-bit DAC (0-5V) for SiPM gain adjustment**
- **Energy measurement :**
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- **Time measurement :**
  - 1 TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on $\frac{1}{2}$ pe
- **Analog memory for time and charge measurement : depth 16**
- **Power pulsing integrated**
- **Low consumption : ~25µW per channel (in power pulsing mode)**
- **Calibration injection capacitance**
- **Embedded bandgap for voltage references**
- **Embedded DAC for trigger threshold**
- **Compatible with physic prototype DAQ**
  - Serial analogue output
  - External "force trigger"
- **Probe bus for debug**
- **12-bit Bunch Crossing ID**
- **SRAM with data formatting 2 x 2kbytes = 4kbytes**
- **Output & control with daisy-chain**

TEST BOARD


S.BLIN
N.SEGUIN
C.DELATAILLE
ATLAS
PMT64
0504
D.CUISY
H.ROSEN
CAO/LAL/ORSAY
(COB)
Control
Altera
GPIB port
USB port