Monolithic Pixels R&D at LBNL

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Devis Contarato

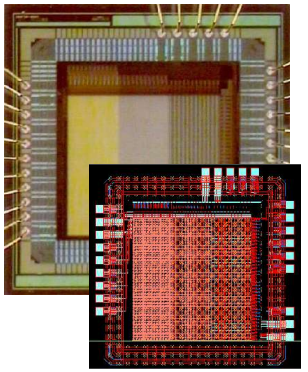
Lawrence Berkeley National Laboratory

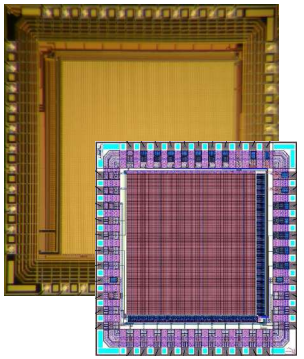
M. Battaglia, L. Glesener, B. Hooberman (UC Berkeley & LBNL), P. Giubilato (LBNL & INFN Padova), J.-M. Bussat, P. Denes, C. Q. Vu (LBNL)

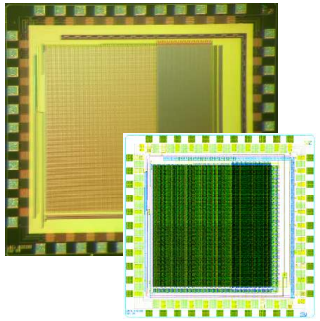
Outline

- **Introduction: monolithic pixels R&D at LBNL**

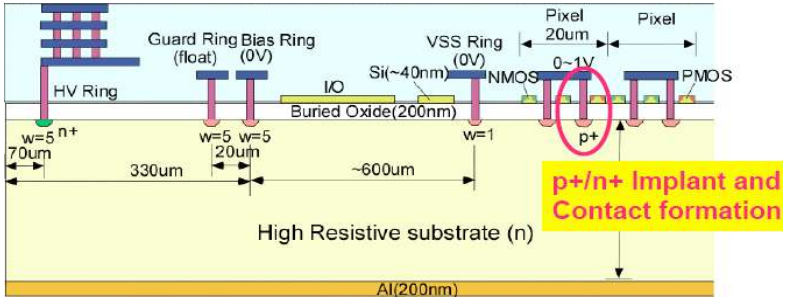
- **CMOS Monolithic Pixels**
  - Summary of results with first 3T prototype
  - Prototype with in-pixel CDS
  - Next submission: prototype with integrated ADC







- **SOI Pixels**
  - First prototype
  - Device simulation
  - First signals



- **Outlook**

Introduction

- LBNL R&D activities on pixel sensors:
  - Pixel prototype design and characterization
  - Sensor simulation in ILC software framework (see M. Battaglia's talk in Sim/Reco session)
  - Readout development
  - Back-thinning tests
  - Pixel module engineering

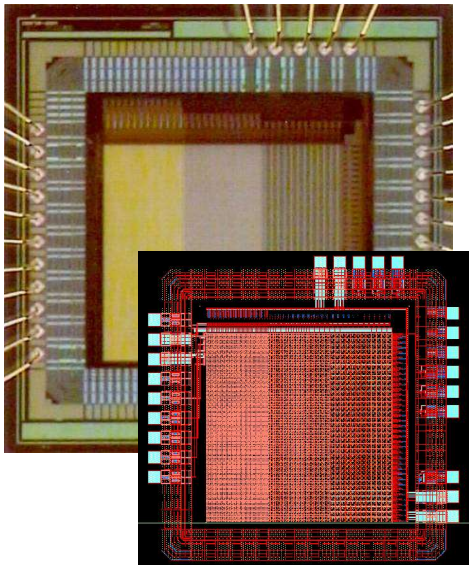
  } → see M. Battaglia's talk in this session

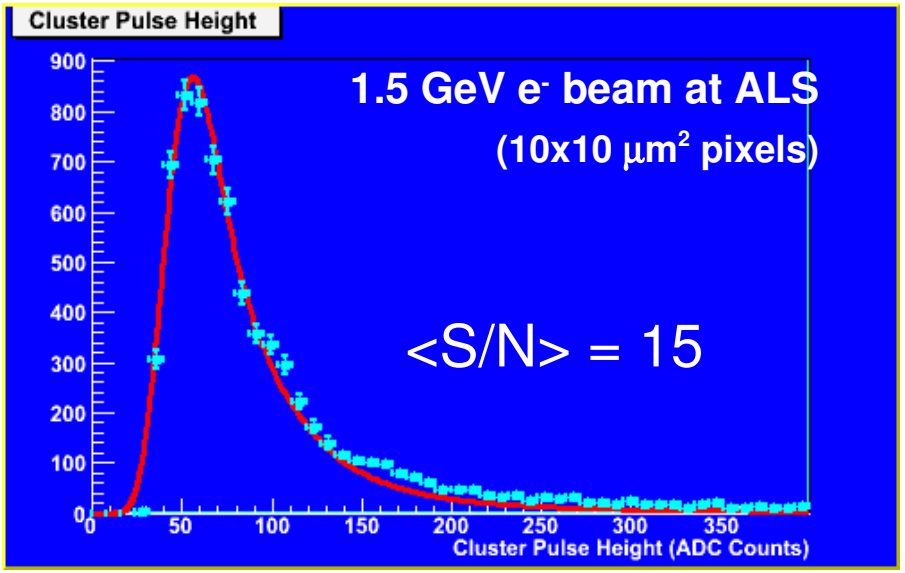
- Synergy with other on-going LBNL activities on CMOS pixels: STAR HFT upgrade, electron microscopy, existing infrastructure from ATLAS pixels

- Availability of test facilities on site:
  - Advanced Light Source: beam-tests with 1.5 GeV e^-
  - 88-inch Cyclotron: irradiations with 30-50 MeV p, <30 MeV n
  - LOASIS plasma accelerator facility, 50 MeV-1 GeV e^-

LDRD-1: first CMOS prototype

- First LBNL test structure
- AMS 0.35 μm OPTO, 14 μm epilayer
- Simple 3T pixels, serial analog output
- 3 matrices with 10x10 μm², 20x20 μm² and 40x40 μm² pixels

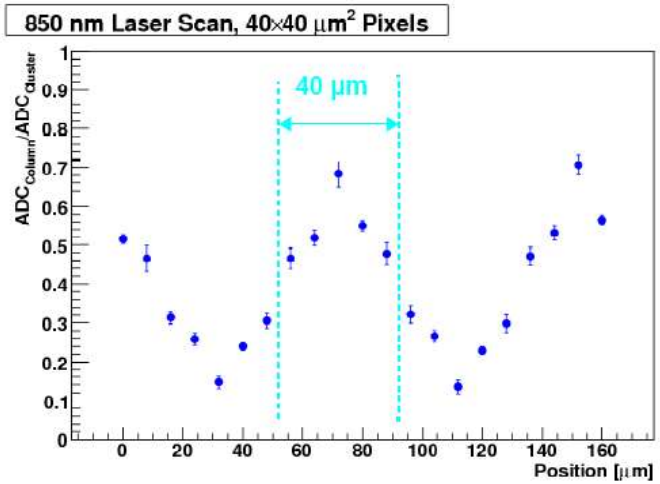




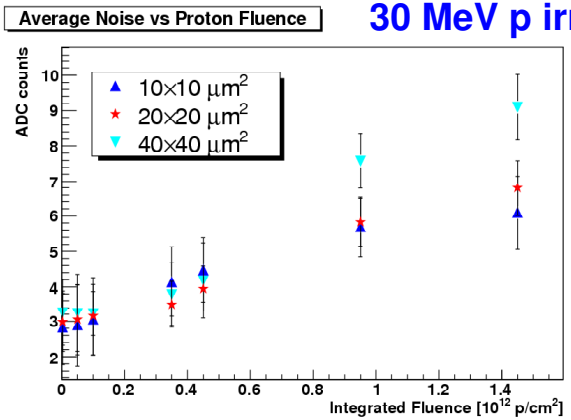
- Resolution study with focused (~10 μm) 850 nm laser spot

Pitch (μm)	Laser Scan	Pixel Sim
10	2.0	1.5
20	3.3	3.2
40	5.1	5.0

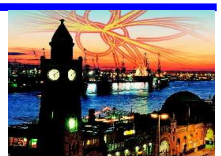
(all values in μm)



30 MeV p irradiation

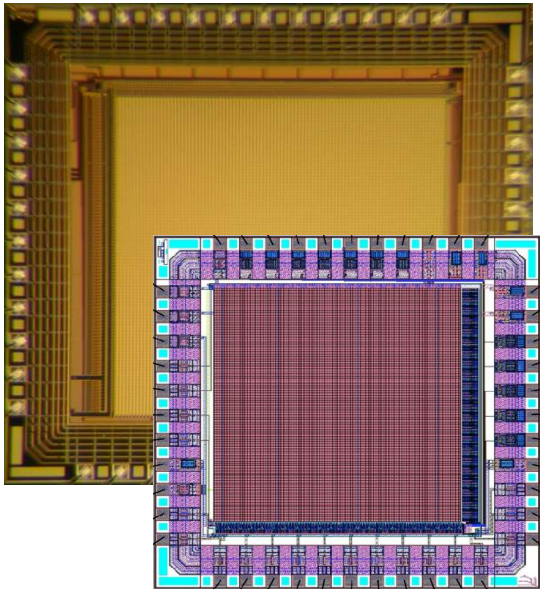


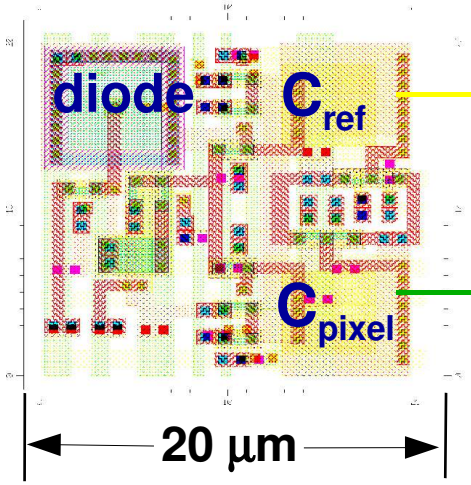
- Radiation Hardness tests @ 88" Cyclotron:
  - 30 MeV p up to 1.45x10¹² p/cm²
  - 1-20 Mev n, no change up to 2x10¹¹ n/cm²

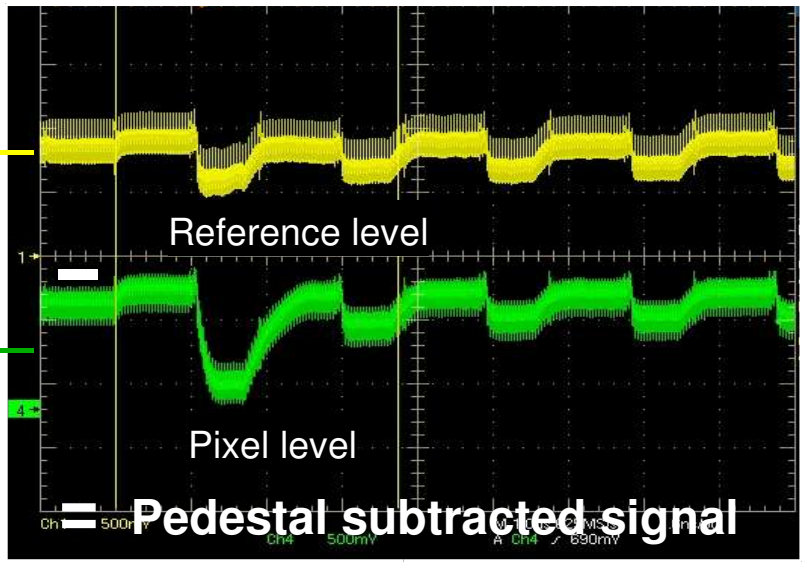


LDRD-2: in-pixel CDS

- LDRD-2: second prototype chip in AMS 0.35 µm OPTO process, 14 µm epilayer
- 20×20 µm^2 pitch with in-pixel CDS: signal and pedestal level stored on pixel capacitors
- 3×3 µm^2 and 5×5 µm^2 diodes
- Read out in rolling-shutter mode
- Circuitry for charge injection tests: study capacitive coupling between pixels
- Tests underway; study of performance w.r.t. to clock frequency, up to 25 MHz





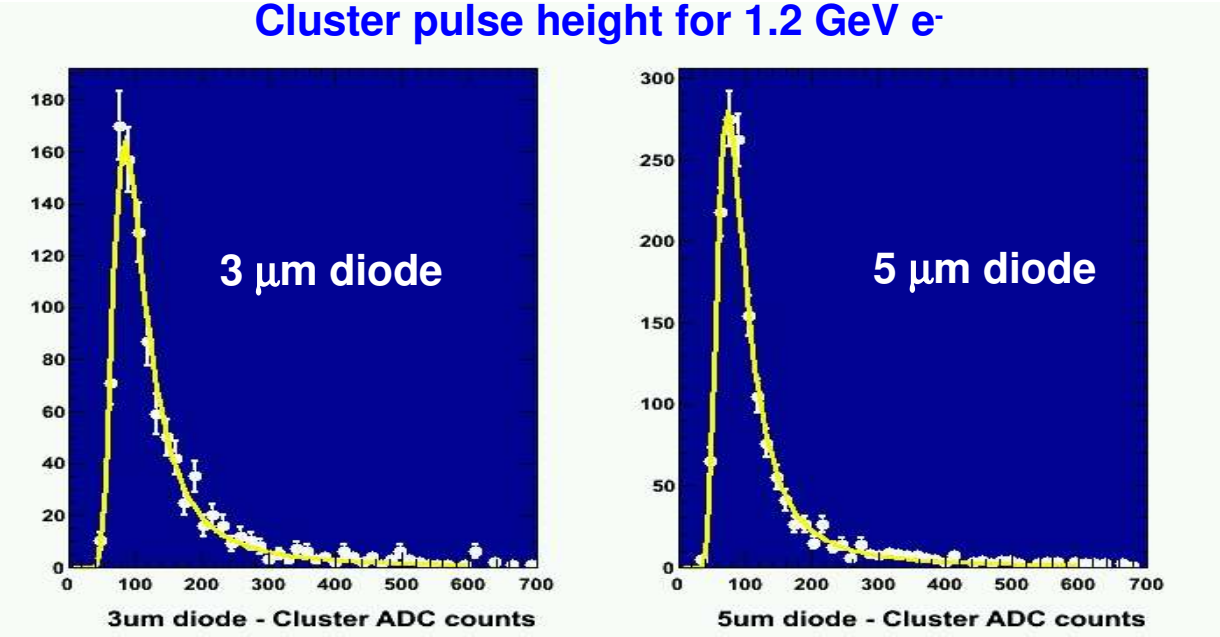


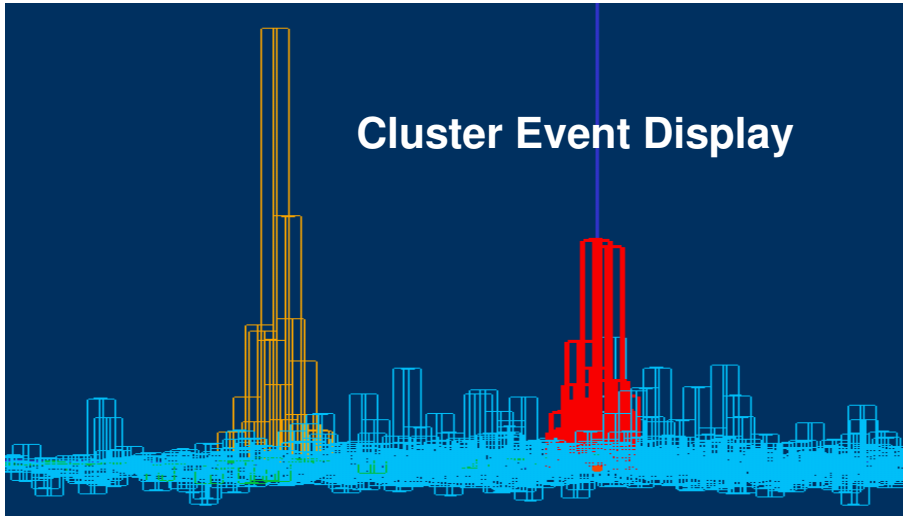
LDRD-2: beam-test results

- Test performed with 1.2 GeV e^- at the Advanced Light Source BTS line
- Preliminary results @ 27°C:

	3 μm diode	5 μm diode
<S/N>	20.4	20.7
<NPixels>	5.1	4.2

- Higher S/N but larger pixel multiplicity w.r.t. LDRD-1 prototype
- Tracking test at FNAL (100 GeV p) in June/July

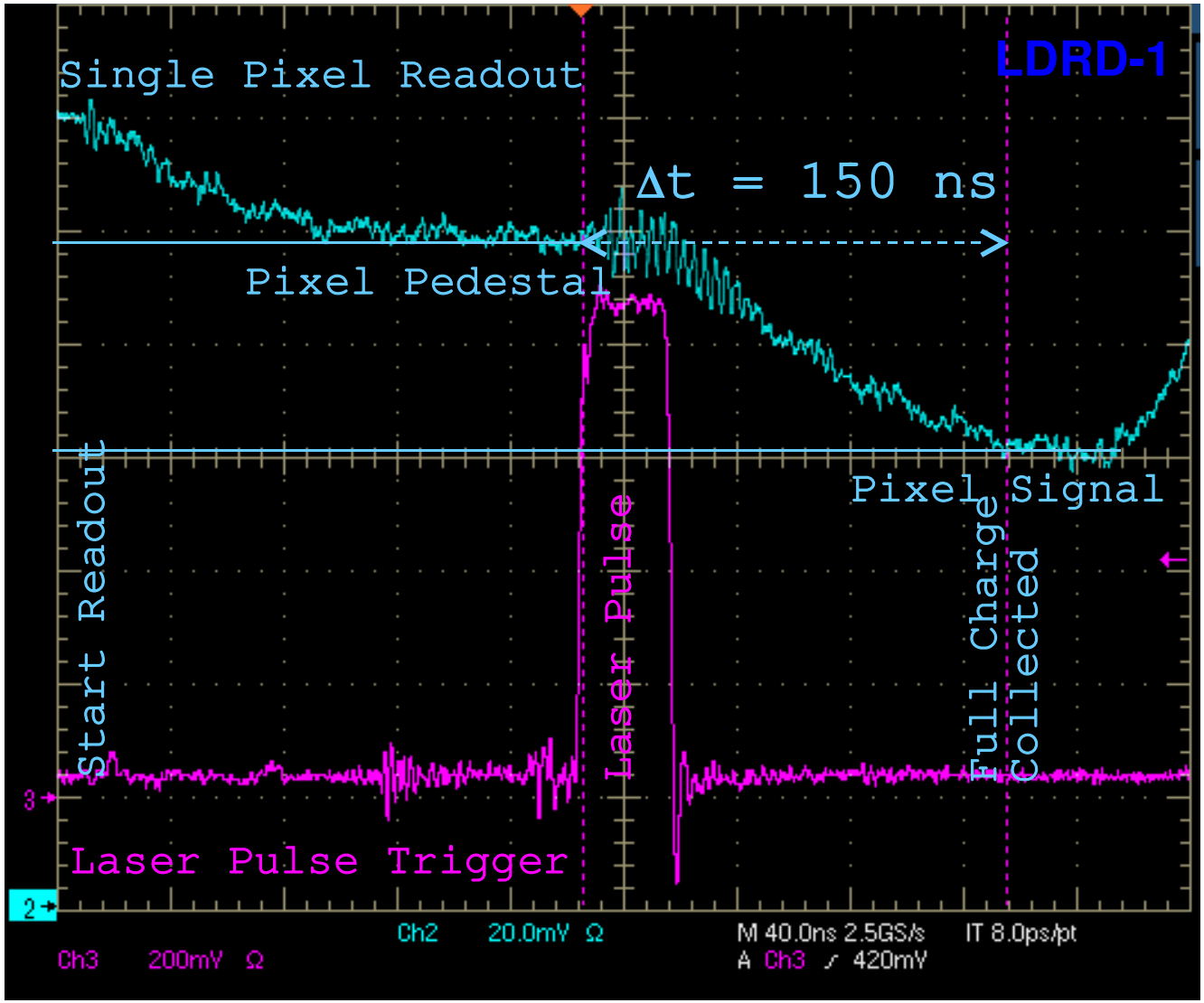




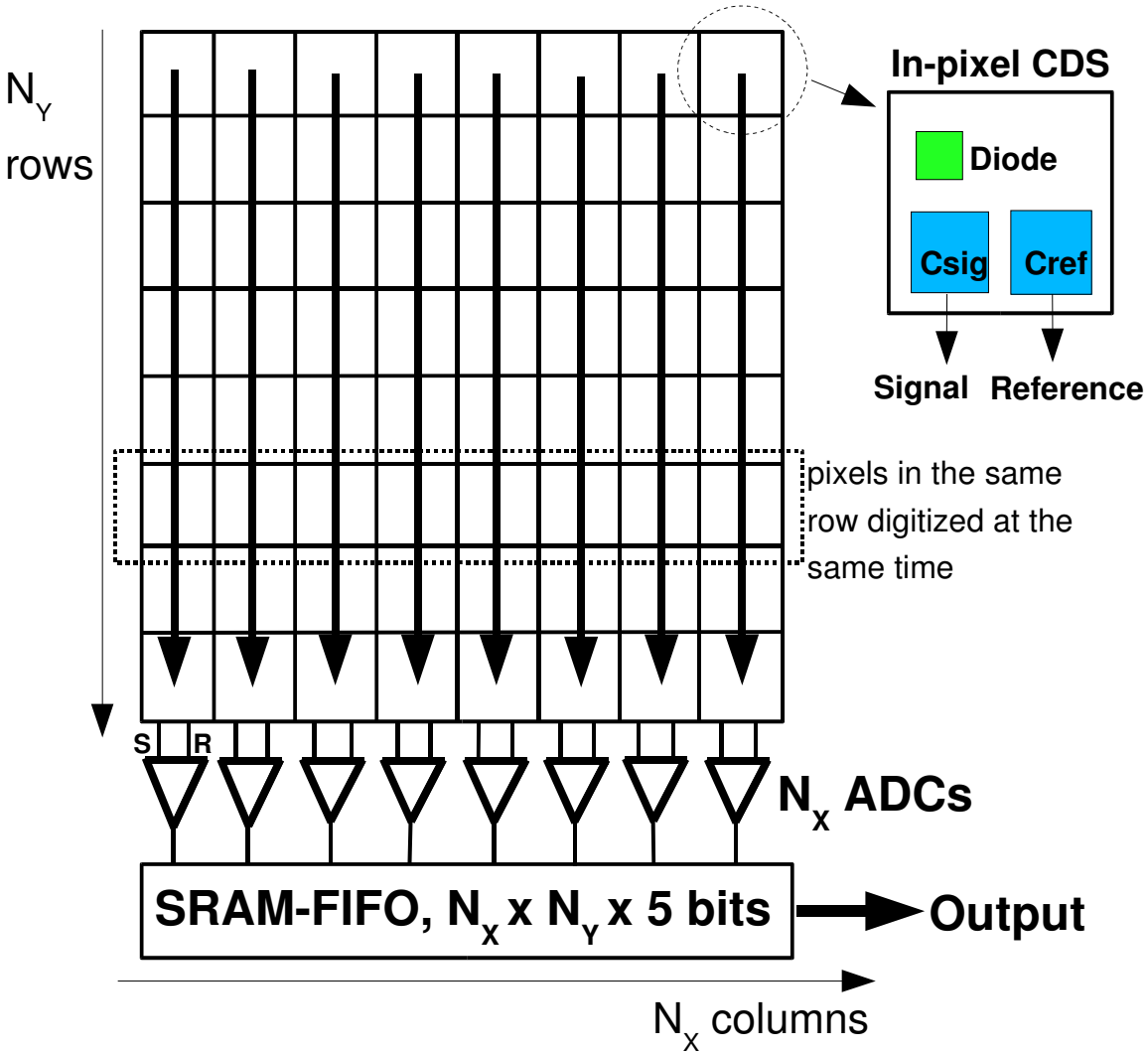
Charge collection time measurement

- First measurement of charge collection time in AMS 0.35 μm OPTO process
- Short (~ns) 1060 nm laser pulse collimated on 20x20 μm^2 pixel (charge = 1 m.i.p.); pulse delayed w.r.t. trigger in order to match pixel readout
- Charge collection time

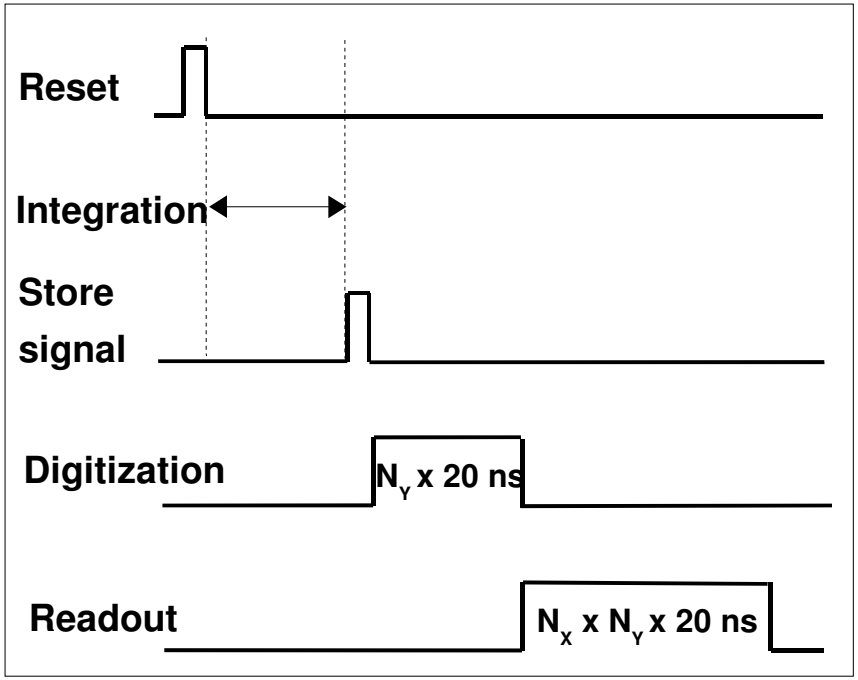
  $\Delta t \sim 150$ ns
- Measurement reproduced both on LDRD-1 and LDRD-2



LDRD-3: integrated ADCs



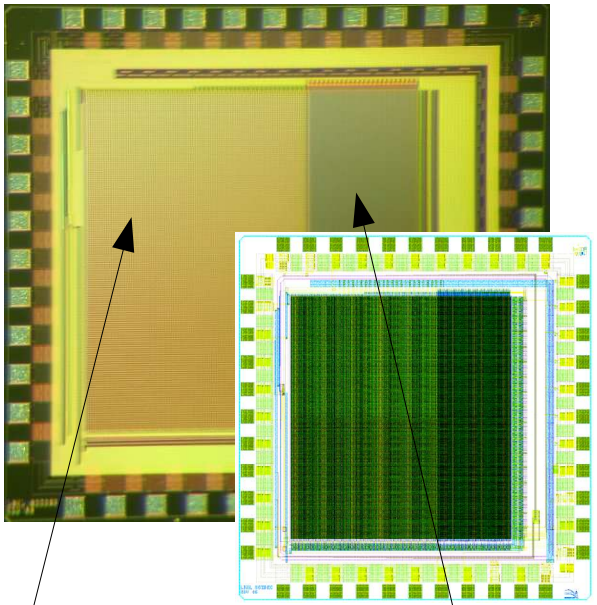
Sample readout scheme @ 50 MHz

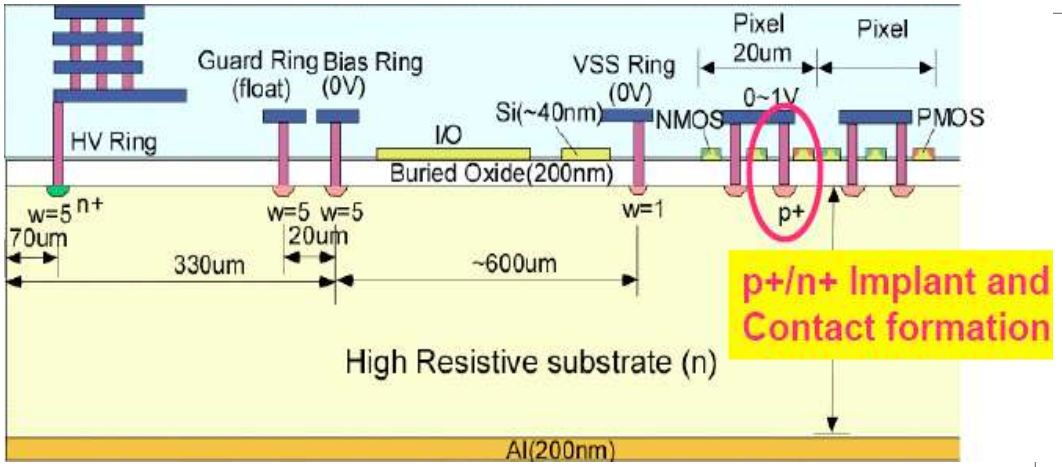


- LDRD-3: next prototype in AMS 0.35 µm OPTO, to be submitted in June/July
- In-pixel CDS
- At the end of each column:
  - 5-bit successive approximation, fully-differential ADCs @ 300 MHz
  - SRAM memory cell

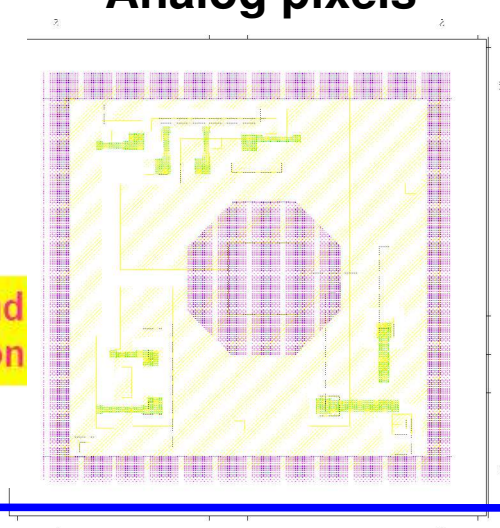
LDRD-SOI pixel prototype

- 0.15 μm OKI fully depleted SOI, 160x150 pixels, 10x10 μm^2 pixels
- 2 analog parts (1.0V and 1.8V, “high” and “low” voltage resp.), 1 digital part; 1x1 μm^2 and 5x5 μm^2 diodes
- Choice of substrate contact and pixel layout justified by TCAD simulations (see next)
- Submitted in Dec. '06 through KEK; pilot run, not optimized in terms of leakage current; optimized run to follow in Fall '07
- Chip received May '07: tests underway

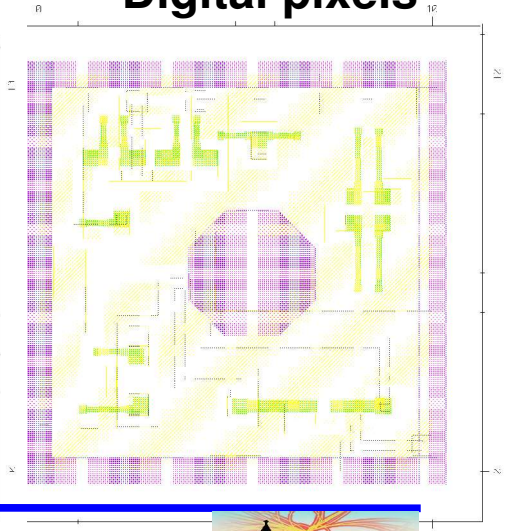




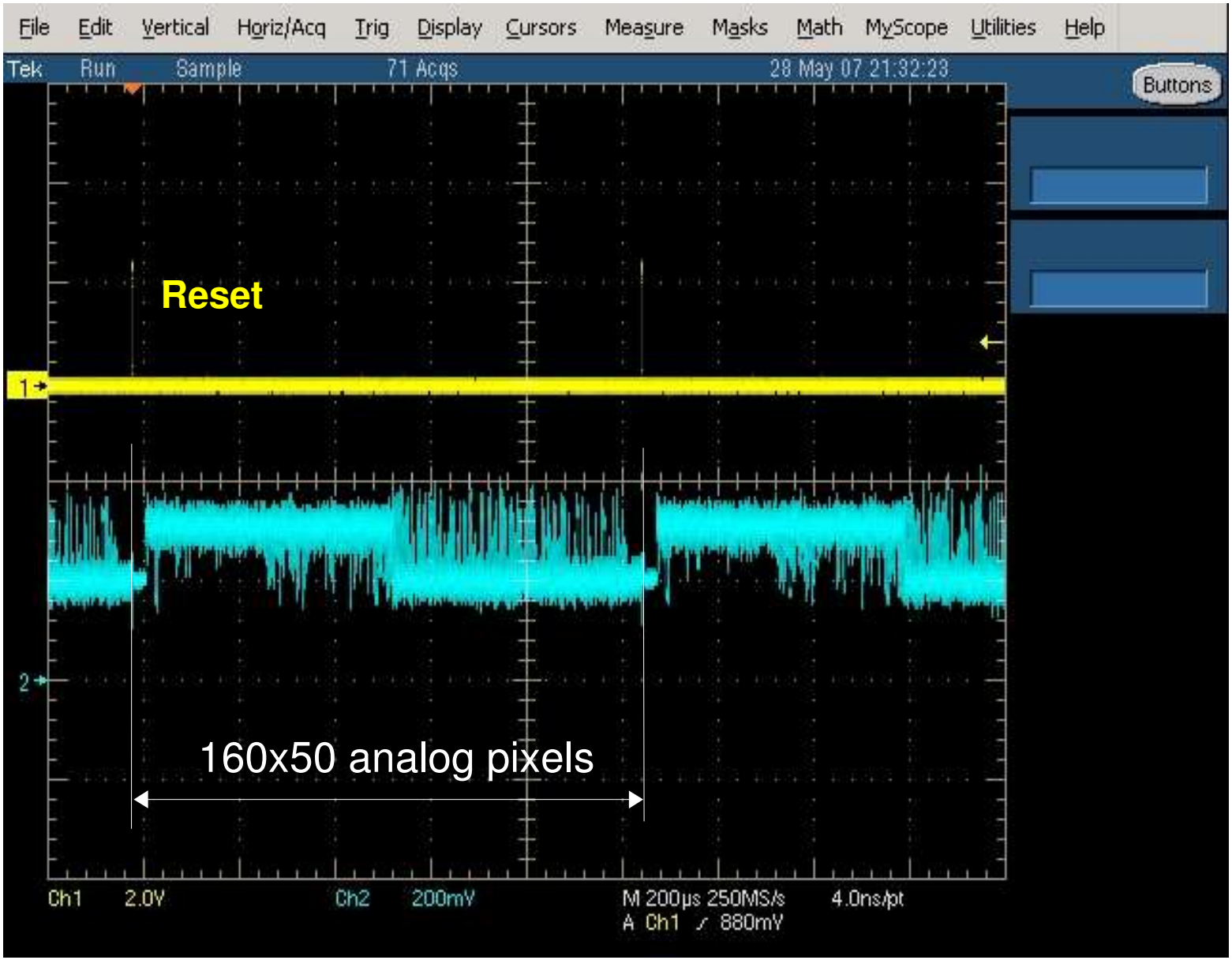
Analog pixels



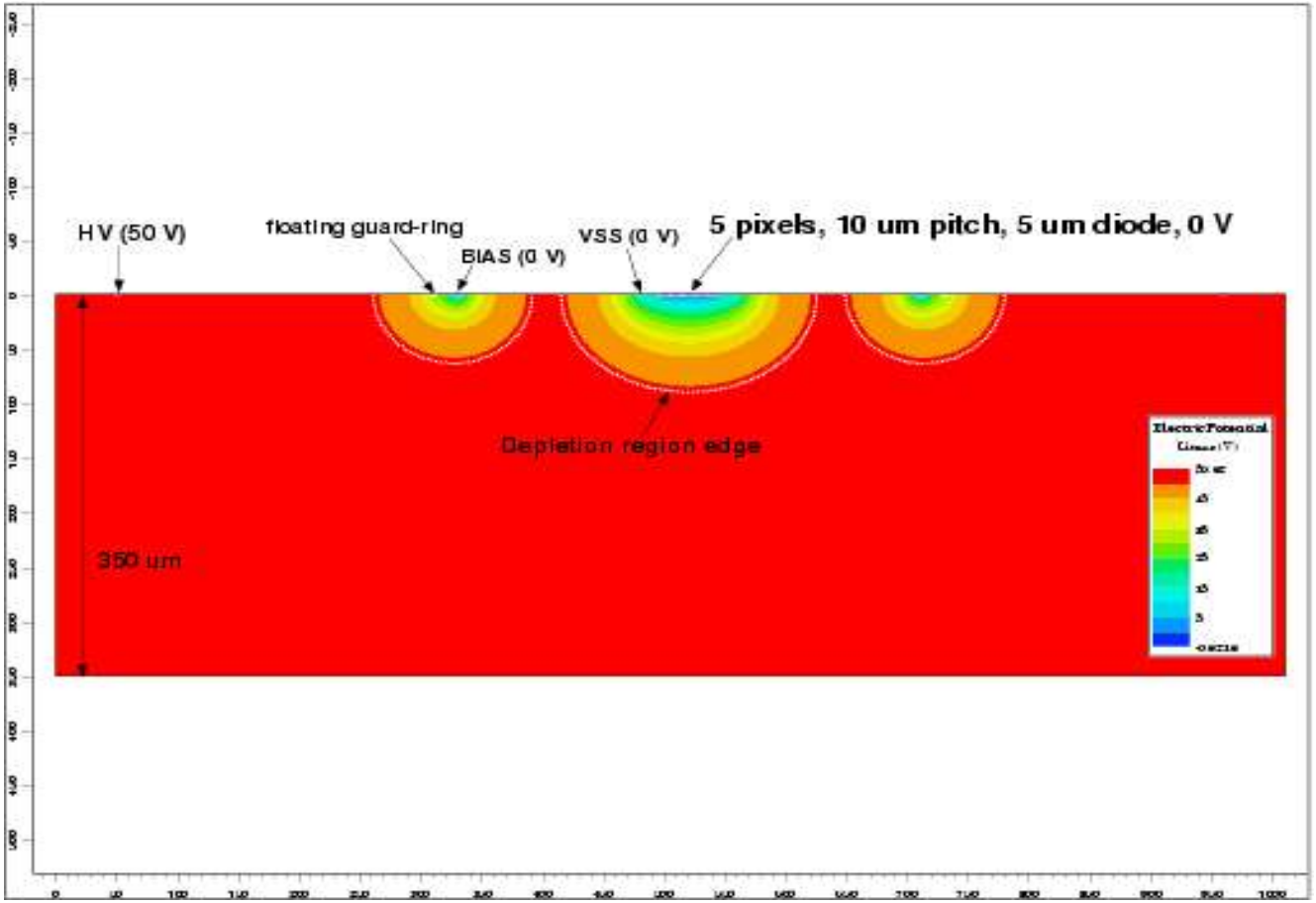
Digital pixels



First signals from LDRD-SOI



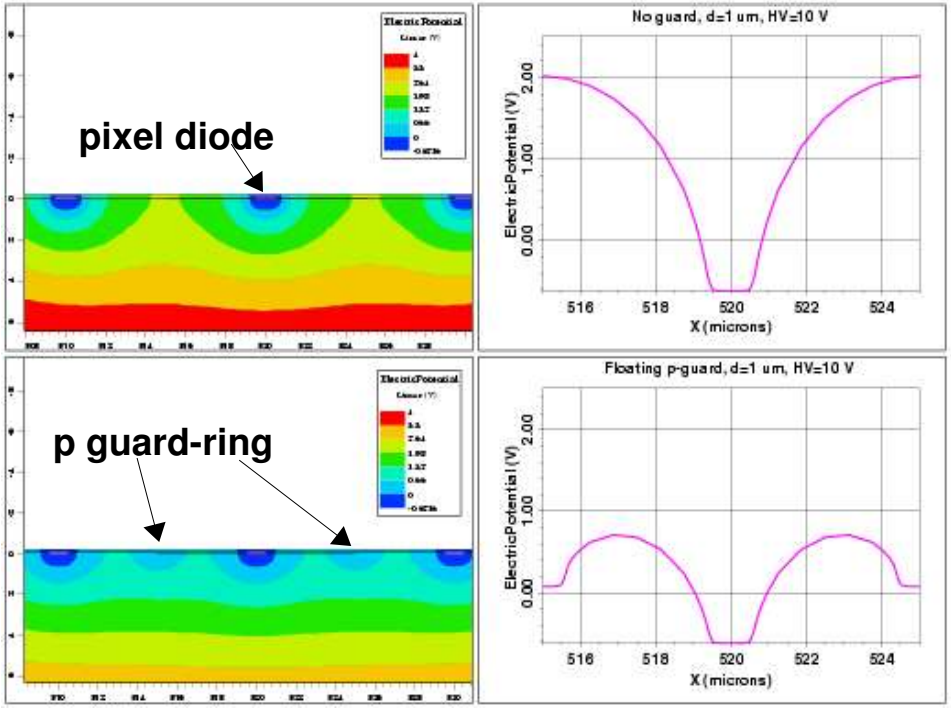
TCAD simulations



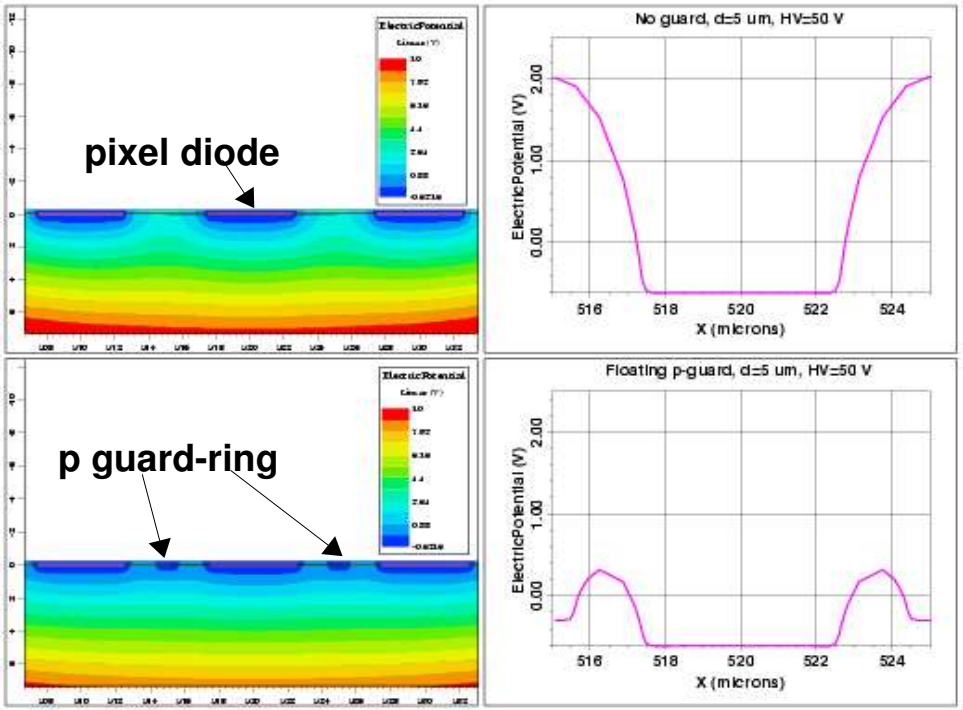
- Simulation performed with Synopsys TCAD (Taurus Device)
- 2D model of 5 pixel cluster (10 µm pixel pitch) and substrate contact regions
- 350 µm thick substrate, n-type silicon (6×10^{12} cm^{-3}); 200 nm buried oxide
- Different diode sizes (1×1 µm^2 and 5×5 µm^2)

Surface potential, choice of pixel guard-ring

1×1 µm² diode, HV=10 V

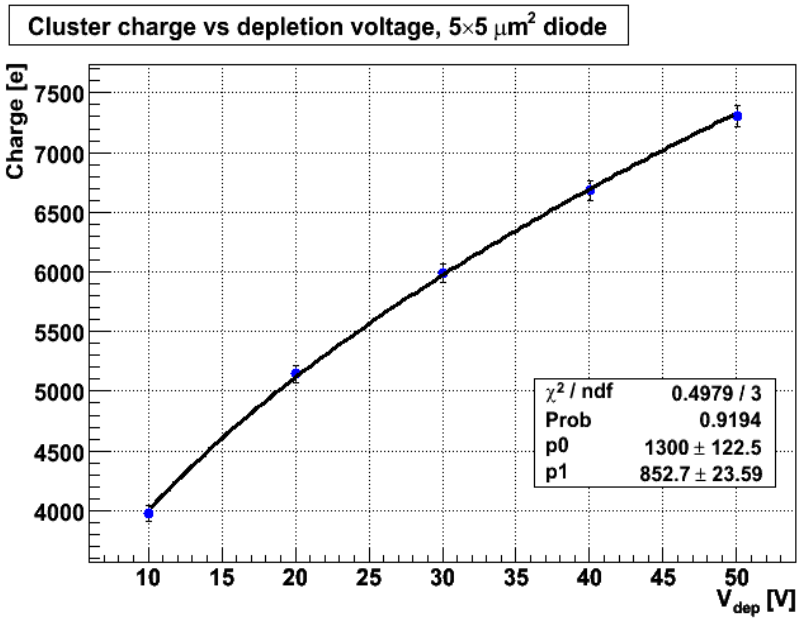


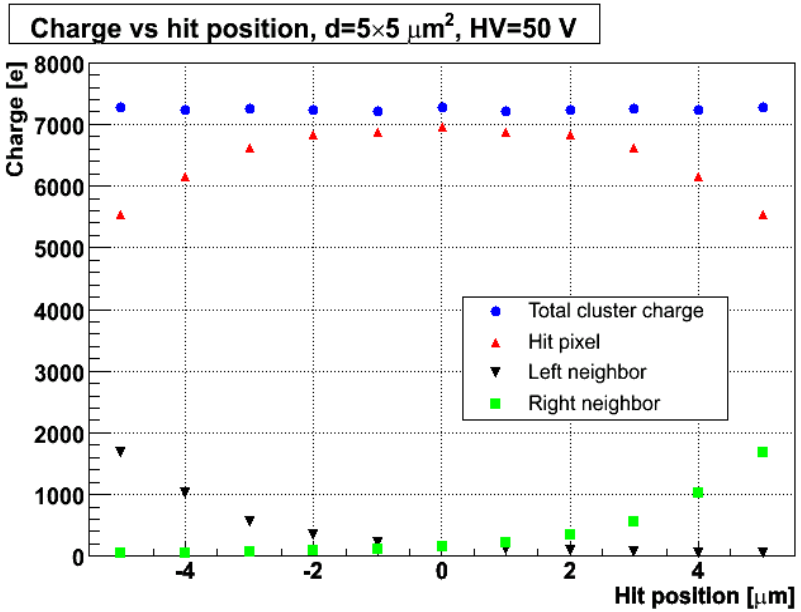
5×5 µm² diode, HV=50 V



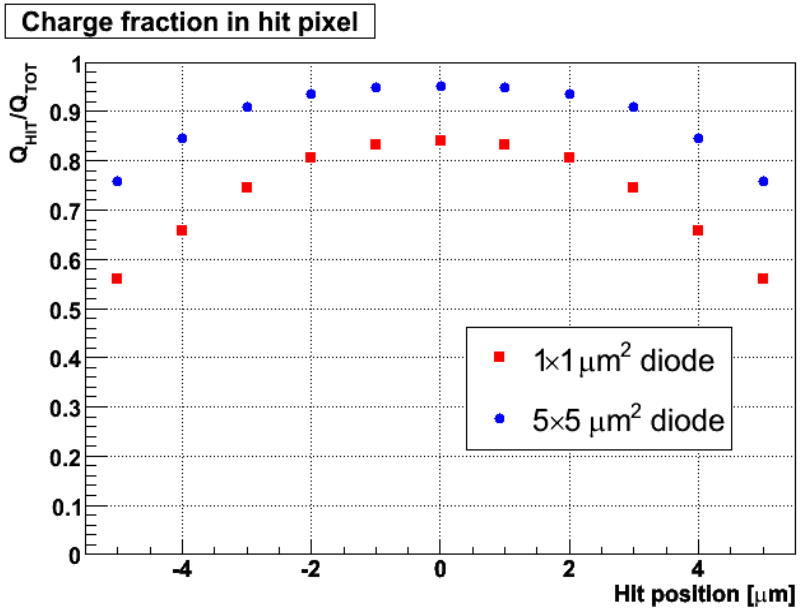
- Pixel surface potential for different diode sizes and depletion voltages
- Potential in-between pixels too high, especially for smaller diode size
- Add floating p-guard structure (1 µm wide) to keep potential low and limit back-gate effects on MOS transistors on top of buried oxide

Charge collection simulation





- Simulate passage of m.i.p. (80 e-h/μm) and charge collection in 5 pixel cluster
- Study collected signal as a function of depletion voltage and of track position within hit pixel
- Total cluster signal ~constant as a function of position within hit pixel
- Most of the charge is collected in hit pixel, expect larger cluster size for smaller diode pitch



Conclusions & Outlook

- Two prototypes of LDRD family produced and tested, exploring various pixel designs and architectures; submission of next prototype with CP readout and 5-bit ADC in Summer

- First prototype in OKI 0.15 µm SOI technology just received, tests underway; next prototype submission in Fall '07 with optimized process. Spin-off of SOI technology for beam instrumentation and diagnostics for LOASIS; plans for tests with low momentum electrons and tunable beam energy

- Tracking tests at forthcoming beam-test at FNAL with 100 GeV p in June/July, employing new 4-plane beam telescope with 50 µm thin CMOS pixel sensors (see M. Battaglia's talk)

- Collaborative efforts with other institutions: DEPFET irradiation with MPI Munich, development of new readout system with INFN Padova, FNAL test-beam with Purdue University and INFN Padova