Tracking and Vertexing
with a Thin CMOS Pixel BeamTelescope and Thin Ladder Studies

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CMOS Pixel Back-thinning

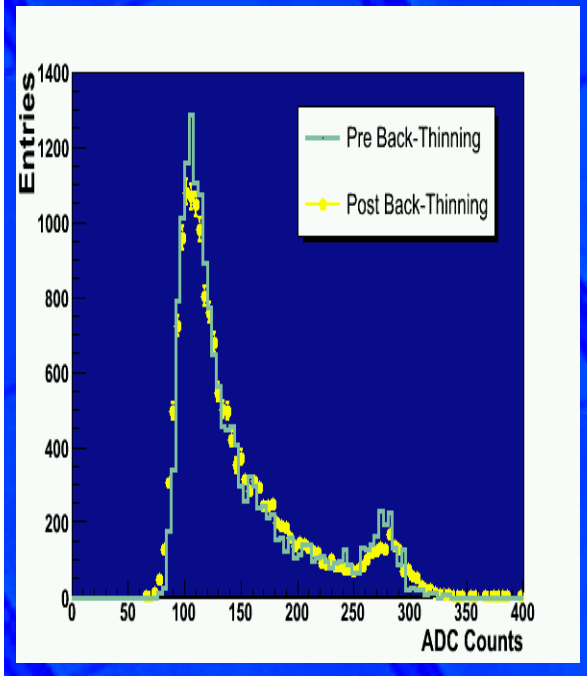
Program of back-thinning of diced chips using grinding process by APTEK;

Thinned over 15 chips,
yield of functional chips~90%,
Process reliable down to 40 μm
Measured thickness of chips:

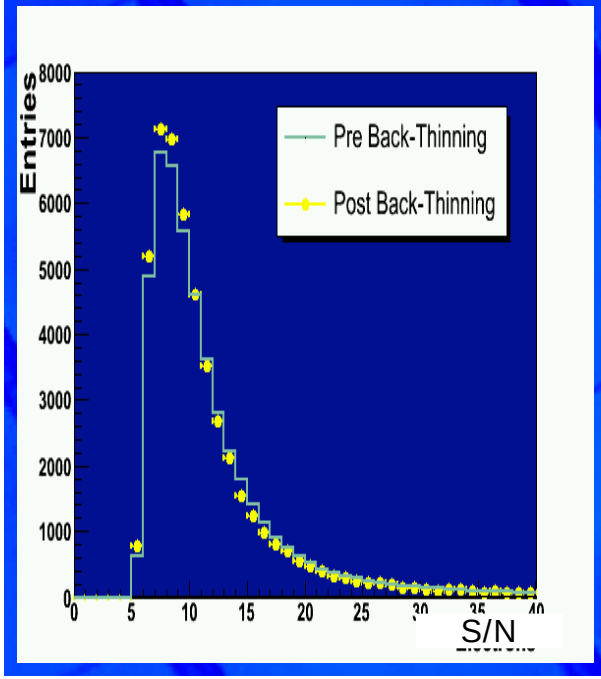
Before	550 ± 0.5
"50 μm"	50 ± 7
"40 μm"	41 ± 6

Study change in charge collection and S/N before/after back-thinning: MIMOSA 5 sensors (1 M pixels, 17 μm, 18x18 mm² surface, AMS 0.6)

^{55}Fe
Determine chip gain and S/N for 5.9 keV X rays



1.5 GeV e⁻ beam
Determine S/N and cluster size for m.i.p.

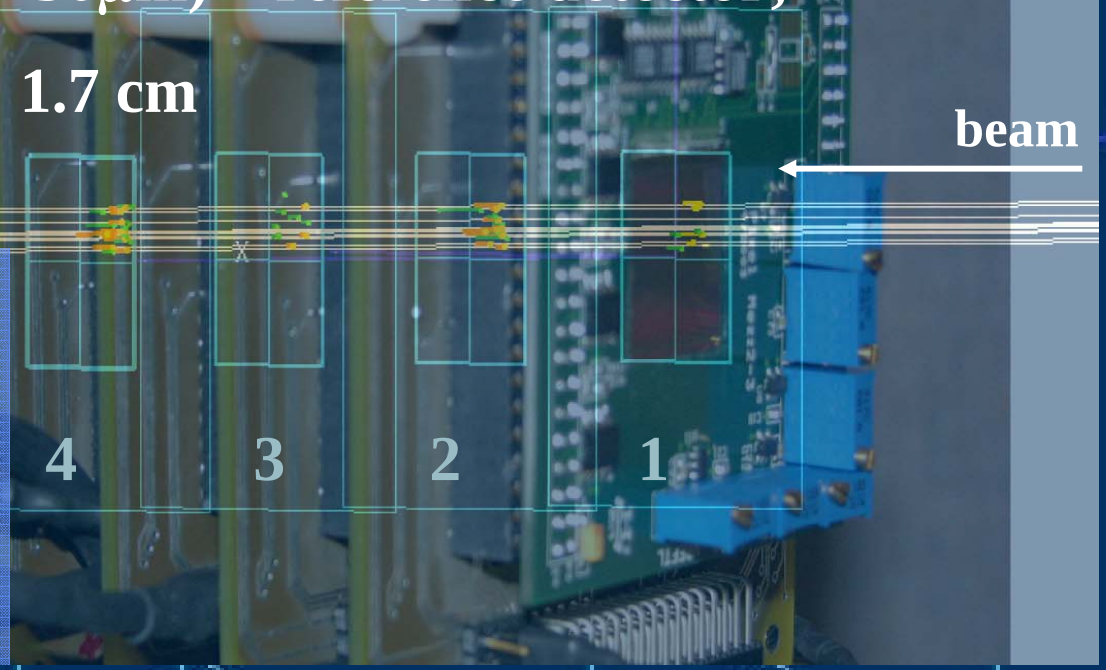


Feasibility of Back-thinning CMOS sensors demonstrated

The LBNL Thin Pixel Pilot Telescope

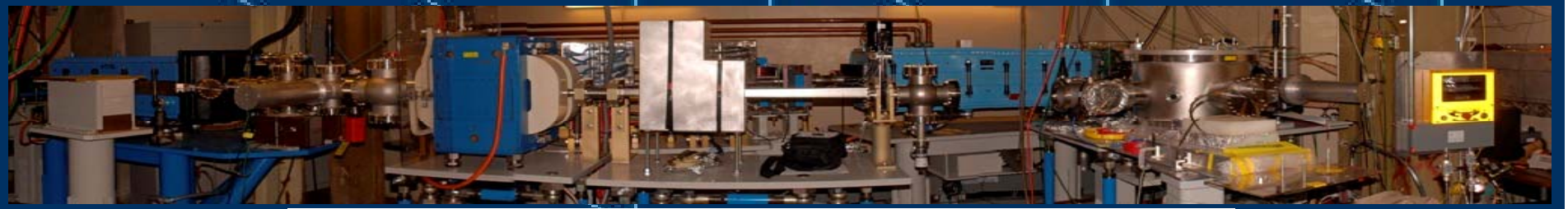
Layout: 3 layers of thin Mimosa 5 sensors (17μm pixels) (40μm + 50μm + 50μm) + reference detector;

Sensor spacing: 1.7 cm



- First beam telescope based on thin pixel sensors;
- Prototype for proposed FNAL MBTF telescope & T966;
- System test of multi-M pixel detector in realistic conditions.

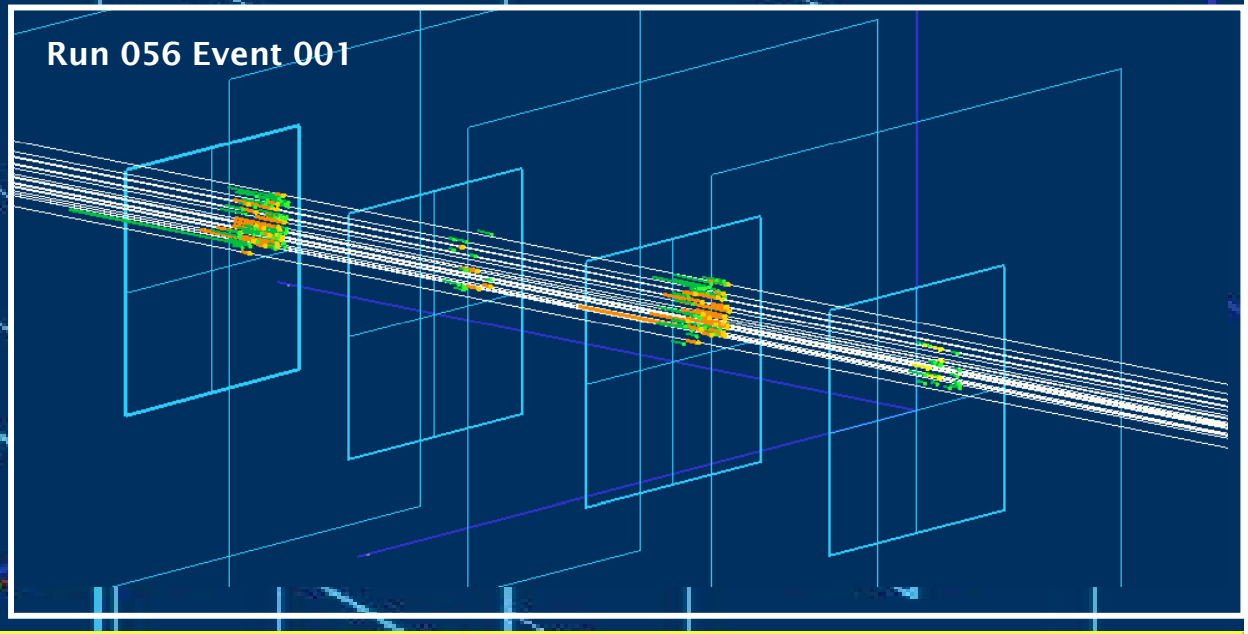
Beam: 1.5 GeV e^- from ALS booster at BTS

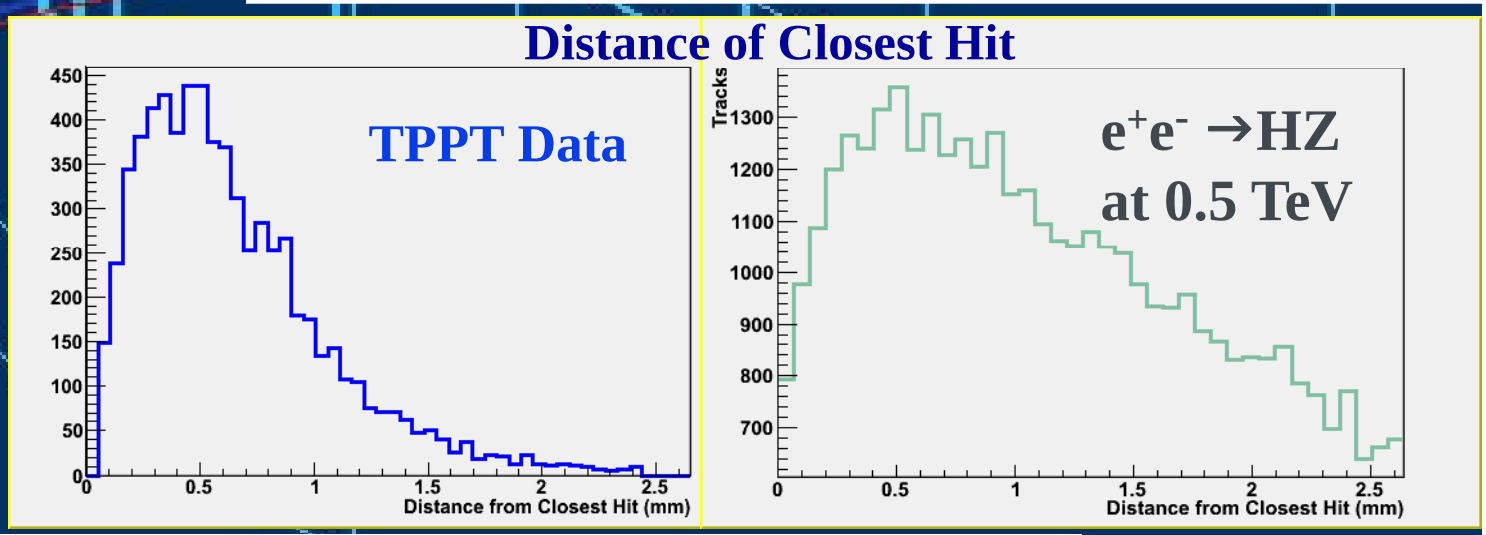


Thin Pixel Pilot Telescope

TPPT allows us to perform detailed studies of ILC VTX particle tracking with various, controllable, levels of track density (0.5-5 tracks mm^{-2}) under realistic conditions;

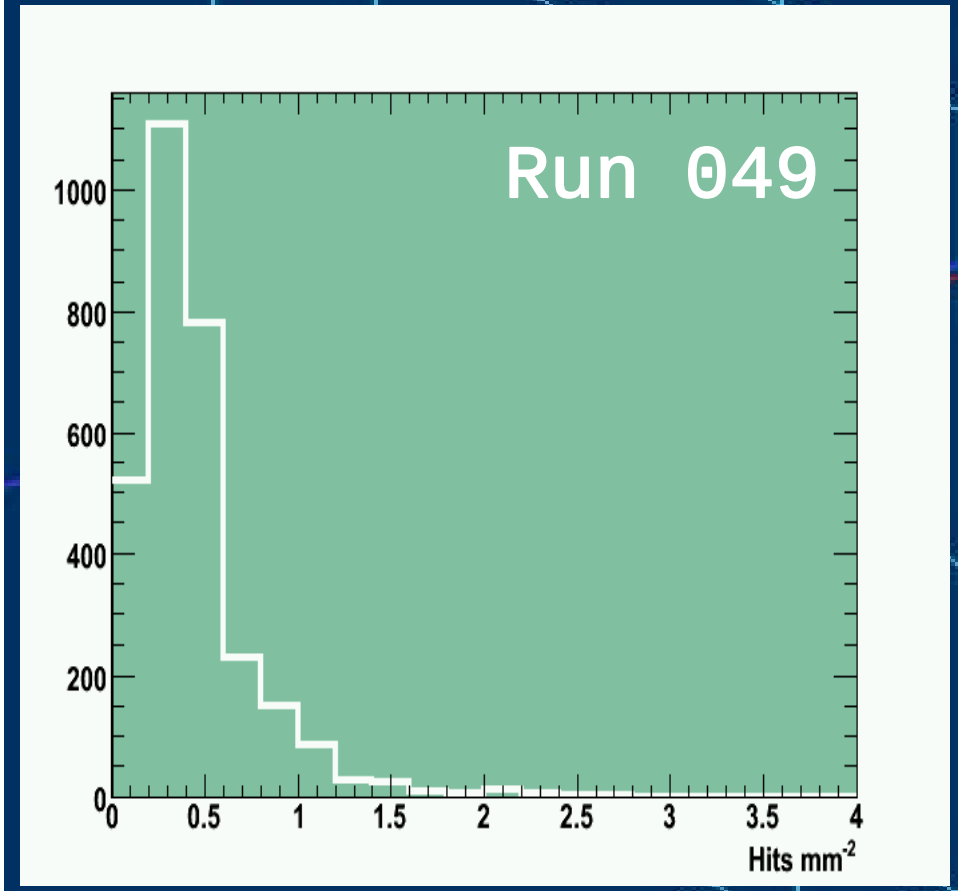
TPPT layout chosen to resemble ILC VTX.

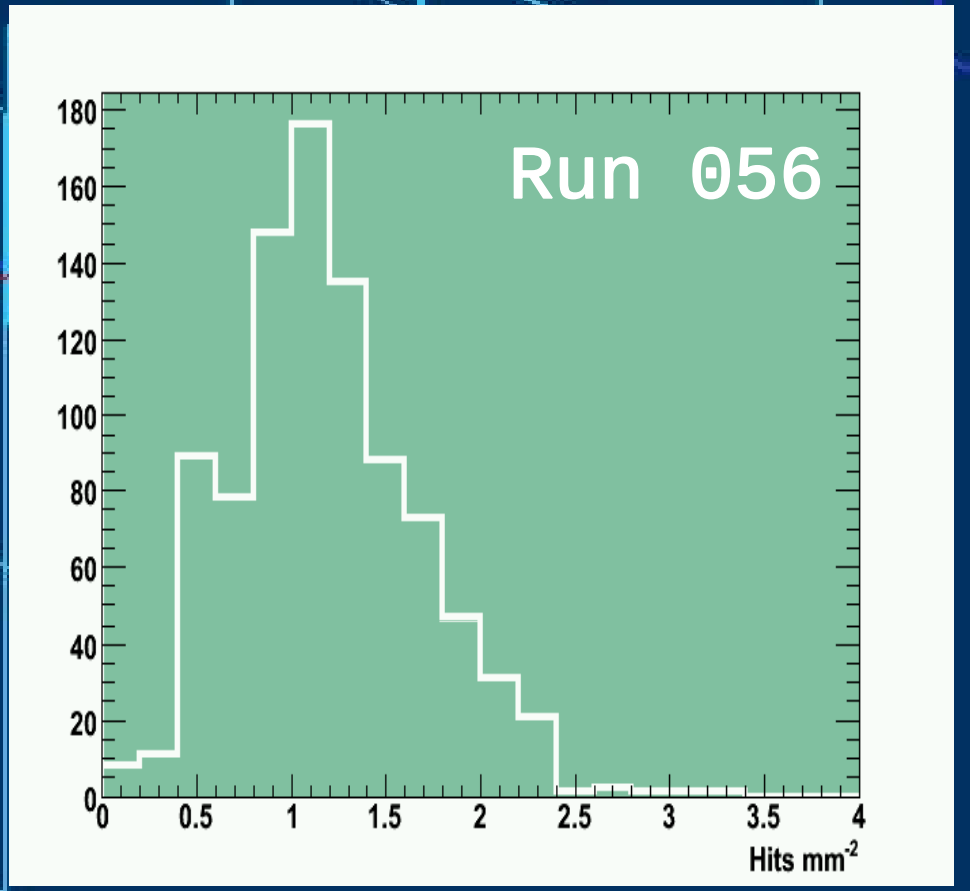




Thin Pixel Pilot Telescope

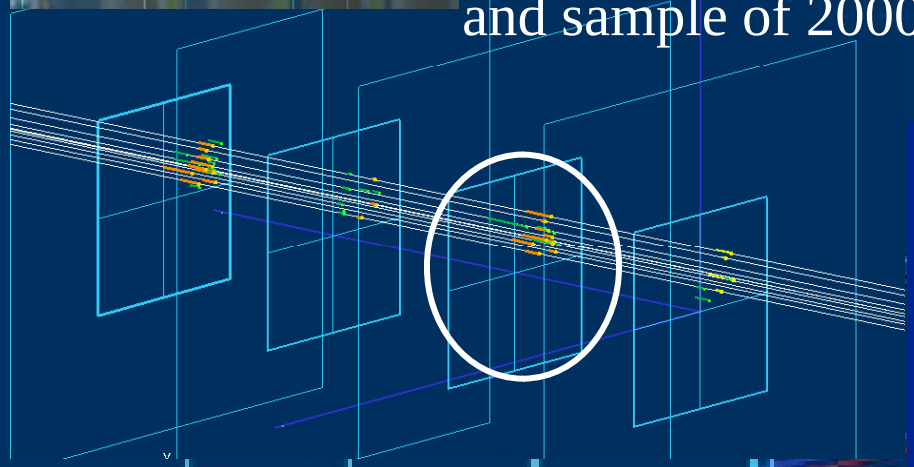
Hit density on TPPT Layer 1

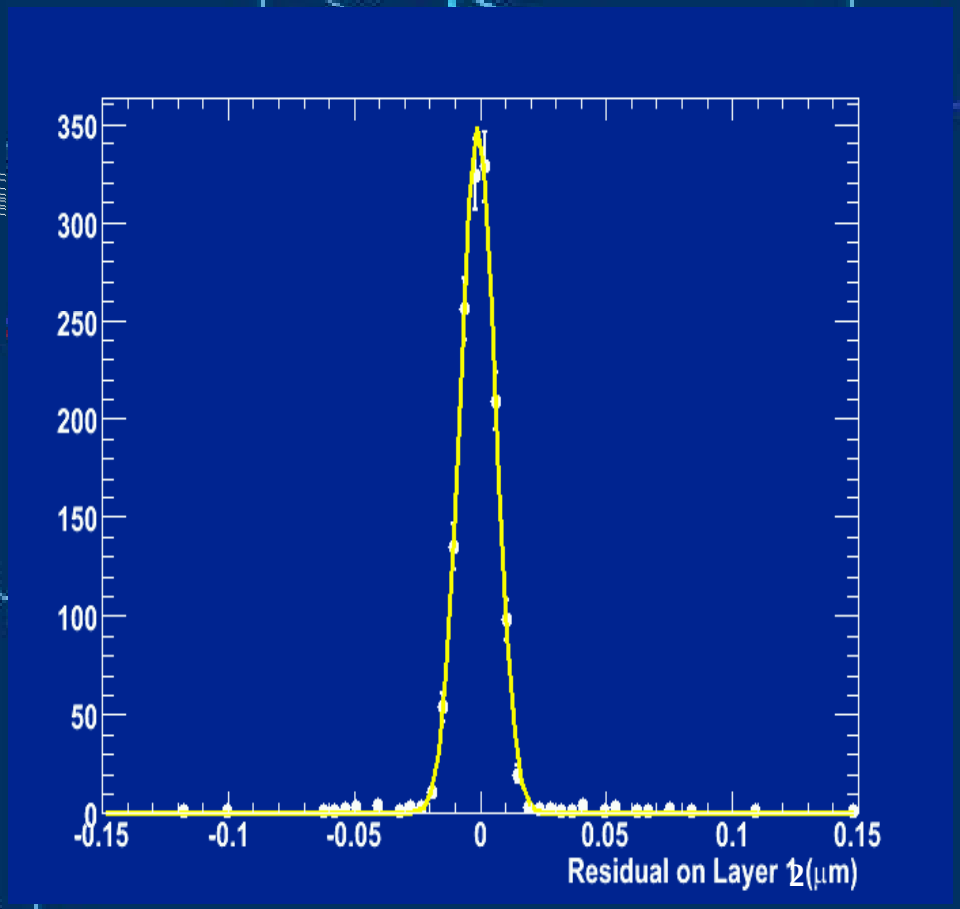




Thin Pixel Pilot Telescope

Alignment performed using ATLAS optical survey machine and sample of 20000 tracks;

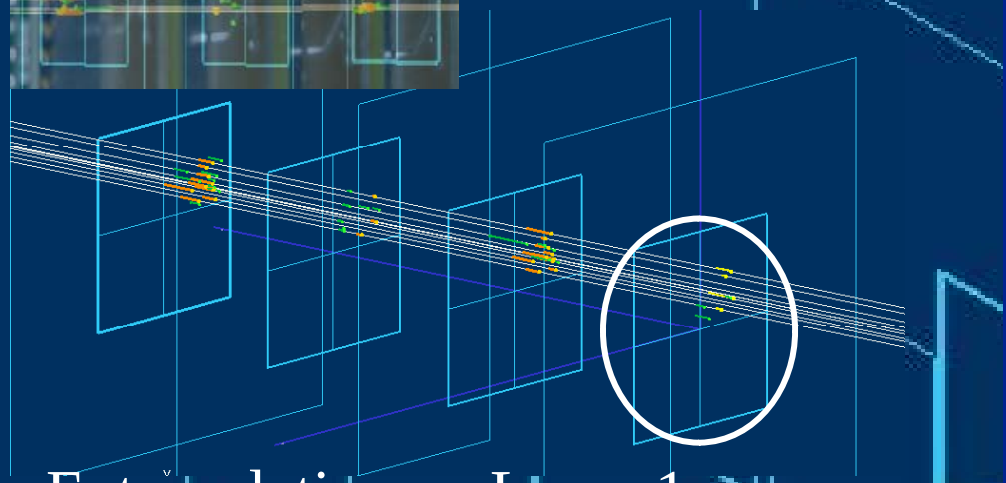




Extrapolation on Layer 2:
Residuals in X

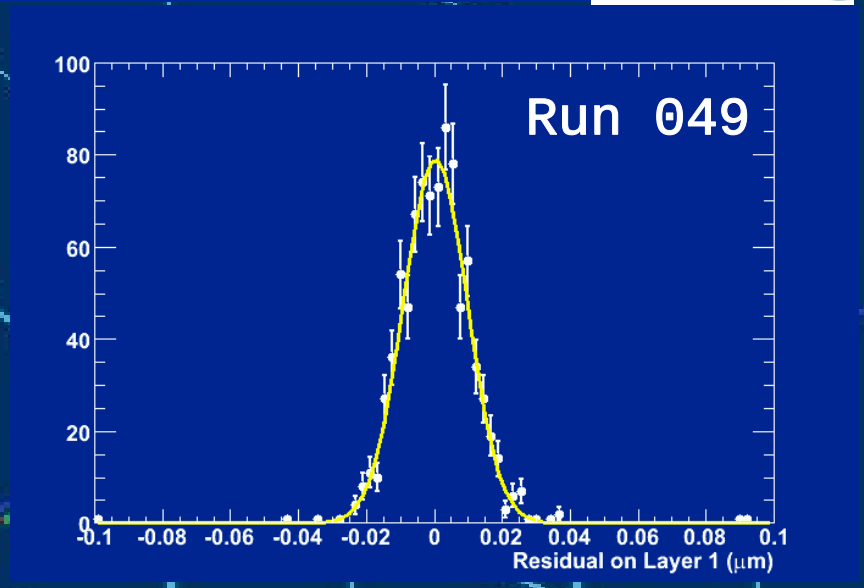
$(6.9 \pm 0.1)\ \mu m$

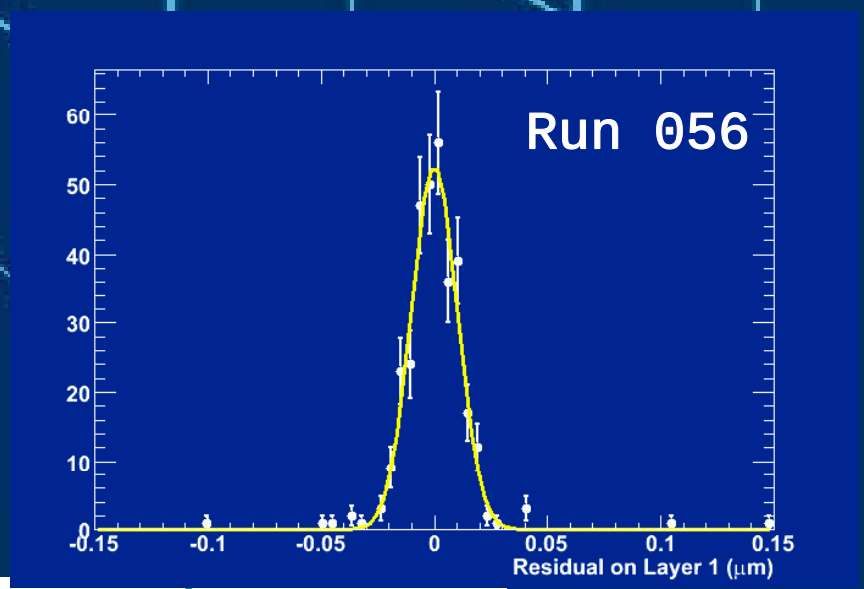
Thin Pixel Pilot Telescope



Extrapolation on Layer 1:

Track Sample	Residual (μm)
2+3 Hits Tracks	9.4 ± 0.2
3 Hits Tracks	8.9 ± 0.5
Low Density	9.2 ± 0.2
High Density	9.9 ± 0.5

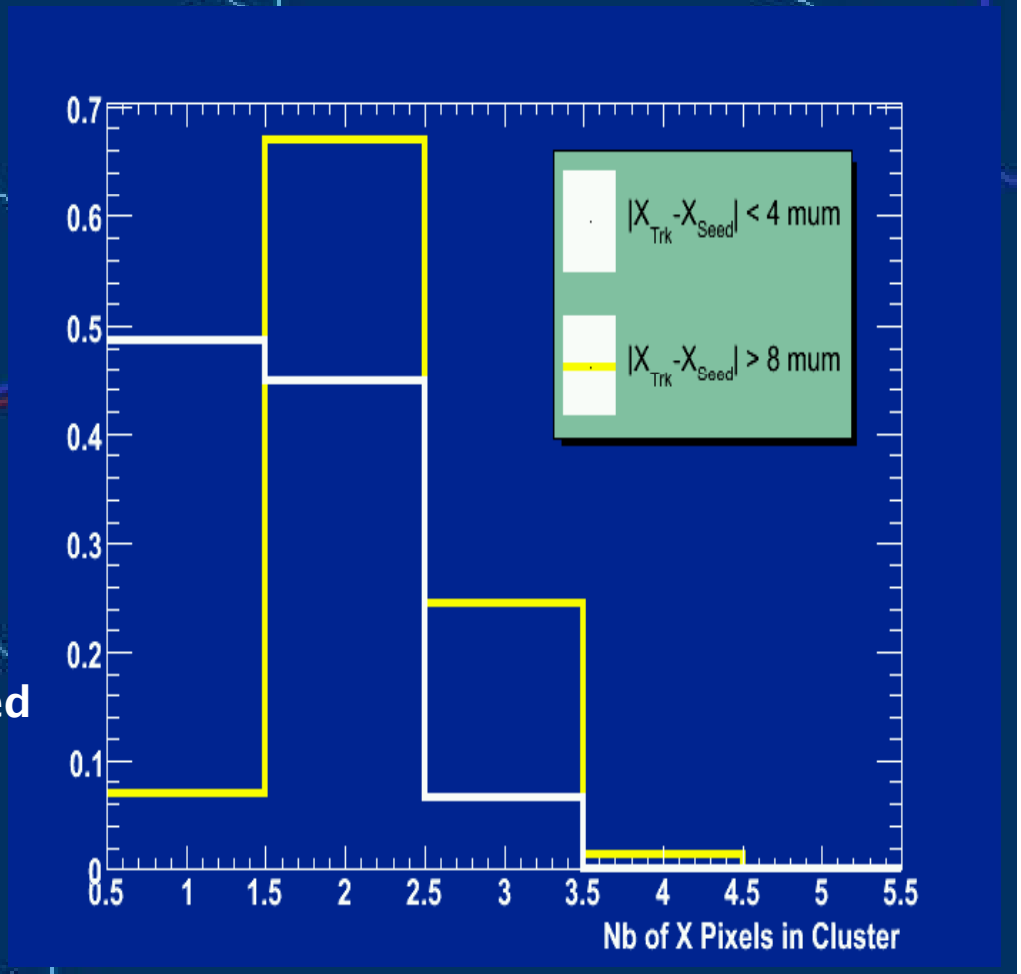




Thin Pixel Pilot Telescope

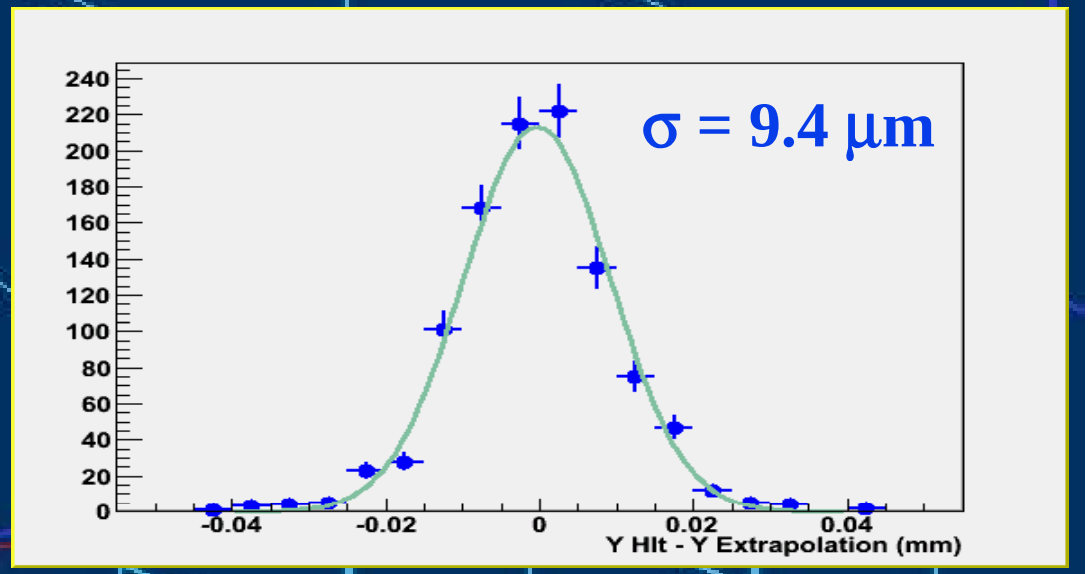
Cluster Shape vs. Track Point of Impact

Despite m.s. limitations, extrapolation resolution is << pixel size allowing some studies of cluster shape vs. track point of impact:

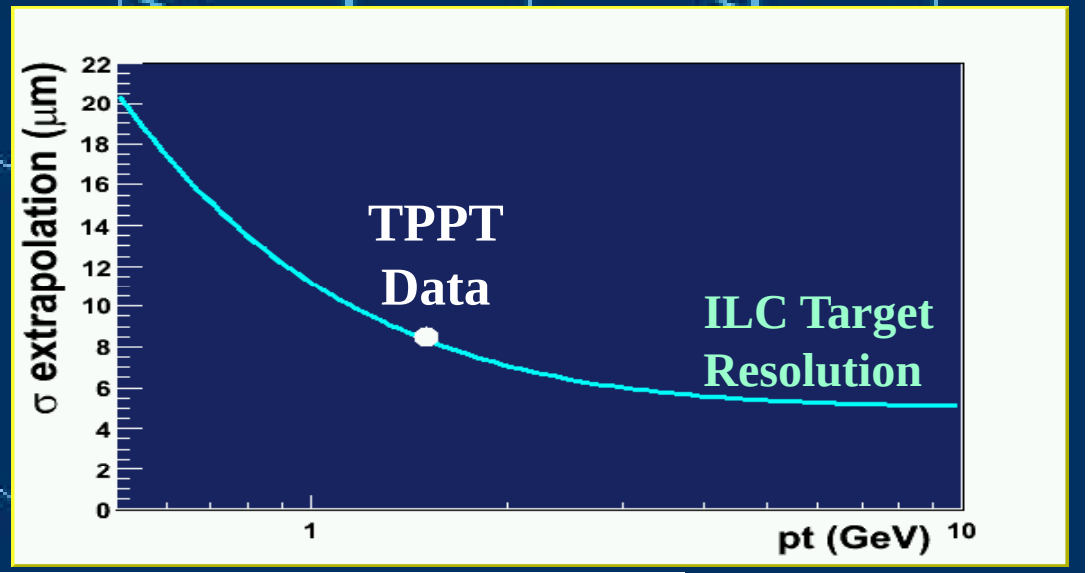


Thin Pixel Pilot Telescope

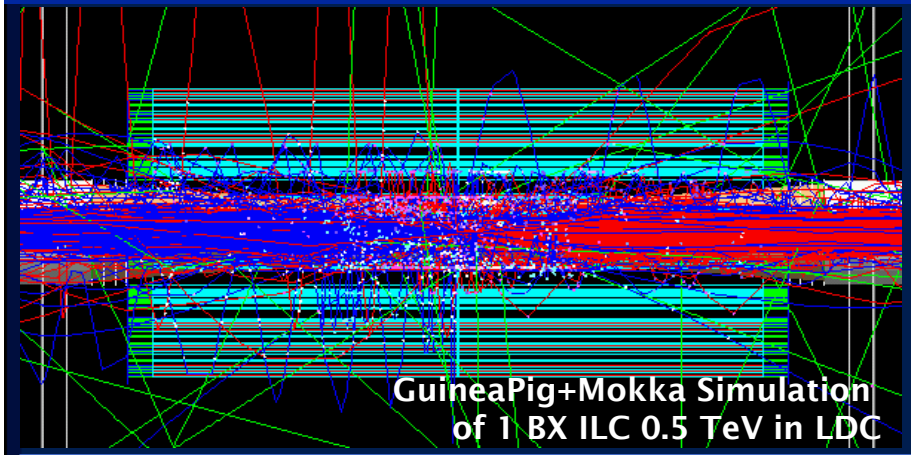
Estimate extrapolation resolution to IP from TPPT data at ALS by unfolding MIMOSA5 resolution (from `G4+Marlin`)

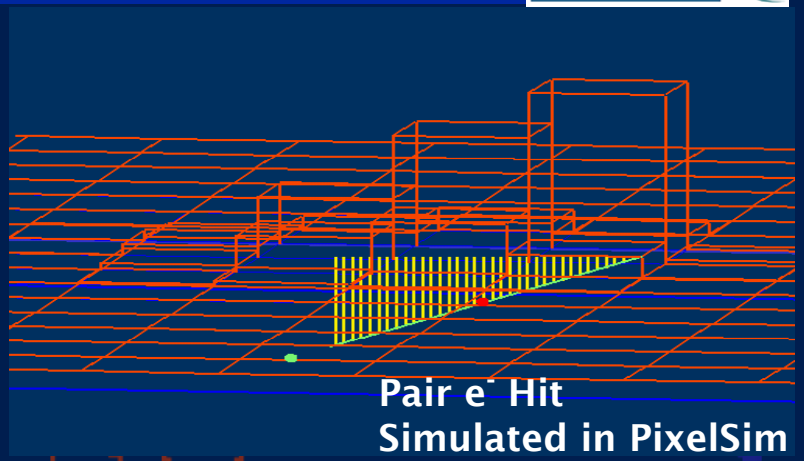


Extrapolation Resolution on Layer 1: σ = 8.5 μm
<u>matches ILC requirements</u>.

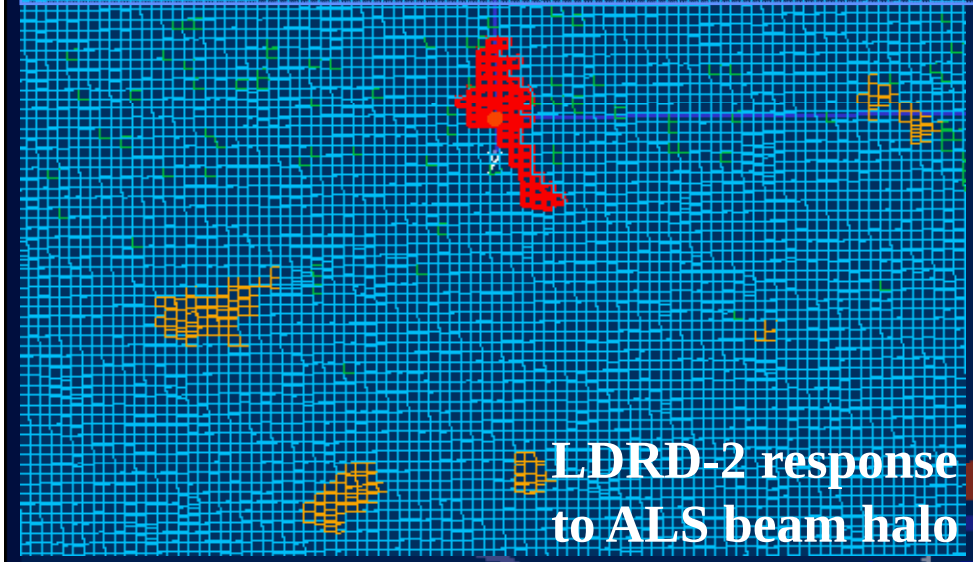


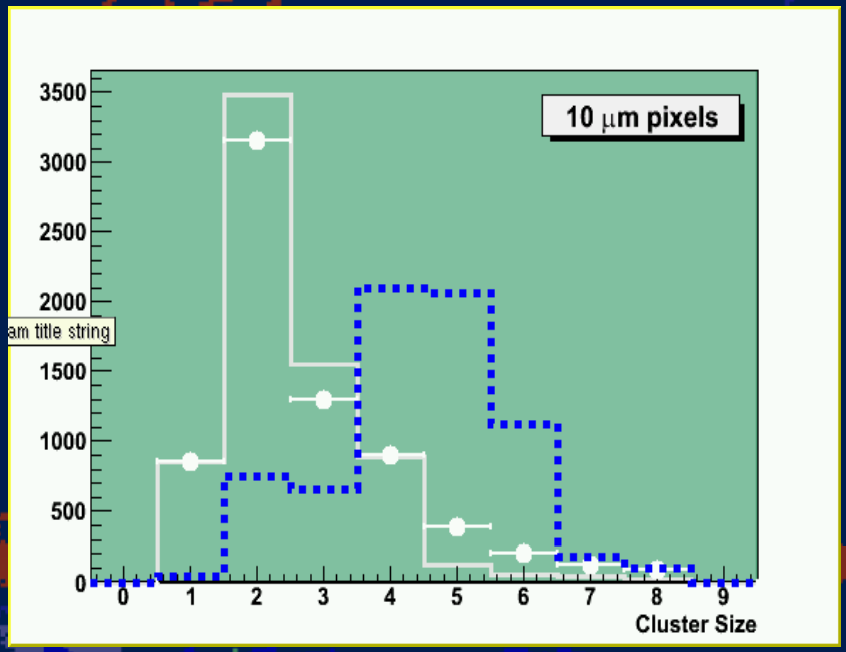
Response to Pair Background



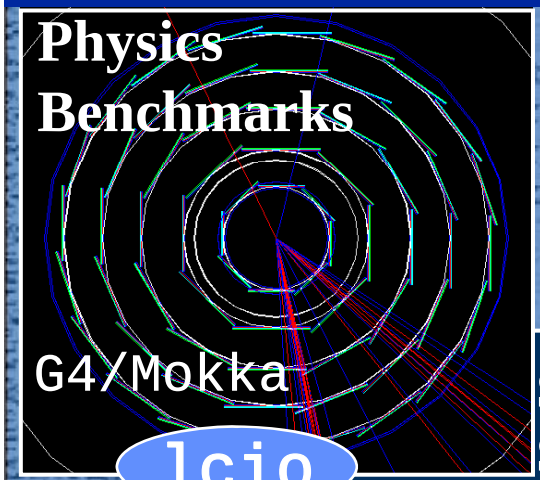


Beam tests using 0.05 - 1.0 GeV e^- beams at **LOASIS** and **ALS** to validate simulation.



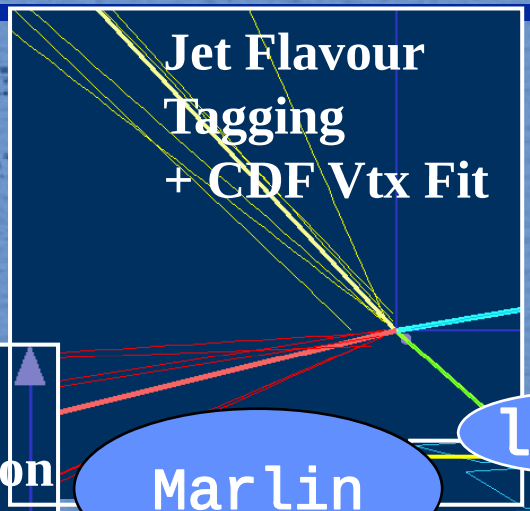


VTX Simulation, Reconstruction, Analysis



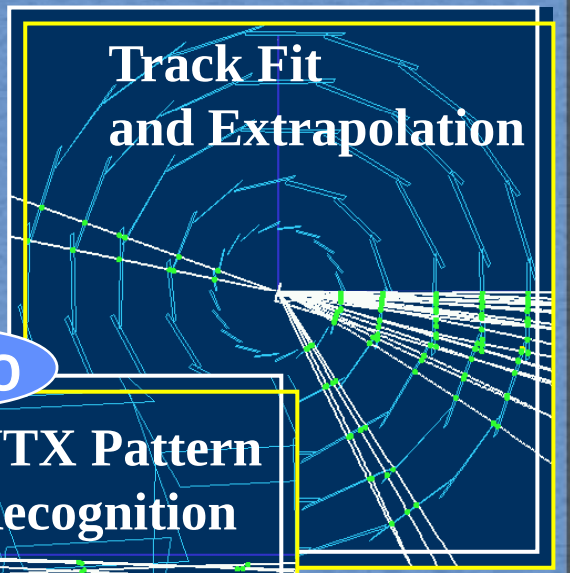
lcio

Sensor
Simulation

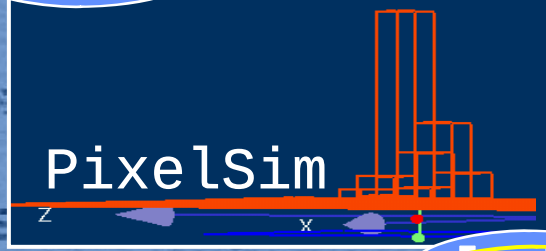


Marlin

lcio



VTX Pattern
Recognition



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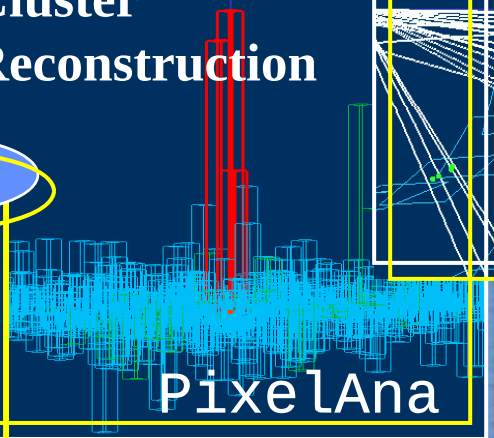
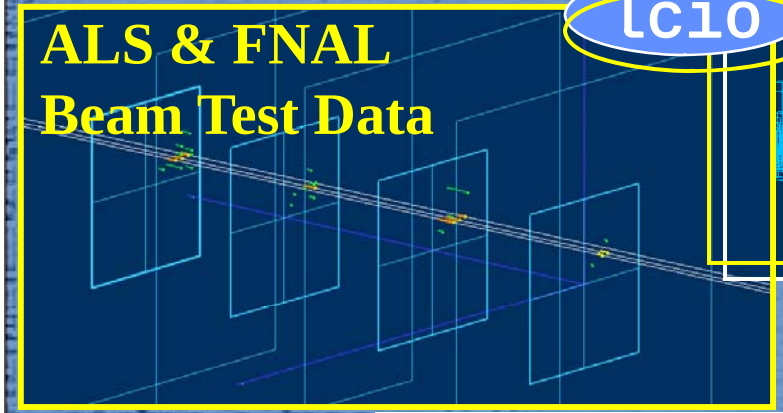
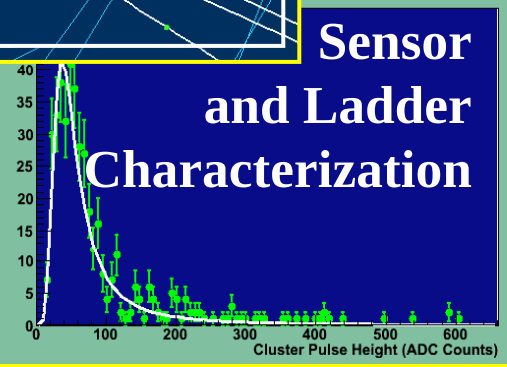
Cluster
Reconstruction







T-966 Beam Test Experiment at Fermilab

Beam Test at FNAL MBTF 120 GeV p beam-line (T-966) (June 25-July 8,2007)
(UC Berkeley + LBNL + INFN Padova + Purdue U Collaboration)

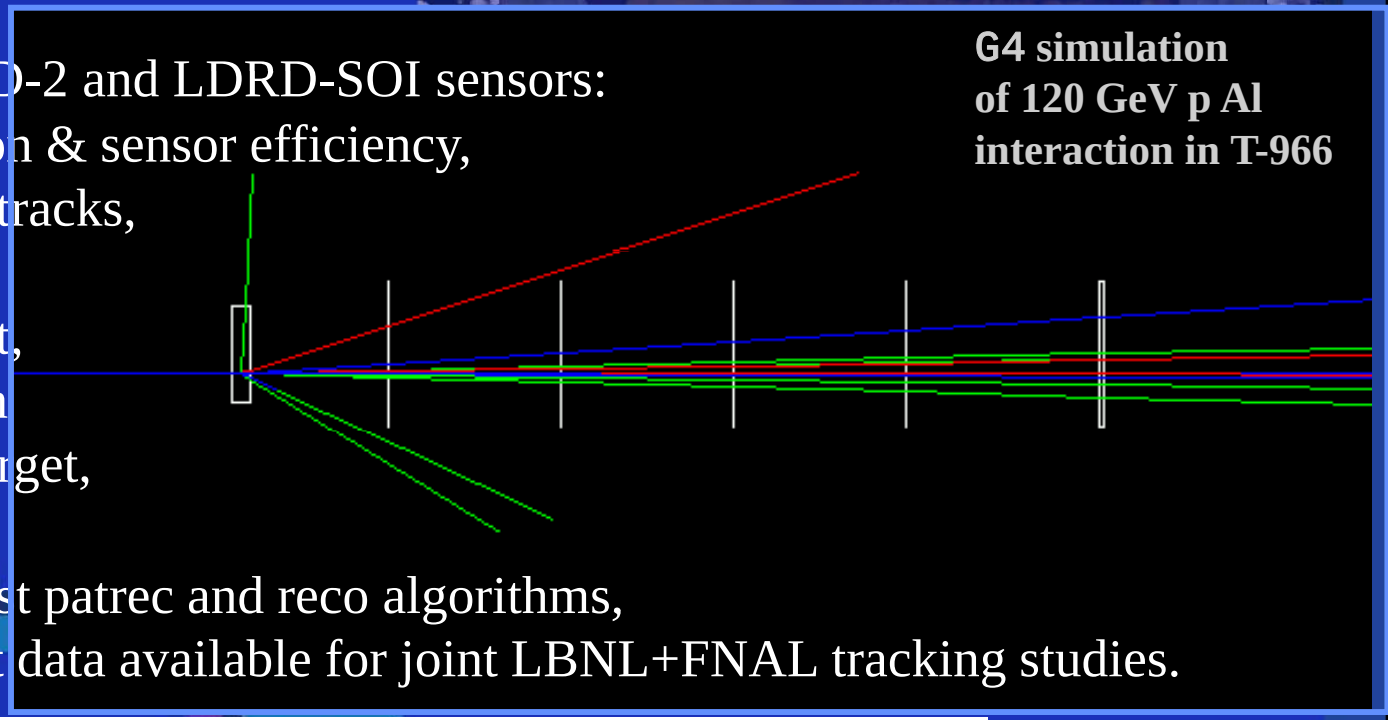
Deploy two pixel beam telescope:

- TPPT-2 telescope: 4 layers of 50μm thick MIMOSA-5 sensors,
- LDRD telescope: 4 layers of LDRD-2 sensors,

ILC-like geometry, extrapolation resolution on 1st plane ~ 1μm

Study LDRD-1, LDRD-2 and LDRD-SOI sensors:

- single point resolution & sensor efficiency,
- response to inclined tracks,
- tracking capabilities in dense environment,
- vertex reconstruction accuracy with thin target,

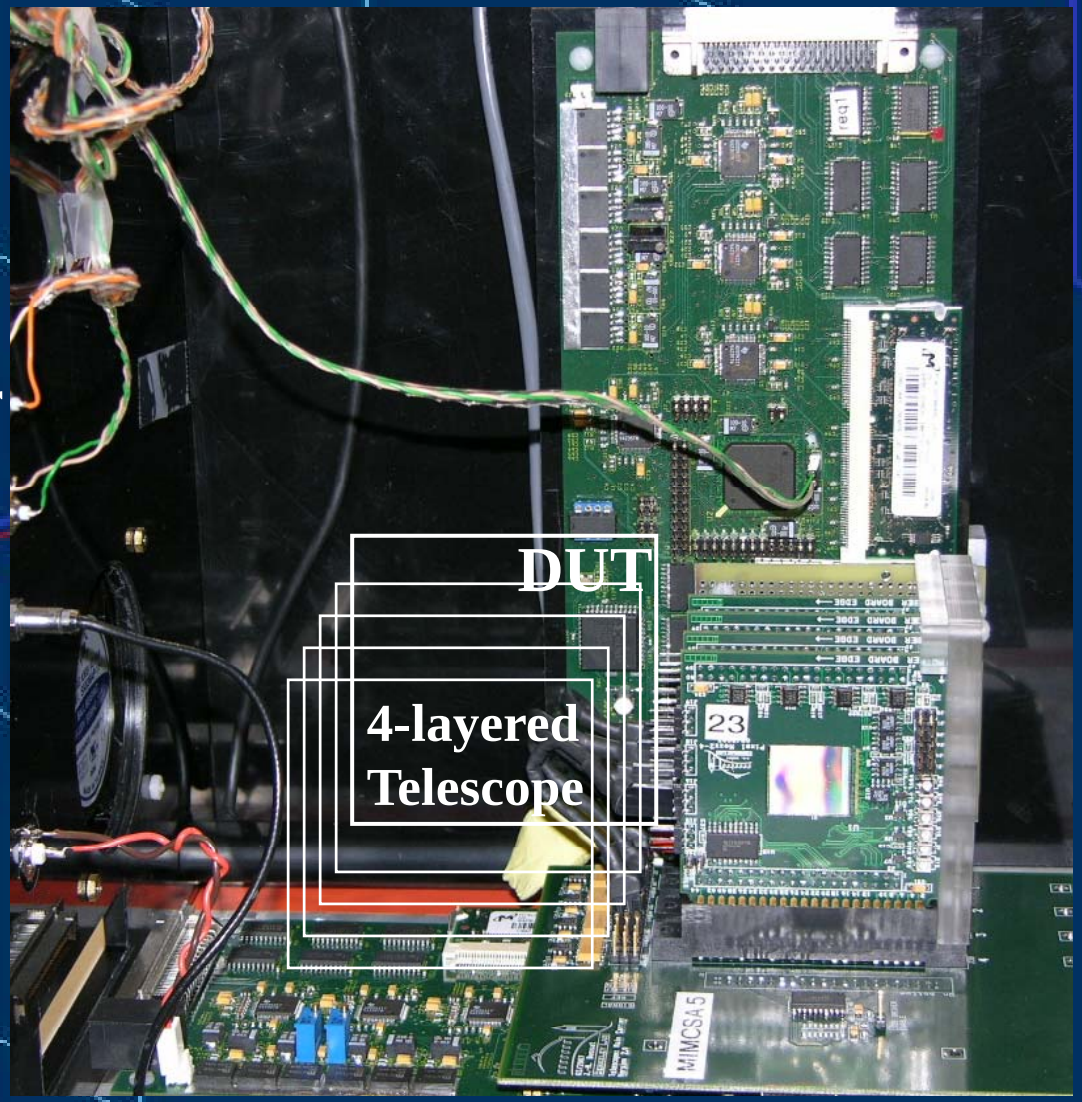


Validate simulation, test patrec and reco algorithms,
plan to make `lcio` hit data available for joint LBNL+FNAL tracking studies.

T966 Telescope

New Thinned MIMOSA5 Telescope (TPPT-2):

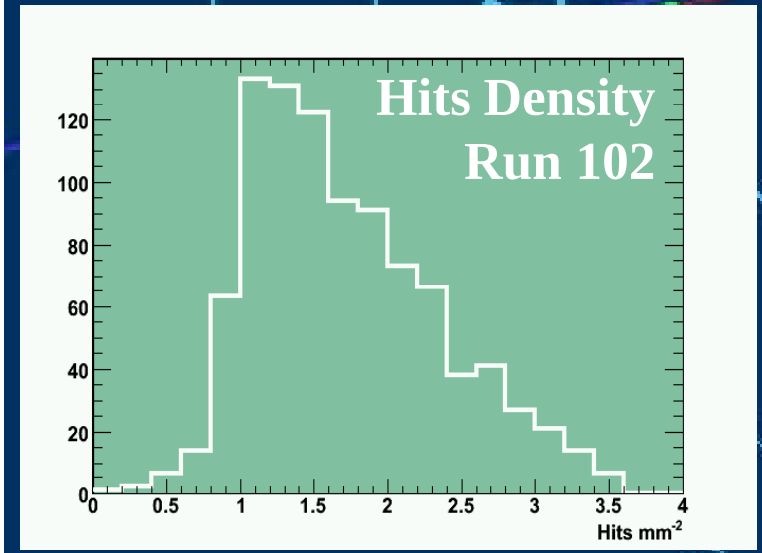
- new mezzanine with low profile components and larger clear region below chip;
- 4 layers of 50 μm thin chips precisely spaced by 1.5 cm;
- precise positioning of chip on mezzanine (< 50 μm) using vacuum chuck;
- DUT installed on computer controlled XY stage for alignment/scan.



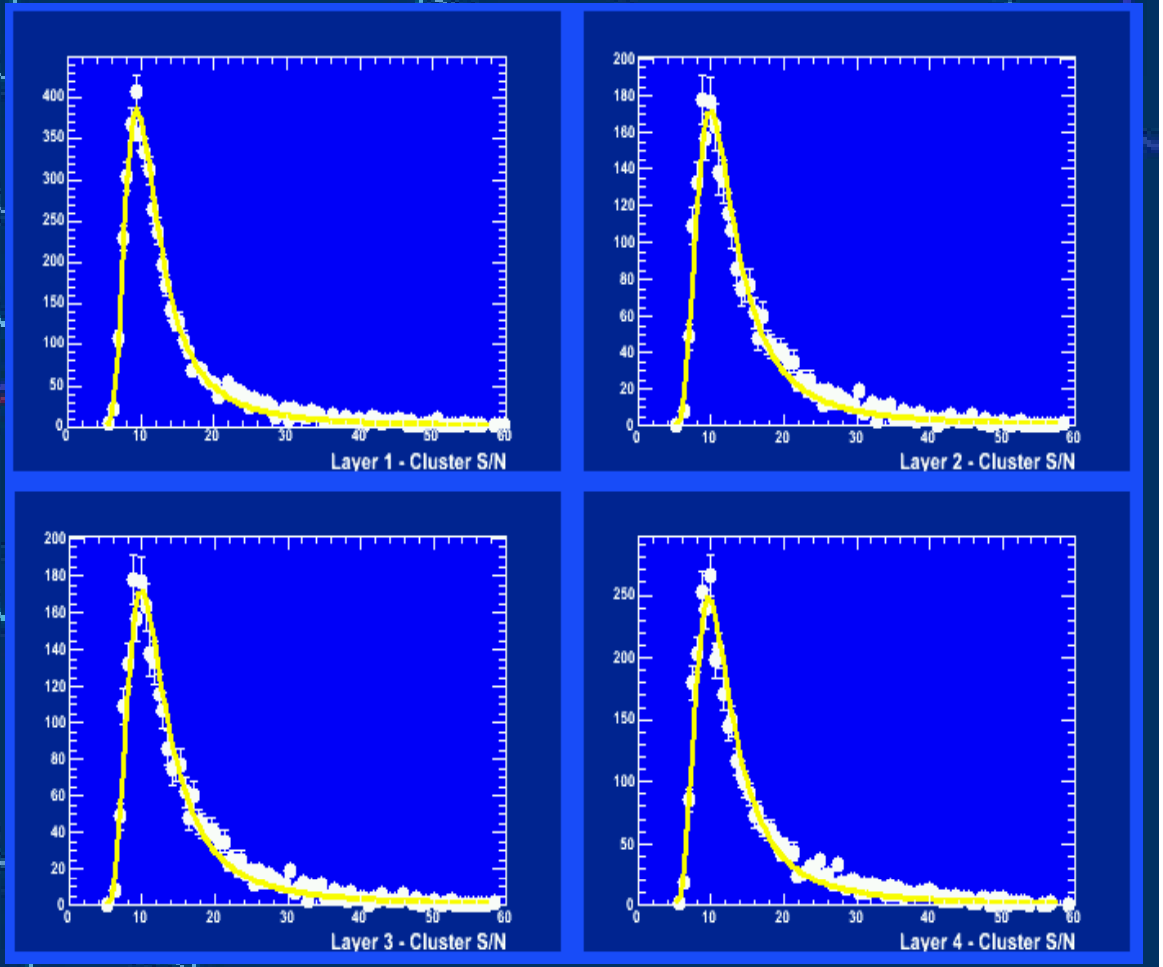
T966 Telescope

Test run of TPPT-2 at ALS
with 1.23 GeV e- beam
(May 2007);

<S/N> ~ 15
Alignment in progress;
Runs with LDRD-2 as DUT.



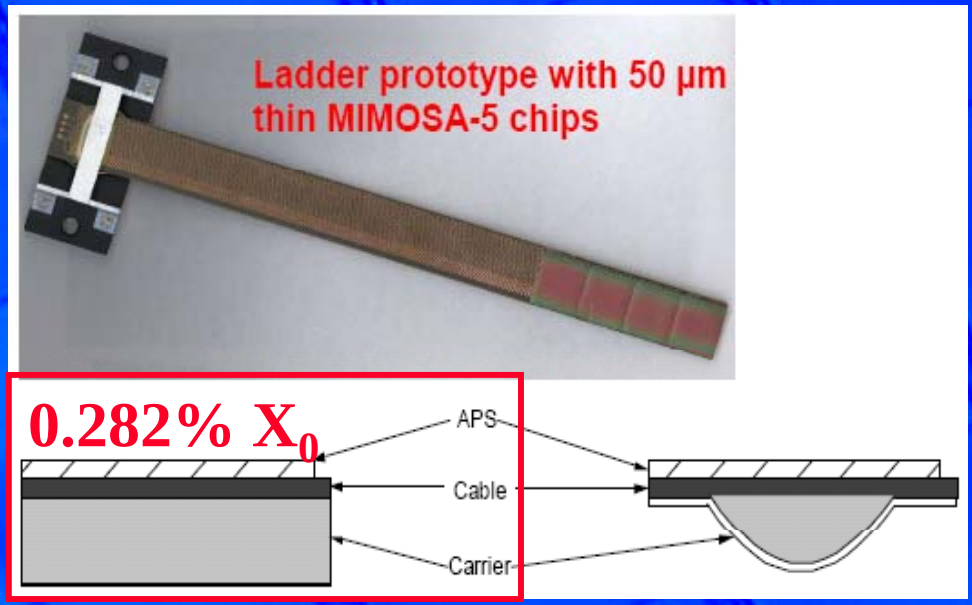
S/N of TPPT-2 detectors @ 27ºC

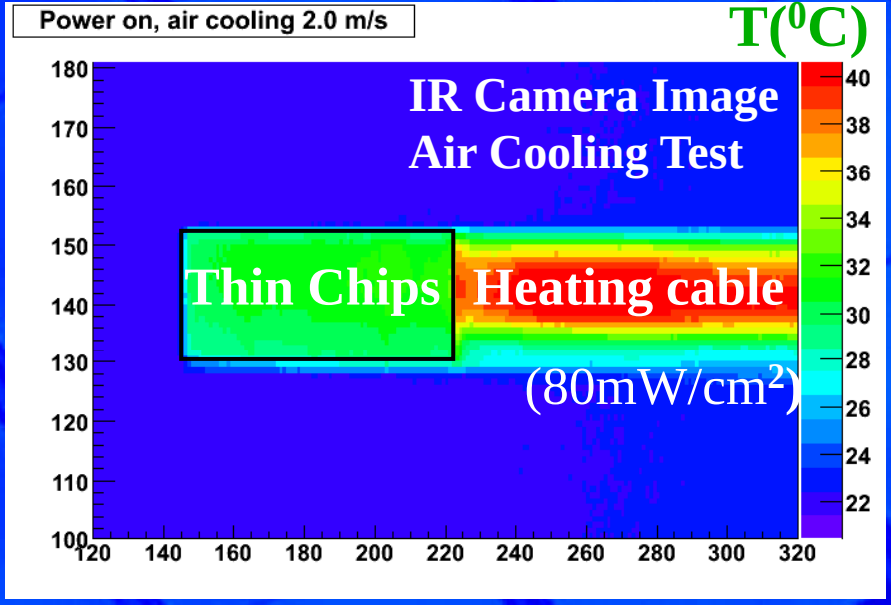


VTX Ladder Design & Testing

LCRD funding supports new program of engineering design, construction and characterization of full ladder equipped with back-thinned CMOS pixel sensors in collaboration with STAR HFT project;

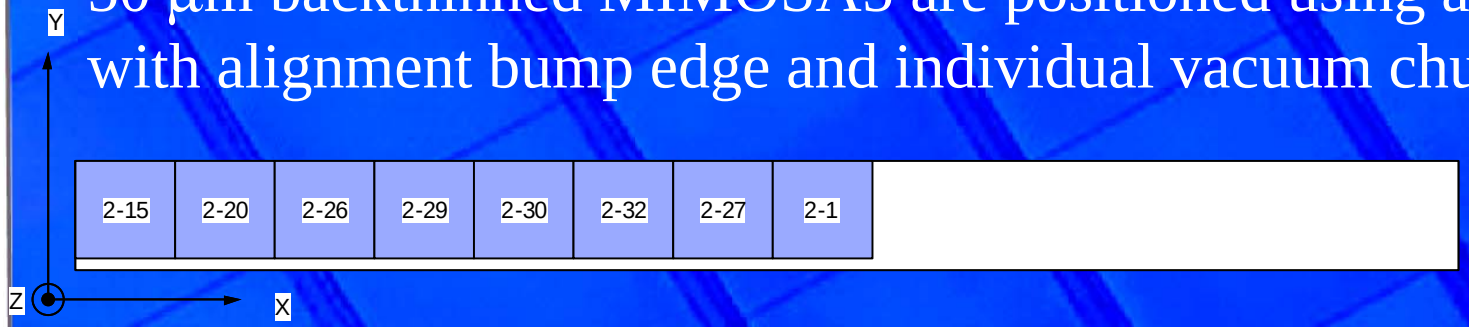
- STAR Low mass carrier: 50μm CFC+3.2mm RVC+50μm CFC (=0.11%X_0);
- Mechanical and thermal characterization of STAR prototype, study of heat removal using low-speed airflow;



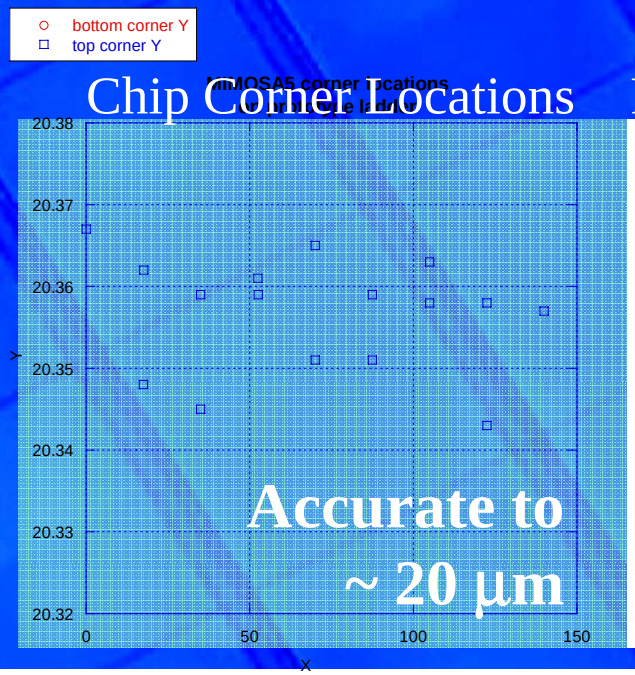


VTX Ladder Design & Testing

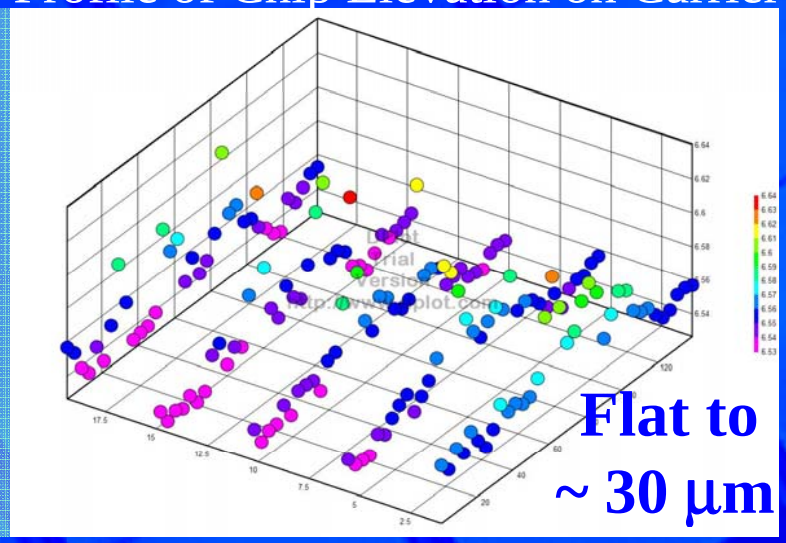
STAR study of accuracy of chip positioning on carrier:
50 µm backthinned MIMOSA5 are positioned using a vacuum chuck with alignment bump edge and individual vacuum chuck valves;



Chip Corner Locations



Profile of Chip Elevation on Carrier

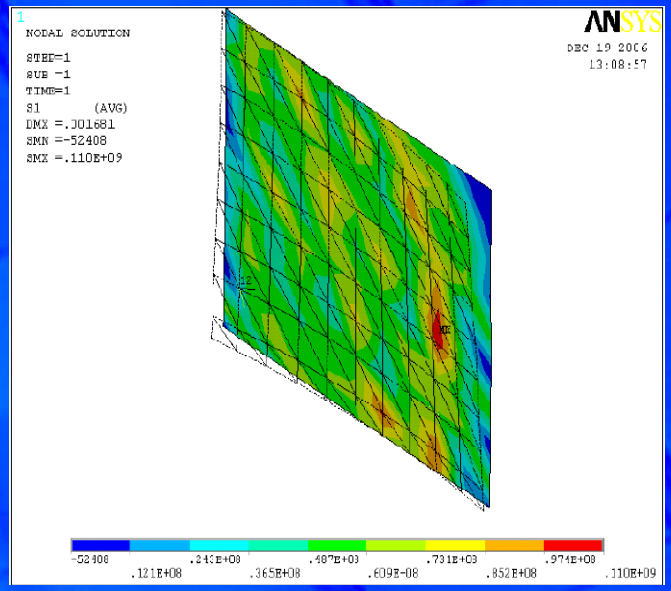


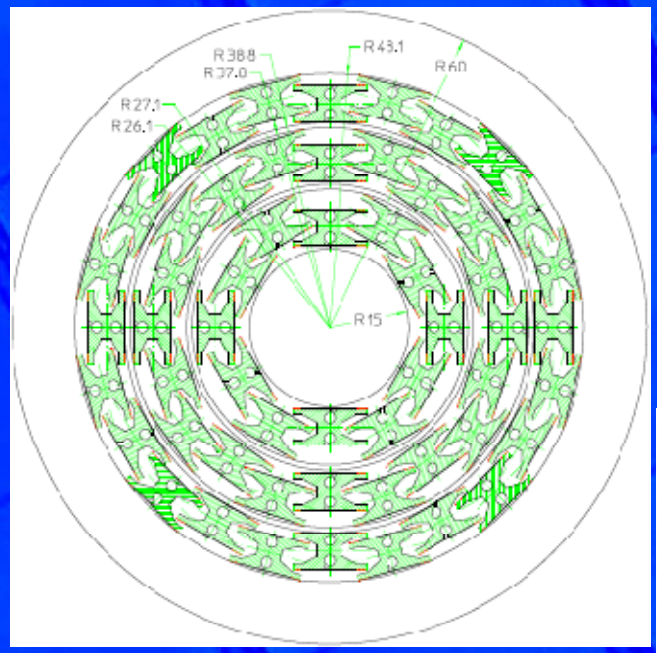
Measurements using Optical Survey Machine with ~ 1 µm accuracy.

VTX Ladder Design & Testing

- FEA of prototype structures: (core-cooled Si/CF/RVC sandwich, Si/Al/RVC sandwich, CVD coated CF) in progress using data from surveys of 40 and 50 μm thin chips, first results promising, test of prototype in 2008;

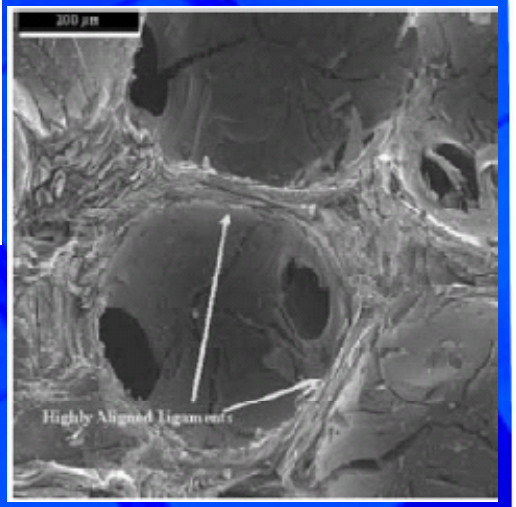
Stress of flattened 50 μm chip





Concept for Symmetric Ladder Sandwich Support with Air Cooling through Core

Low density (0.2-0.6g/cc)
High thermal conductivity
(40-180W/m K) carbon foam



Conclusions

- Successful program of CMOS pixel chip back-thinning to 40 μm and characterisation;

- First Thin Pixel Beam Telescope commissioned at LBNL ALS, extrapolation resolution matches expectations;

- T-966 Beam Test experiment will use two new beam telescopes for broad program of tracking and vertexing studies on FNAL 120 GeV p beam;

- Program of design, characterisation of lightweight ladder carried out as LCRD project in close collaboration with LBNL STAR HFT group.