ILC Vertex Tracker Ladder Studies At LBNL

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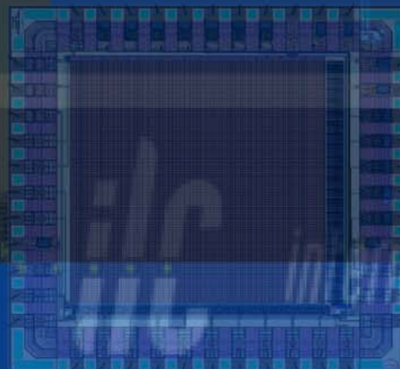


international linear collider

Mechanical Test Facilities at LBNL

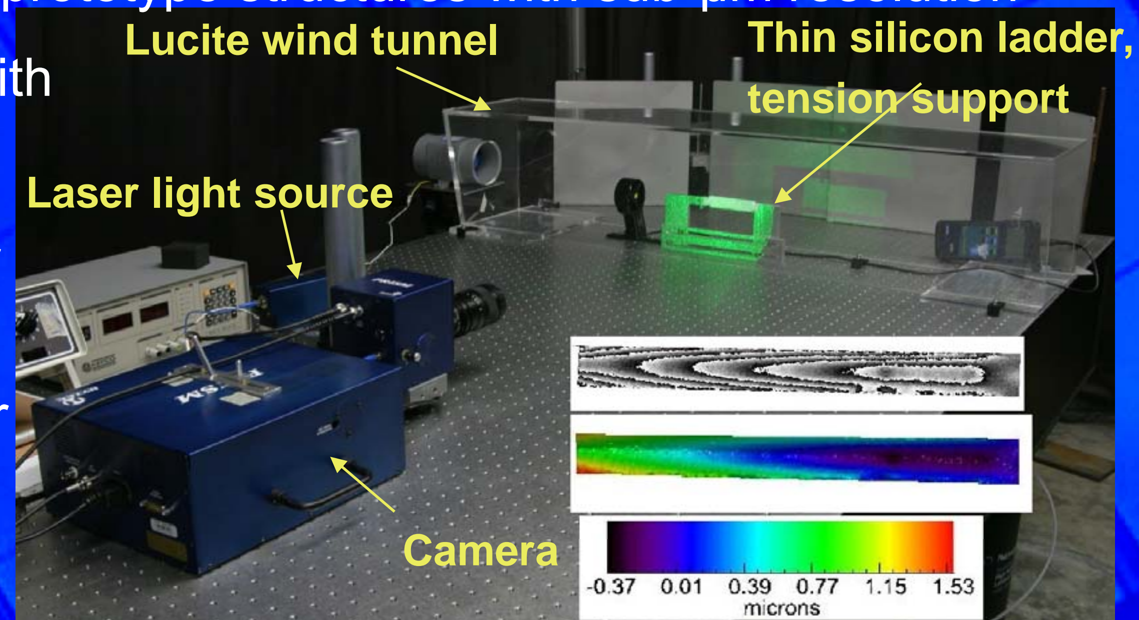
- **Environmental chamber (down to -70ºC)** for characterization of temperature cycling and humidity effects on prototype ladders

- **High resolution IR camera** for studying temperature gradient of prototype ladders

- **Facility for studies of cooling and mechanical stability with nitrogen and air flow**, equipped with a **laser holography system** for real time measurement of distortions in prototype structures with sub-μm resolution

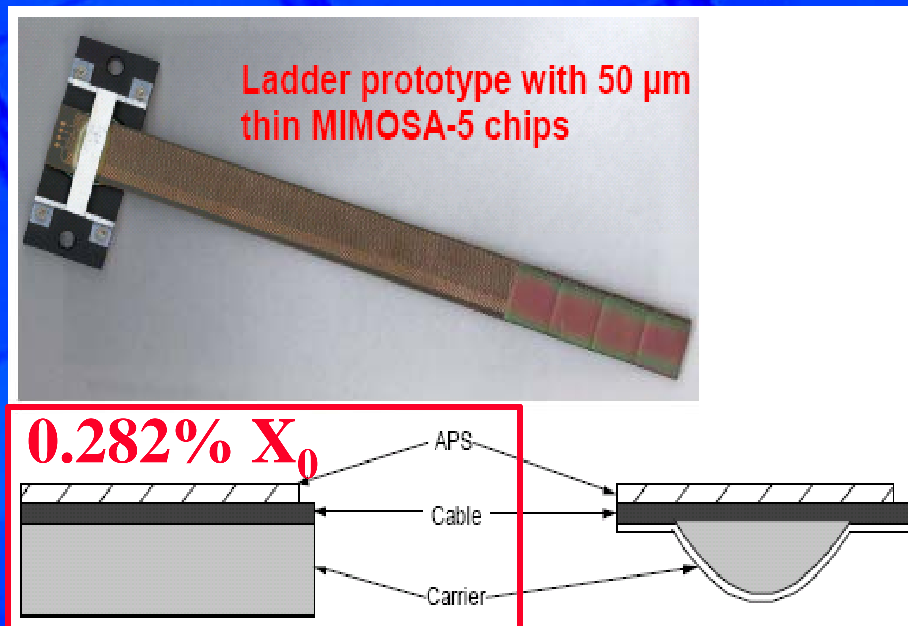
- **Capacitive probe system** with sub-μm resolution; study displacements and vibrations induced by air cooling or other forces

- **Composite materials lab** for fabrication of light structures



VTX Ladder Design & Testing

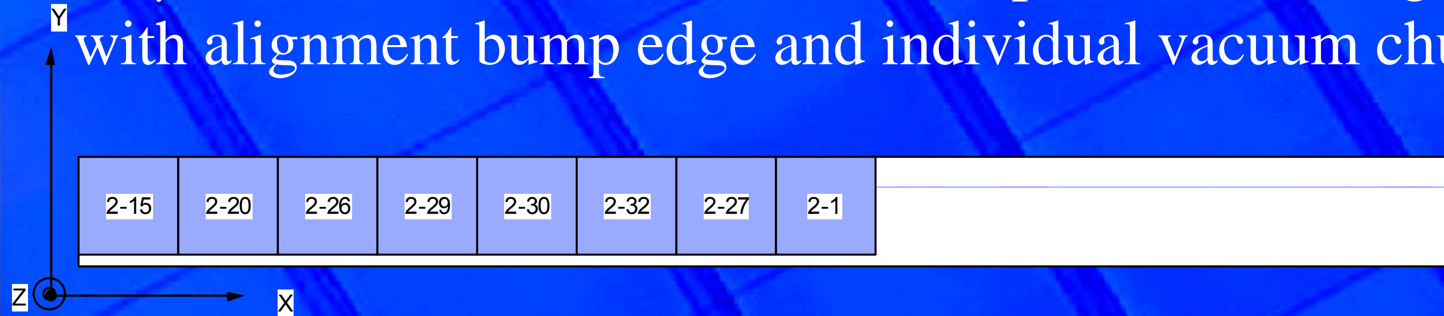
- **LCRD** funding supports new program of engineering design, construction and characterization of full ladder equipped with back-thinned CMOS pixel sensors in collaboration with STAR HFT project
- **STAR** low mass carrier: 50µm CFC+3.2mm RVC+50µm CFC (=0.11% X_0)



Component	% radiation length
MIMOSA detector	0.0534
Adhesive	0.0143
Cable assembly	0.090
Adhesive	0.0143
CF / RVC carrier	0.11
Total	**0.282**

VTX Ladder Design & Testing

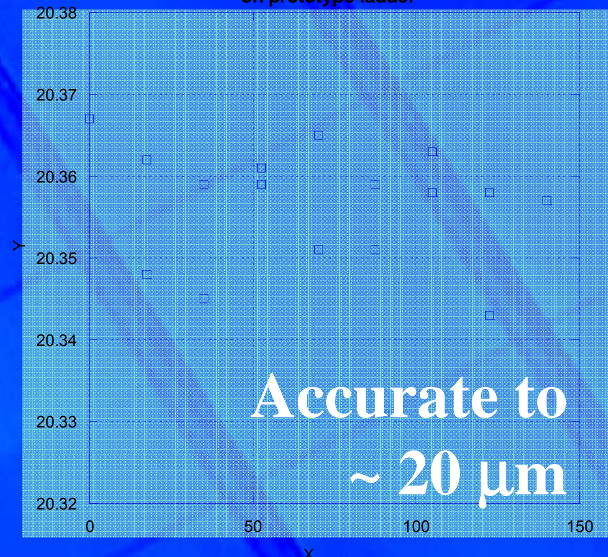
STAR study of accuracy of chip positioning on carrier:
50 μm back-thinned MIMOSA5 are positioned using a vacuum chuck with alignment bump edge and individual vacuum chuck valves

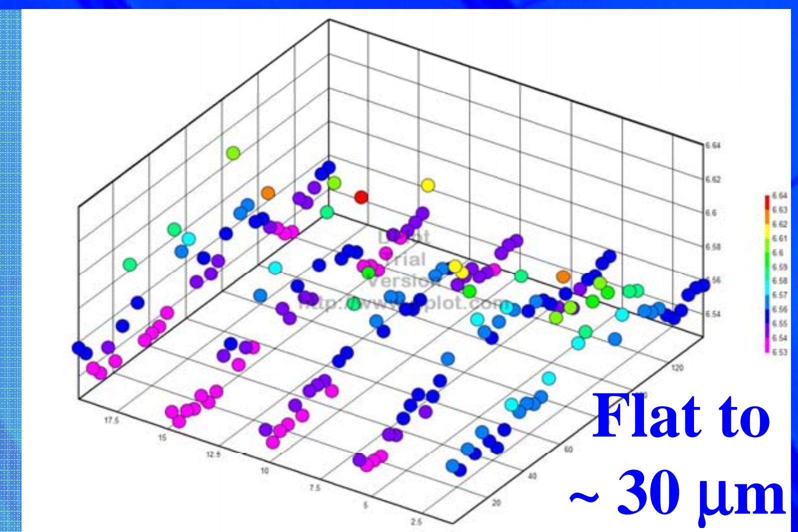


Chip Corner Locations

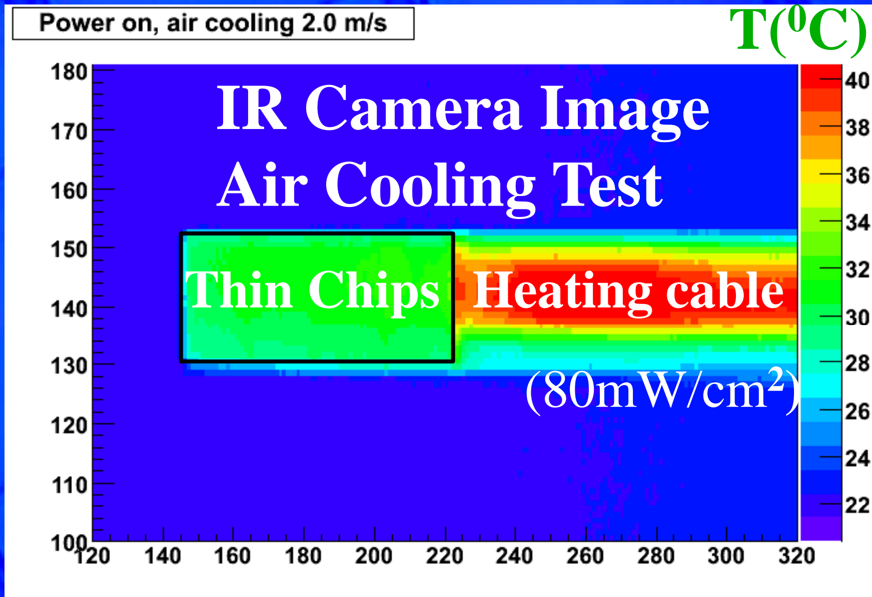
Profile of Chip Elevation on Carrier

Measurements using Optical Survey Machine with ~ 1 μm accuracy.



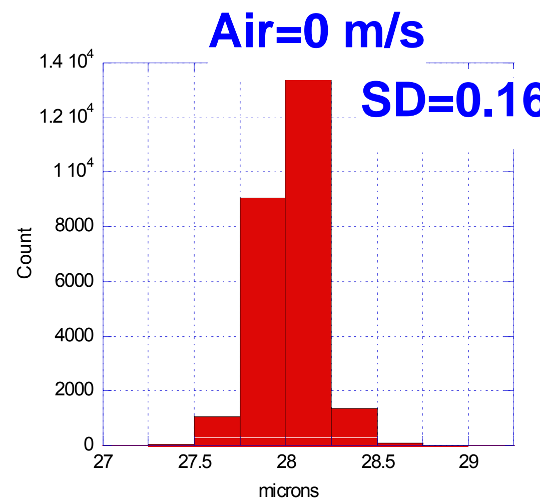


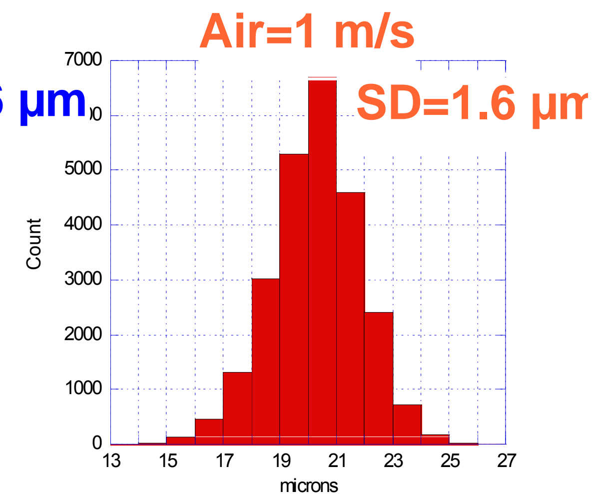
VTX Ladder Design & Testing



• Mechanical and thermal characterization of STAR prototype, study of heat removal using low-speed airflow

• Vibration from air cooling measured with capacitive probe; location distribution with SD~1 μm at 1.0 m/s airflow on unsupported end of ladder



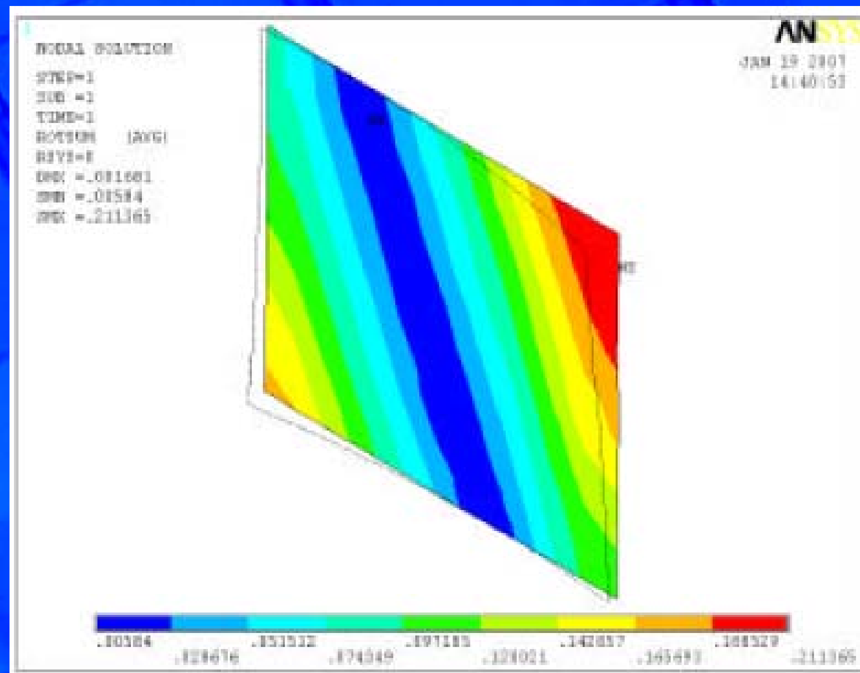


Thin CMOS Pixel Studies

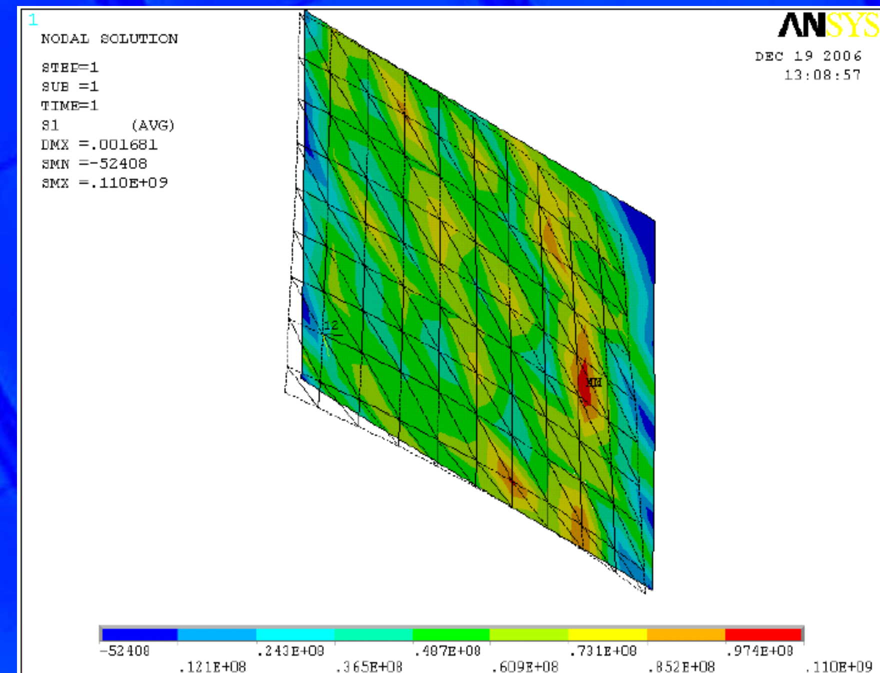
- Back-thinning of diced chips using grinding process by Aptek Industries
- Thinned over 15 MIMOSA5 chips, process reliable down to 40 µm, yield of functional chips~90%
- Measured chips thickness:

Before	(550±0.5) µm
"50 µm"	(50±7) µm
"40 µm"	(41±6) µm

Surface map of 50 µm chip (measured)



FEA stress analysis of flattened 50 µm chip



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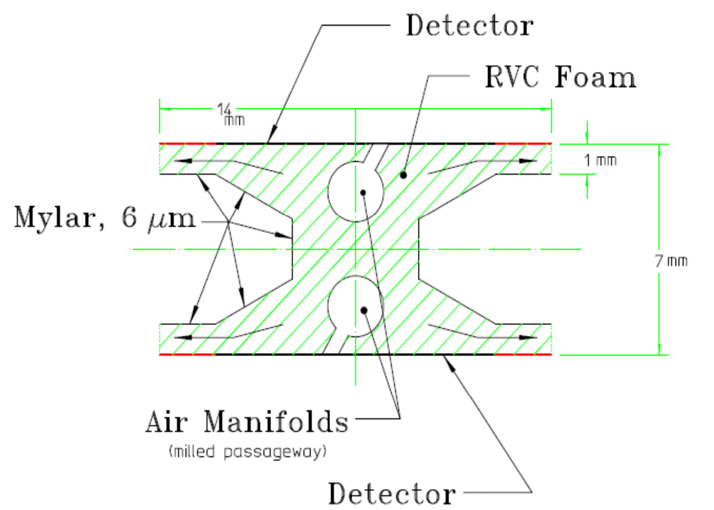
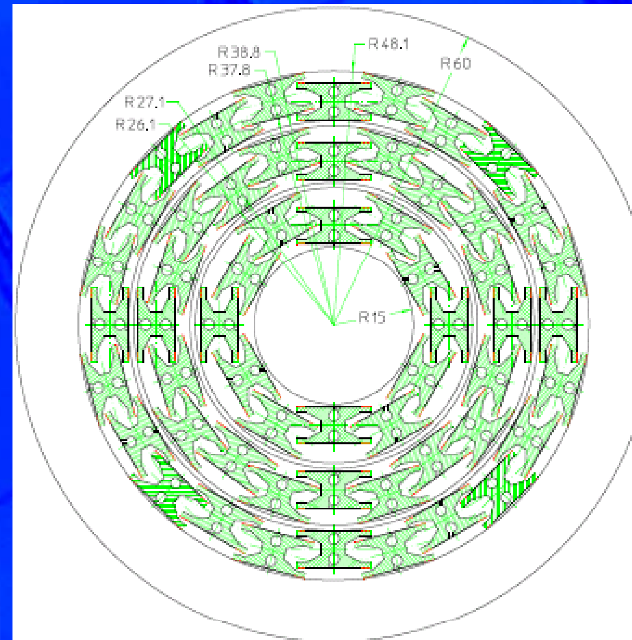
VTX Ladder Design & Testing

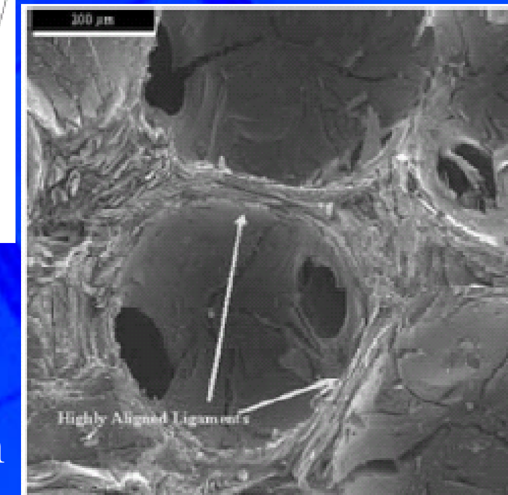
• FEA of prototype structures (core-cooled Si/CF/RVC sandwich, Si/Al/RVC sandwich, CVD coated CF) in progress using data from surveys of 40 and 50 µm thin chips, first results promising, test of prototype in 2008

Ladder side view





Concept for Symmetric Ladder Sandwich Support with Air Cooling through Core



Low density (0.2-0.6g/cc) High thermal conductivity (40-180W/m K) carbon foam