HLRF Interlock Module & ATCA Platform R&D Plan

ILC-LCWS 2008

November 18, 2008

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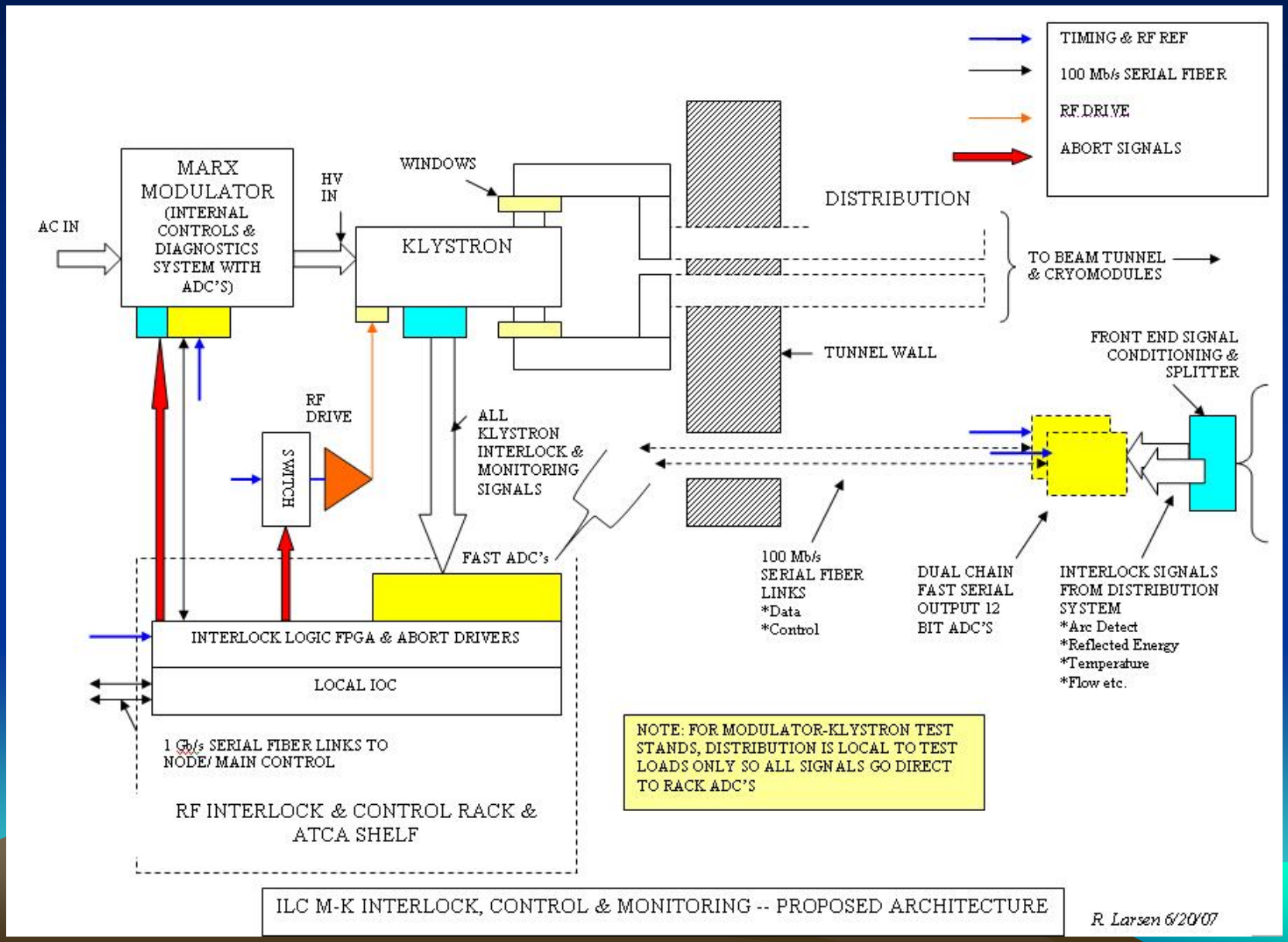
For SLAC National Laboratory

L-Band Test Stand Team

Outline

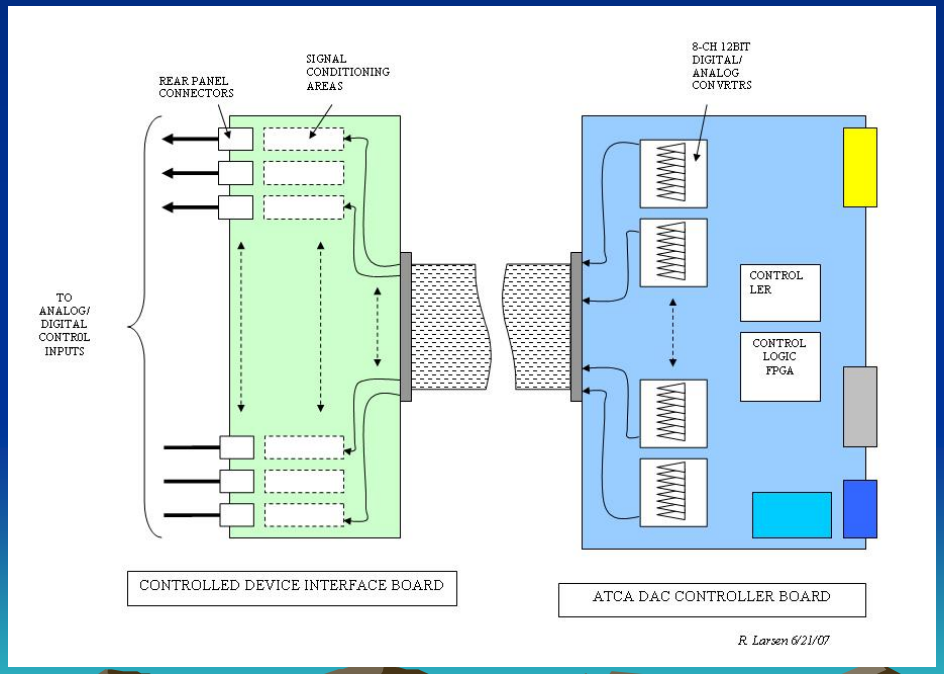
- L-Band Test Stand Interlock Architecture
- Fast Fault Finder (F3) FPGA Module
- ATCA* & MicroTCA HA Platform R&D
- Summary Status & Plans
- **Advanced Telecom Computing Architecture*

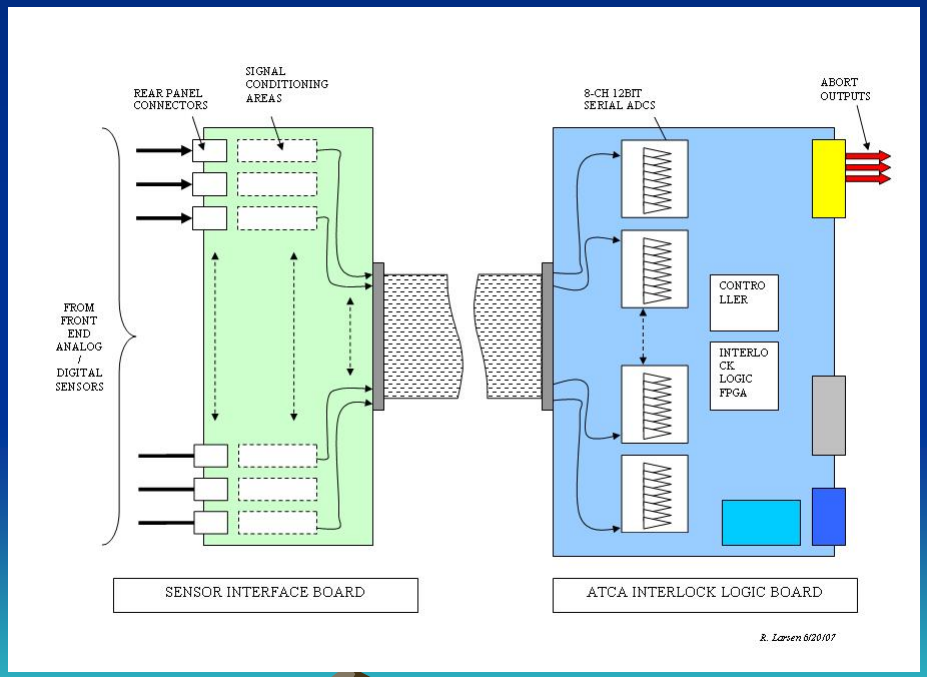
Initial M-K Interlock Concept



Initial I/O Concept

- Aimed at ATCA Platform
- Control & Sensor signal conditioning near source
- Standard high density cables interconnects (could be serial)

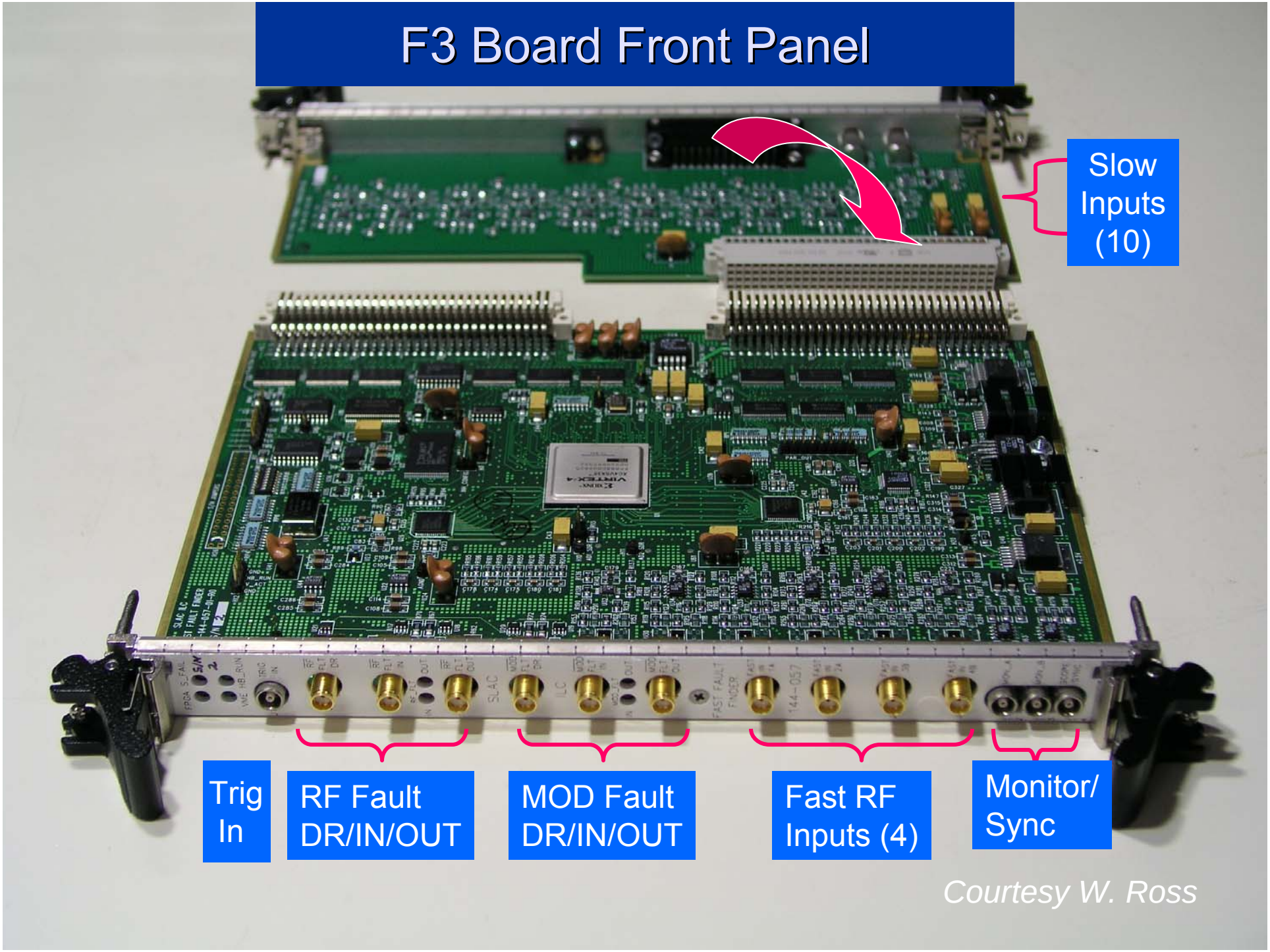




Implementation Phase I

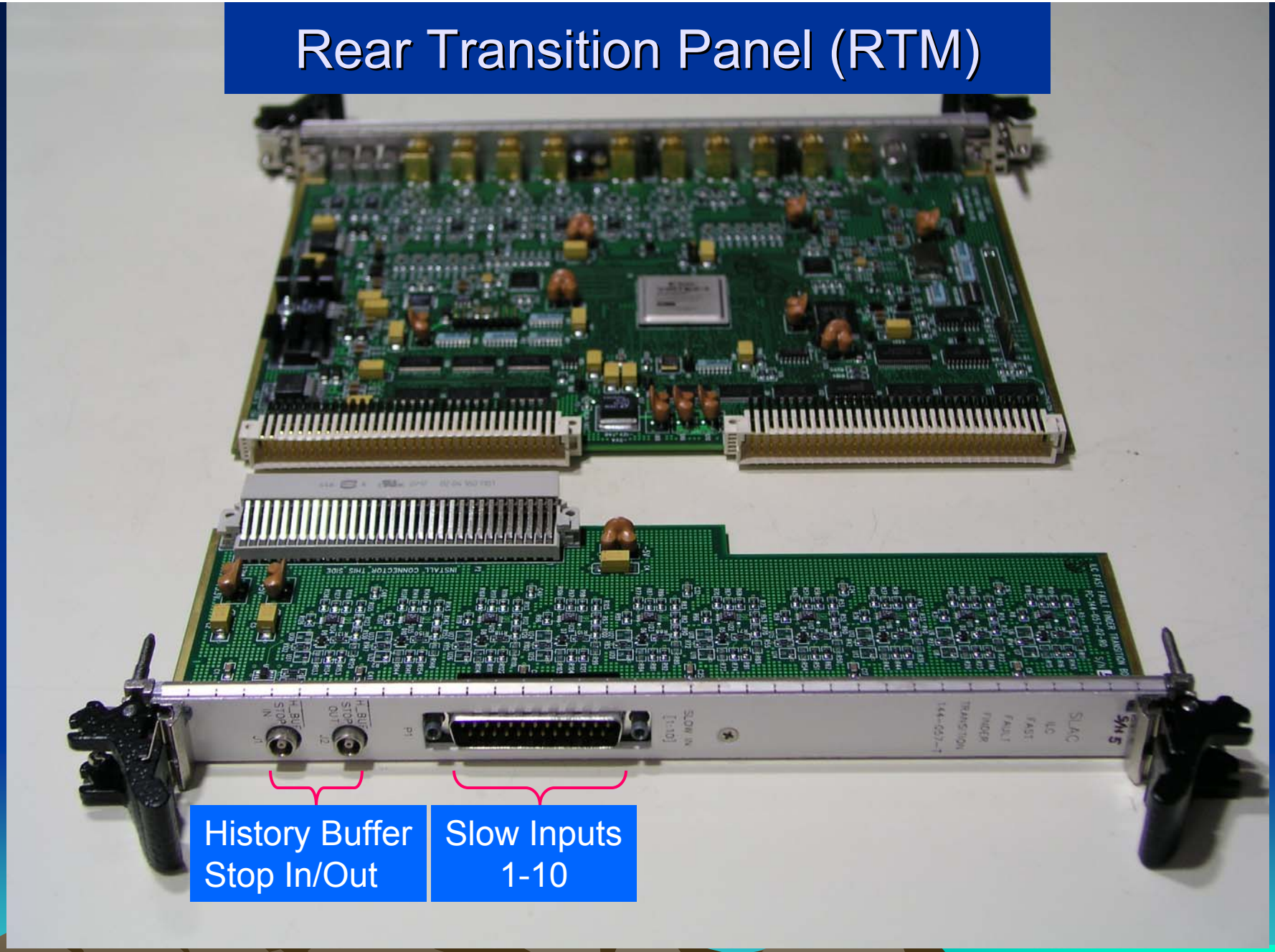
- Novel FPGA Based VME Module
  - Fast Fault Finder (F3)
  - 4 fast (1 μSec) and 10 slow (1 mSec) channels per 1-wide module
  - Same internal fast ADC's for all channels, decimated clock for slow DC channels (10 MHz fast, 2 KHz slow channels)
  - Open collector abort outputs to expand number of modules/ channels
  - RTM rear high density (10 Ch) cable entry in single width
- Rationale:
  - PLC's cannot handle fast aborts, require additional fast detection system of antiquated NIM logic
  - Combining fast & slow signals into one efficient programmable module eliminates need for separate PLC system
  - FPGA also provides digital filtering, waveform sampling, post-trigger readout of abort signals, history buffer readout for both fast & slow channels

F3 Board Front Panel

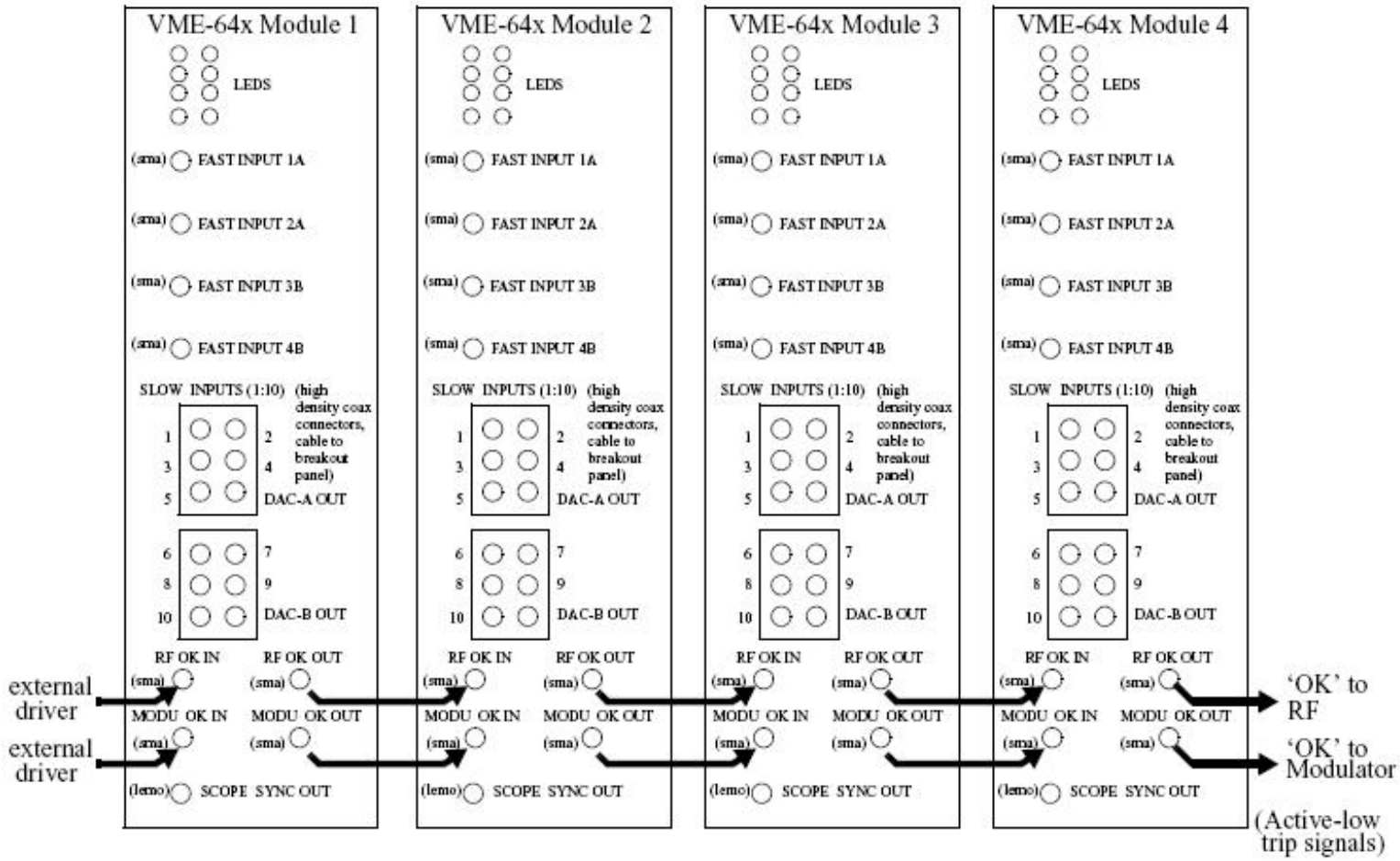


Courtesy W. Ross

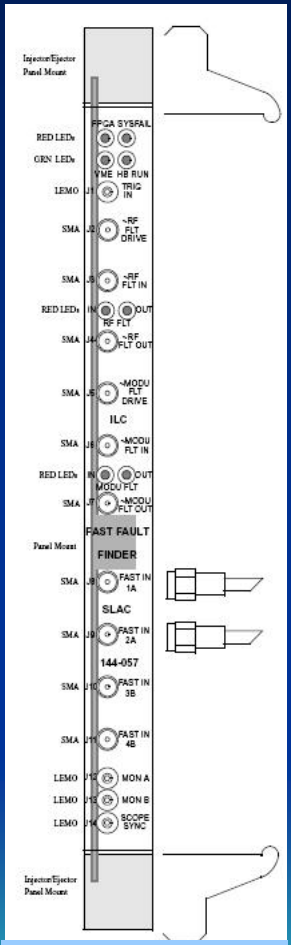
Rear Transition Panel (RTM)



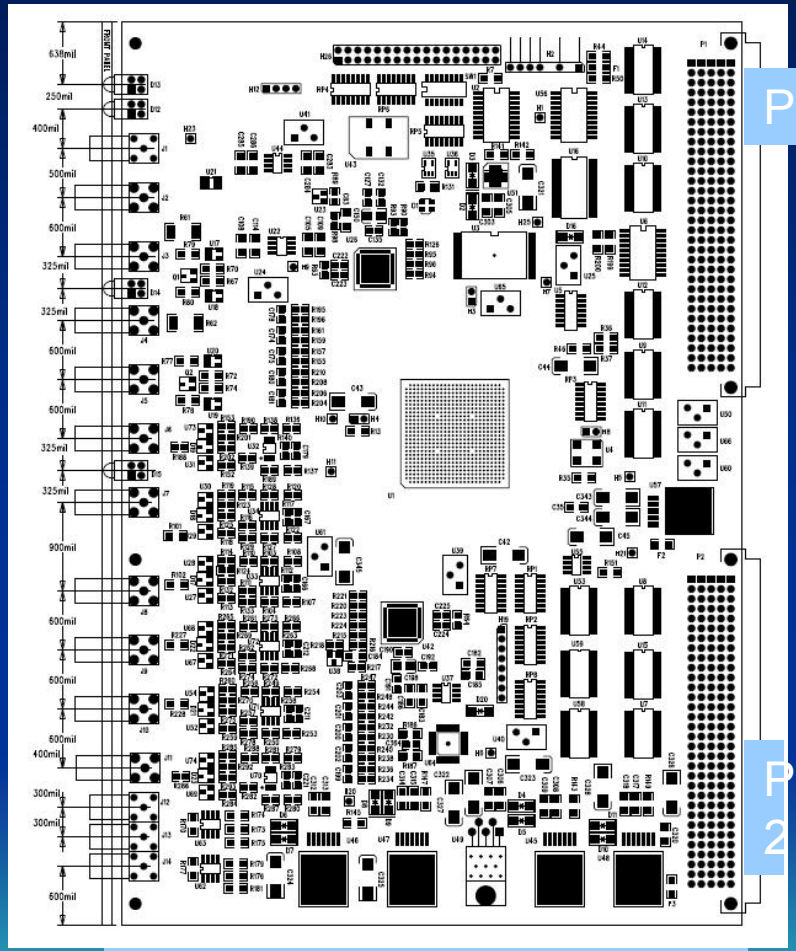
Fast M-K Interlock Concept



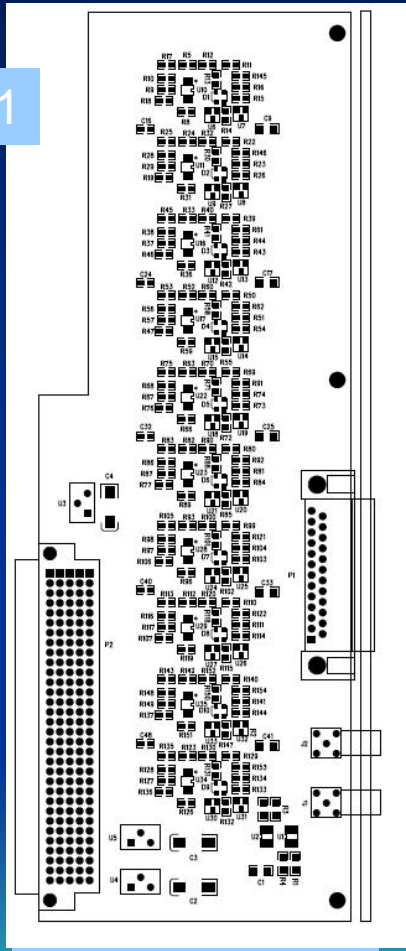
F3 – Fast Fault Finder Layout



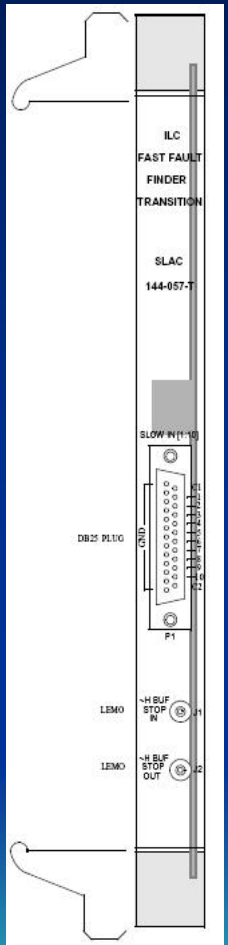
Front Panel



Fast Fault Finder (F3) Board



Rear Transition



Rear Panel

Courtesy W. Ross

F3 Front & Rear Panels

Trigger In

RF FLT Drive

RF FLT In

RF FLT Out

Modu FLT Drive

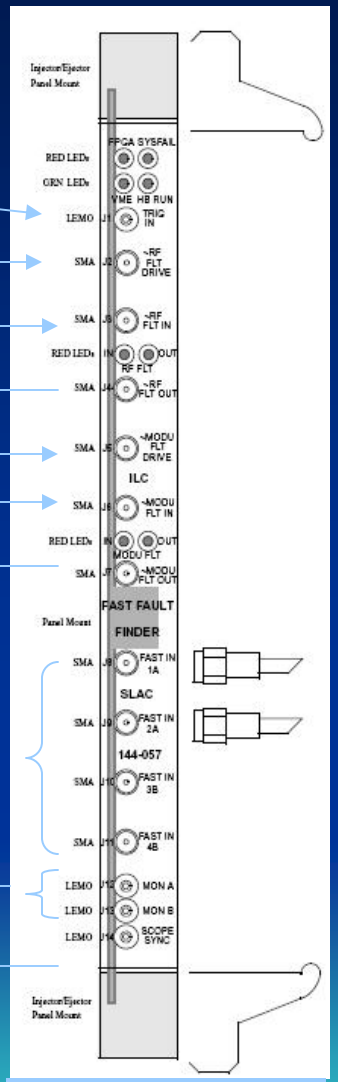
Modu FLT In

Modu FLT Out

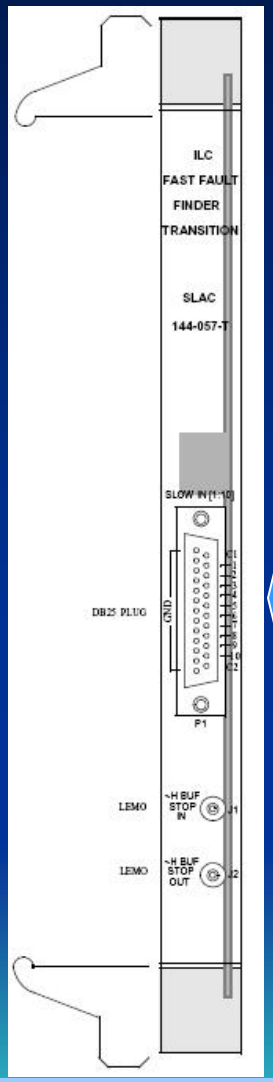
Fast Interlocks In (4)

Monitors Out (2)

Scope Sync Out



Front Panel



Rear Panel

Slow Interlock Signals In (10)

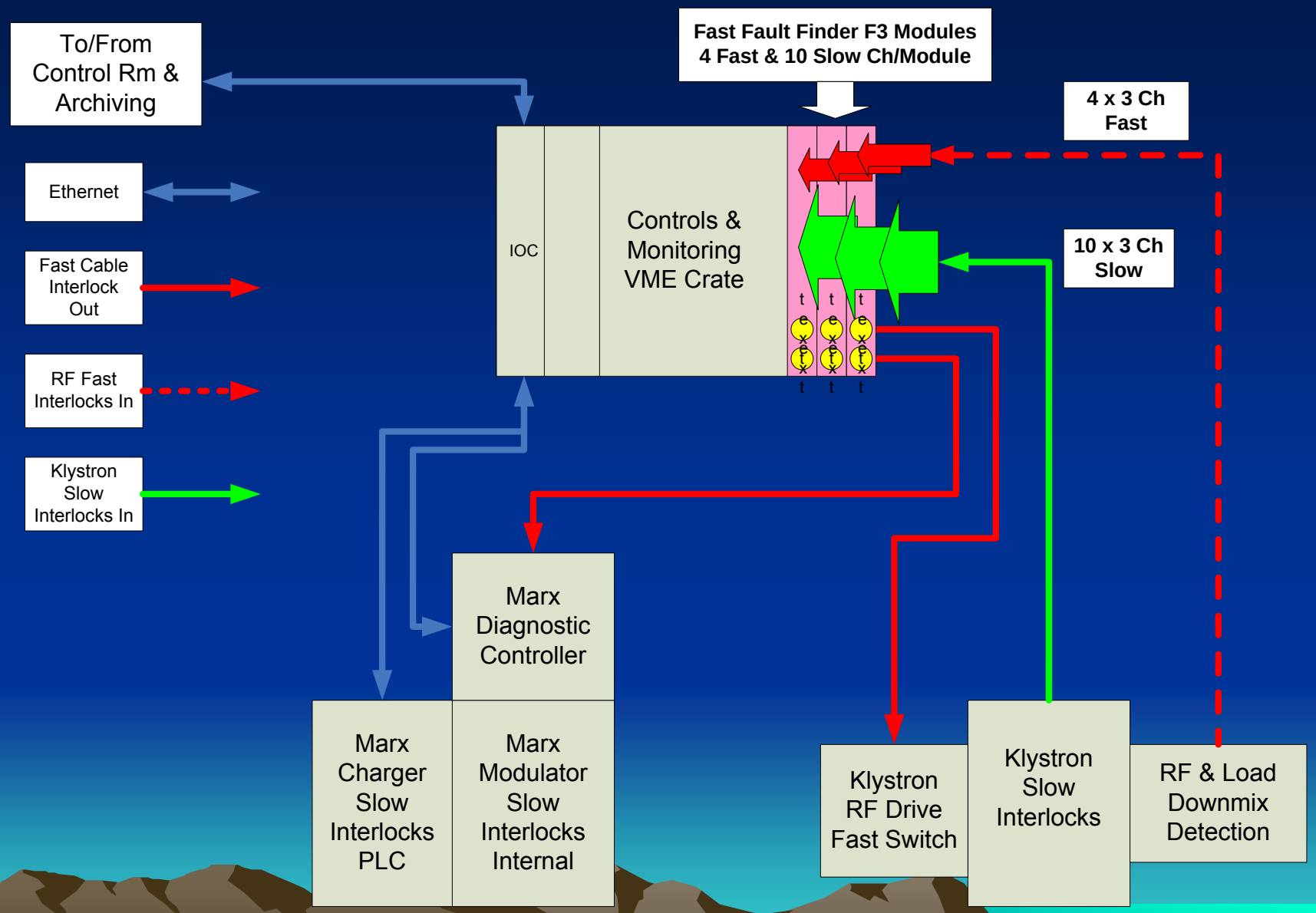
Buffer Stop In

Buffer Stop Out

- 4 Fast, 10 Slow Interlock Inputs per F3 Module
- Front Panel Fault (FLT) Signals Daisy-Chain Between Modules
- Front panel fast interlocks fail-safe, independent of local backplane or crate controller

Courtesy W. Ross

M-K Interlock Block Diagram-VME

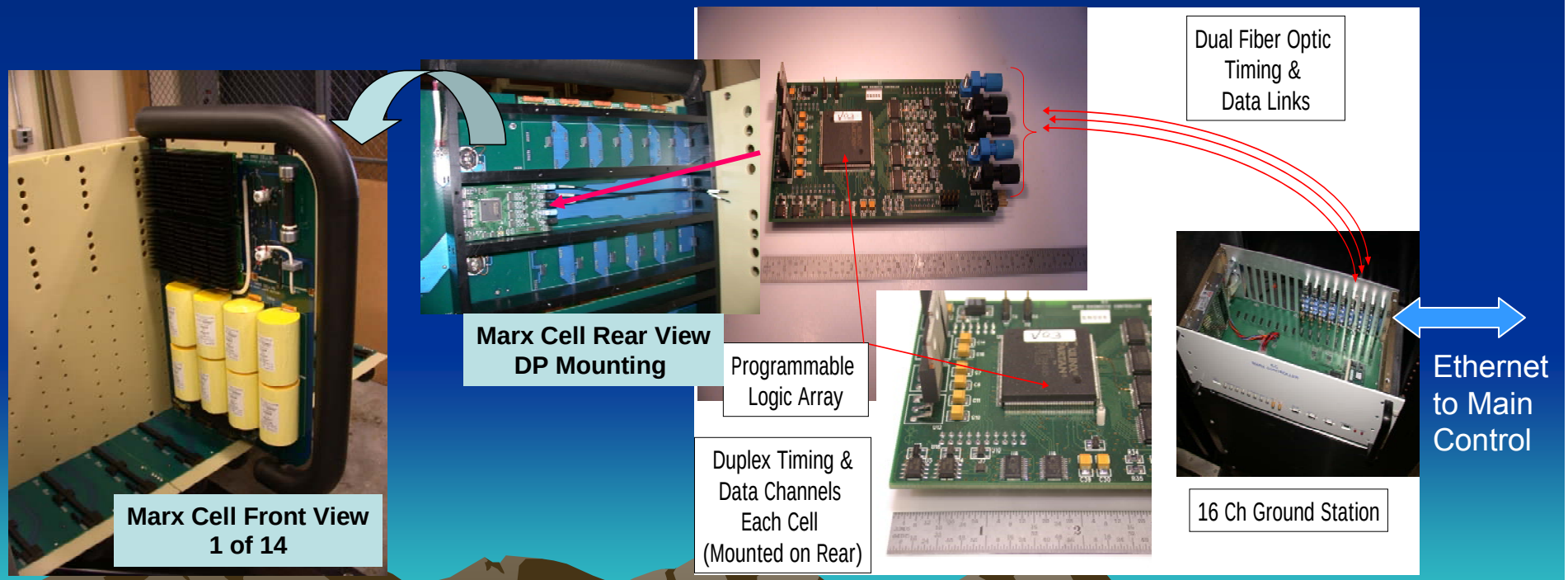


M-K Interlock Architecture

- Marx Modulator
  - Internal monitoring, interlock & protection system
  - Diagnostic Controllers on each of 16 cells
    - Drive IGBT's
    - Capable of waveform sampling pulse V, A
  - Internal Ground Station
    - Sends timing, programmable delay triggers to each cell
    - Collects data, interfaces to overall control & interlock system

Marx Diagnostic Controls

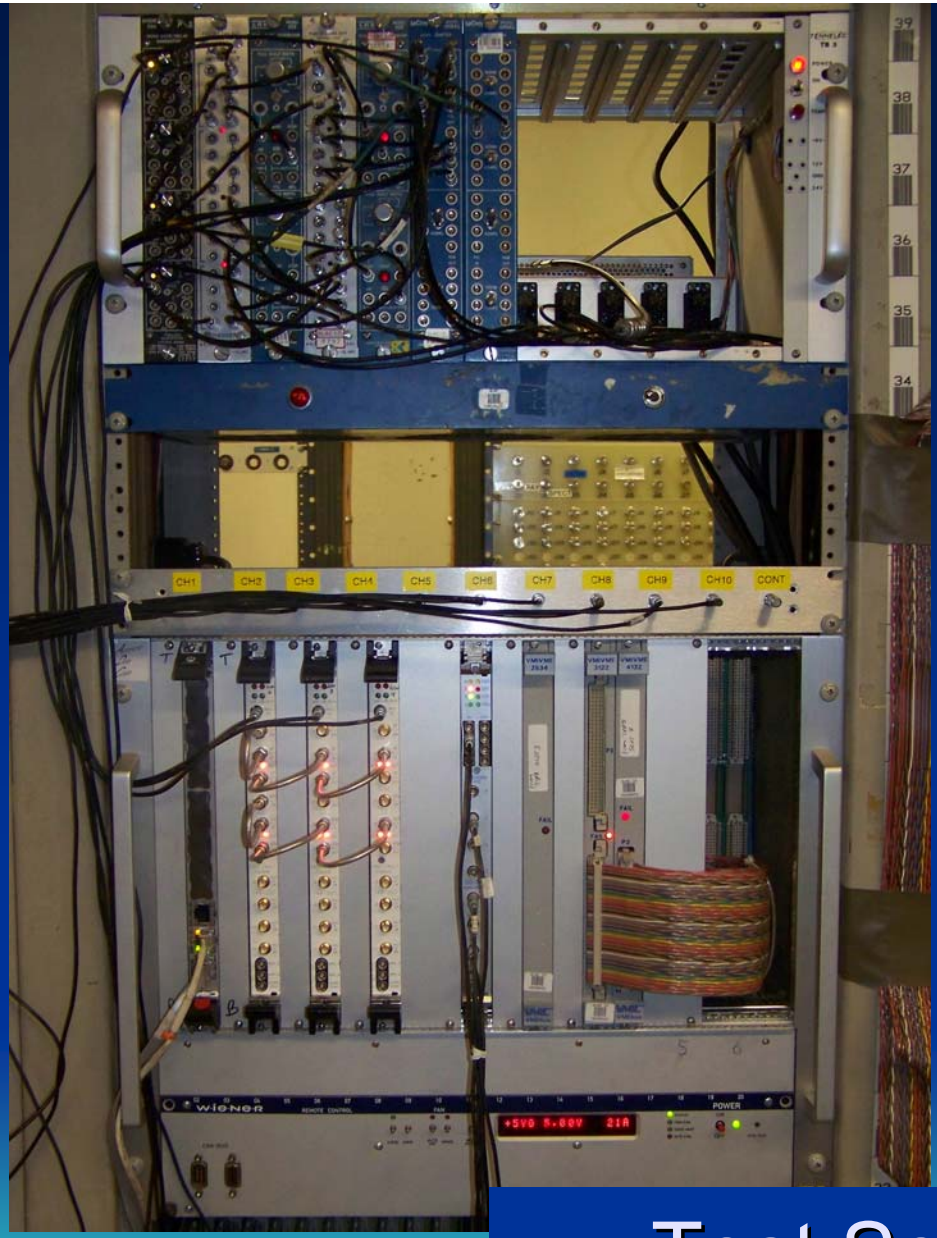
- Diagnostic Controller Functions
  - Monitor Marx cell internals from control room
  - Set points, trip margins, temperatures, trends, fast & slow waveforms
  - Generate fast global interlock on command
  - Ultimate goal: Take evasive action to avoid machine interruption



Courtesy J. Olsen

Klystron, Infrastructure Interlocks

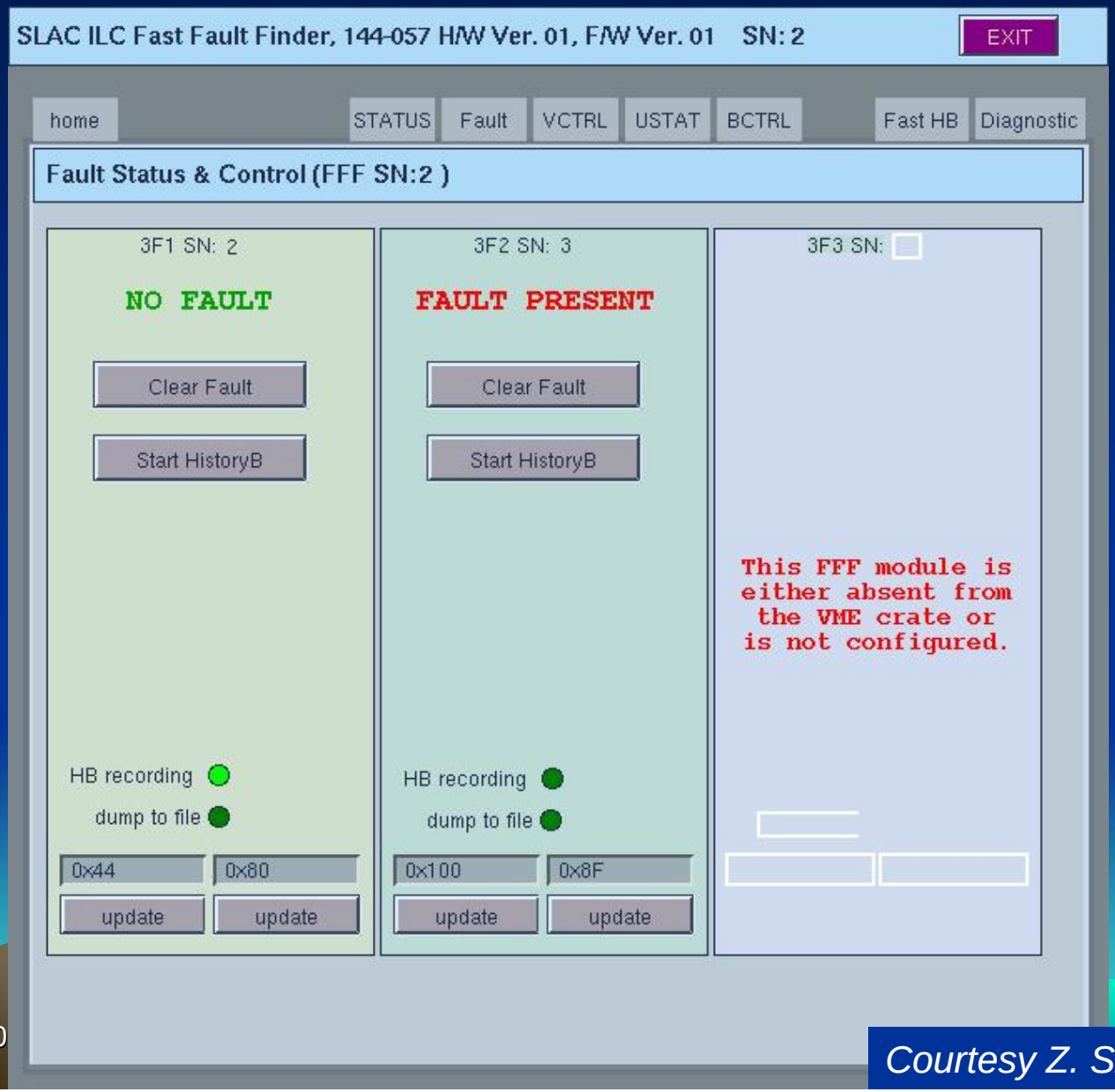
- Monitored within abort set points in FPGA
  - High voltage current, voltage
  - Solenoid, filament power supply voltage, current, temperature, water flow
  - Body and collector temperature, water flow
  - Klystron vacuum, waveguide pressure
  - Load waveguide pressure, temperature
  - RF load flow, temperature
  - Oil tank level, temperature
  - RF Signals: Forward & reflected power, arc detection, power difference between outputs



Test Setup

Courtesy Z. Szalata

F3 User Interface



Courtesy Z. Szalata

Sample Average Value HB Display

Sample values from HB channels (FFF SN:2) Help

	sample #	value read		Lower Limit	Upper Limit	Tick Limit	RF	Mod
fast ch1	2000	323	count	-100.00	100.00	0.00	off	off
fast ch2	1000	-4	count	-100.00	100.00	0.00	off	off
fast ch3	1000	335	count	-100.00	100.00	0.00	off	off
fast ch4	1000	-4	count	-100.00	100.00	0.00	off	off
Solenoid flow	500	-0.05	gpm	-48.83	48.83	0.00	off	off
Klys collect flow	500	0.05	gpm	-48.83	48.83	0.00	off	off
Klys body flow	500	0.29	gpm	-48.83	48.83	0.00	off	off
RF load flow	500	0.49	gpm	-48.83	48.83	0.00	off	off
Klys filament	500	0.39	amps	-48.83	48.83	0.00	off	off
Klys filament	500	0.44	Volt	-48.83	48.83	0.00	off	off
Klys fil to	500	0.10	Volt	-48.83	48.83	0.00	off	off
Tank oil level	500	0.49	cm	-48.83	48.83	0.00	off	off
WGuide pressure	500	0.73	Tor	-48.83	48.83	0.00	off	off
slow ch10	500	0.29	spare	-48.83	48.83	0.00	off	off
slow calib 1	500	0.59	none	-50.00	50.00	0.00	off	off
slow calib 2	500	0.10	none	-20.02	43.02	0.00	off	off
			Diff Ch A	-1000.00	1000.00	0.00	off	off
			Diff Ch B	-100.00	100.00	0.00	off	off

Read Updt: Passive

Diff Gain Ch 1A: 0.0000 Diff Gain Ch 3B: 0.0000

Diff Gain Ch 2A: 0.0000 Diff Gain Ch 4B: 0.0000

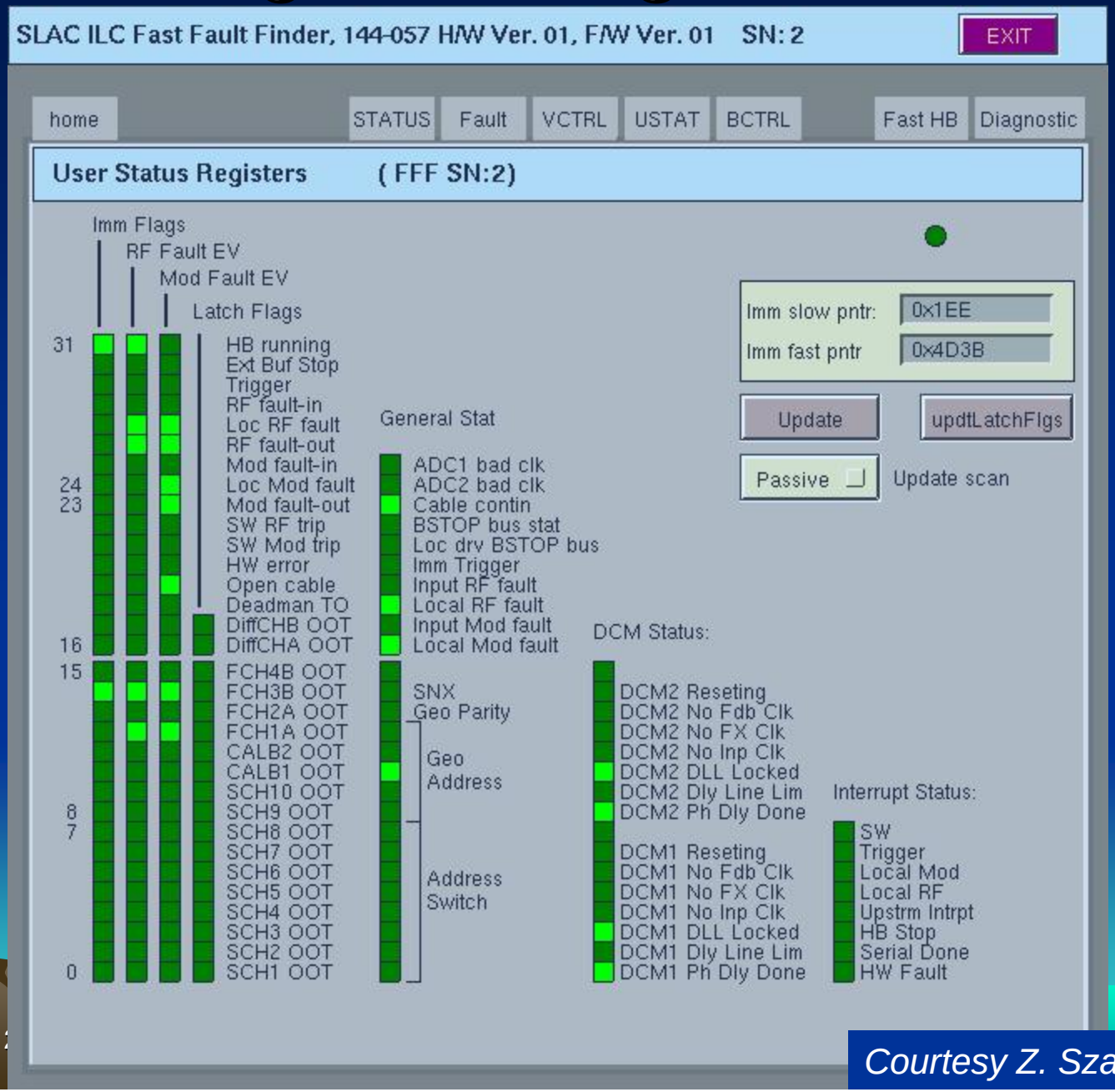
Save

Restore

File Name: 3f1FaultSetup.txt

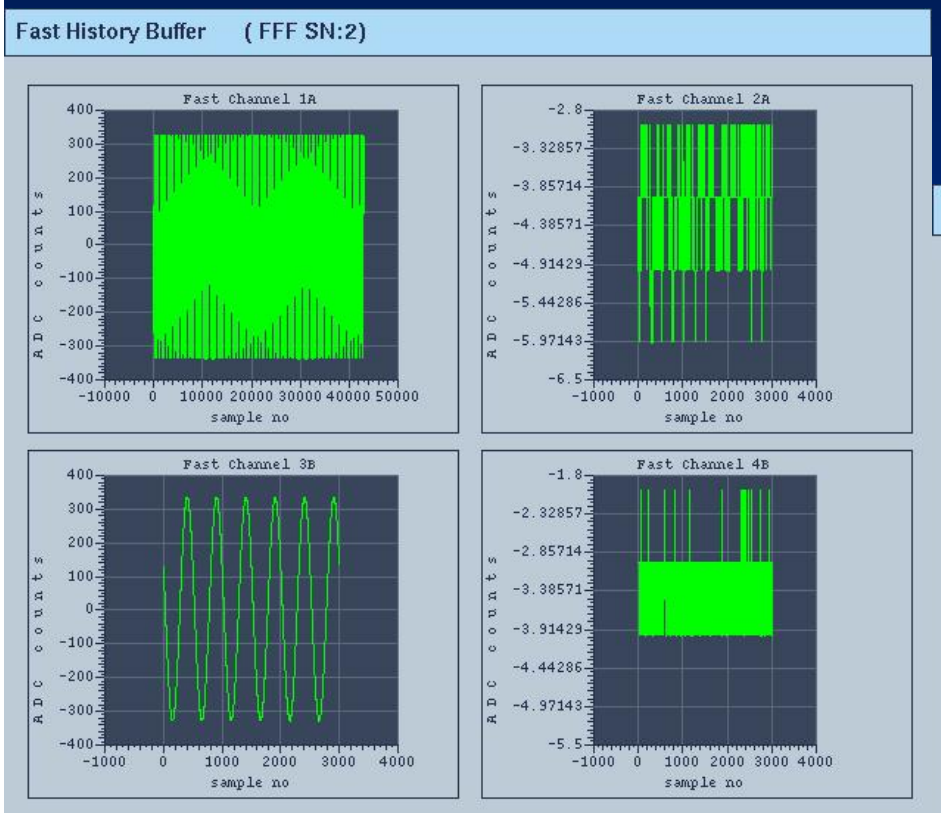
Courtesy Z. Szalata

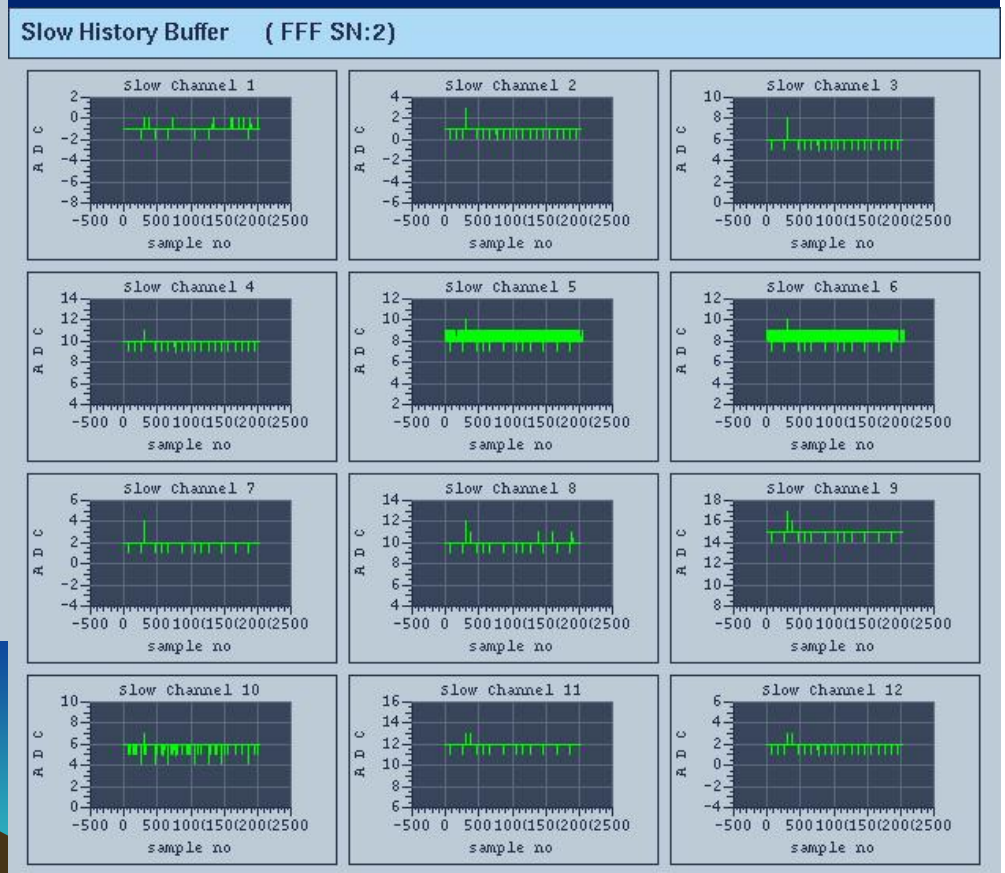
Status Register Diagnostic Screen



Courtesy Z. Szalata

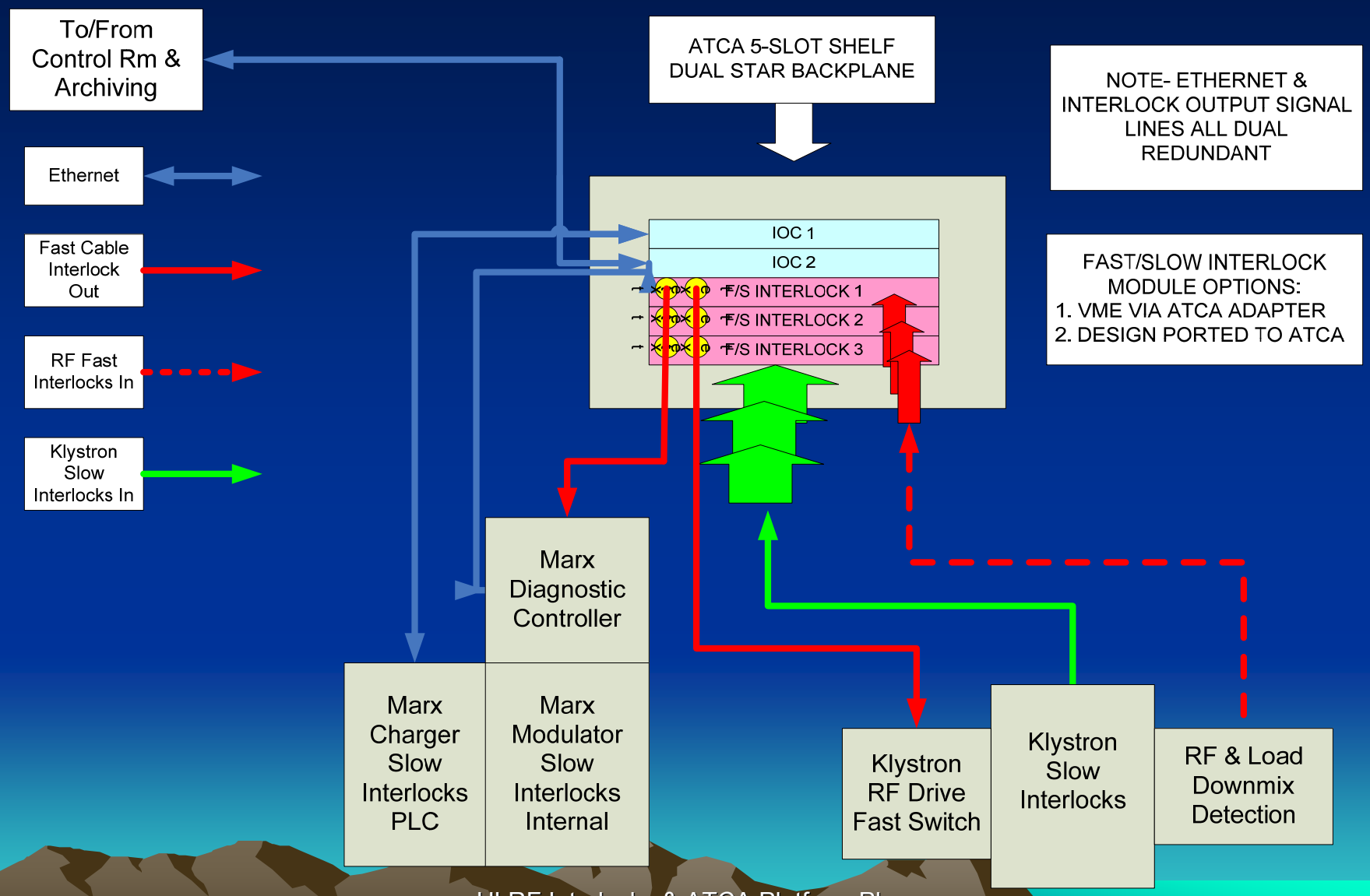
Fast & Slow Ch ADC Displays





Courtesy Z. Szalata

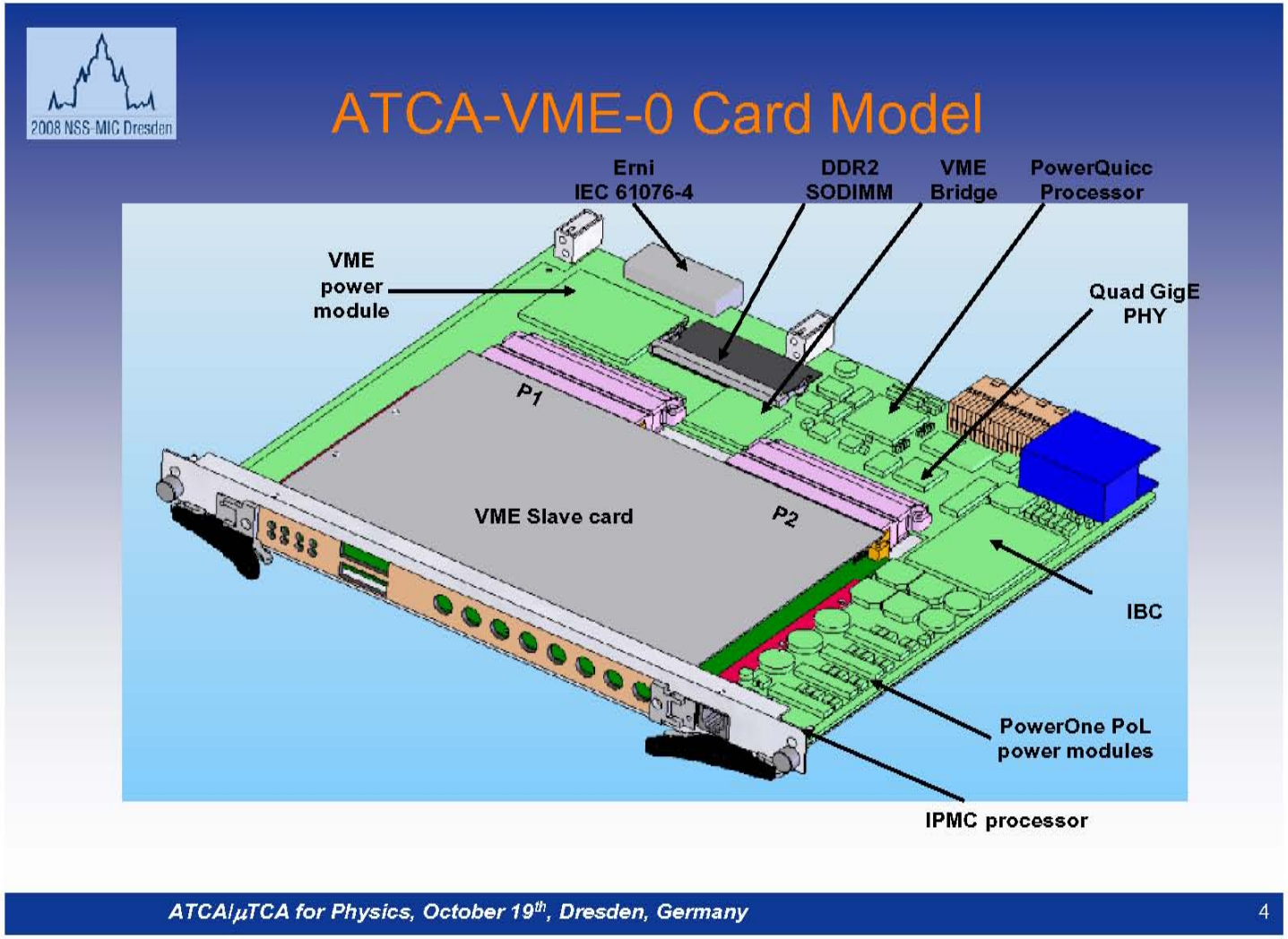
Phase II: ATCA Redundant System



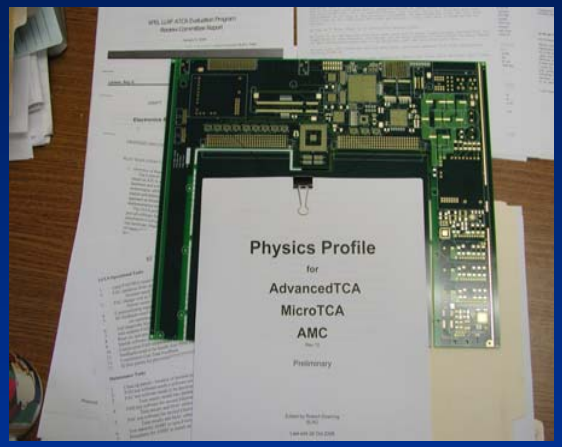
Phase II Goals

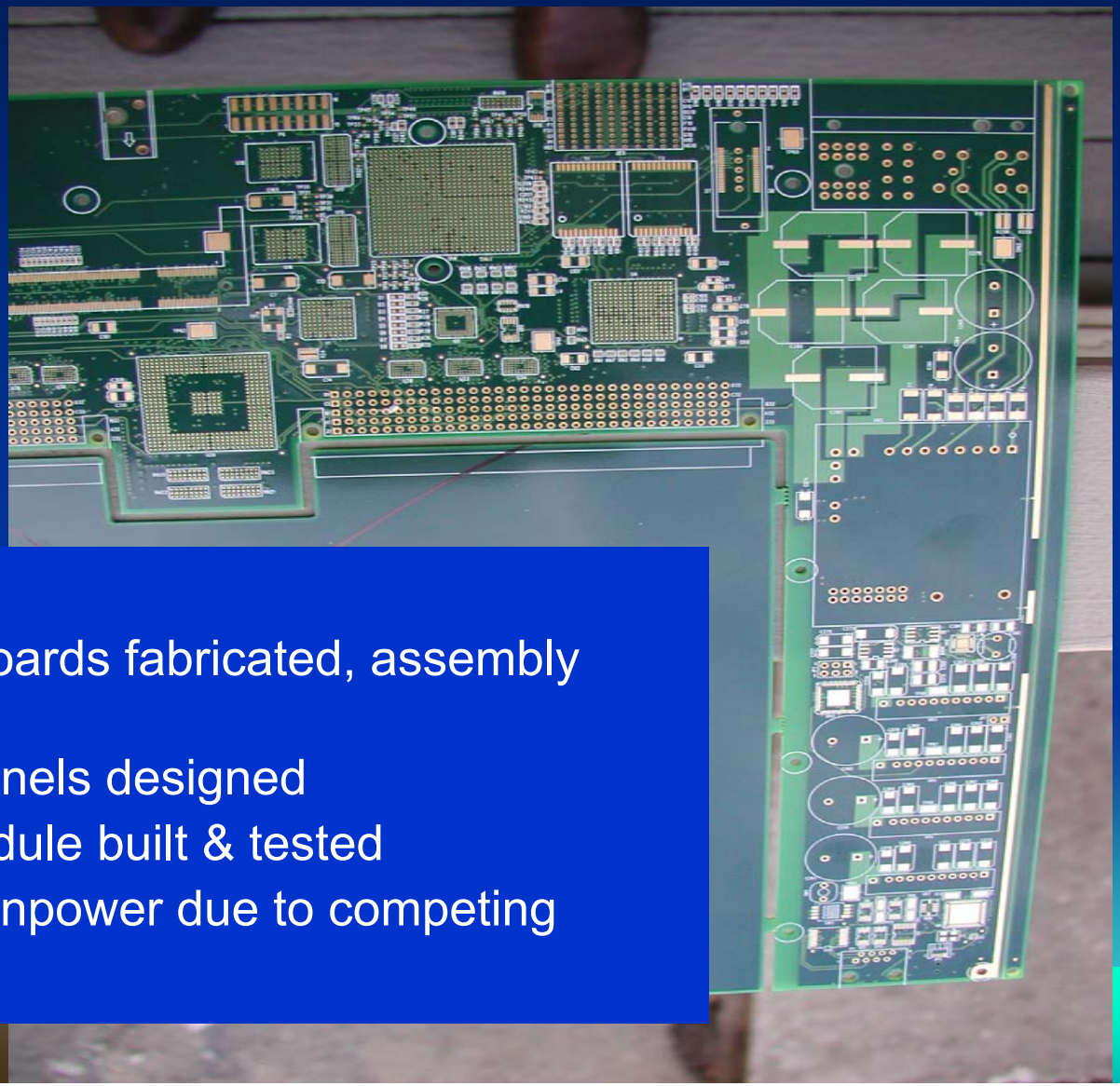
- Test ATCA features in operating environment
  - N+1 redundant controllers, networks, power supply, fans
  - Intelligent Platform Management Interface (IPMI, IPMC)
  - Hot swap capable
  - Auto-failover software
- Method(s)
  - Mount VME modules into ATCA Adapters, or
  - Port VME F3 design to ATCA, or
  - Port VME F3 design to MicroTCA (AMC mezz. Cards)

VME-ATCA Adapter



Prototype ATCA-VME Adapter Board





- Status
  - Four 18-layer boards fabricated, assembly starting
  - Card guides, panels designed
  - VME power module built & tested
  - Short of test manpower due to competing projects

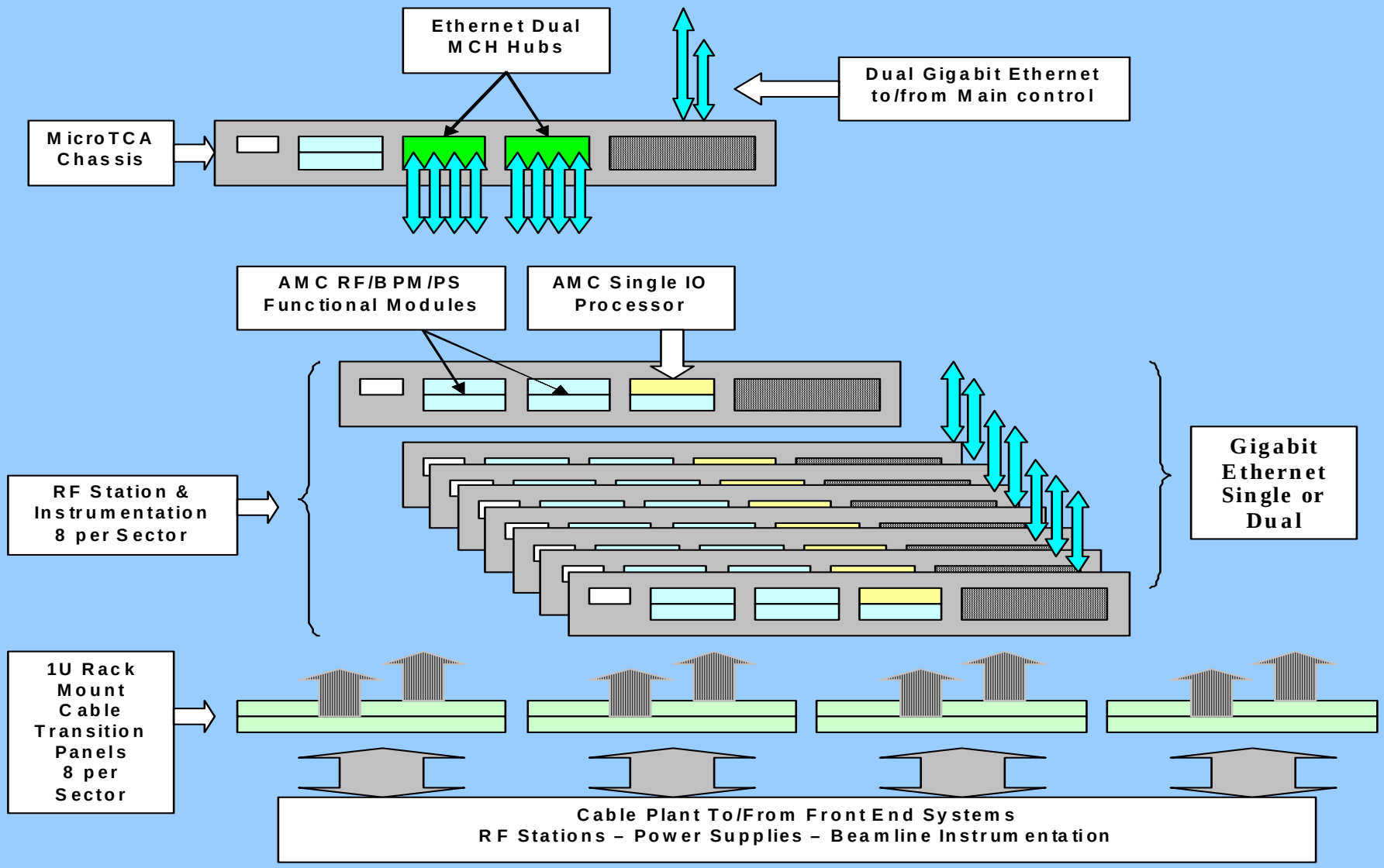
ATCA Physics Standards Workshops

- Dresden ATCA Workshop Oct 18-19-08
  - In conjunction with NSS-MIC, ~50 attendees, 11 industry & lab tutorials, demos; 12 contributed papers
  - Largest activity at DESY
    - ATCA for LLRF system
    - MicroTCA for Interlocks & machine protection
  - Several other labs including SLAC, IHEP building powerful DAQ boards on full ATCA platform
  - Strong manufacturing interest in physics shown at workshop
  - ***Proposed developing xTCA standard extensions for physics applications under PICMG Working Group via Physics Profile Draft Document; collaboration with industry***
  - ***Proceeding to implement***
- Next ATCA workshop/tutorials planned for May 2009 IEEE Real Time Controls conference, Beijing; NSS-MIC 2009 in Orlando FL

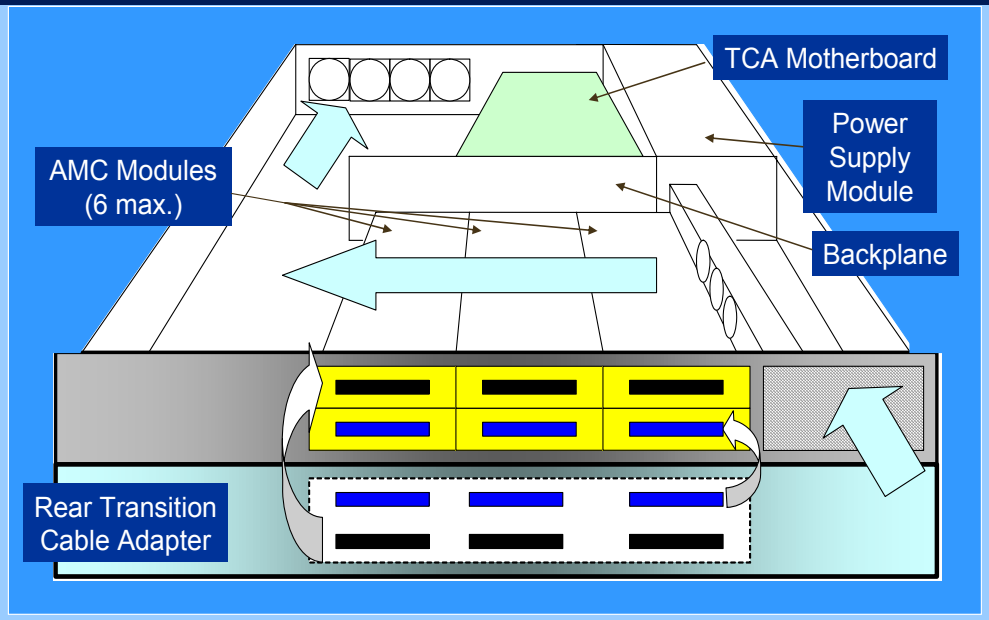
Controls Application at SLAC

- Plan approved to replace central VAX, CAMAC in Linac RF stations, beamline instrumentation
  - Convert 80 RF Stations and instruments for LCLS, 2-4 year project
  - Later convert remaining 160 RF Stations, Damping Rings, Injector for HEP experiments
- Exploring MicroTCA platforms, Advanced Mezzanine Card (AMC) options, HW-SW-FW
  - Modern serial GbE platform with embedded IPMI infrastructure, AMC IOC, AMC payload slots
  - Scalable redundancy features as required
- Purchased integrated development platforms, IO modules for experimentation

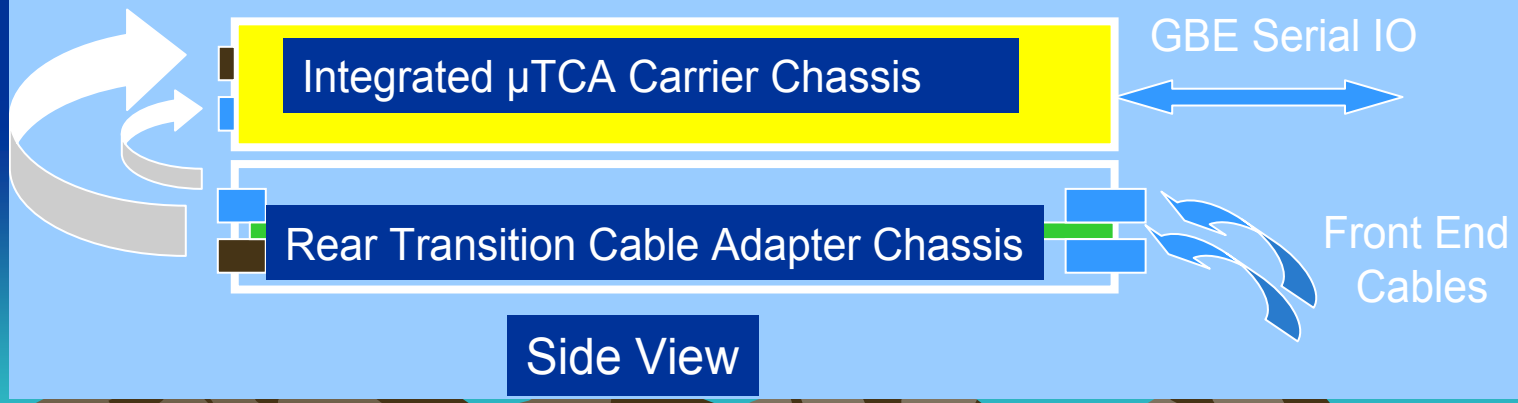
Linac Controls Upgrade Concept Stage 2



Front End Cable Transition Adapter

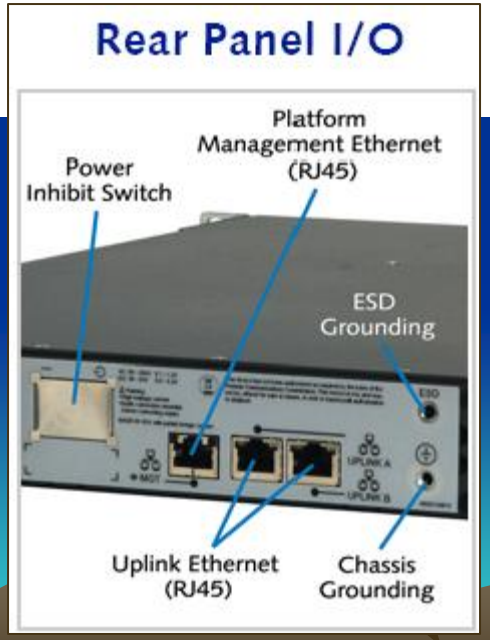


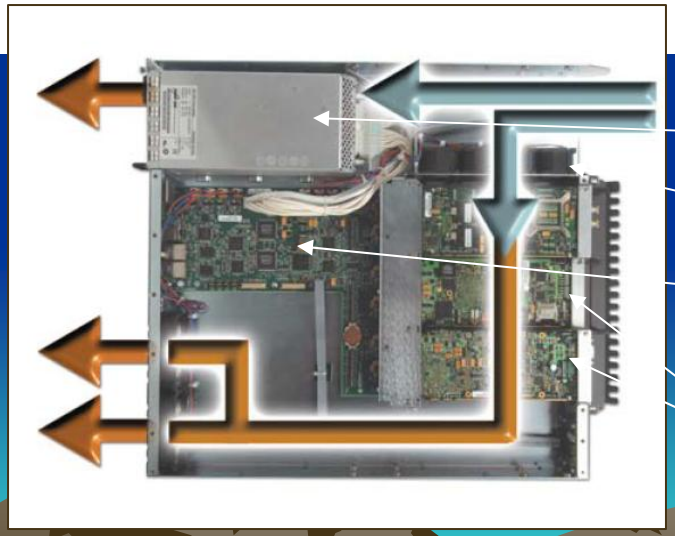
- Develop standard adapter with analog, RF, digital connector options
- Cable entry from rear top or bottom of racks



Integrated 1U Chassis w/ IOC & NexusWare Software

Performance Technologies MTC5070 (2 purchased)





-48V Bulk Supply

Redundant Fans

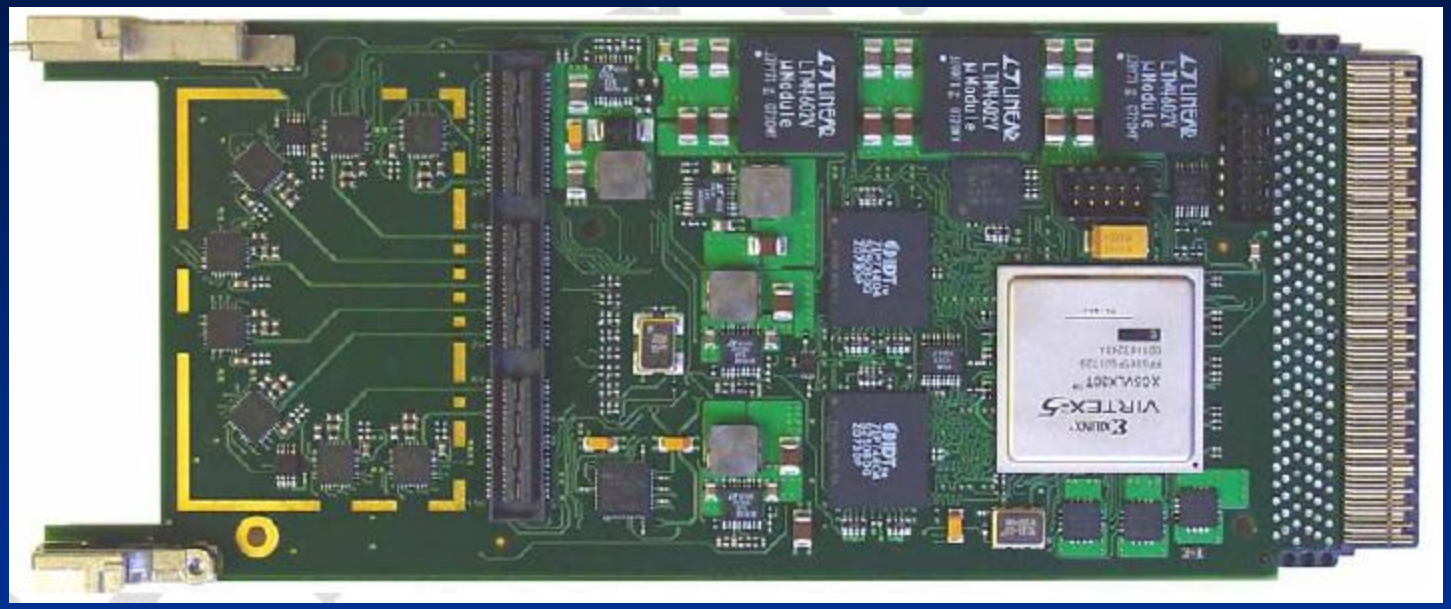
Embedded Shelf Manager & Hub Switch

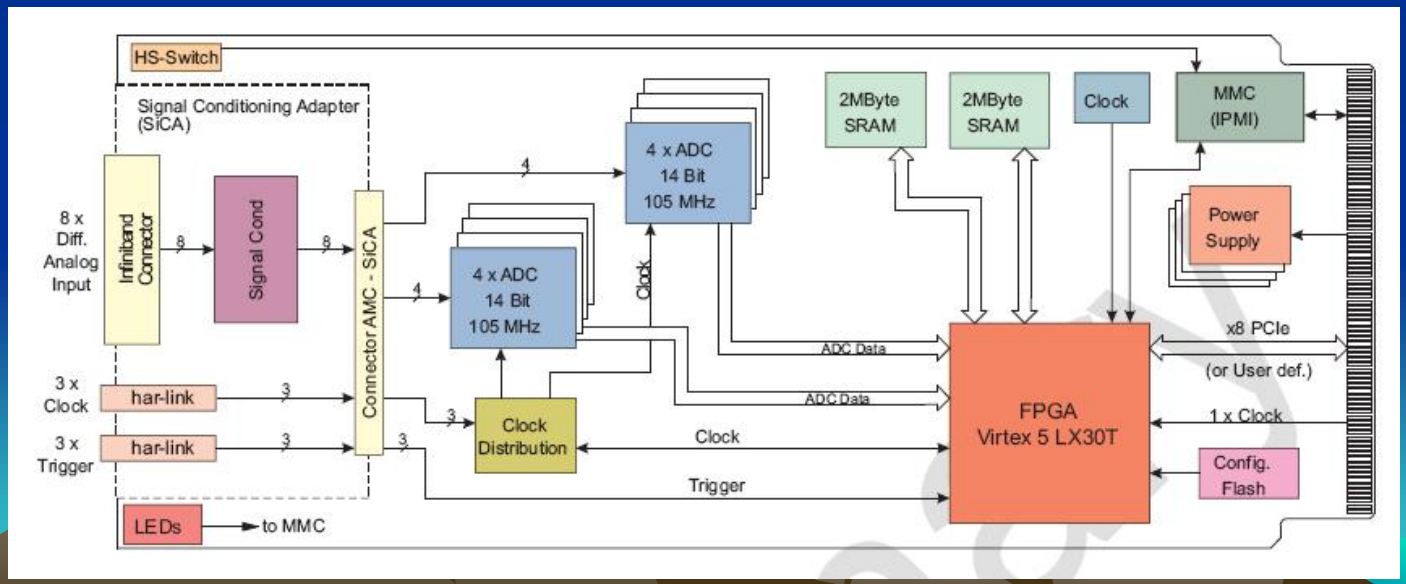
AMC Payload

AMC IO Modules Purchased

- TEWS Technologies
  - ADC 8 Ch 14bit 105 MS/s AMC (2)
  - Adapter AMC-Industry Pack (IP) (2)
  - ADC 16 Ch 16 bit 100 KS/s IP (2)
  - DAC 16 Ch 16 bit 100 KS/s IP (2)
- VadaTech
  - Adapter AMC-PCI for PCI CAMAC Branch Driver (2)

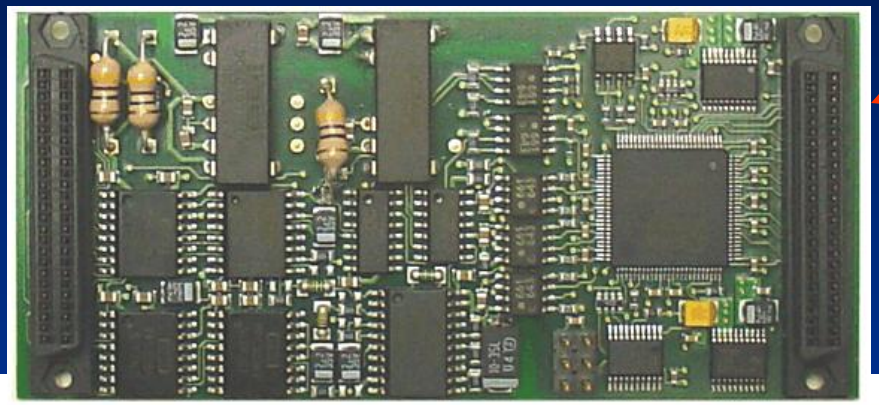
AMC Module –TAMC900 ADC



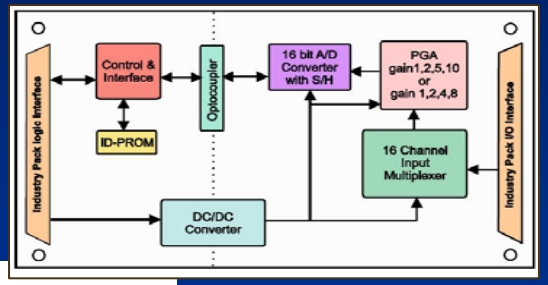


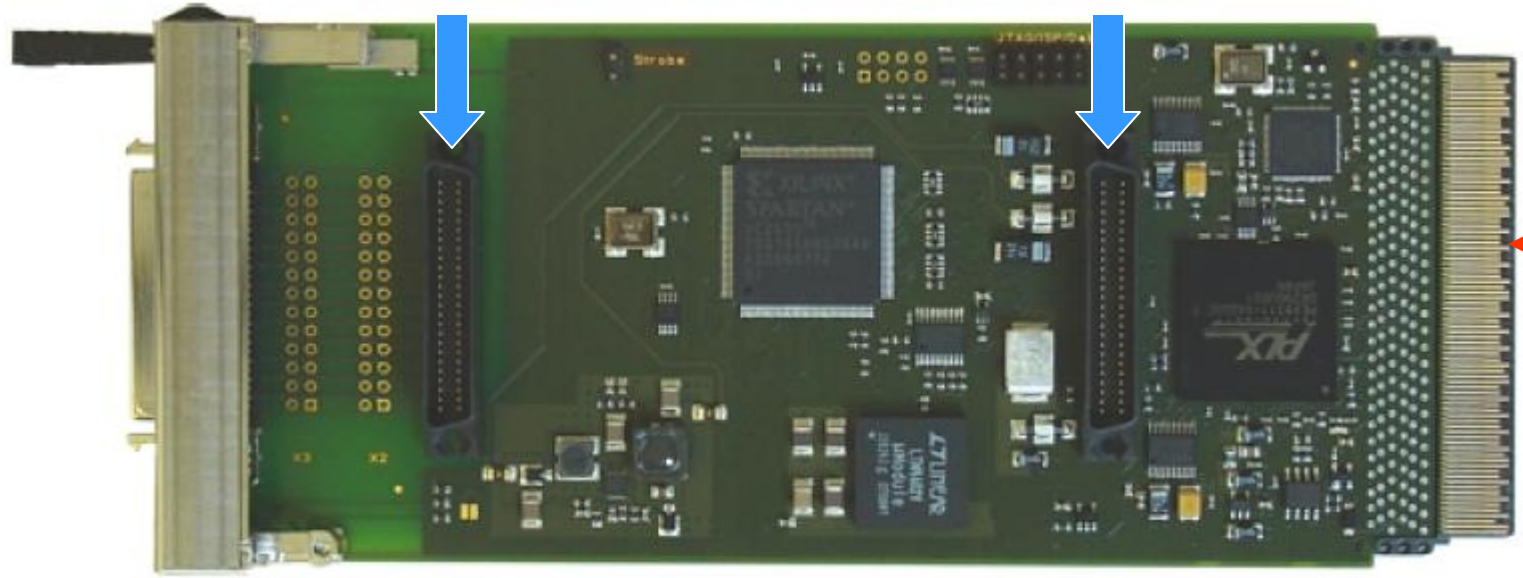
**8 Ch 14 Bit 105 MS/s ADC Brd~
**~7x3 inches
**Edge card connector 85 contacts per side
**Virtex 5 FPGA
**FW under design @ DESY

AMC-IP Carrier (TEWS)



IP ADC 16 Ch 16 Bit
100 KS/s





AMC-IP
Adapter
w/Xilinx
Spartan II

AMC-PMC Carrier (VadaTech)

Request More Information

AMC100

AMC Site Carrier For PMC/PrPMC Modules

DESCRIPTION

The AMC100 is a double width, full-height module, based on the AMC.1 Specification. The AMC100 allows PMC or PrPMCs to be installed in an AMC slot. The PMC/PrPMC PCI-X bus runs at 133MHz. The J4 connector of the PMC/PrPMC is routed to the front panel of the AMC module. For PMCs and PrPMCs that are PICMG 2.15 compliant, the Gigabit Ethernet ports are routed to the AMC connector per AMC.2 specification.

This modular approach allows an AdvancedTCA chassis to integrate the large numbers of PrPMC modules as well as PMC I/O modules that are available in the market. The AMC100 can be configured to run in non-transparent, transparent or root complex mode.

Key Features | Downloads | Related Products

- Support for PMC and PrPMC modules
- 64-bit PCI-X @133MHz
- IPMI 2.0 Compliant Module Management Controller (MMC)
- 32-bit IPMI RISC Processor
- IEEE Std P1386.1-2001 (PMC) Compliant
- ANSI/VITA 32-2003 (PrPMC) Compliant
- RoHS Compliant
- OS Support for: Linux, Windows, Solaris and VxWorks
- AMC.1 and AMC.2 Compliant
- PCIe x4 Lanes
- Transparent or Non-Transparent Operating Modes
- PMC J4 connector routed to front panel Mini SCSI type connector or Gigabit transceiver to AMC.2

PMC w/ FPGA
Currently used in VME IOC
CAMAC Serial Branch Driver
Prototype

Summary Status & Plans

- VME Interlock System
  - F3 FPGA based test stand interlock system in test, hardware installation continuing, interlock software nearing completion
- VME-ATCA Adapter
  - Board loading underway; will need IPMI, driver software development to complete
  - Reference design for future AMC carrier board
  - Future: Implement ATCA adapter version of test stand interlocks
- AMC's in MicroTCA promising for future controls upgrade
  - Commercial AMC, IP products can perform most SLAC linac controls functions
  - Collaborating with DESY to get fast ADC Firmware
  - Plan initial experimental tests in FY 09
- *Future:*
  - *Port controls designs directly to generic AMC FPGA modules with front-end plug-in options*
  - *optimize use of xTCA infrastructure over more payload modules*