SPIROC tests @ DESY

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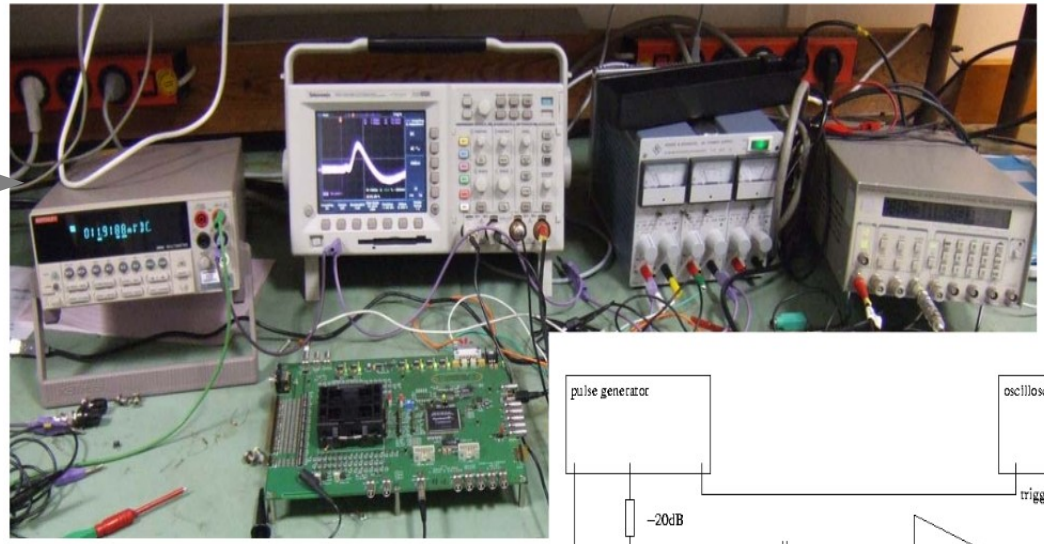
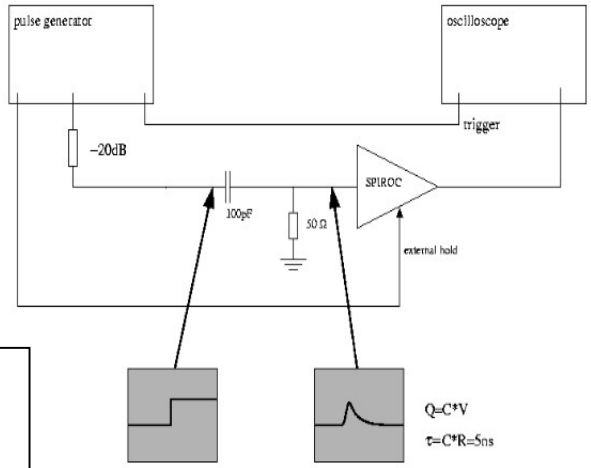
status of measurements – analog part

Test setup:

Pulser + Coupling C +

Oscilloscope





outline

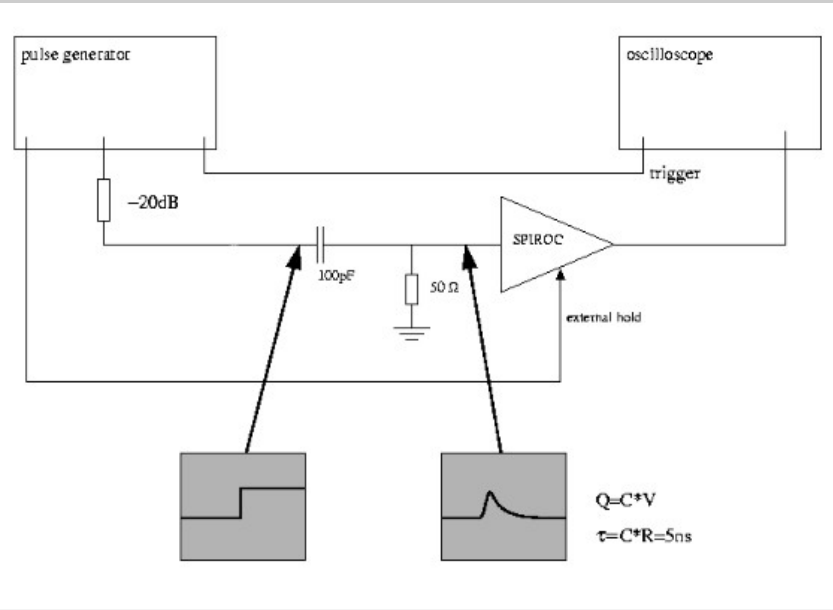
- external trigger
  linearity puzzle
    large feedback nonlinearity
    track & hold
  noise study
    different feedback
    different shaping time
- auto-trigger
  jitter & trigger
  inter-calibration

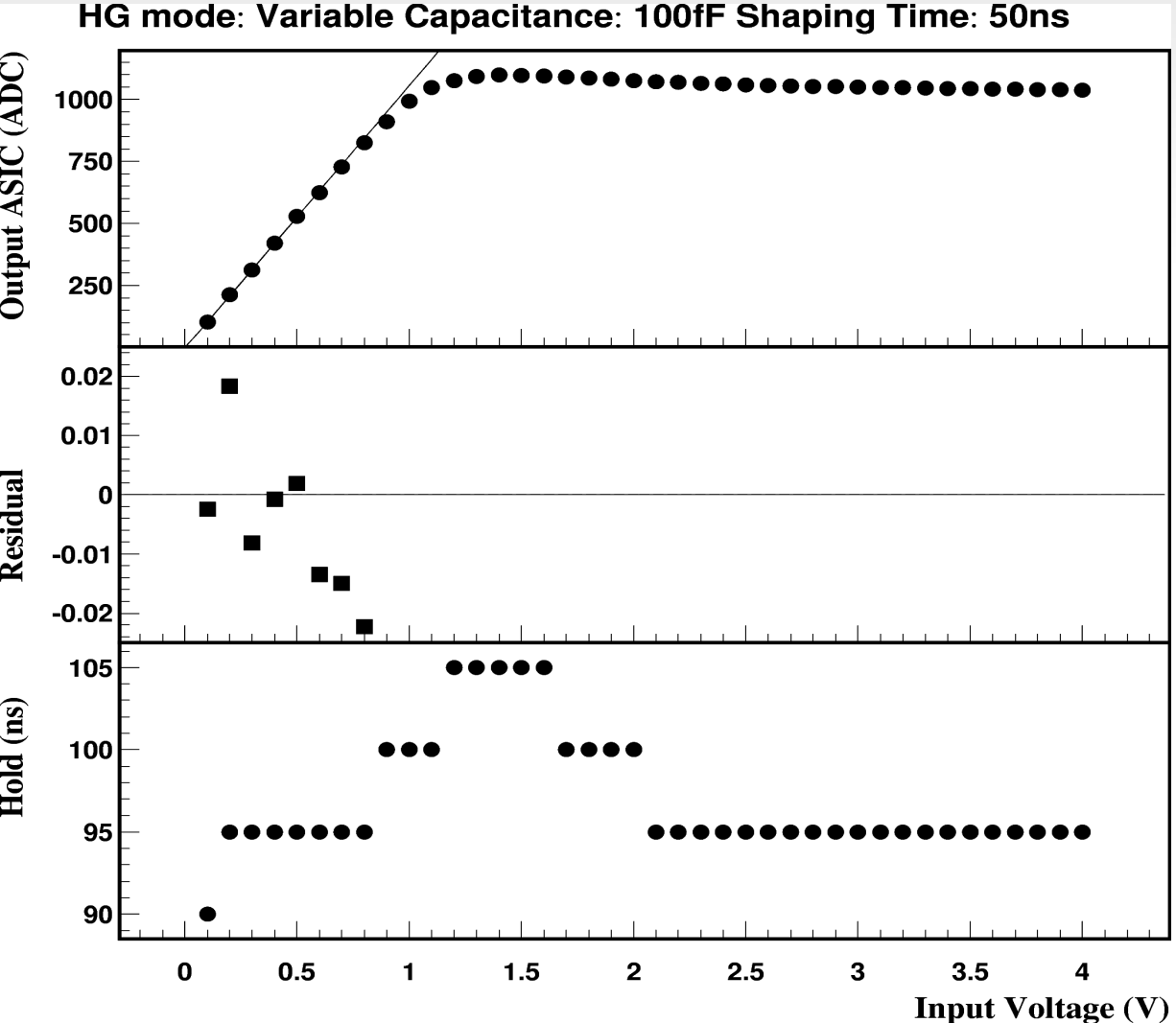
linearity puzzle (external trigger)

external hold - linearity

Q=Cc*V*0.1 , Cc=100pF

0.1 - 20dB attenuator





High Gain mode

voltage-scan @

50ns shaping time

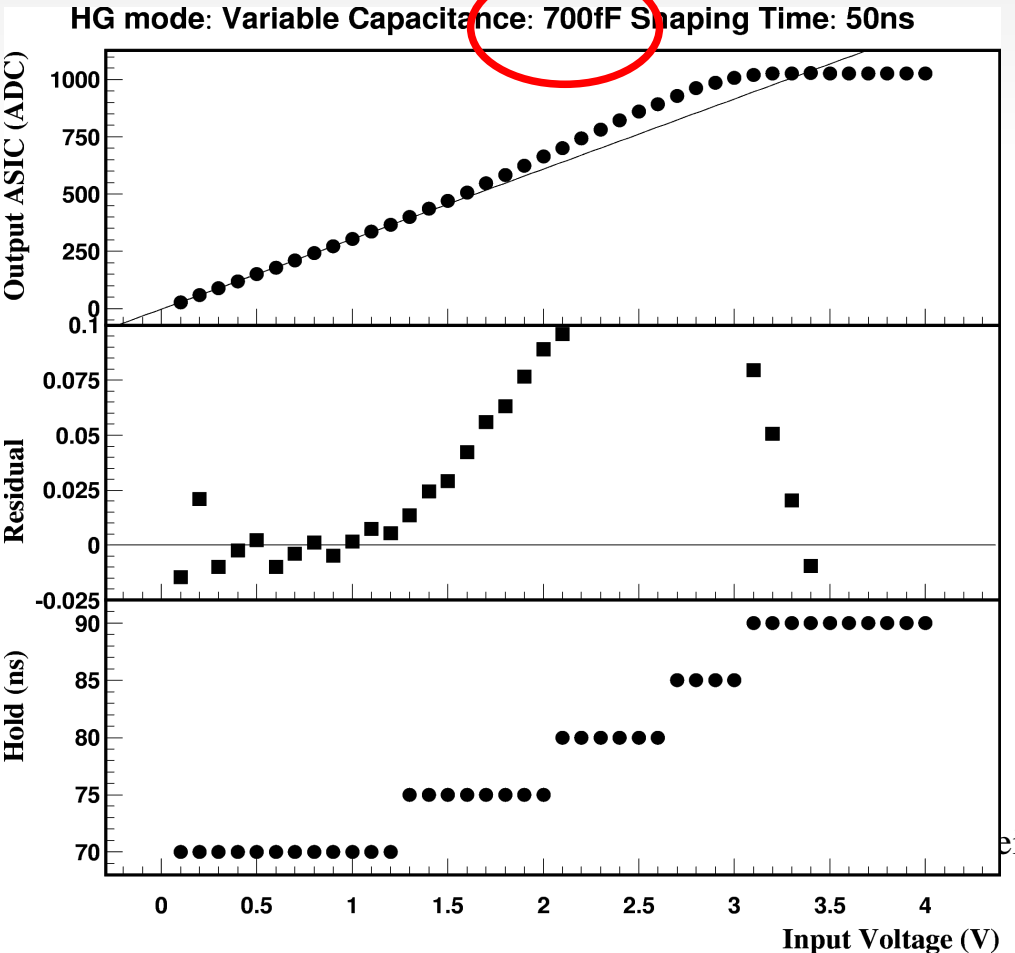
different feedback cap.

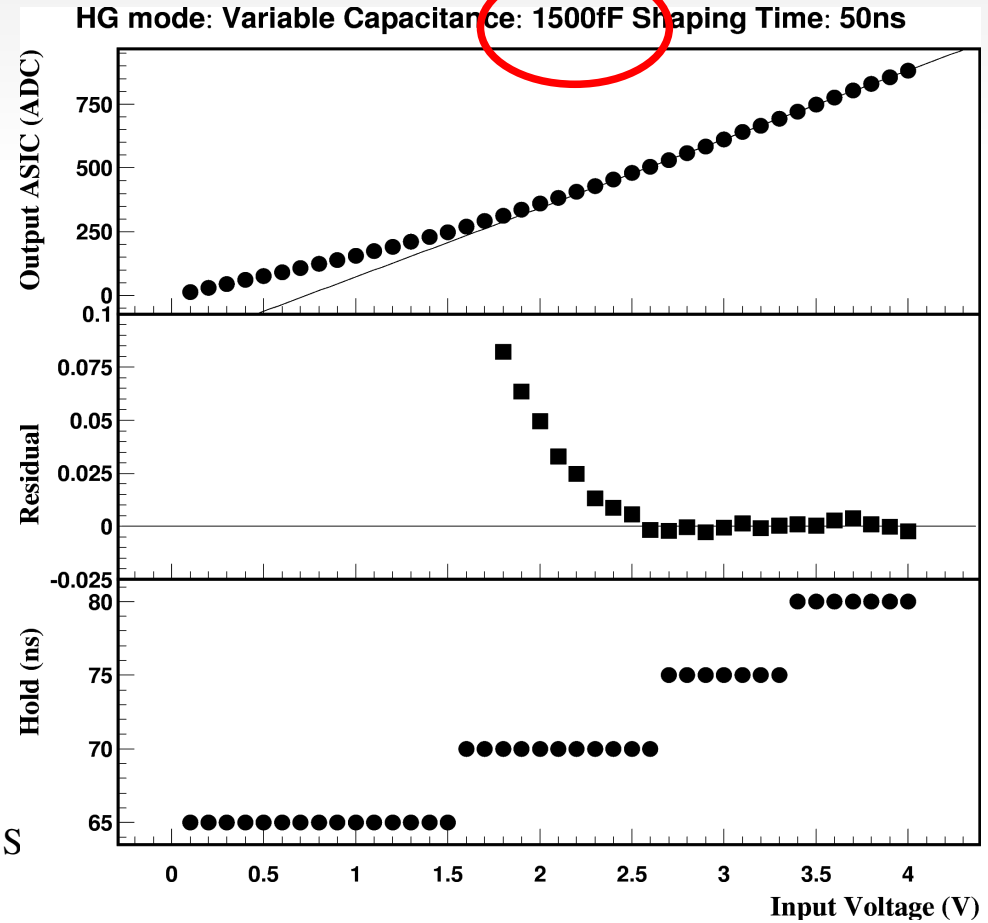
peaking time not fixed

external hold - linearity

both high & low gain path

non-linearity appears when operating at higher Feedback Capacitance

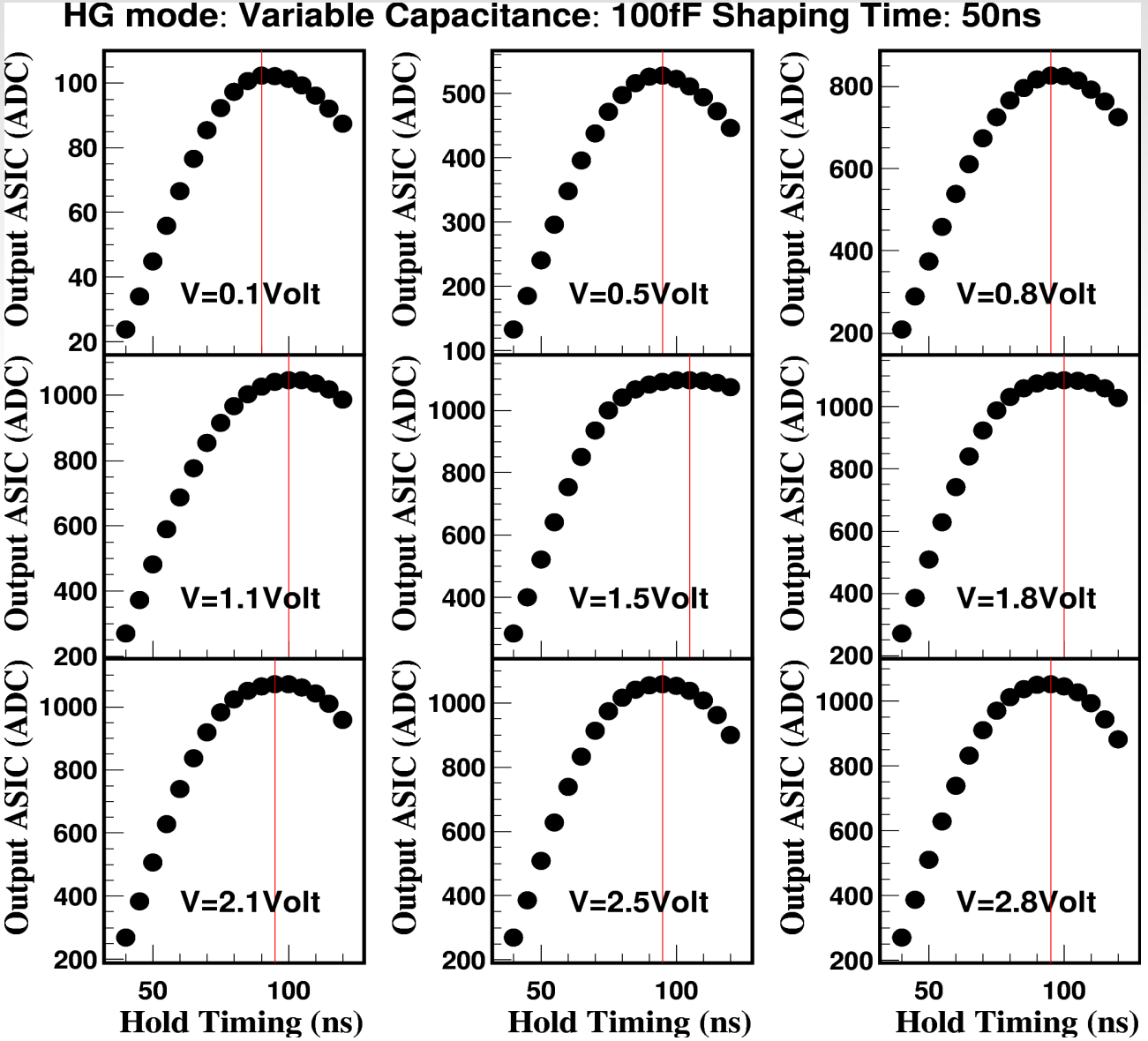




Analog output with external hold

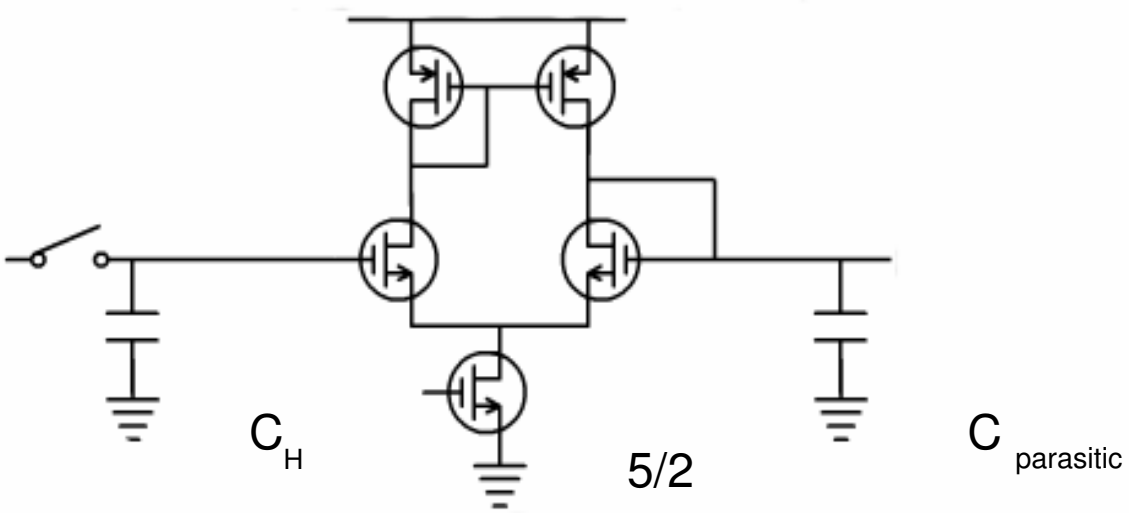
HG & LG mode

Peaking time increases with increasing input charge



non-linearity puzzle

- track & hold buffer



I_Q=1 uA -> 50 uA

buffer-nonlinearity reason:

1. parasitic capacitance ~ 1-2 pF
2. small transistor in weak inversion as current source

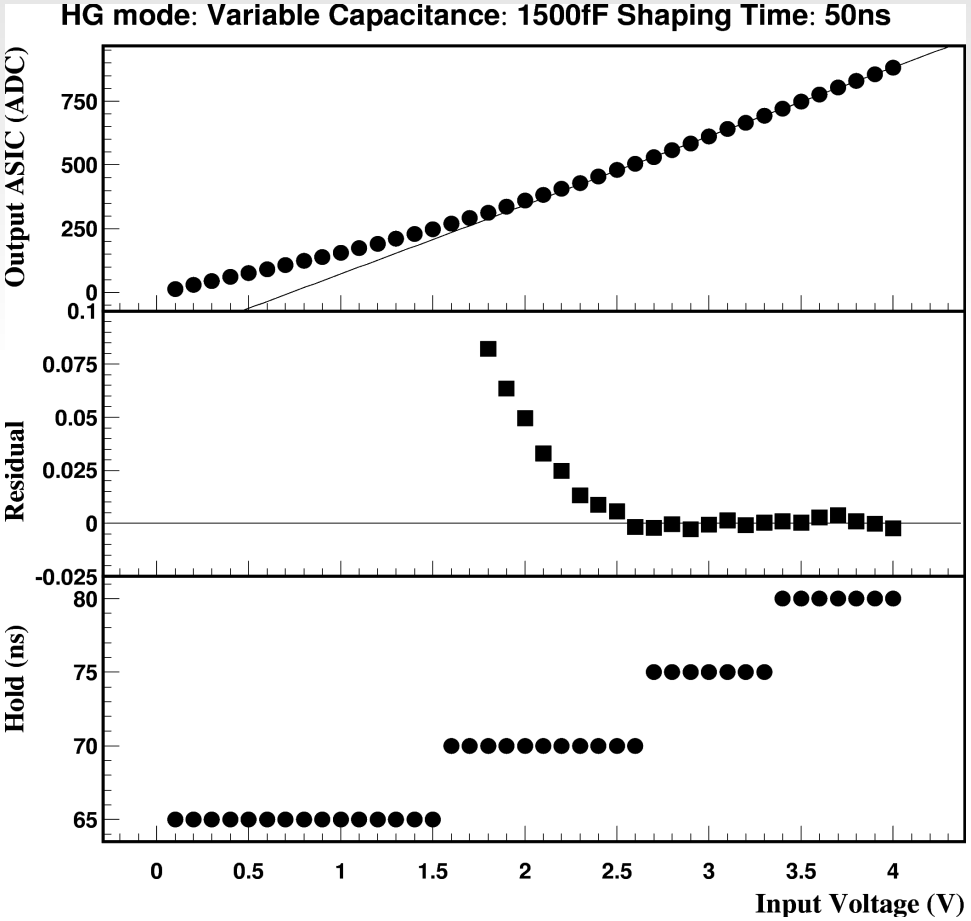
=> small slew rate 1 mV / ns

1. large bias current 50 uA
2. small transistor in strong inversion leads to high Vds(sat)

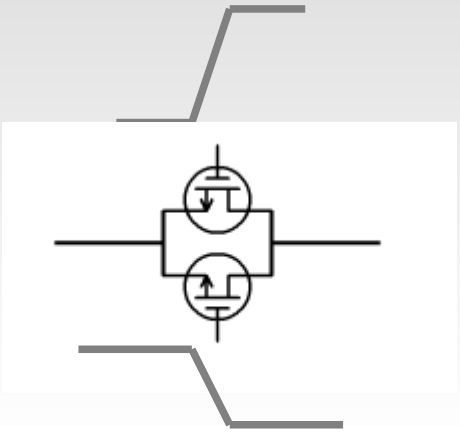
=> first several pts are not linear

sulution: decrease bias current of T&H buffer

peak time puzzle



dummy switch

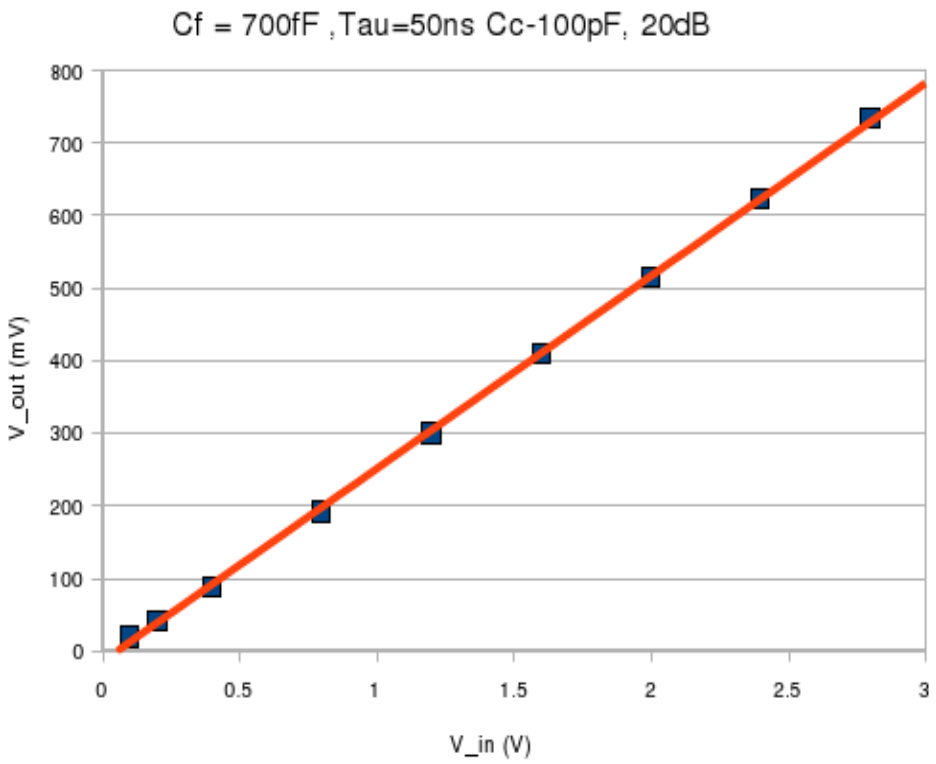


dummy switch designed for compensation of small signal channel charge injection

still need investigation in simulation

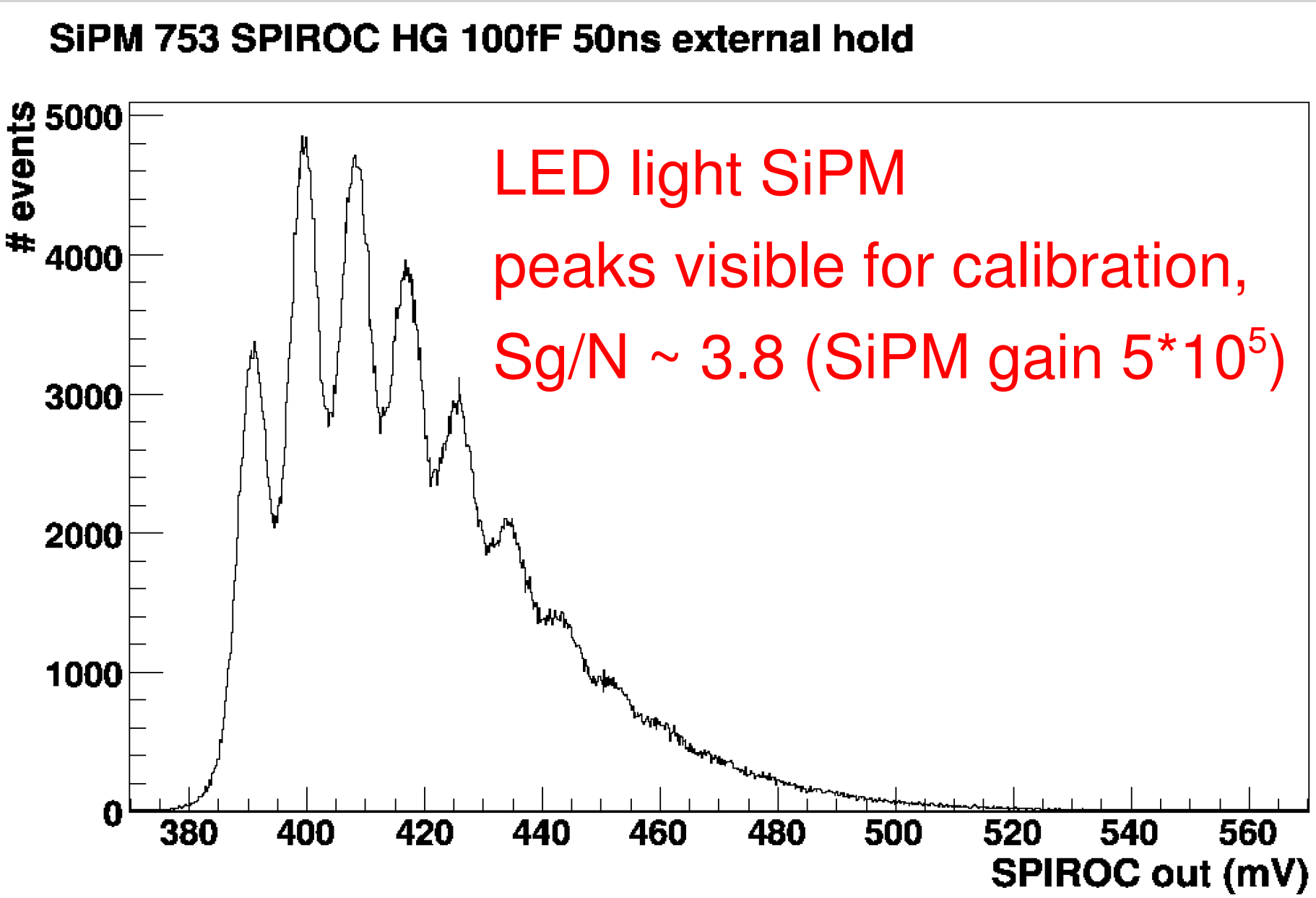
Linearity Improvement

- after reducing the bias current of T&H buffer



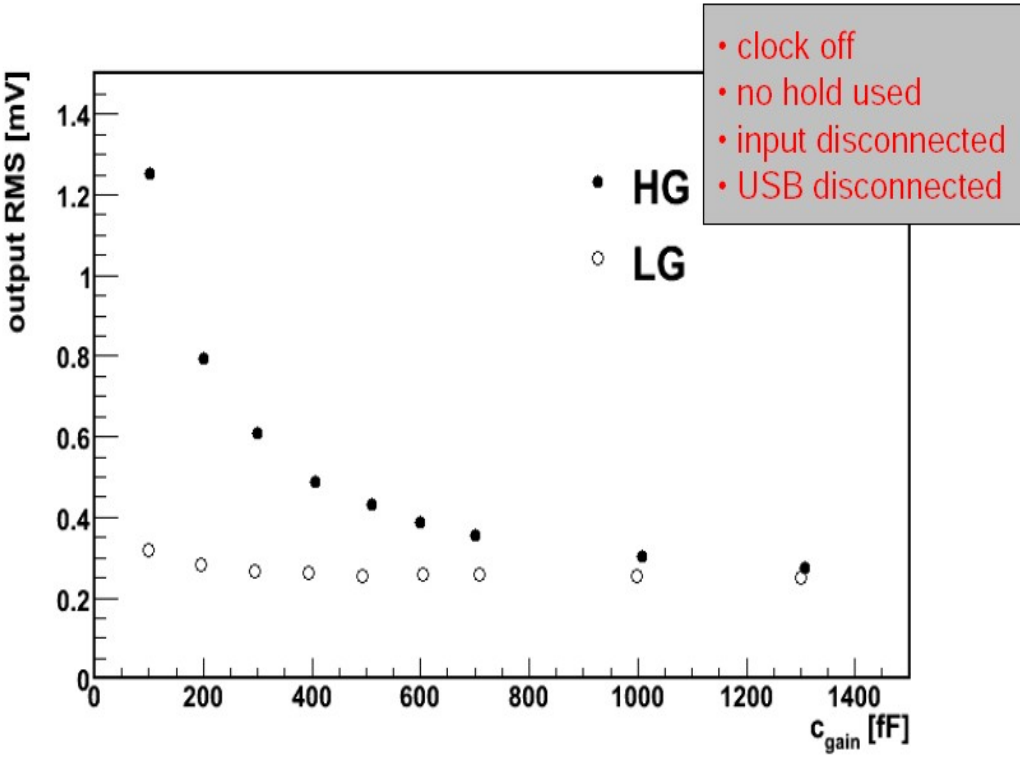
- up to 700fF feedback linear
- peaking time fixed (from non-held signal), switch charge injection needs investigation

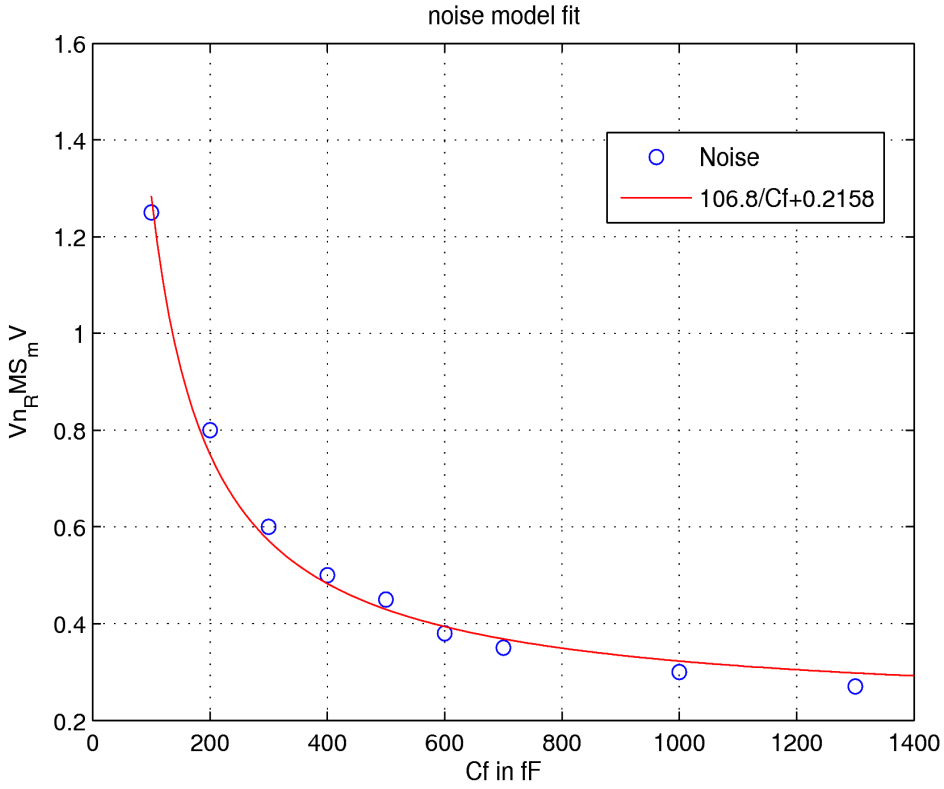
noise (external hold)


SiPM 753 SPIROC HG 100fF 50ns external hold
events
5000
4000
3000
2000
1000
0
380
400
420
440
460
480
500
520
540
560
SPIROC out (mV)
LED light SiPM
peaks visible for calibration,
Sg/N ~ 3.8 (SiPM gain 5*10^5)

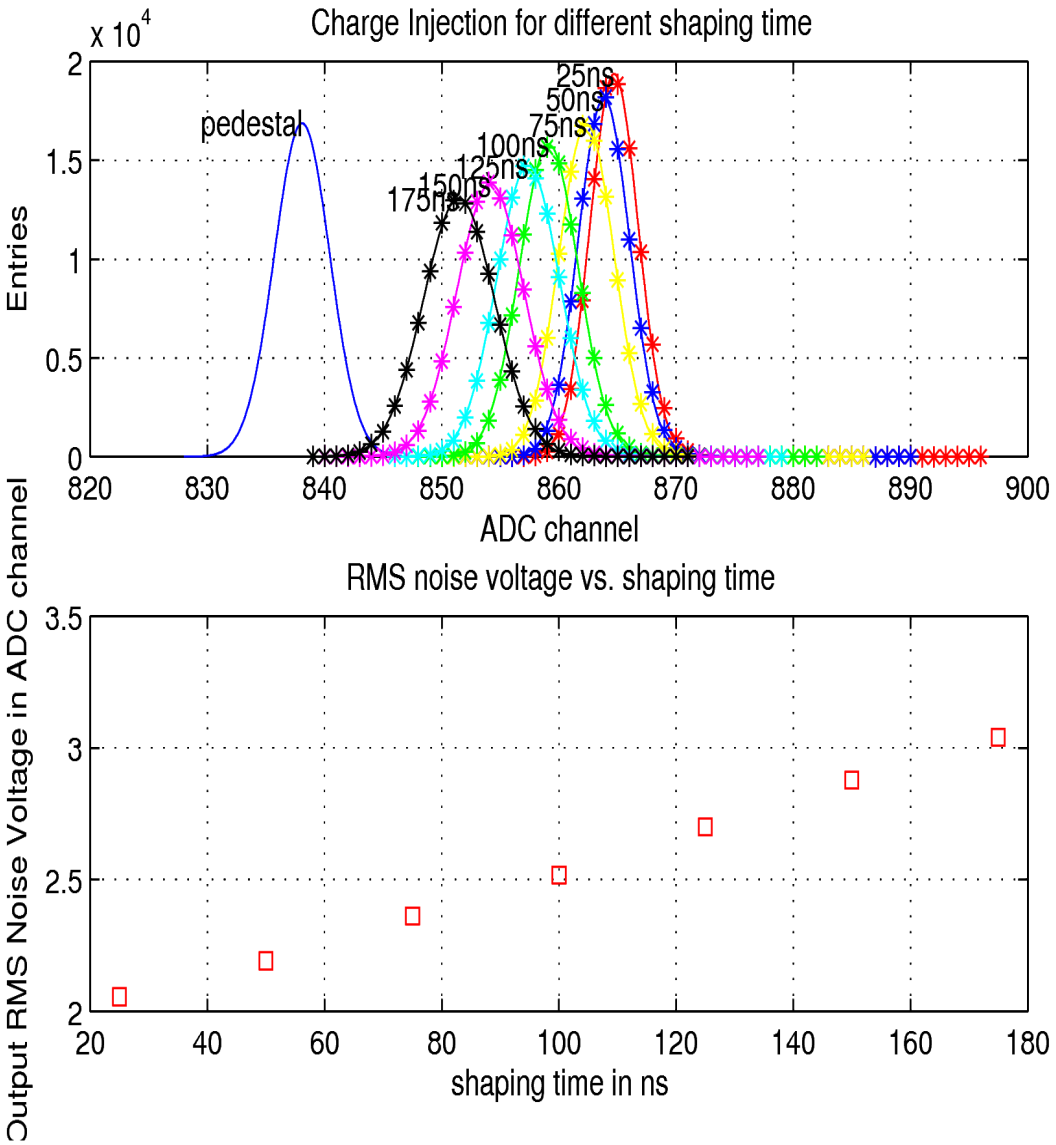
noise study

chip output noise vs. different feedback capacitance





noise vs. shaping time



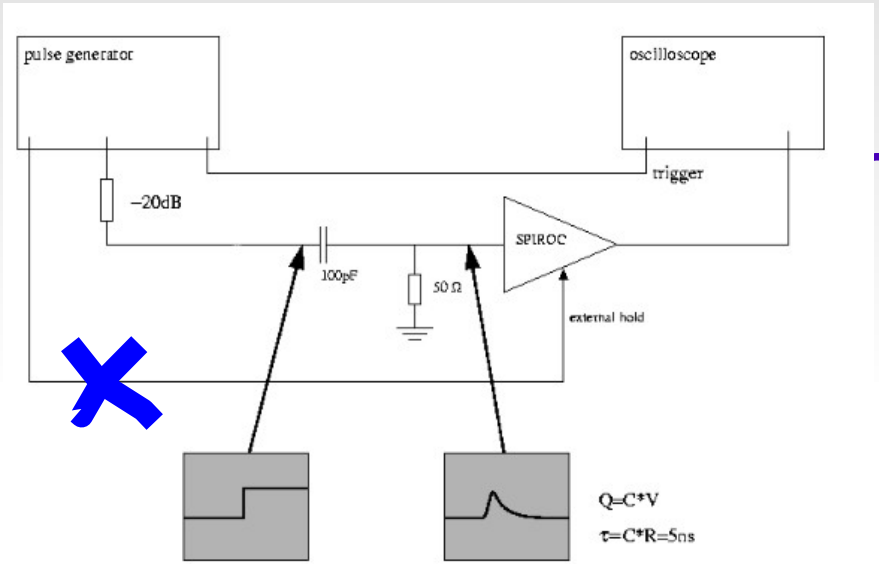
signal decrease with shaping time : consistent with theory calculation and simulation

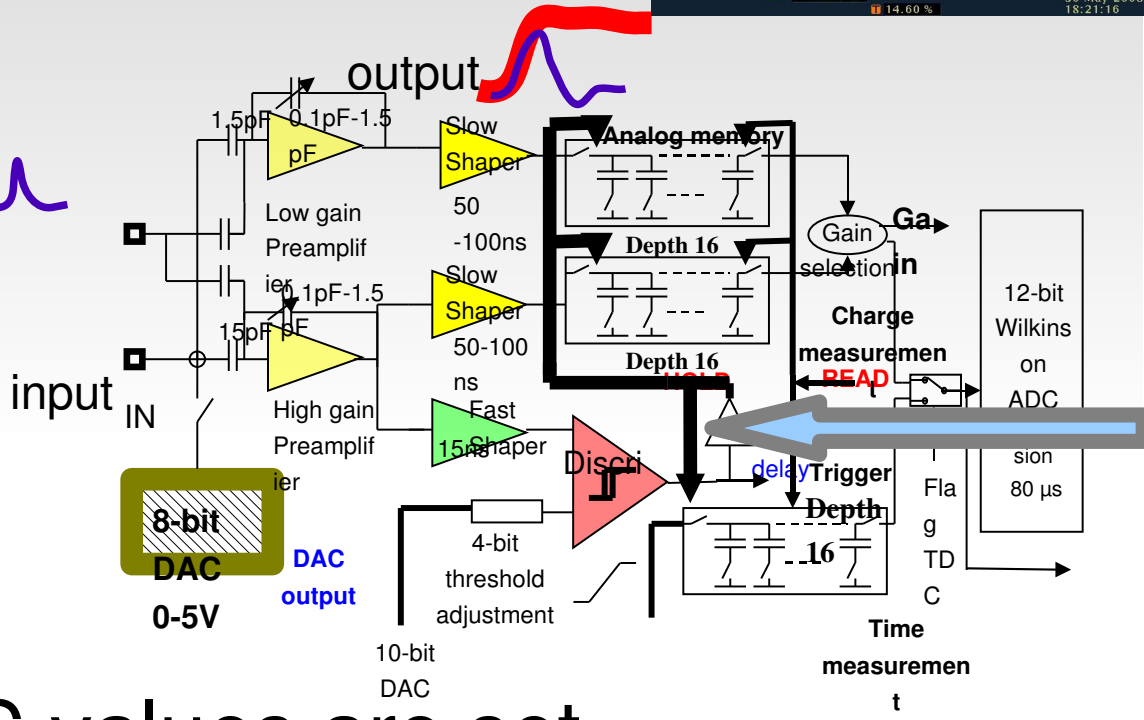
noise increase with shaping time not normal

low frequency noise (from DAC noise ?)

auto-trigger mode

Auto-trigger mode





* Different threshold DAC values are set at the discriminator in the fast shaping line

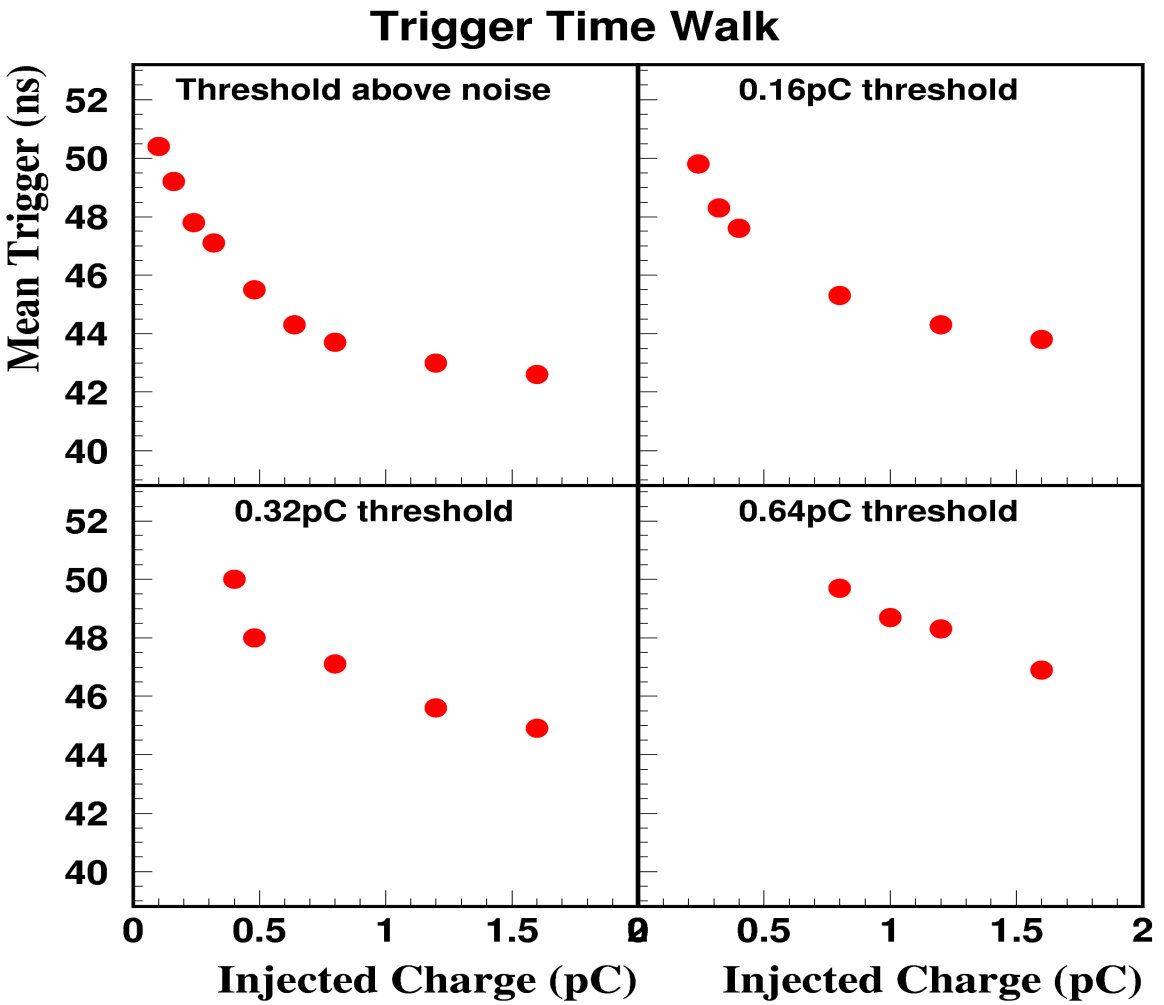
==> trigger time-walk(threshold) ==> trigger jitter(noise)

Auto-trigger mode

SiPM Gain – $0.5*10^6$

0.08pC – one pixel

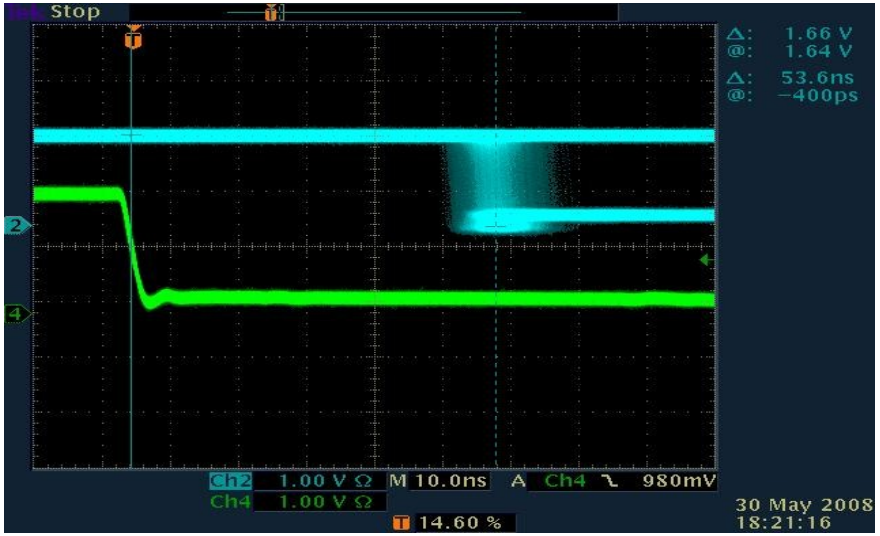
Time walk small @ threshold half a MIP

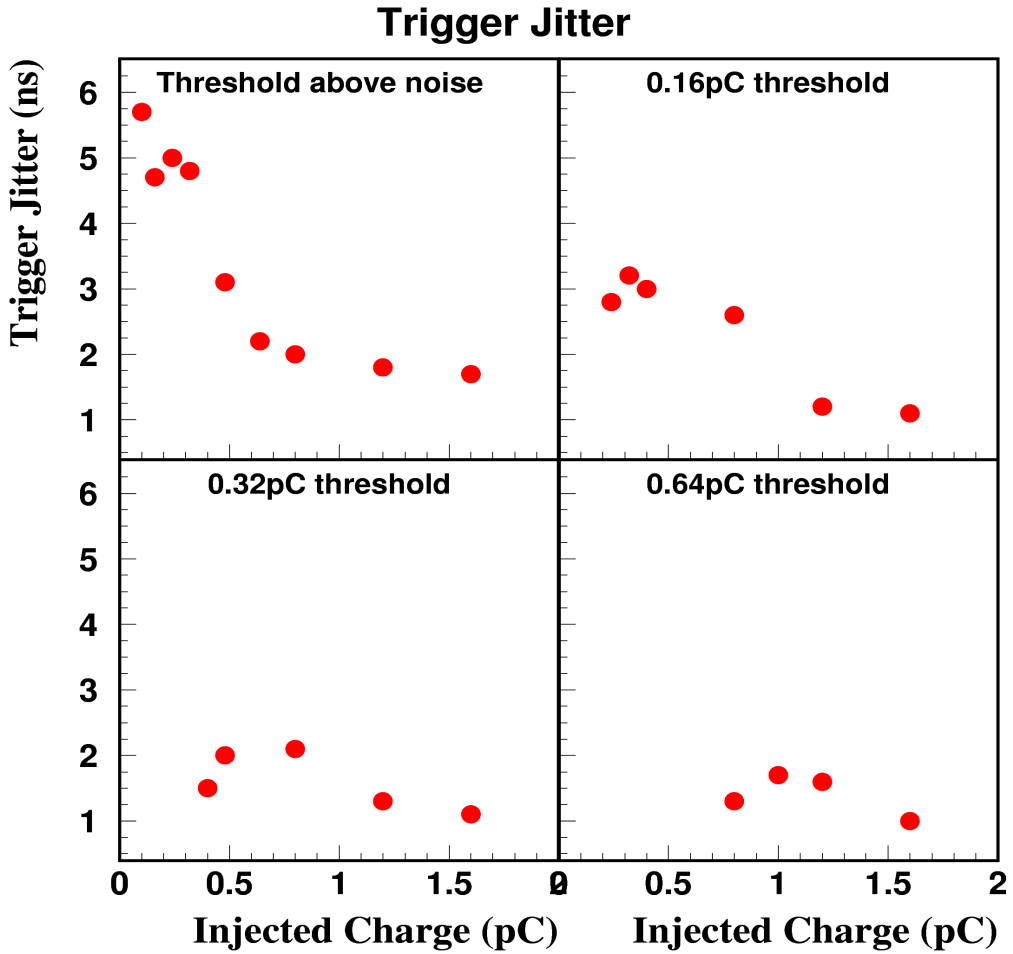


Auto-trigger mode

standard dev. value

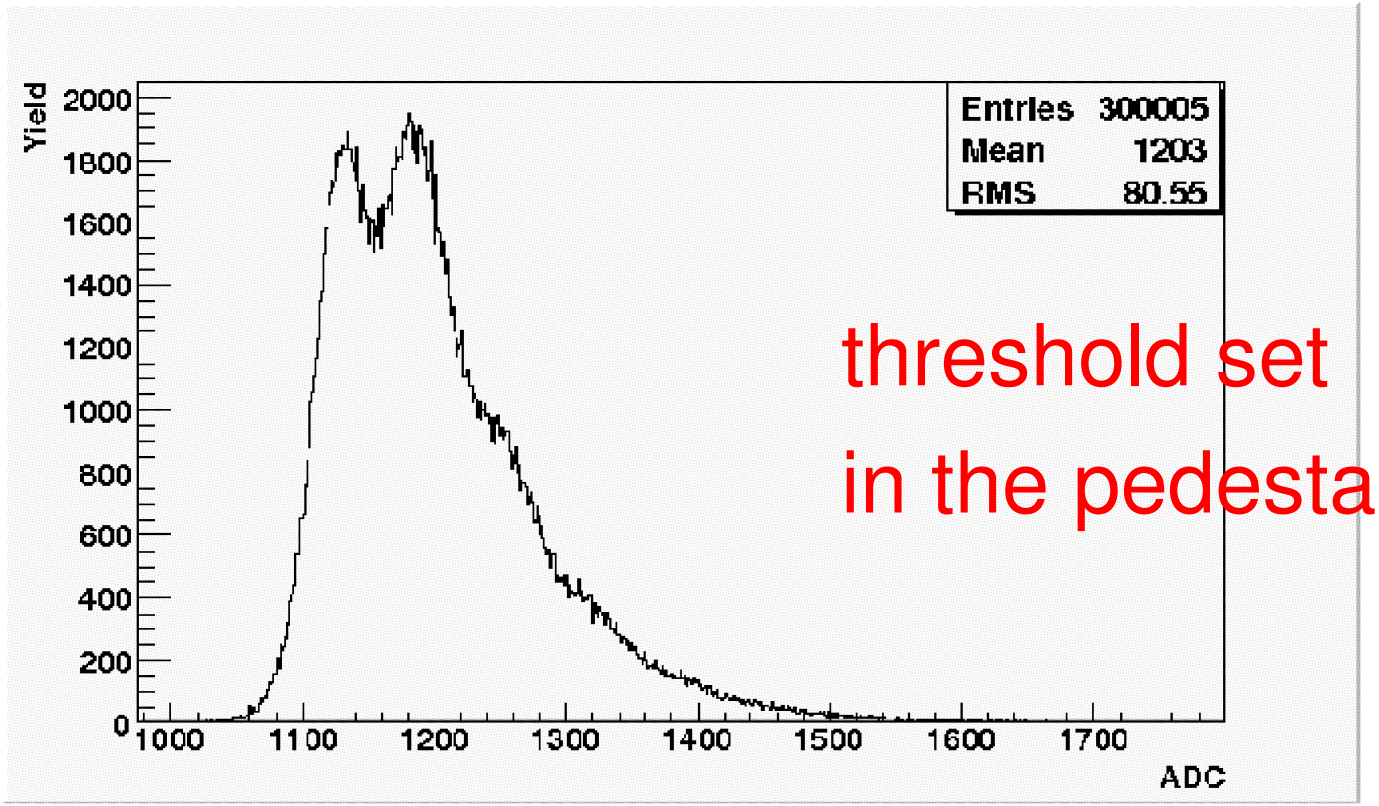
large at low threshold





Auto-trigger mode

thermal noise spectrum with auto-trigger

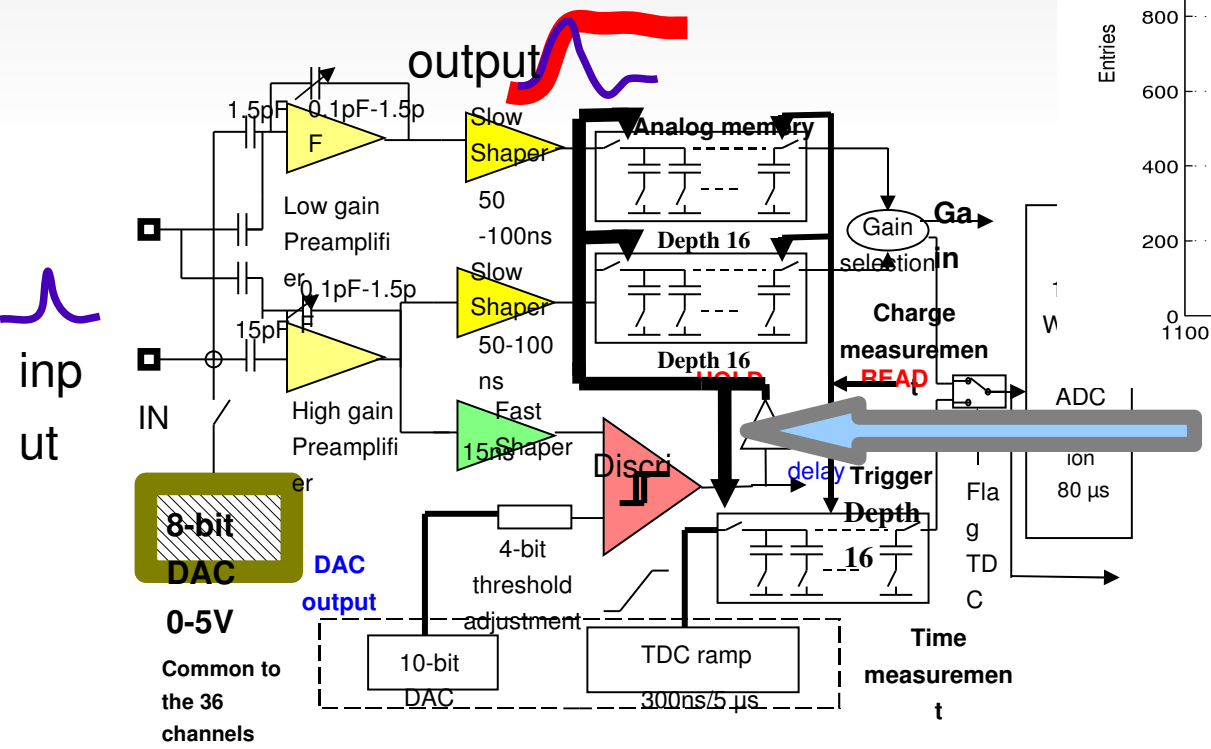


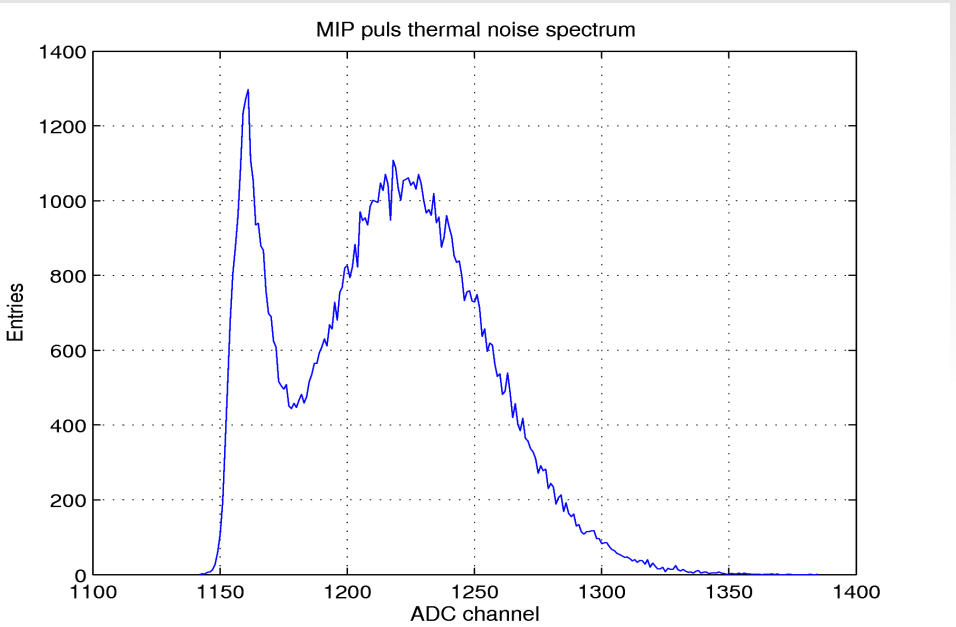
threshold set

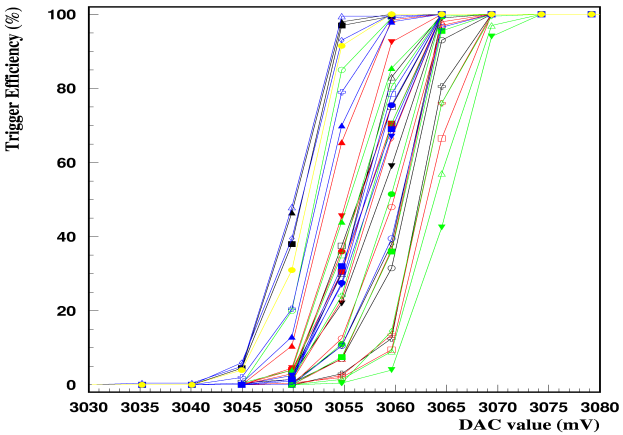
in the pedestal peak

inter-calibration

- threshold level – s-curve (average value, gaussian noise)







inter-calibration

- high and low path calibration (with auto-trigger)

$$LY[pixel] = \frac{Amip}{G} * I_{inter-cali}$$

$$I_{inter-cali} = \frac{A_{calibration}}{A_{physics}}$$

conclusion

- linearity improved new buffer bias current
- peaking time need to be investigated
- time walk & jitter small at ½ MIP threshold

outlook

- SPIROC1b : ADC conversion with external ramp