

Report on GRPC/DHCAL in Europe



CIEMAT, IHEP, IPNL, LAL, LAPP, LLR, "Bologna"

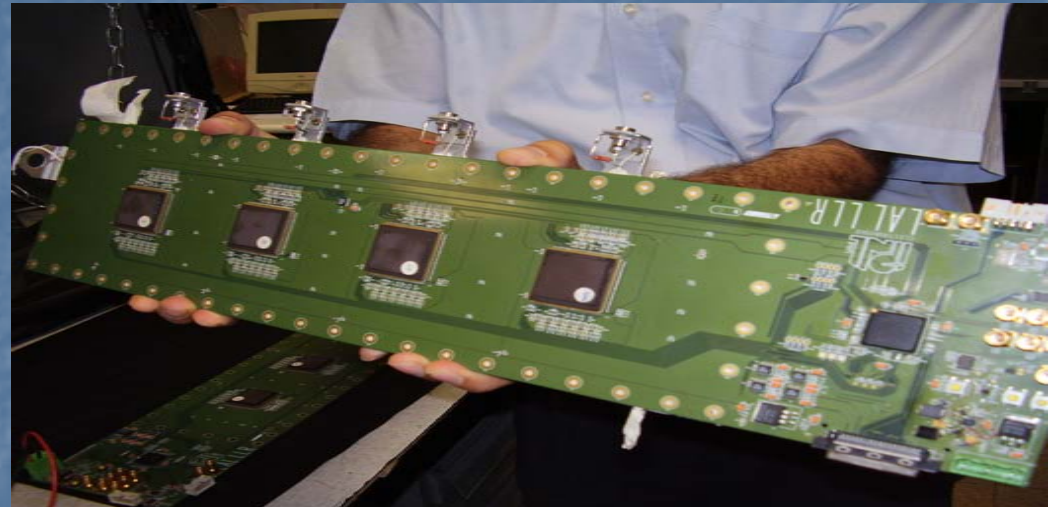
I. Laktineh
IPN-Lyon

Outline

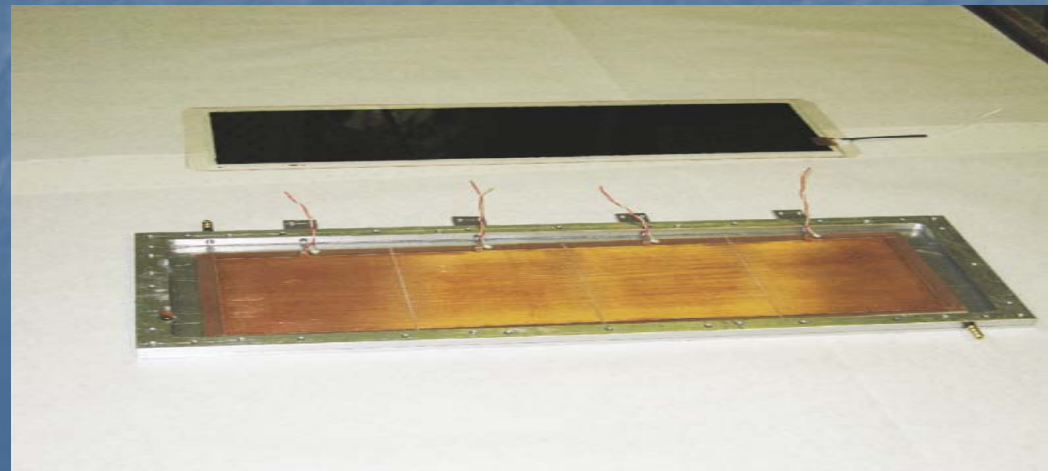
- Mini DHCAL
- Towards the 1 m² project
- Perspectives

Mini DHCAL

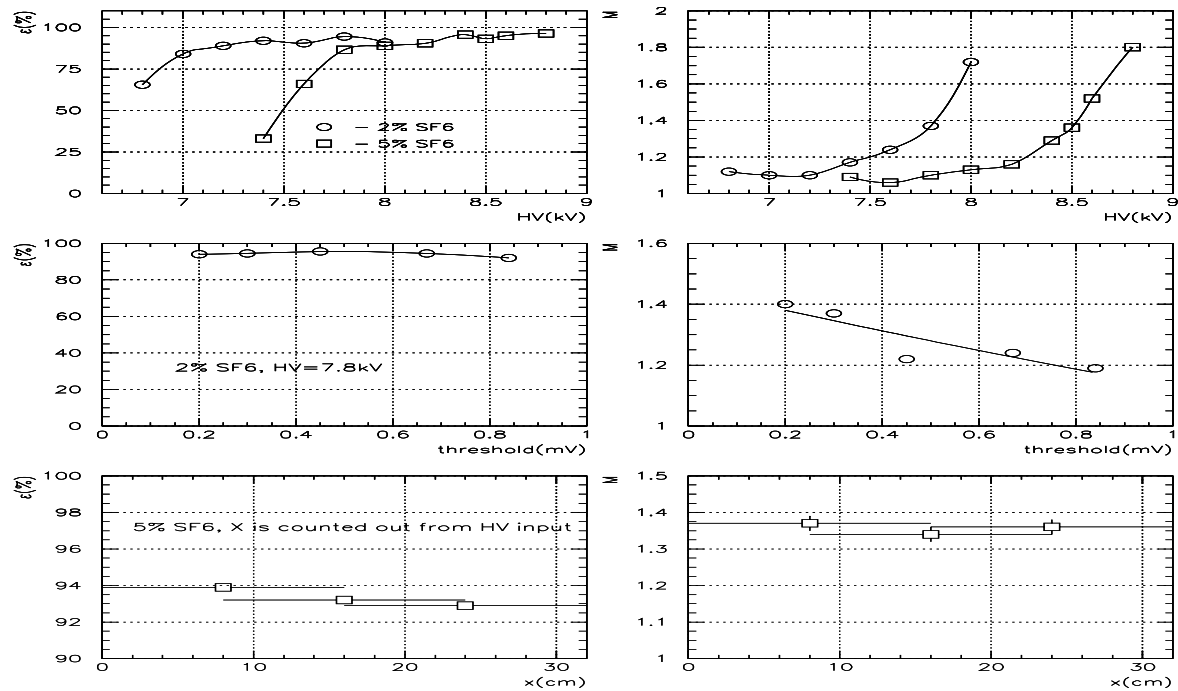
PCBs equipped with
4 hardroc1 + FPGA + USB
IPNL + LAL + LLR



Standard RPCs
(graphite + fishing lines)
IHEP



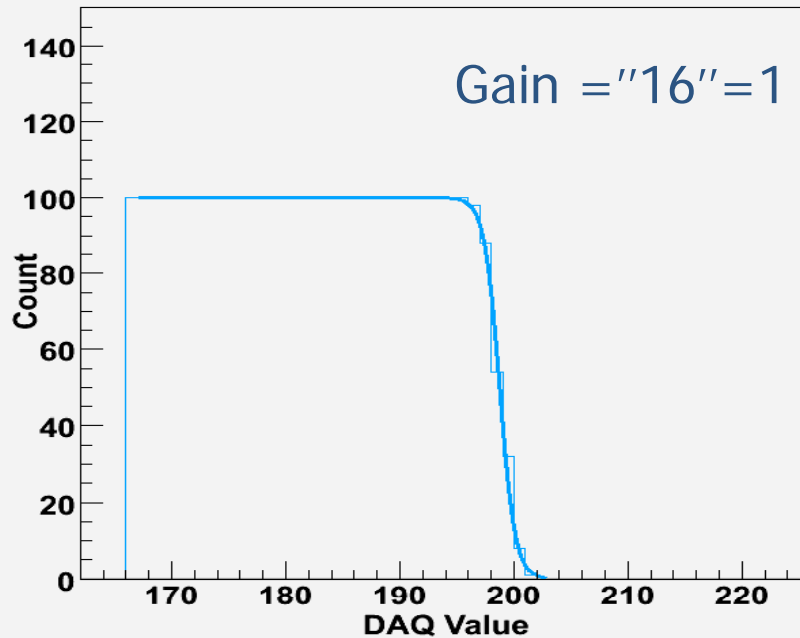
GRPC were tested at IHEP with standard electronics and then sent to IPNL



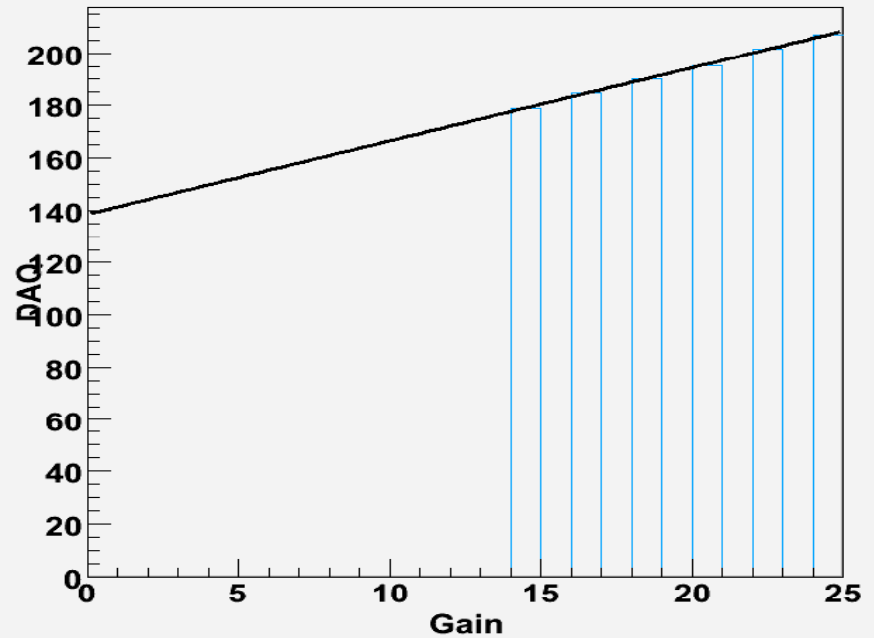
Read-Out calibration

The purpose of the calibration is to have a homogeneous response of the electronics.

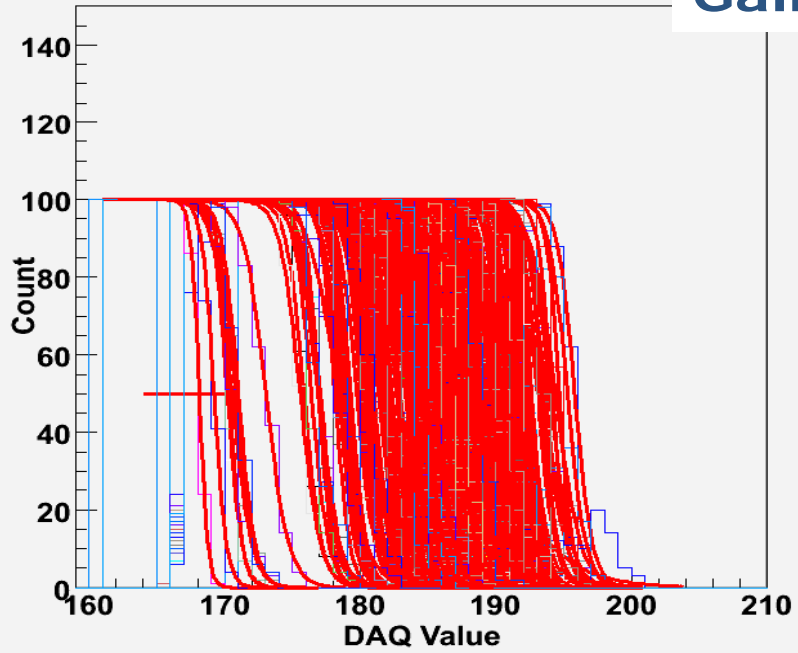
ASIC 4 Voie 63



ASIC 1 Pente de conversion.



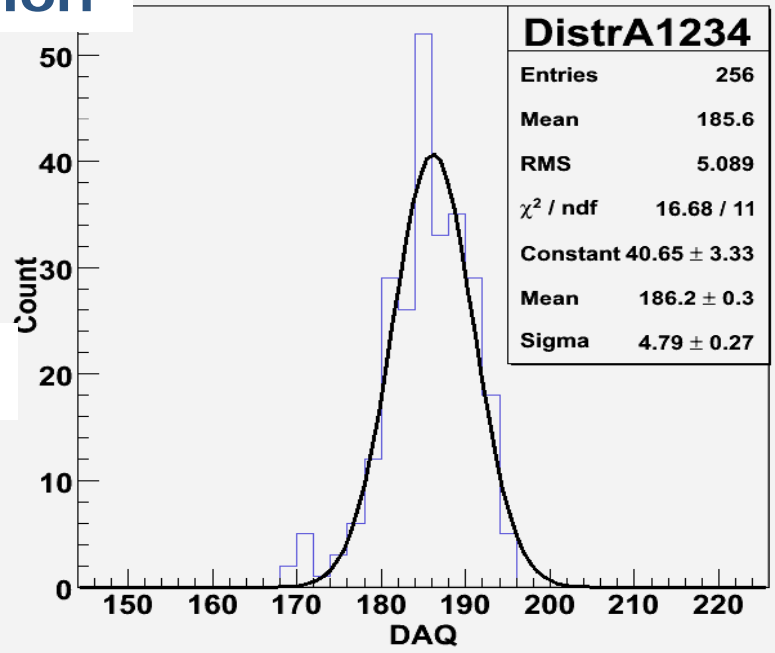
ASIC 1, 2, 3, et 4 Avant Corrections



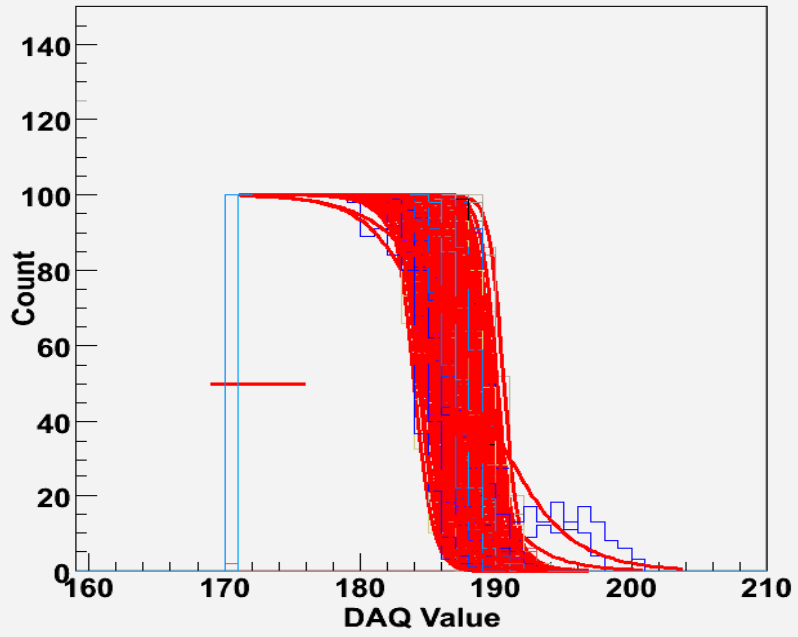
Gain correction

before

2, 3 et 4 Distribution des SCurves.

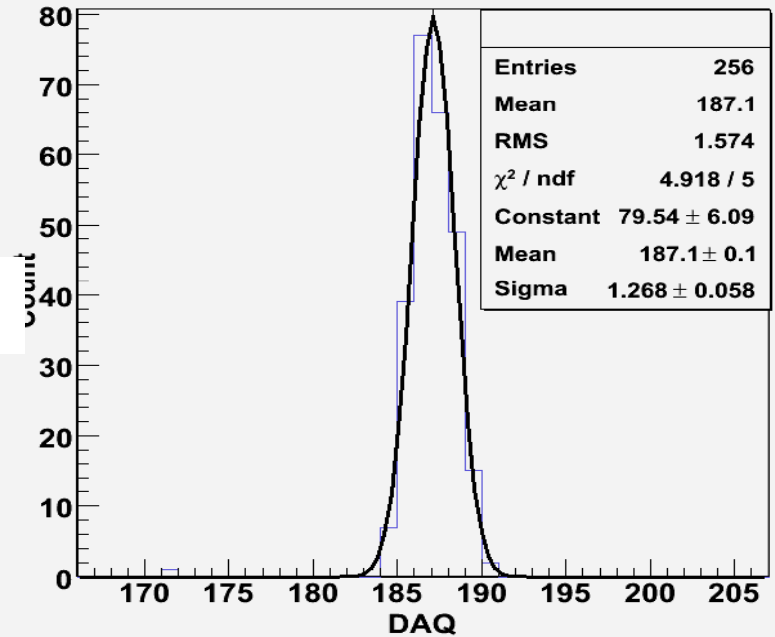


ASIC 1, 2, 3, et 4 Apres Corrections

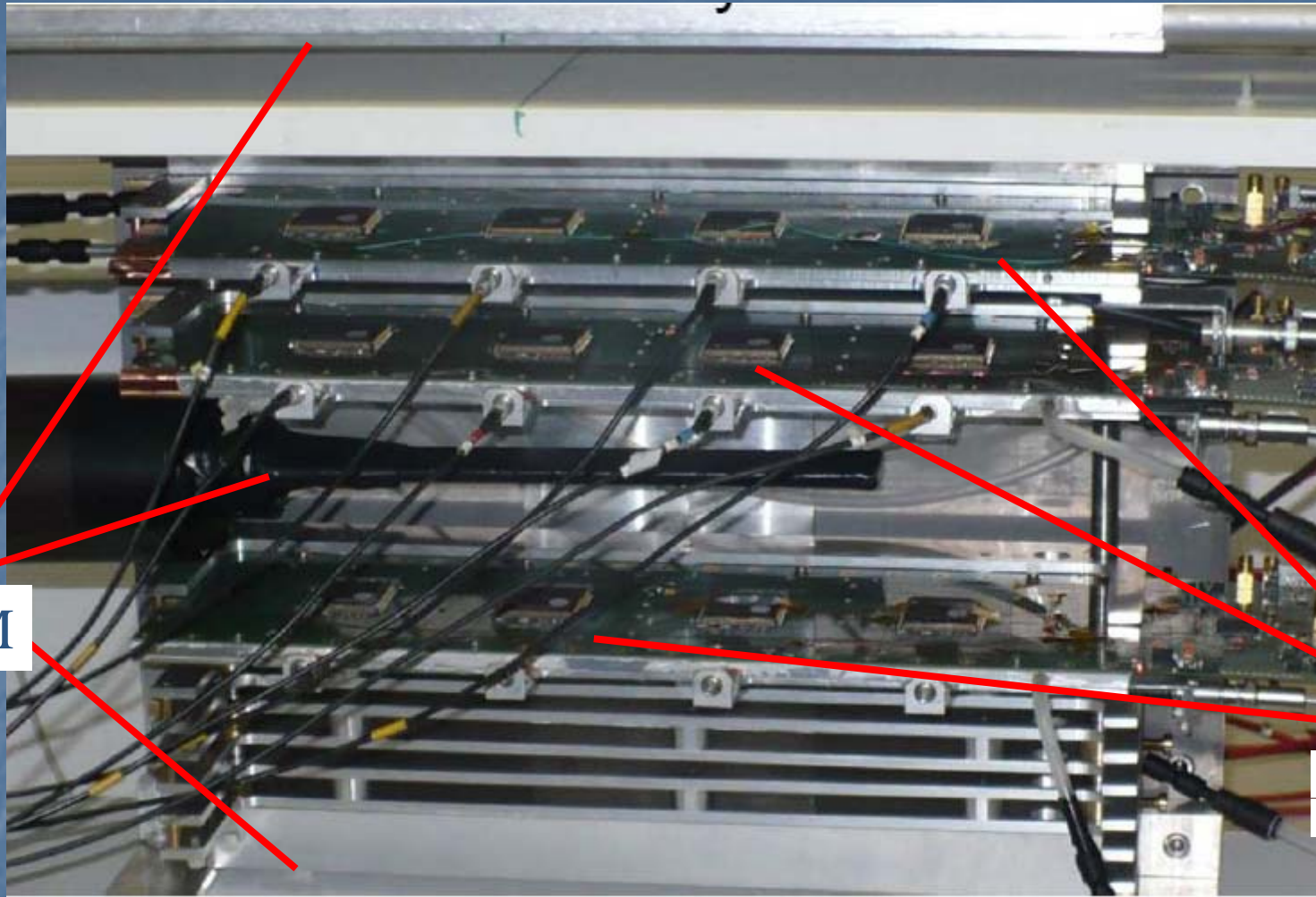


after

ASIC 1, 2, 3, et 4 Distribution des SCurves Corrigees.



Calice-Ma

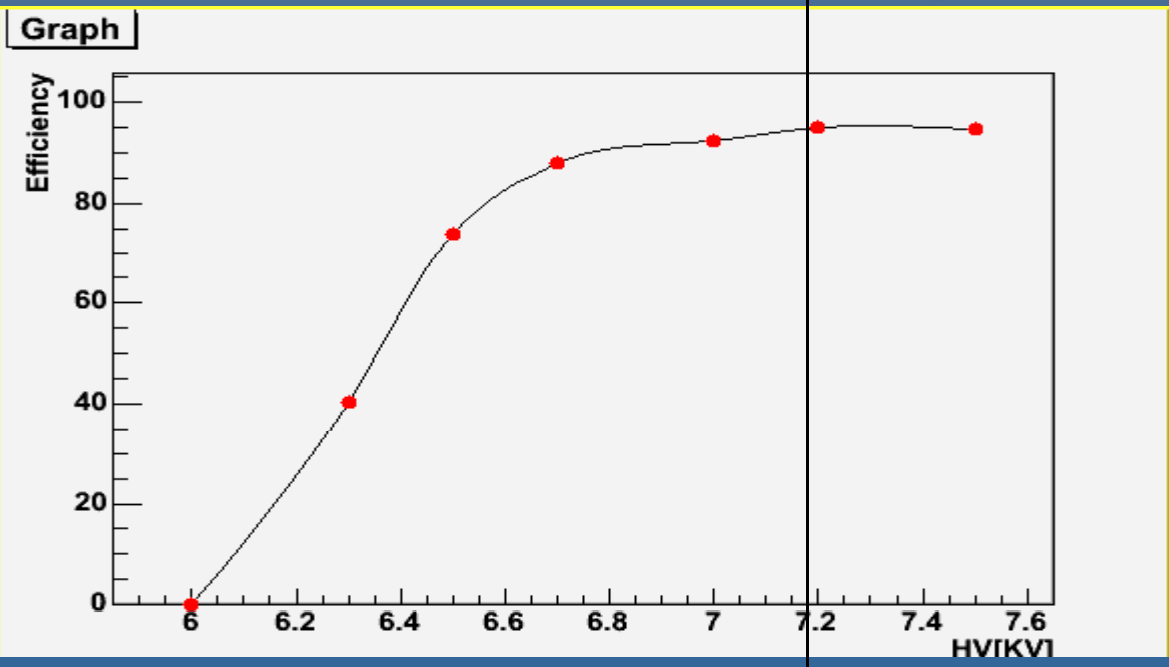


Sci+PM

GRPC

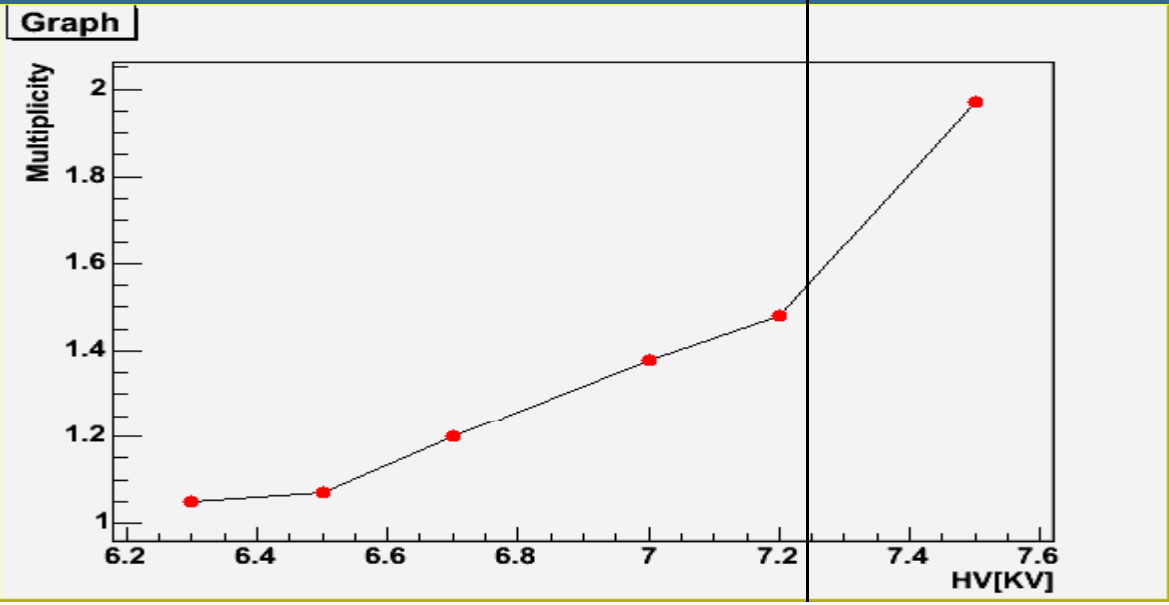
Cosmics bench

GRPC
32X8 pads
graphite



TFE 93%
Isobutene 5%
SF6 2%

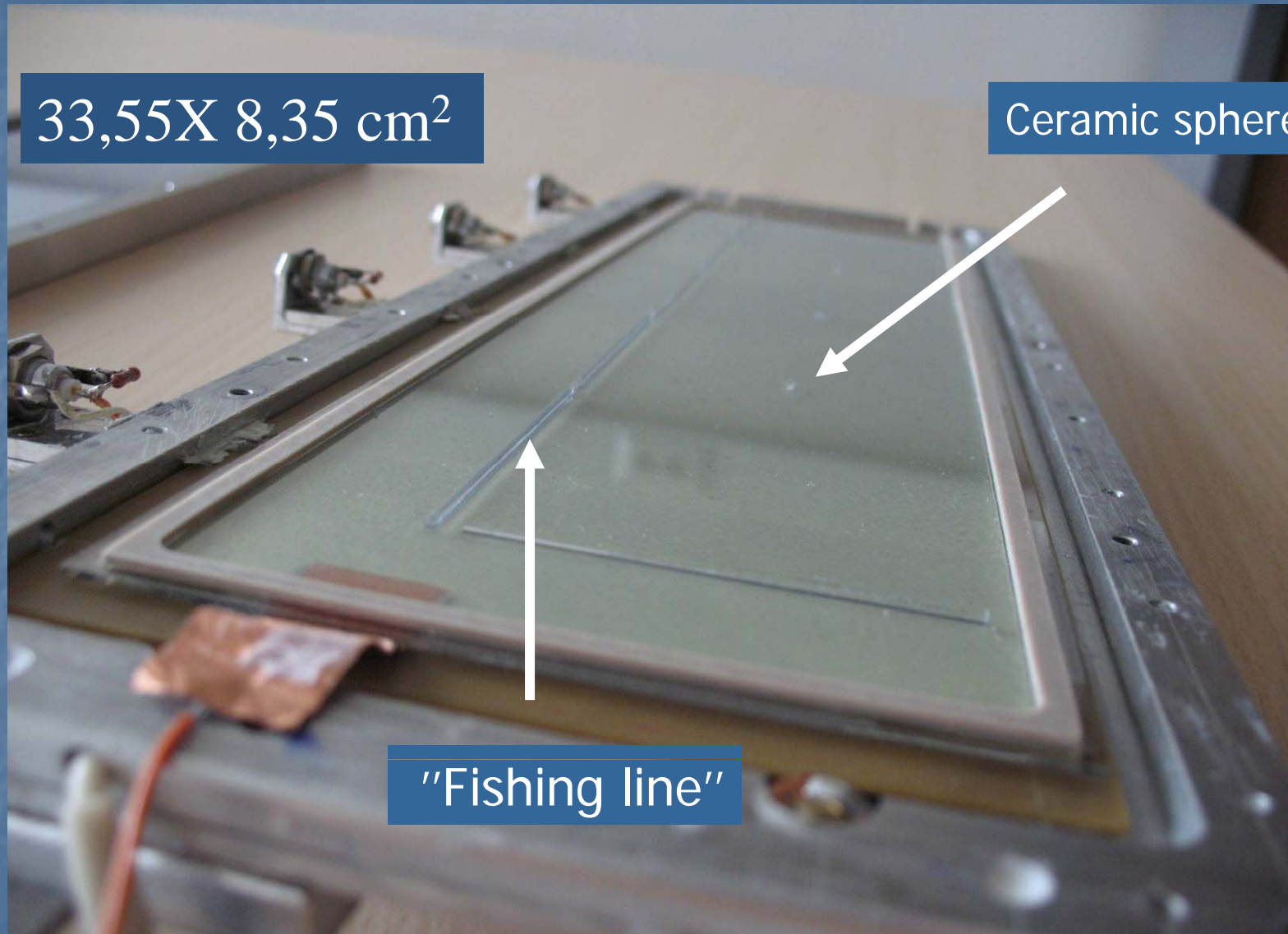
Threshold= 190 DAQ.U \approx 100 fc

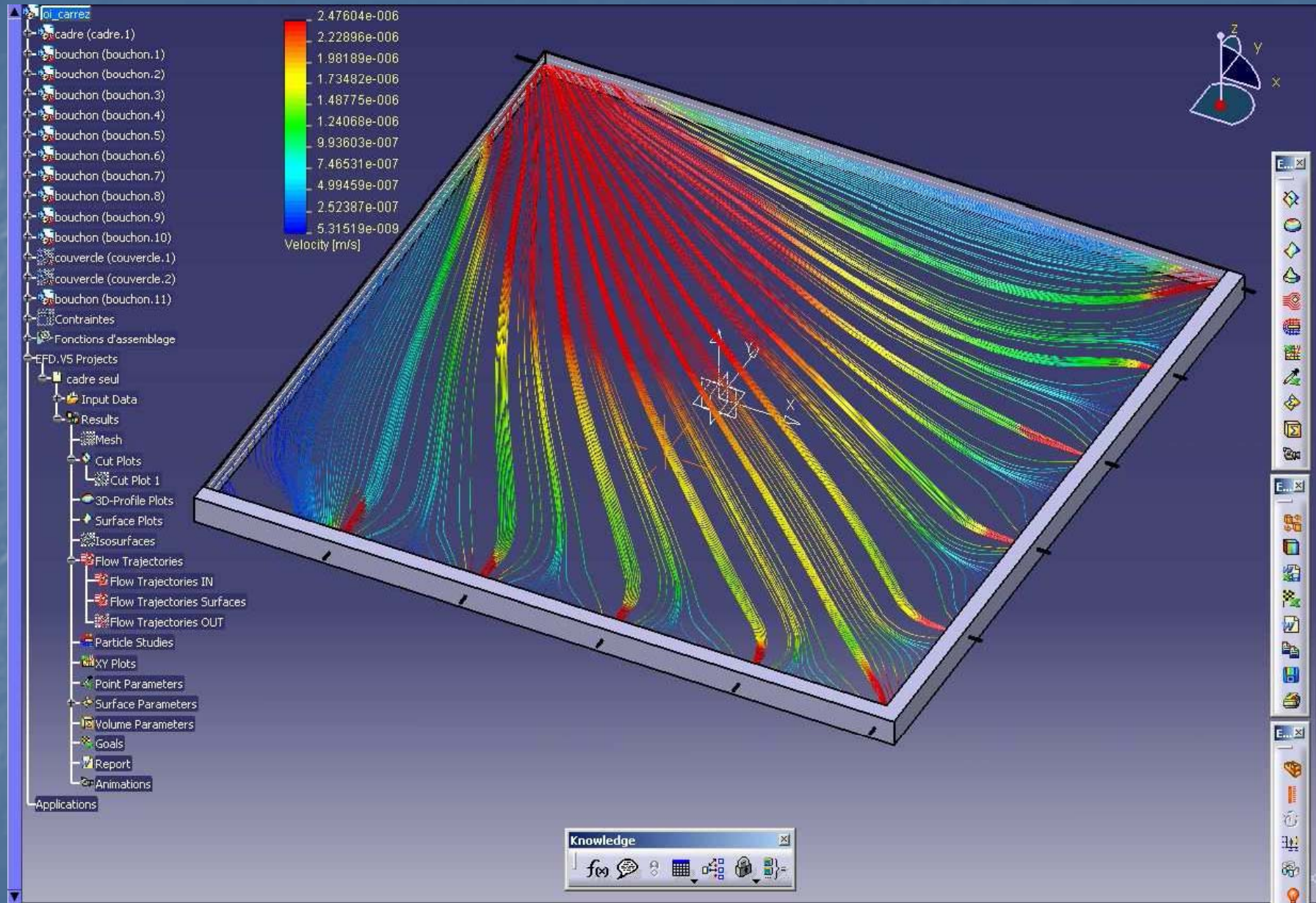


New GRPC developments

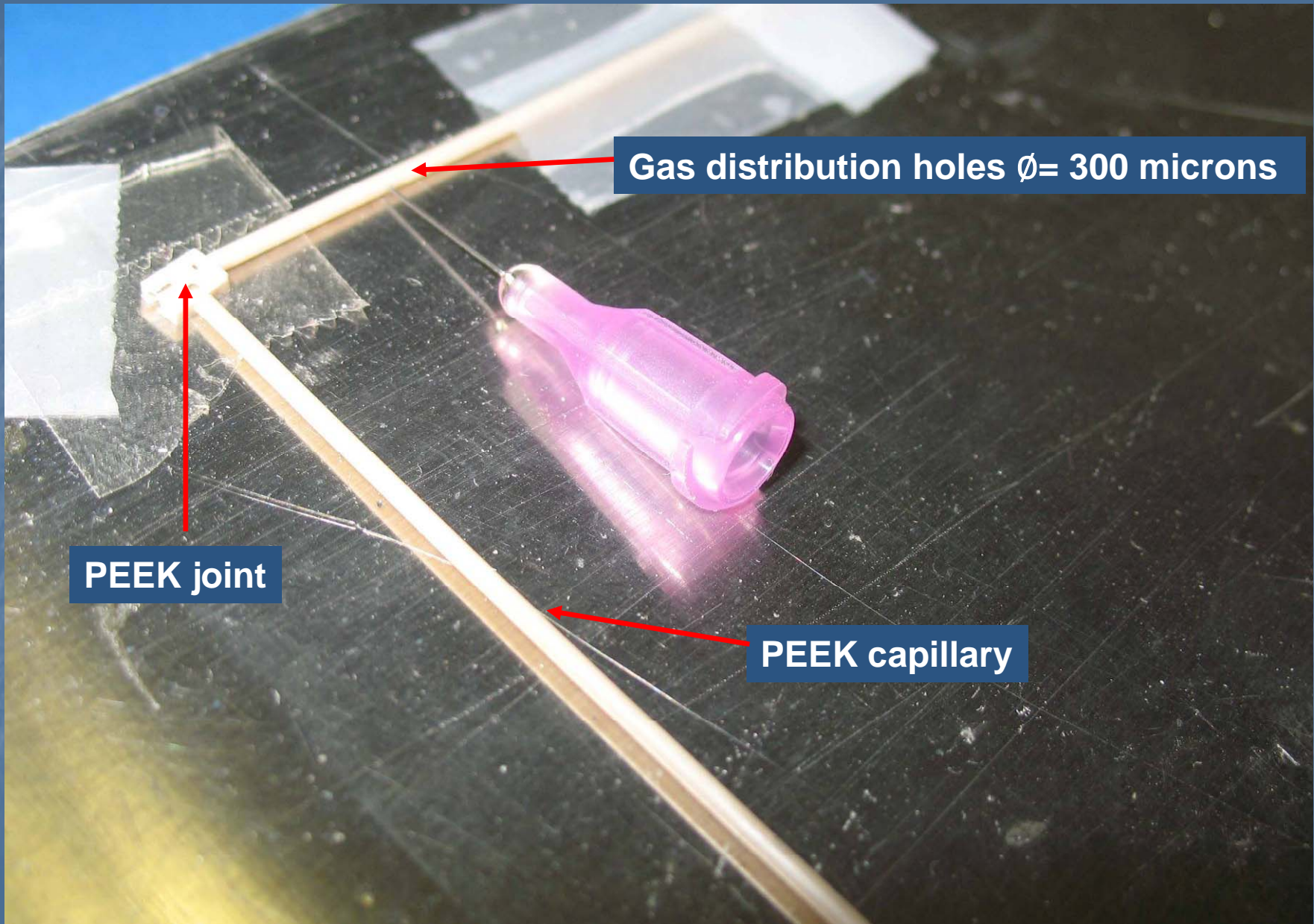
- Try new resistive paintings : Licron, statguard to reduce cross-talk
- Try new gas distribution systems : to improve gas distribution
- Try new spacers/frame to reduce dead zone
- Try new HV connection system to reduce related noise

solution1





Gas circulation simulation for solution1



PEEK joint

Gas distribution holes $\varnothing= 300$ microns

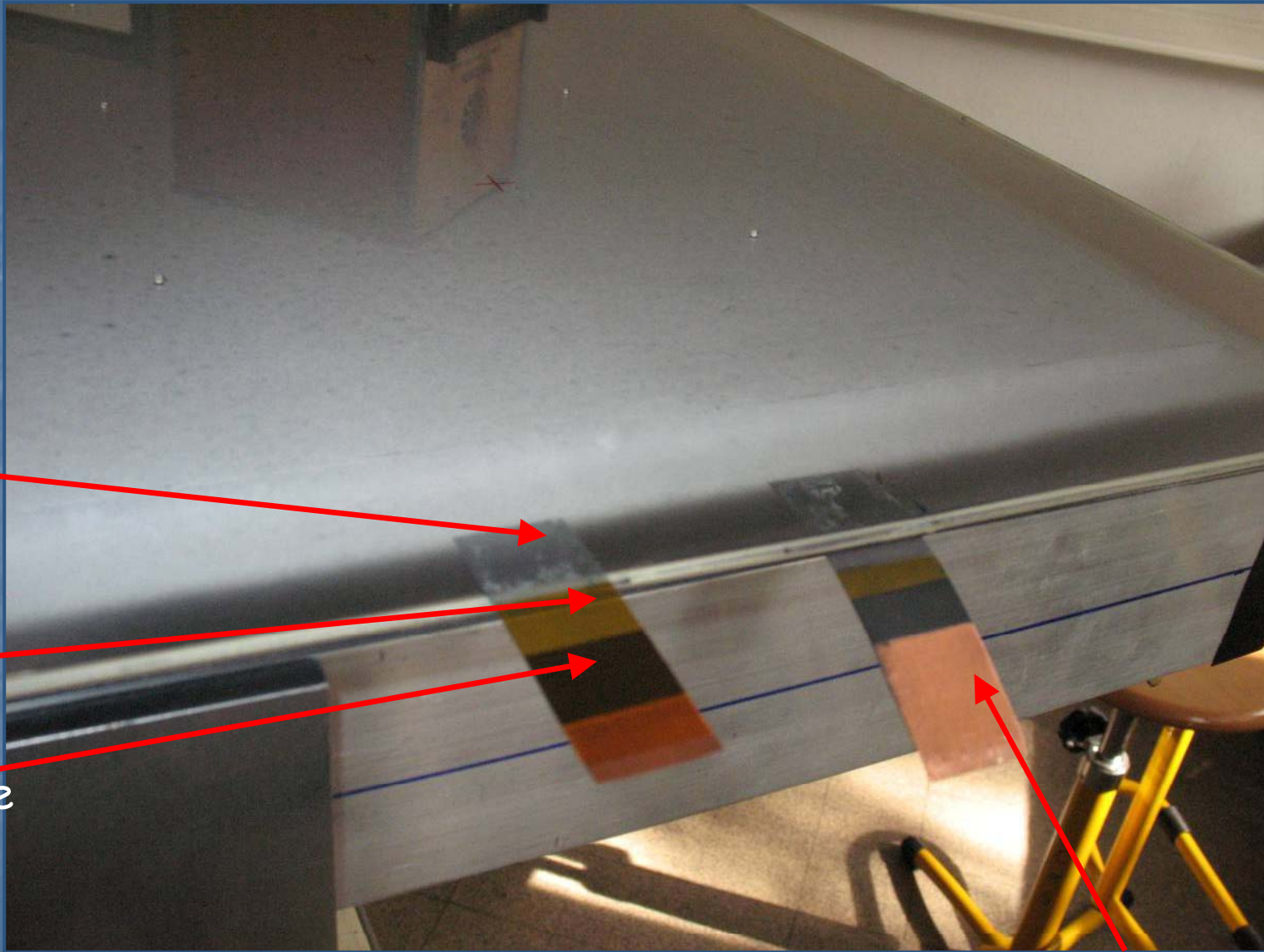
PEEK capillary

HV connection

Scotch
+
Licron

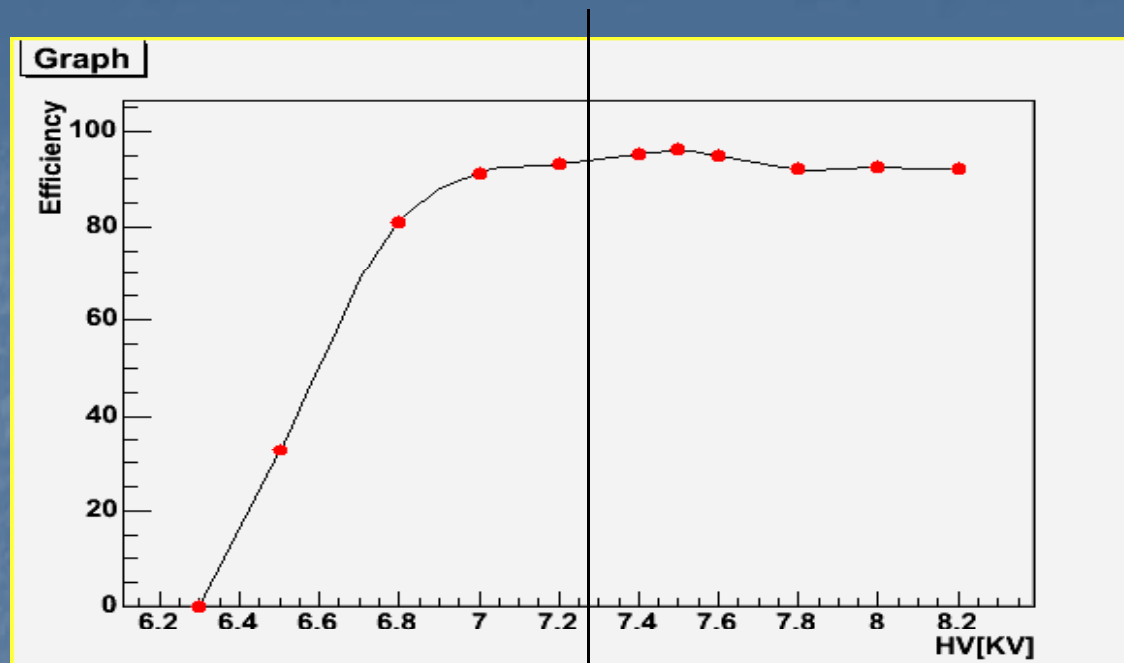
Kapton

Graphite



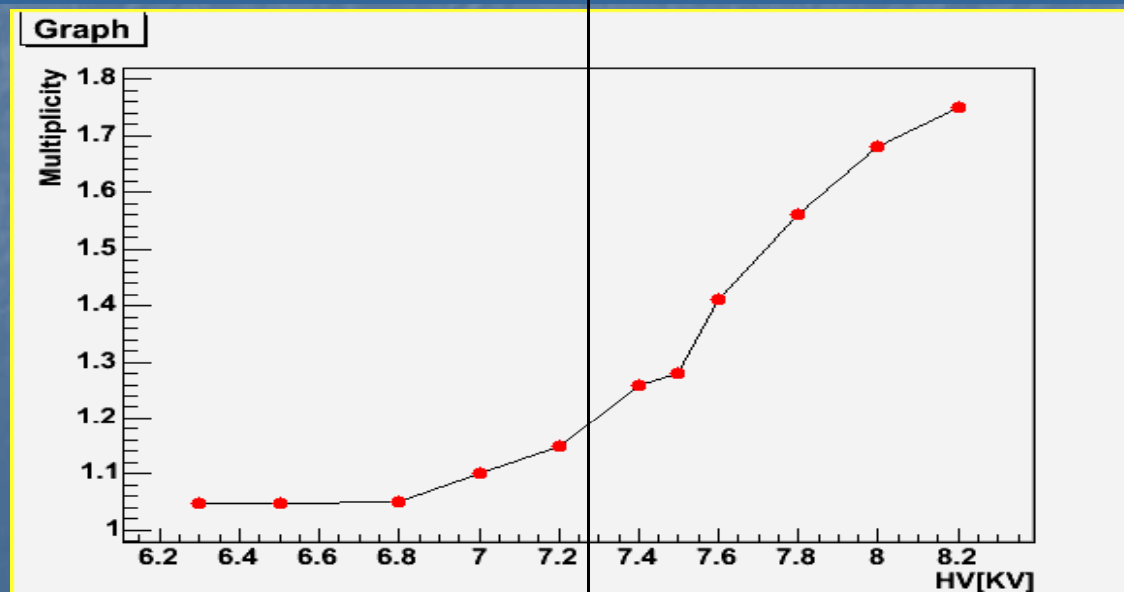
Cooper

GRPC
32X8 pads
licron



TFE 93%
Isobutene 5%
SF6 2%

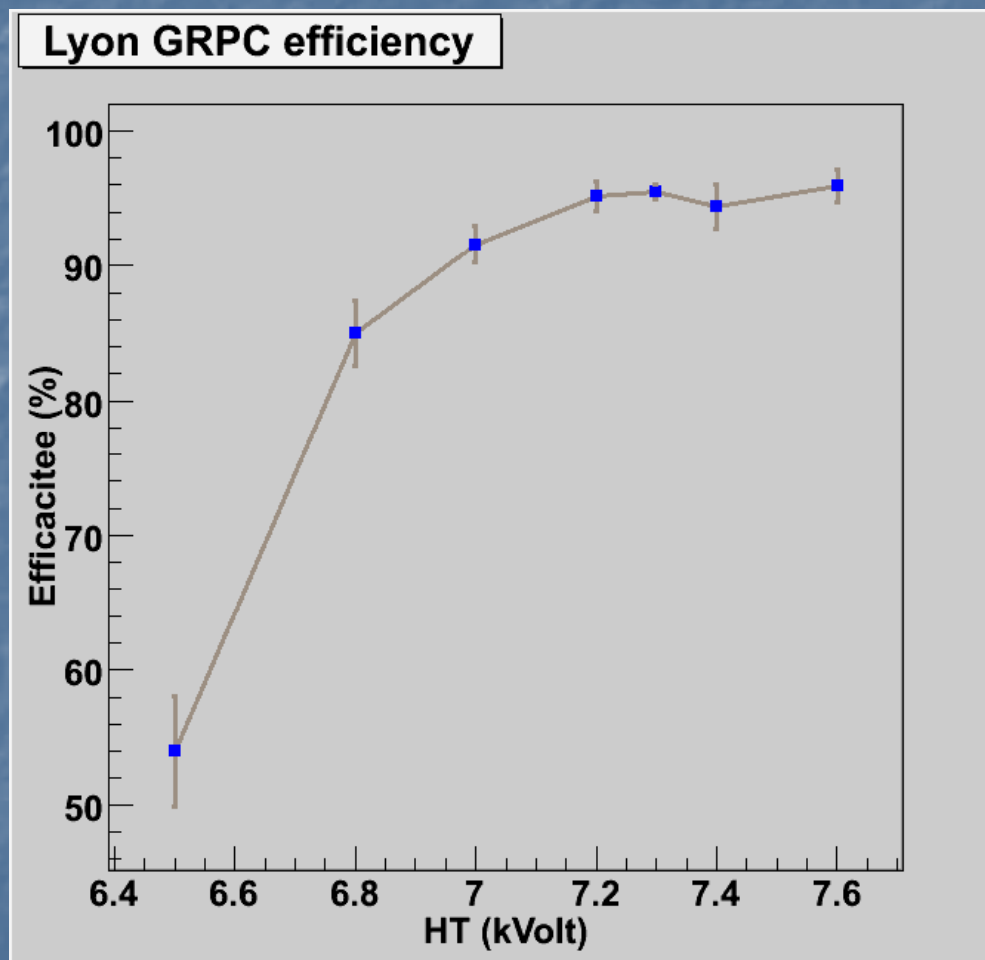
Threshold= 190 DAQ.U \approx 100 fc



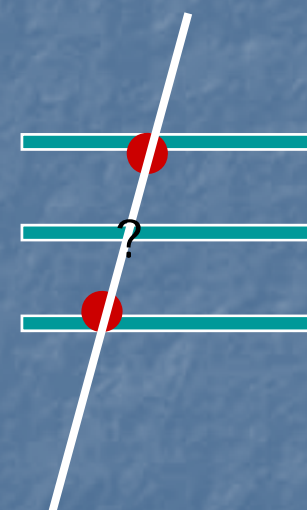
Noise 2-3 times
lower

Efficiency obtained using tracks built with the other GRPCs

GRPC
32X8 pads
licron



TFE	93%
Isobutene	5%
SF6	2%

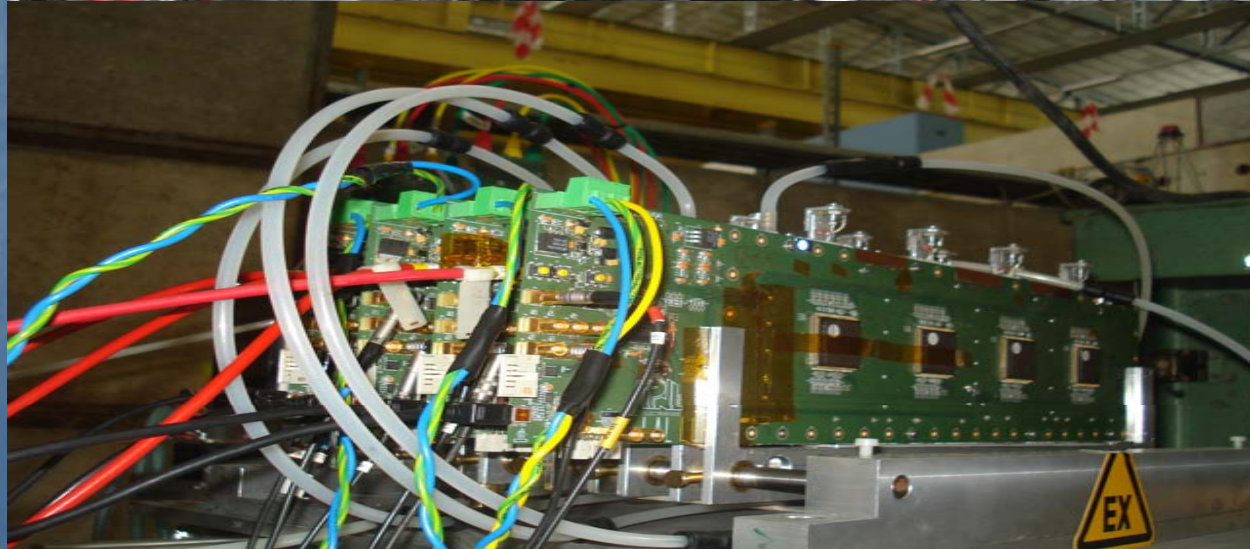
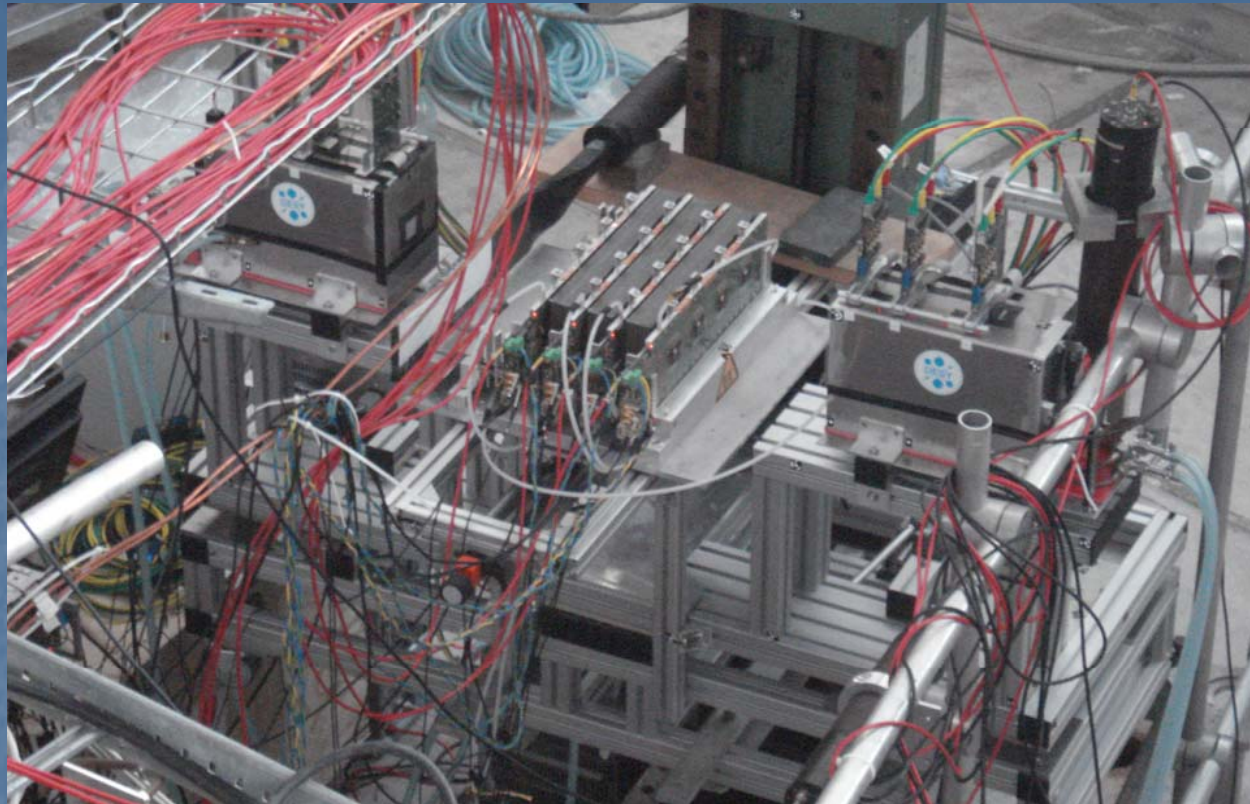


Threshold= 190 DAQ.U \approx 100 fc

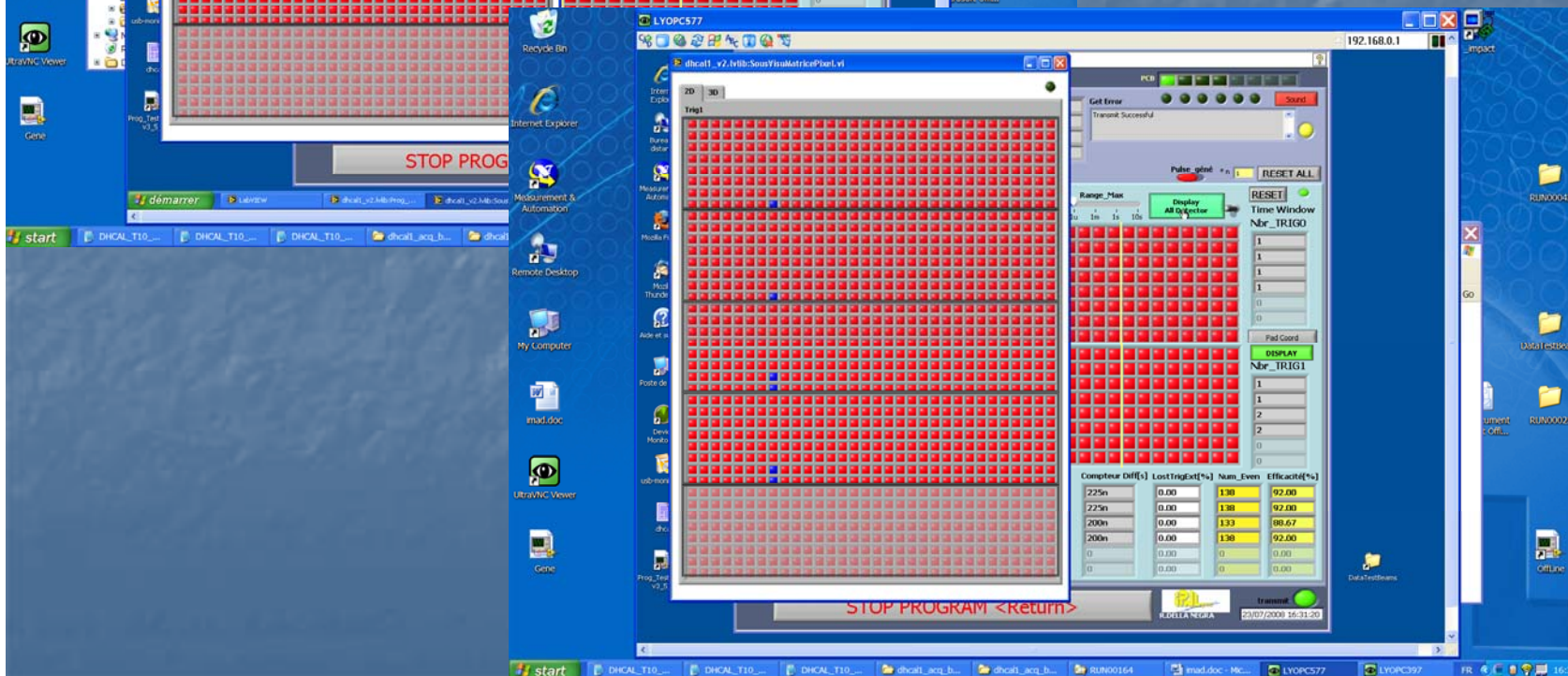
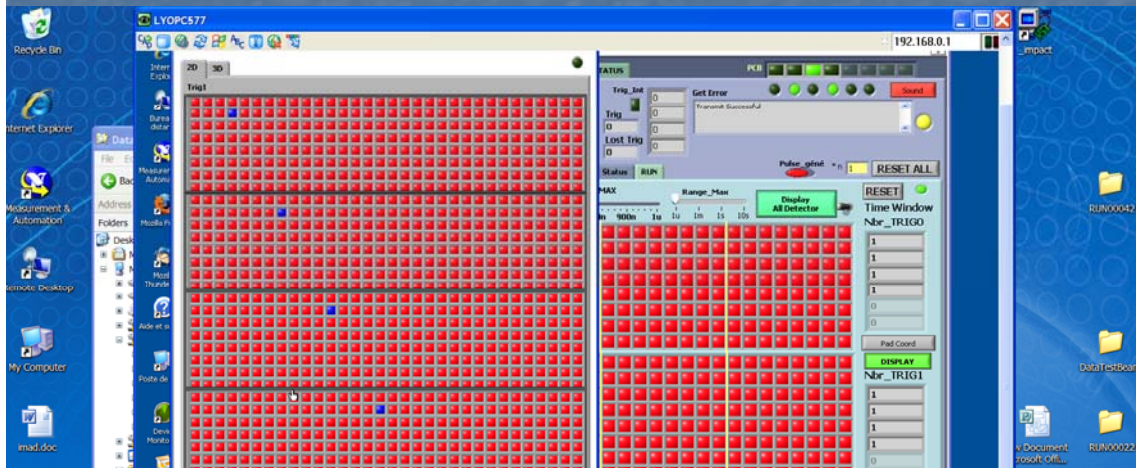
I.Laktineh Calice-Manchester

Mini DHCAL

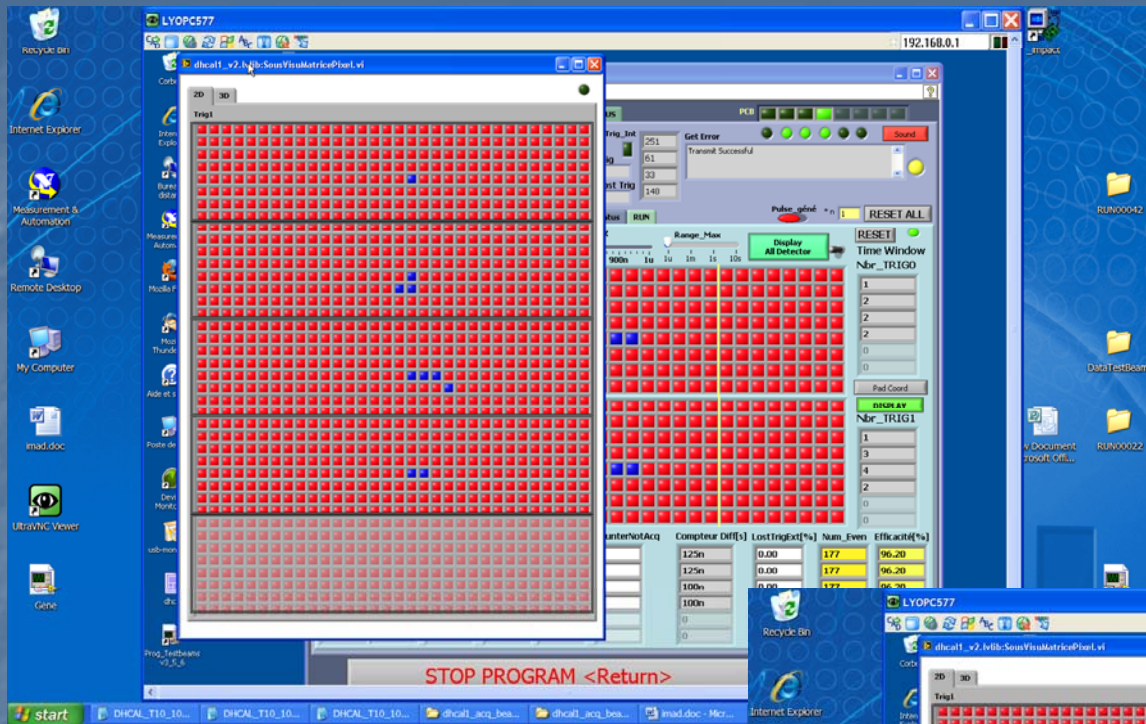
- 4/5 GRPCs with/without steel slabs
- Common readout through a USB-hub
- Muons, pions, different energies, different angles
- Triggers: Eudet telescope setup/Scintillator-PM



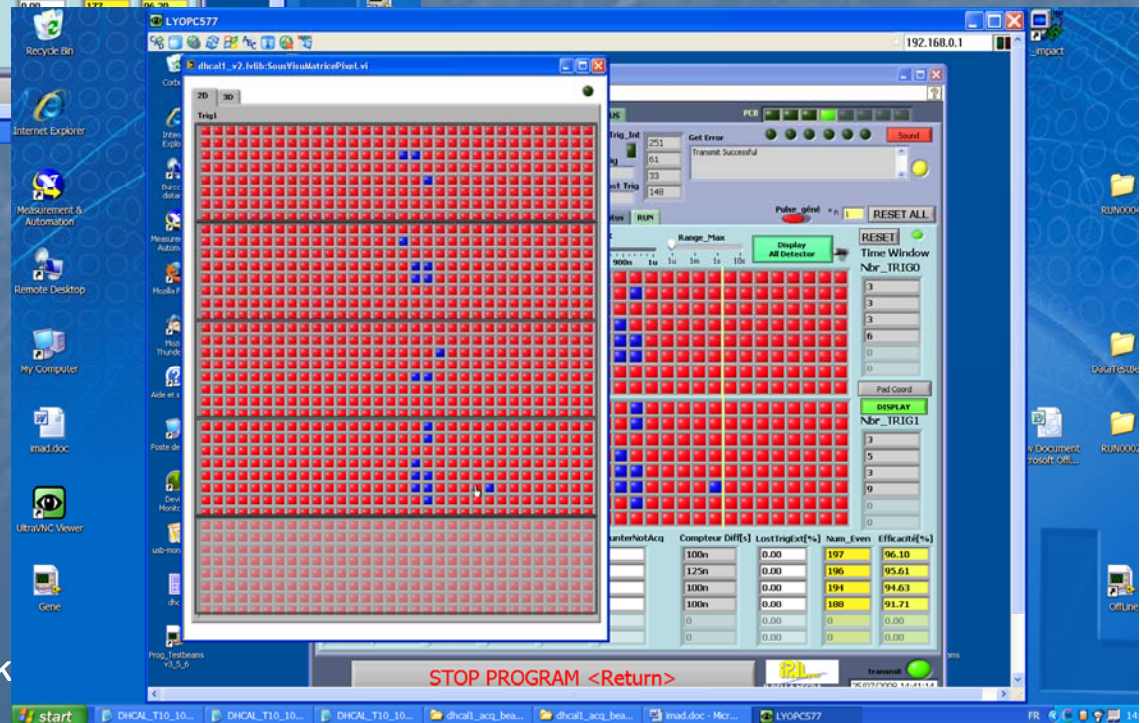
Muons : Different angle exposure



Pion: no absorber in front of the first GRPC



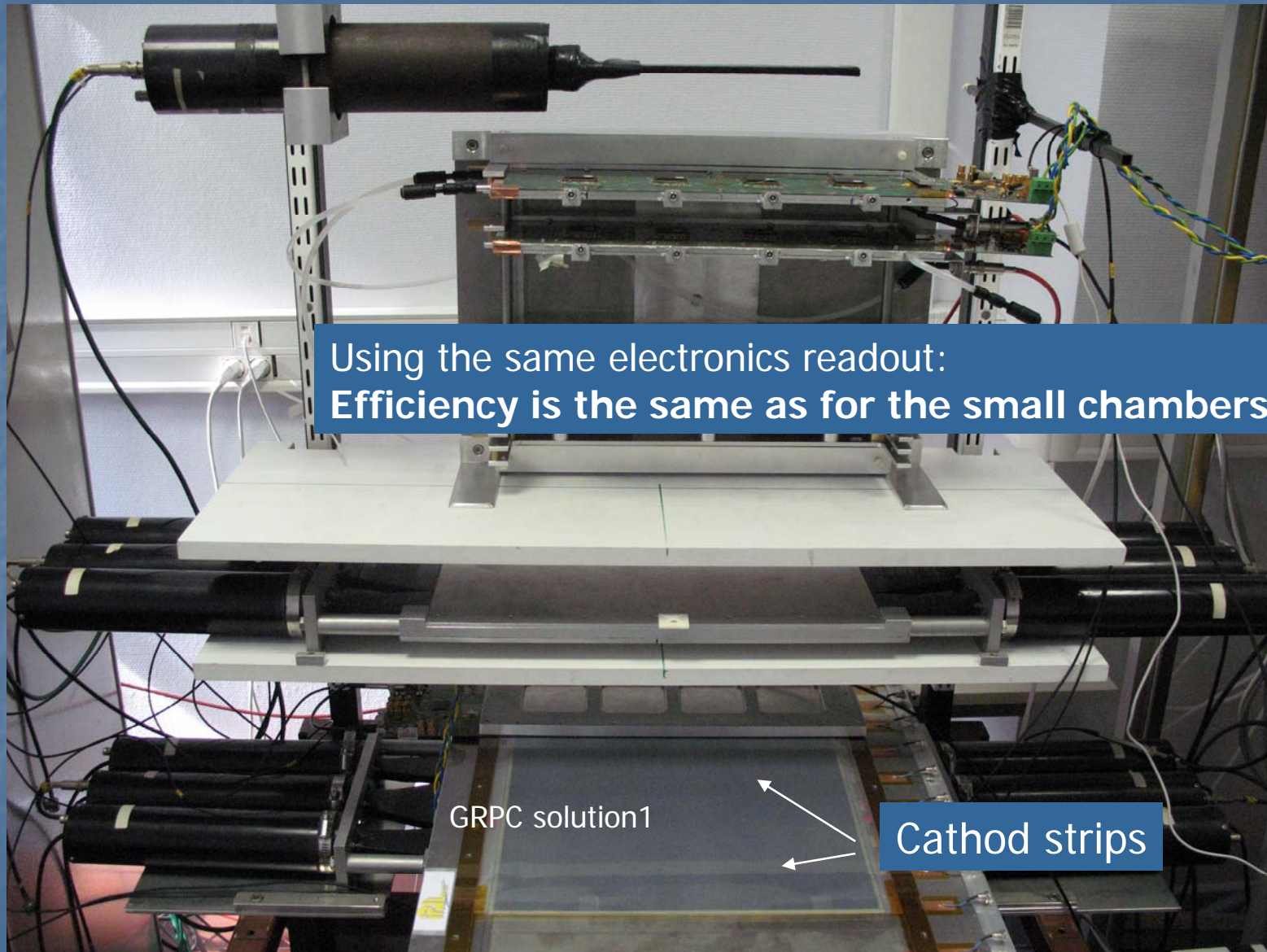
Pion: absorber in front of the first GRPC



I.Lak

Toward the 1M² prototype

50 X 32-pad prototype



Using the same electronics readout:
Efficiency is the same as for the small chambers

GRPC solution1

Cathod strips

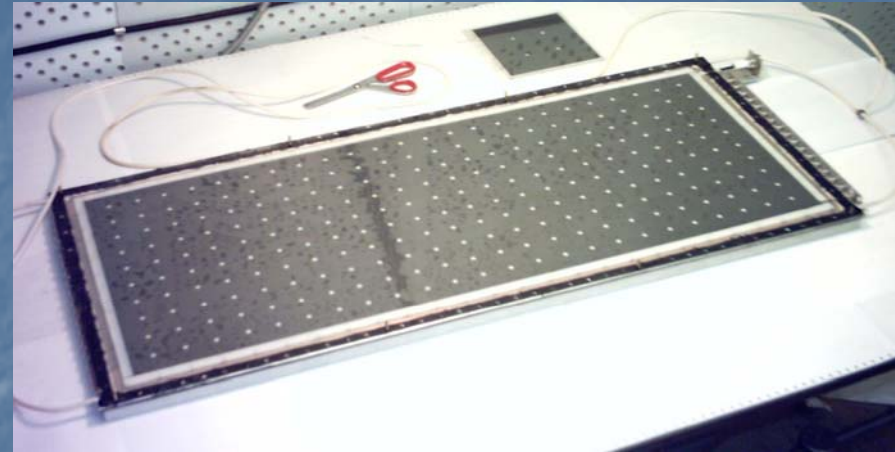
40x100-pad prototype

RPC with sensitive area of 36x96 cm² was produced to incorporate 32x32 =1024 pads of 1 cm² area.

For read-out the 2 anode PBs with 16x32=512 pads were used.

Connections between pads and the 64 ch. FEE are made by microcoax 50 ohm cables.

It was found that tightness between anode PB and RPC gas volume is needed.



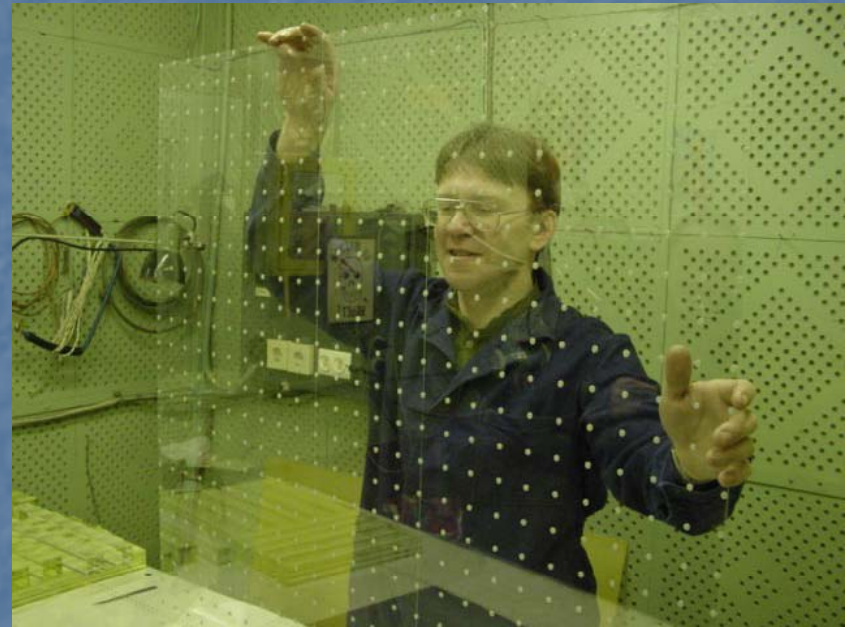
1 m² prototype with strips

16x and 16 y strips of 6 cm width

Detailed study of the plane was performed in cosmic rays.

In general :

- the plane is robust and hermetic;
- inefficiency of about 6% is compatible with the geometrical one due to spacers;
- uniformity of efficiency on the large scale is (94+/-2)%;
- current in HV circuit is 1 μ A;
- noise at the plateau knee of about 0.45 Hz/cm² is acceptable.



How to readout large surface GRPC?

- Building a large size GRPC: ok
- New generation electronics readout : ok
- **Associated readout electronics to large size GRPC should be demonstrated.**

How to read out large surface GRPC?

Solution:

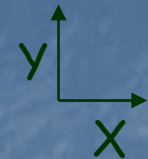
- Conceive and realize large PCB
- Connect PCBs together to build large size anode
- Rigidify the anode using a part of the absorber
- Fix the detector on the anode
- Connect anode to DIF → Signal

Conception of Large PCB :

- An important point to determine the PCB size was the industry capacity to produce high class PCBs (buried vias...)
- The PCB design was based on
 - 1- using the same layer structure as the one of the previous 4-chip board
 - 2- optimizing the signal transmission between the different asics on the same PCB
 - 3- taking into account the connection between two adjacent PCB and connection between the PCB and the DIF

PCB DESIGN

50 cm



GND Connector ASU to ASU on Y axis

ASU to ASU connector

ASU to ASU connector

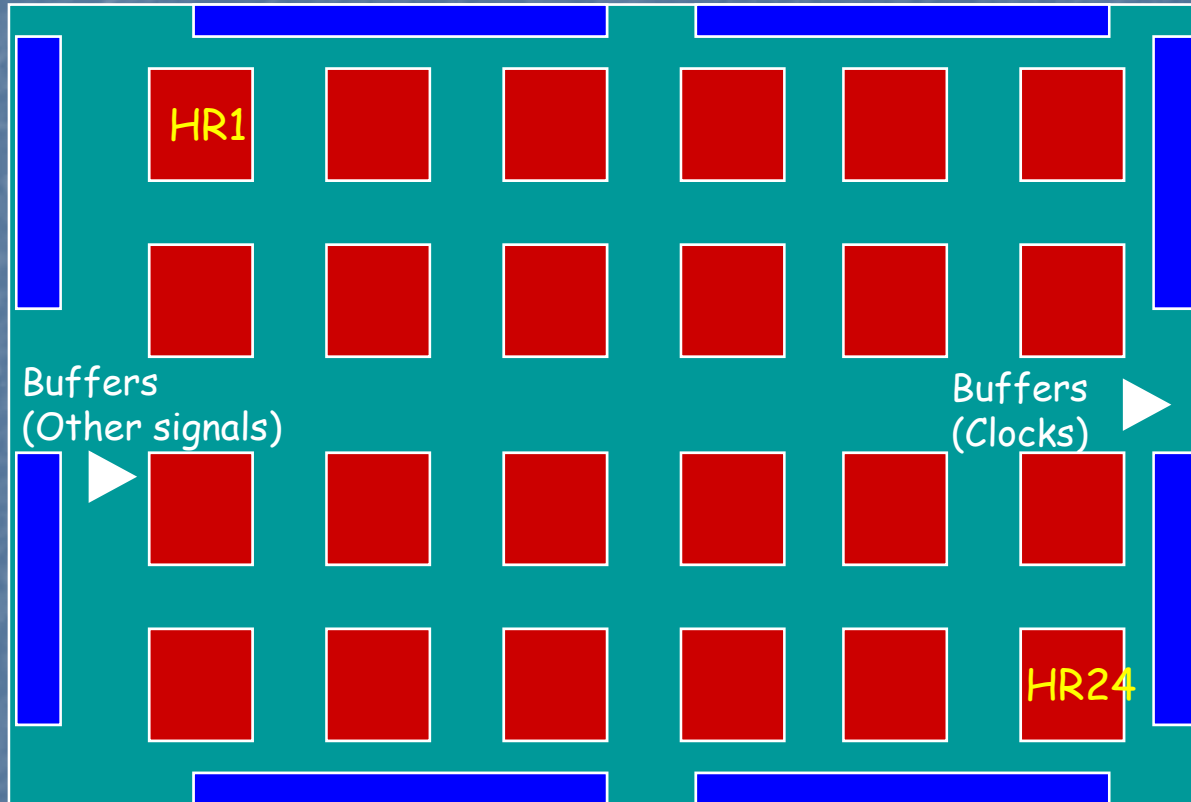
33.3 cm

Buffers (Other signals)

Buffers (Clocks)

Power and Gnd Connector ASU to ASU on X axis

DIF connector

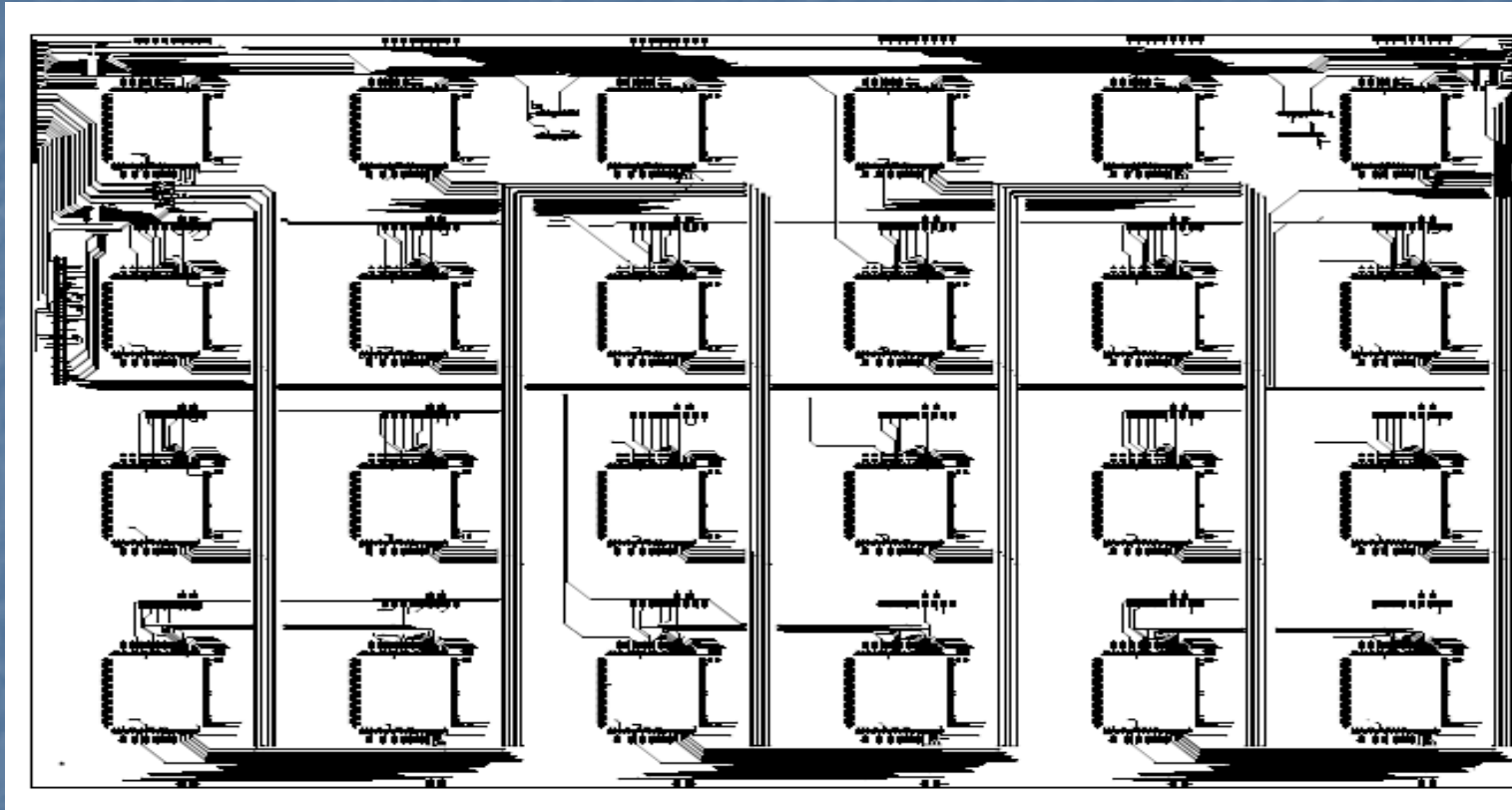


GND Connector ASU to ASU on Y axis

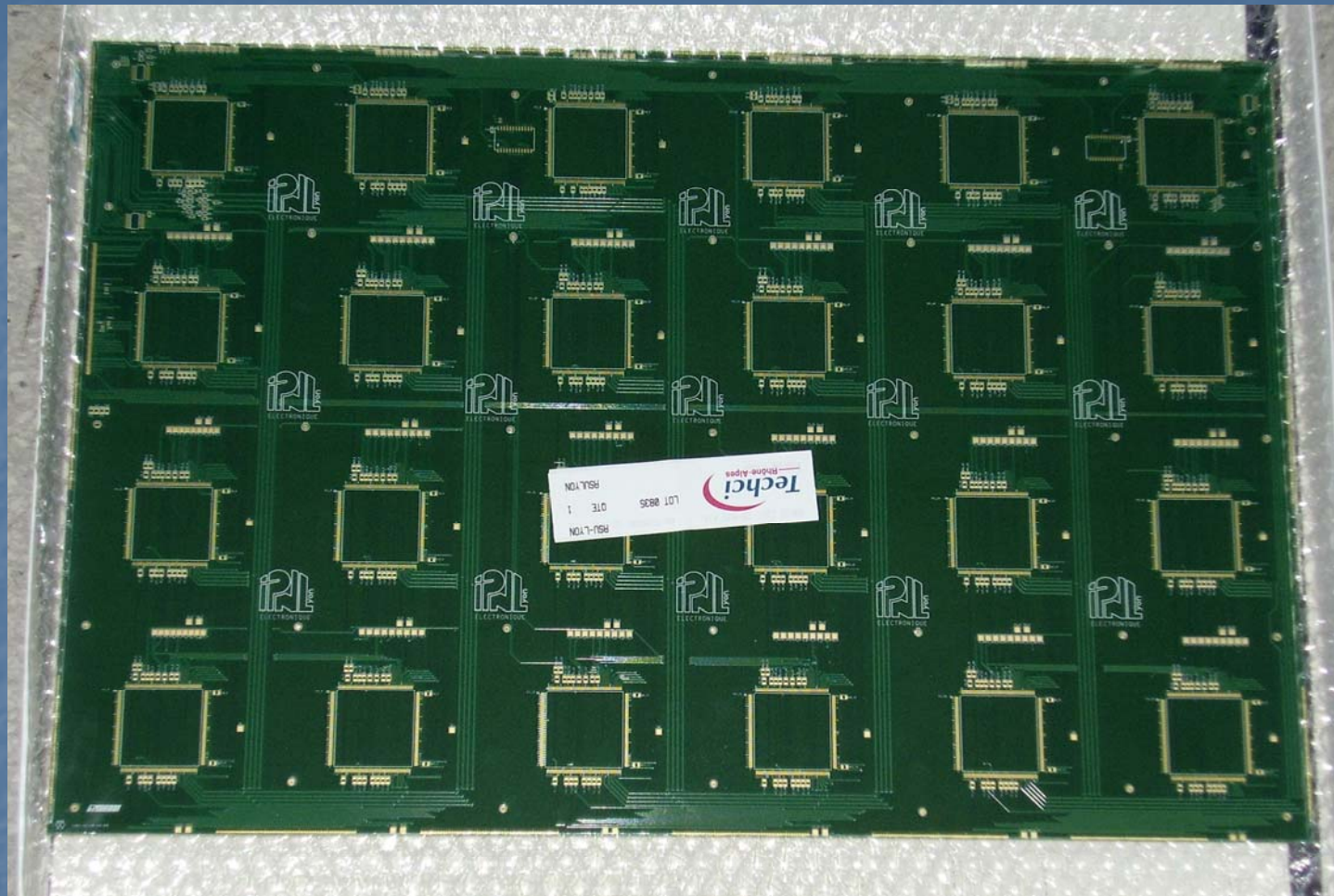
1536 pads on Bottom Layer

Buried and Blind Vias (Same as the last PCB with 4 HR)

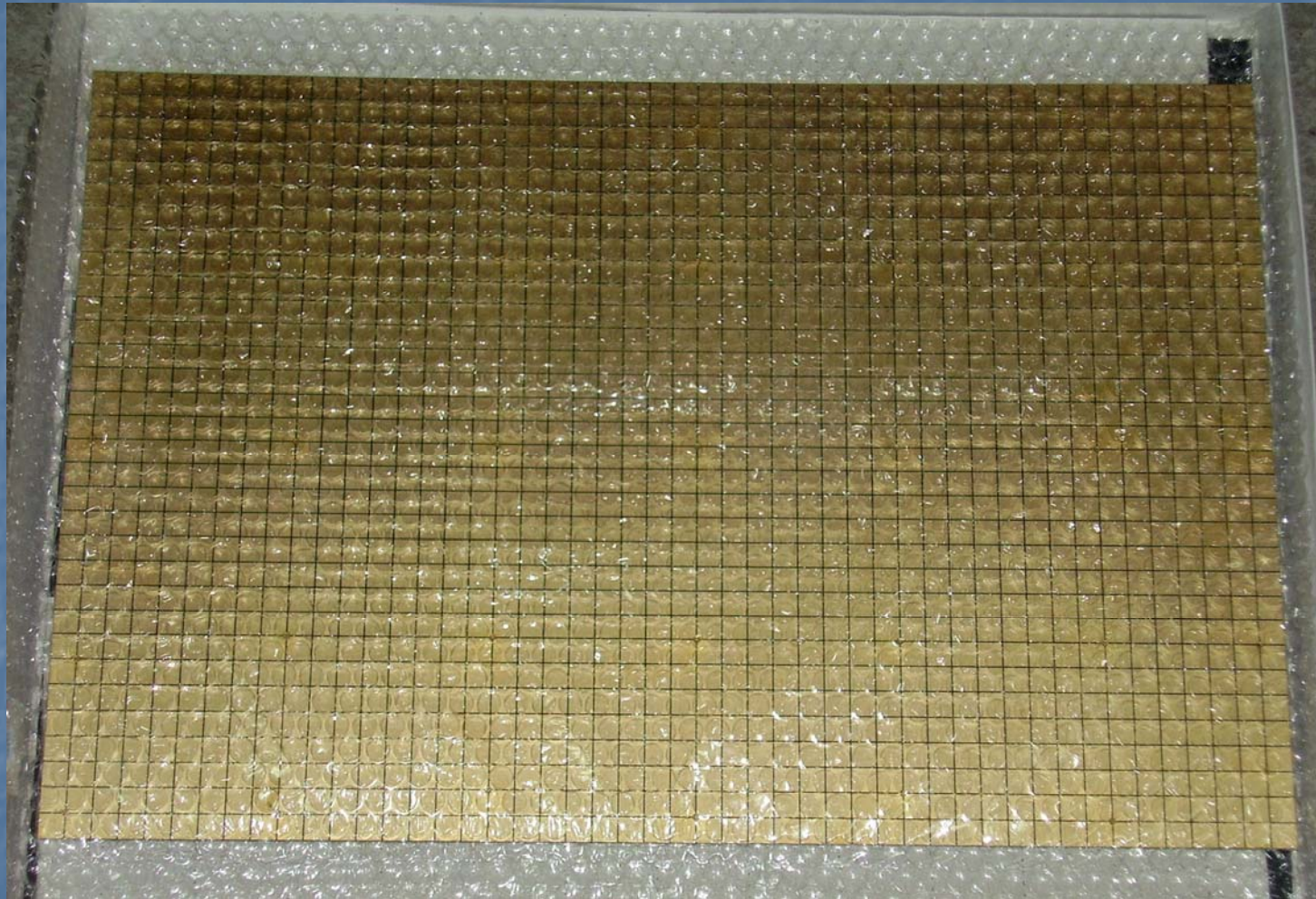
24-asic PCB design



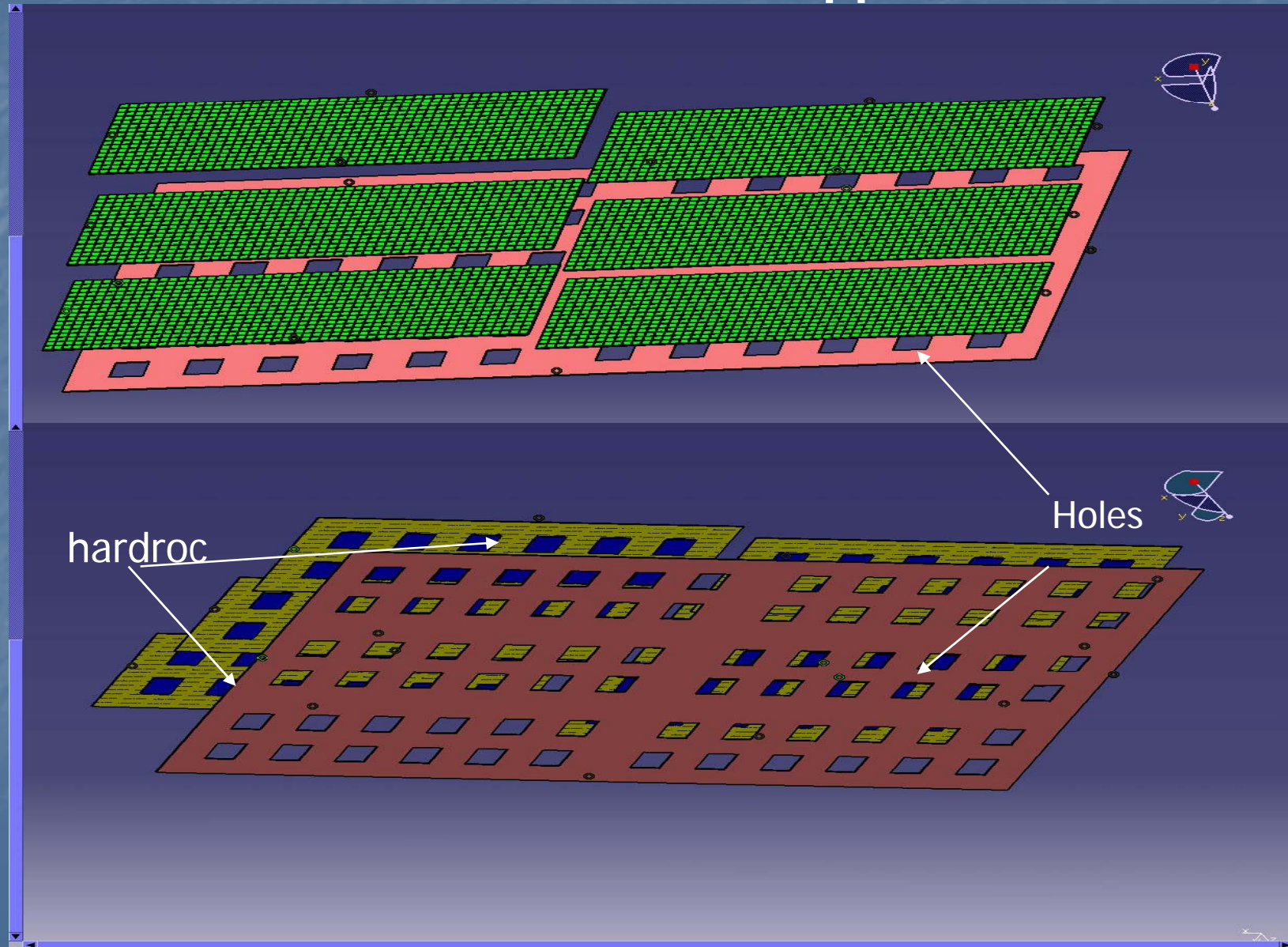
30 holes for M1 screws were distributed on the PCB for fixation on the absorber

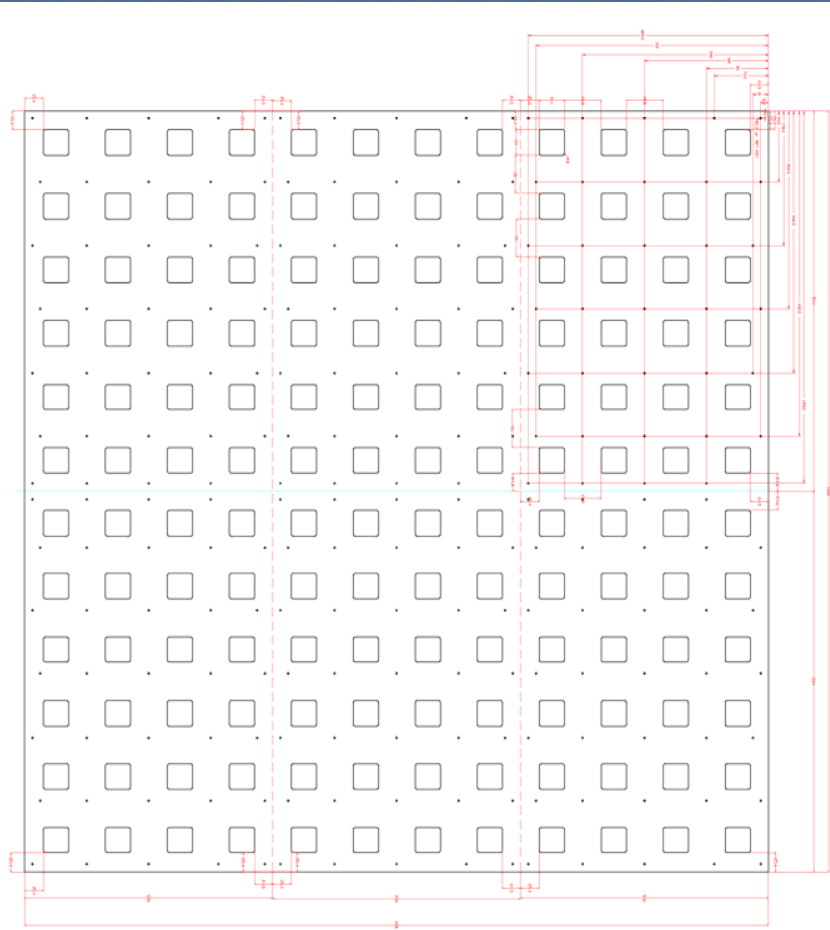


6+2 PCBs were recently produced (end of August)

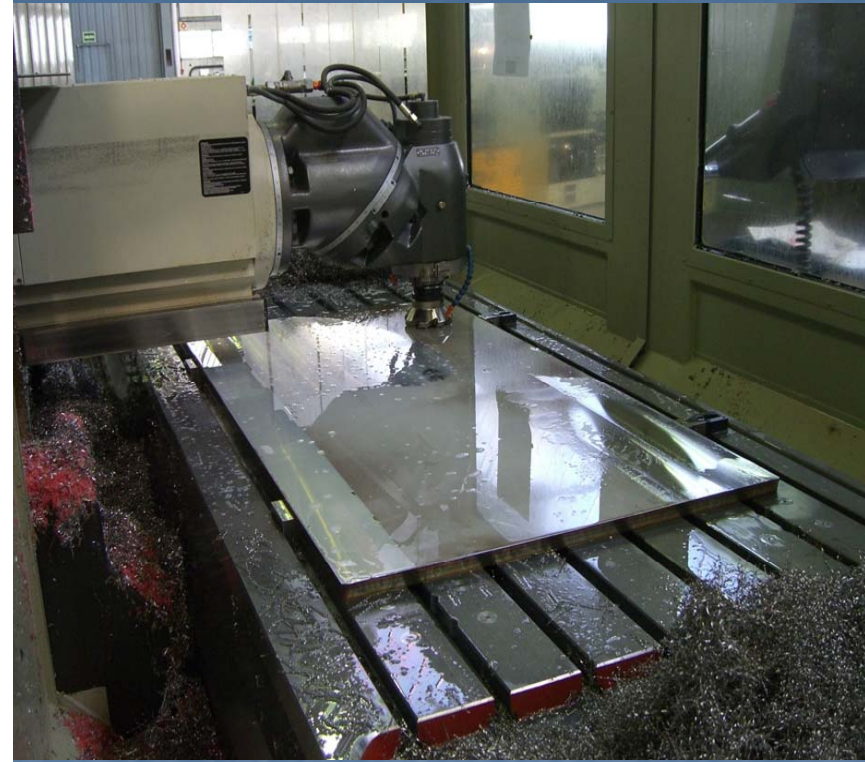


PCB connection : Assemble 2 X 3 PCBs on 1M² Support





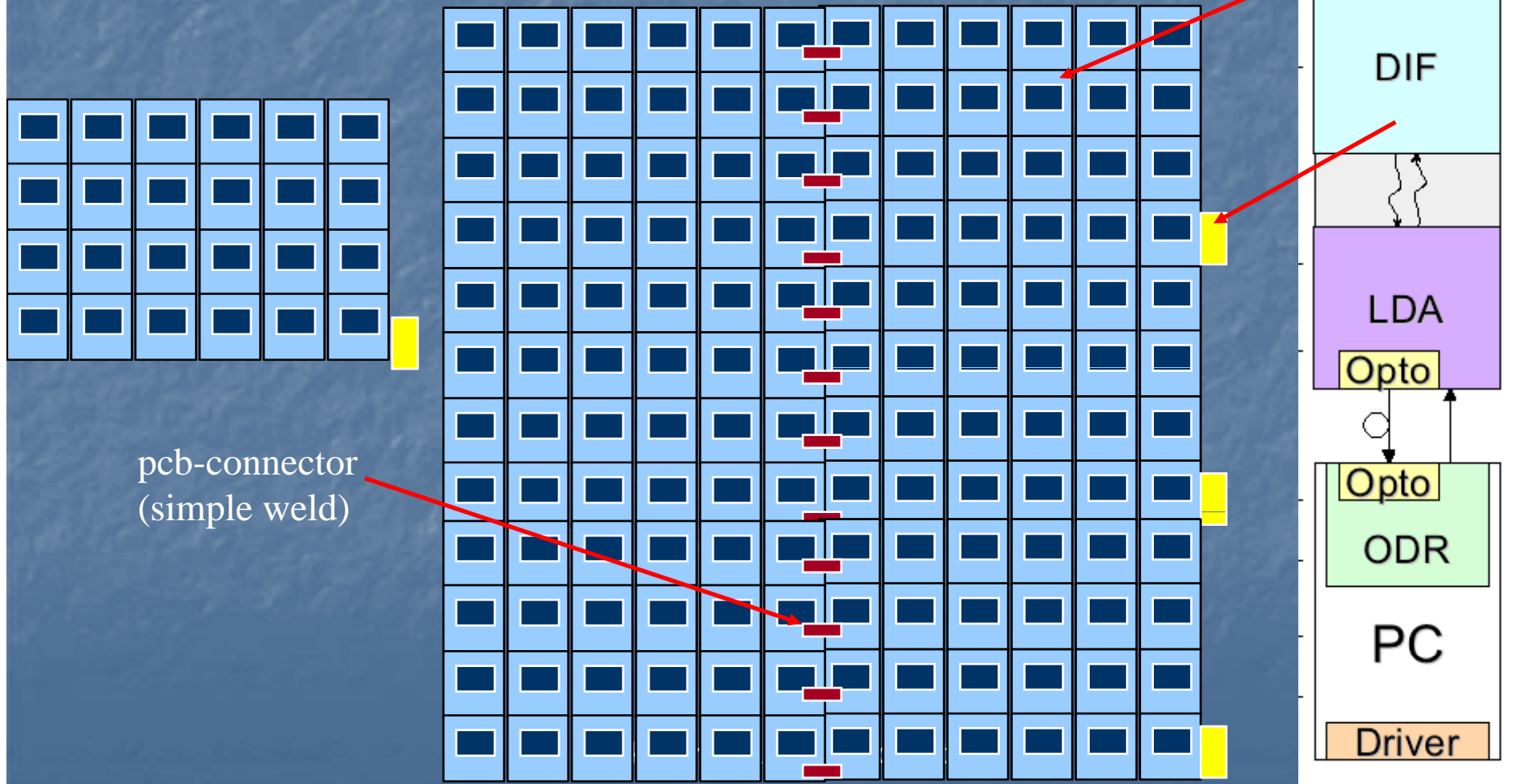
Support thickness = 2 mm



1M2 Support is designed and will be produced soon by ciemat

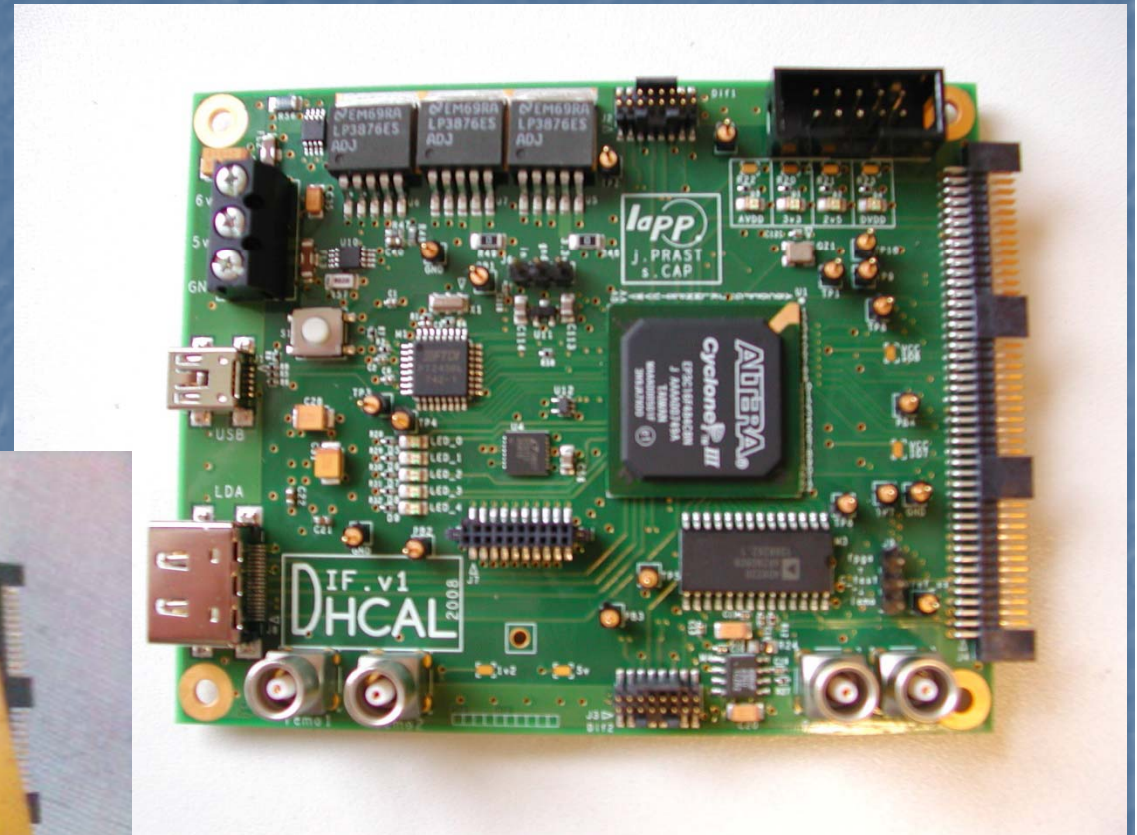
Connection to DIF

The pcb were conceived to allow connection PCB-PCB only in one direction → 3 DIF are necessary



DIF (LAPP)

10 DIF were produced
DIF :
8 cm * 10 cm * 1.6 mm
10 layers (6 for signals)



Firmware was developed and tested :
slow control+ digital readout

DIF

A specific **software** acquisition readout based on **Xdaq/usb** is developed in phase with the firmware development

- DIF low level access : OK
- Slow control : tested
- Digital acquisition : individual functions tested, integration in progress
- Event builder : in progress
- Analog Acquisition : in progress
- Monitoring : Developed , tests in progress with real DIFs

Some screenshots...

A manual mode that can control individually each parameter of one Hardroc on one DIF

ManualControl
 http://134.158.141.182:1972/urn:xdaq-a

Architecture logicielle - Comba... ManualControl

FTDI support
 ResetFT245 FT245GetStatus

Register access
 Address 0 Data 0 Read Write

Command access
 Command 0 SendCommand

ResetFPGA ResetHardroc ResetBCID ResetSC ResetSR R...

PowerAnalog PowerDAC PowerSS PowerDigital PowerADC

Slow control
 FT101001
 Configure SLC Manual ReadSLCStatus

Hardroc for manual access 0

Numerical readout
 StartAcquisition SendExtTrigger SendRamFull_Ext StartReadout:

Analog readout
 Timer Hold Register 0 StartAnalogAcq SendAnalogTrigg

DIF Imon gain 50
 Slab Imon gain 50
 Monitored channel 3
 Sequence function Sequence

EnableMonitoring MonitorAVDDShdn MonitorDVDDShdn

Terminé

ManualControl
 http://134.158.141.182:1972/urn:xdaq-application:lid=21/

Architecture logicielle - Comba... ManualControl

Manual configuration of hardroc 0 on DIF FT101001

Global settings

En_RamFull
 En_Dout
 En_TransmitOn
 En_Out_Discr
 En_Out_Trig_Int
 En_Trig_Int
 En_Trig_Ext
 En_Out_Raz_Int
 En_Raz_Int
 En_Raz_Ext
 Bypass_Chip

Misc

Valid_DC
 Sw_50f
 Sw_100f
 Sw_100k
 Sw_50k
 Choix_Caisson
 Sw_Ssc0
 Sw_Ssc1
 Sw_Ssc2

Power supply

On_Otadac
 On_Dac
 On_Pa
 On_Buf
 On_Ss
 On_W
 On_Otaq
 On_Fsb
 On_Discr

8 bits parameters

Header 0
 Dac0 100
 Dac1 9

ValidTrig	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
cTest	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Gain00	Gain08	Gain16	Gain24	Gain32	Gain40	Gain48	Gain56
Gain01	Gain09	Gain17	Gain25	Gain33	Gain41	Gain49	Gain57
Gain02	Gain10	Gain18	Gain26	Gain34	Gain42	Gain50	Gain58
Gain03	Gain11	Gain19	Gain27	Gain35	Gain43	Gain51	Gain59
Gain04	Gain12	Gain20	Gain28	Gain36	Gain44	Gain52	Gain60
Gain05	Gain13	Gain21	Gain29	Gain37	Gain45	Gain53	Gain61
Gain06	Gain14	Gain22	Gain30	Gain38	Gain46	Gain54	Gain62
Gain07	Gain15	Gain23	Gain31	Gain39	Gain47	Gain55	Gain63

Save

Terminé

PCB connection to detector

Temporary solution:

Use spacers to press electronics board against the detector inside a box. This allows to replace one detector with other avoiding the risk to harm the electronics board

Longtime solution : Glue? Solution should be the ILC one

We are open to suggestions and collaboration

Summary for the 1M² project

Hardroc1 chips are produced and currently under test

PCB are produced

Cabling will be performed by the end of September

DIF are produced and under test

Software is being developed

Detectors: Three kinds of 1M² GRPC detectors will be produced
IHEP,IPNL,INFN-Bologna

Connection between electronics board and detector is investigated

Beam test in November at CERN if things go as expected

Toward the 1M³ prototype

- Electronics :
Hardroc2 was designed and submitted
return expected for October
- Detector :
The November beam test will allow us to
choose the better GRPC detector
- Absorbers : Some tests were done in CIEMAT workshop
Production of high surface quality Steel
absorbers is possible and will be scheduled

1.- Ciemat mechanical workshop.

Milling Machines:

- 1 CNC machine of aprox 4x1 m2 working table. Accuracy of aprox 0.03 mm/m, with temperature compensation.

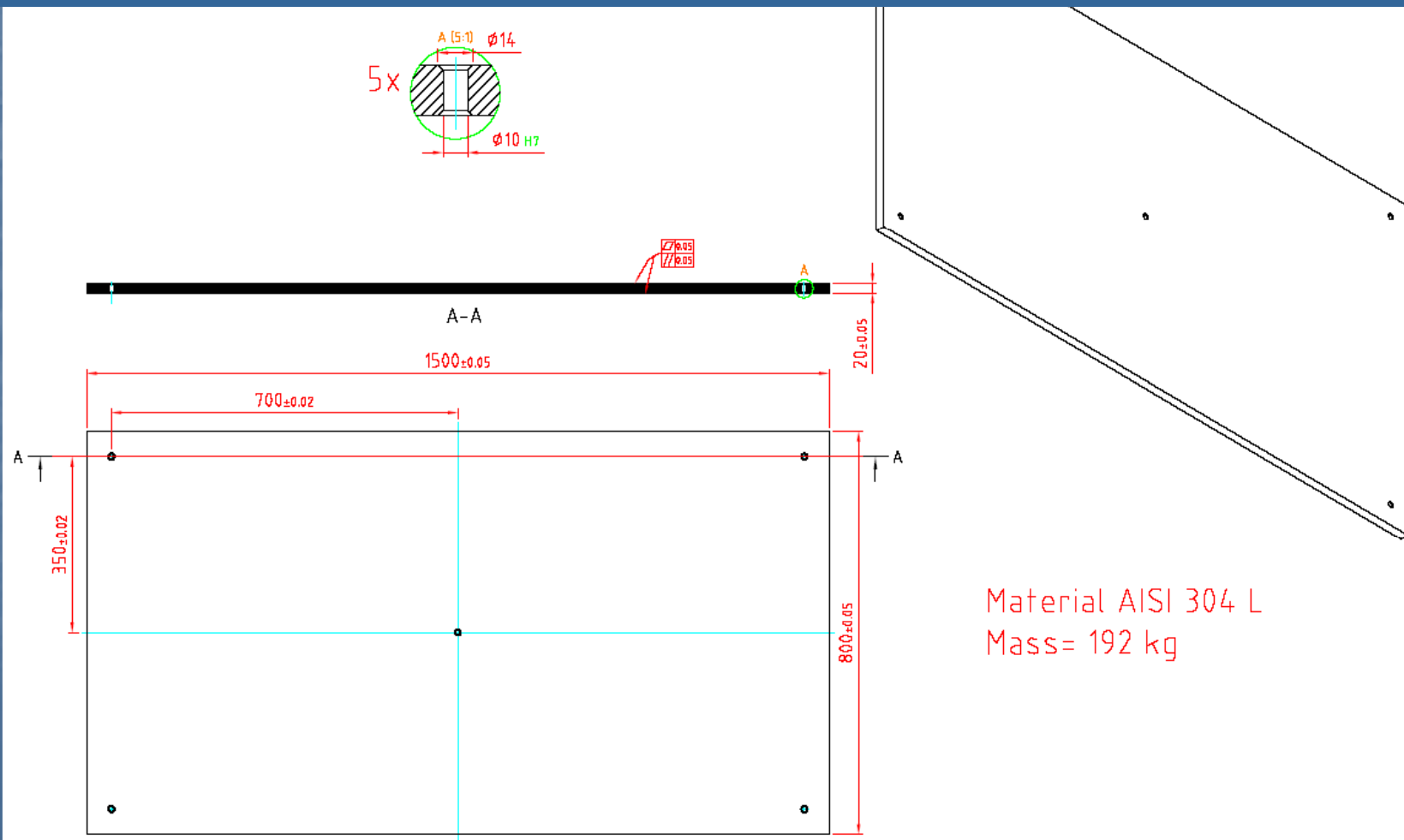


This is the machine that can be used to produce the plates for the HCAL prototype.
I.Laktineh Calice-Manchester

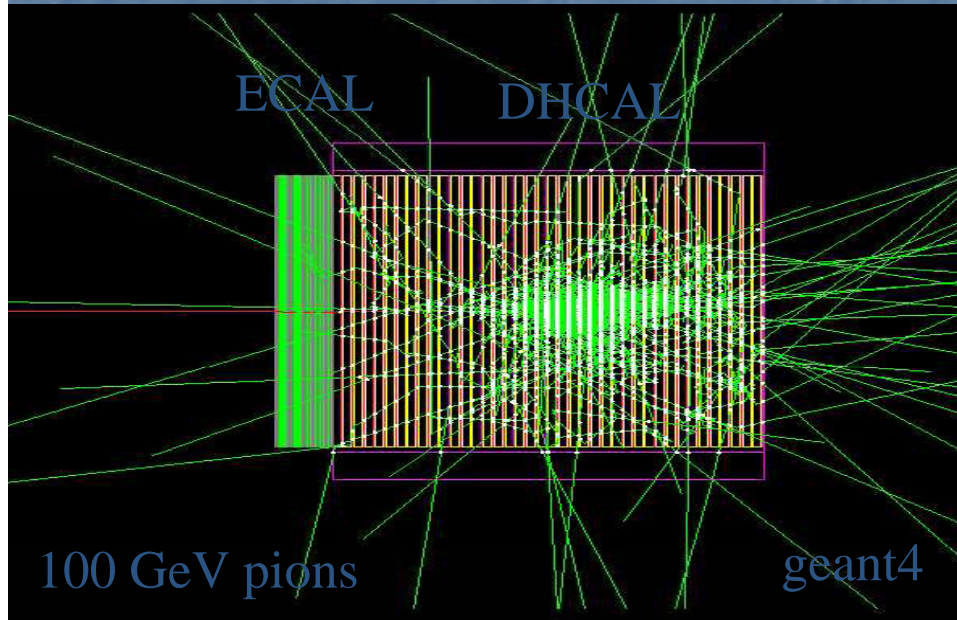
2.- Test on a plate of 1510x810x25 mm³

To study the capacity and possibilities of the Ciemat workshop to produce the prototype:

- To verify the planarity of the plate we was used a comparator on the CNC machine. And to verify the CNC machine we will use interferometer measurements (not yet finished). The final planarity of the plate will be measure by the interferometer, if this is considered necessary.
- We was machining a plate of AISI 304 L, to obtain the following plate:

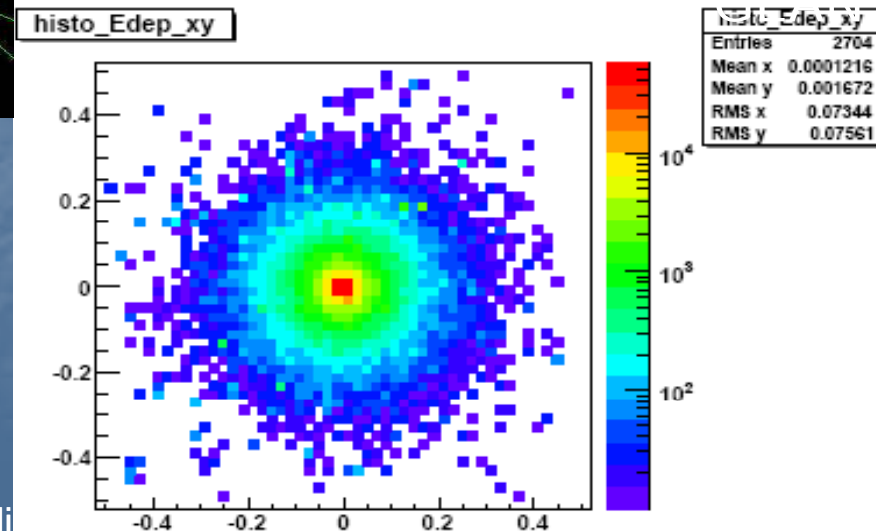
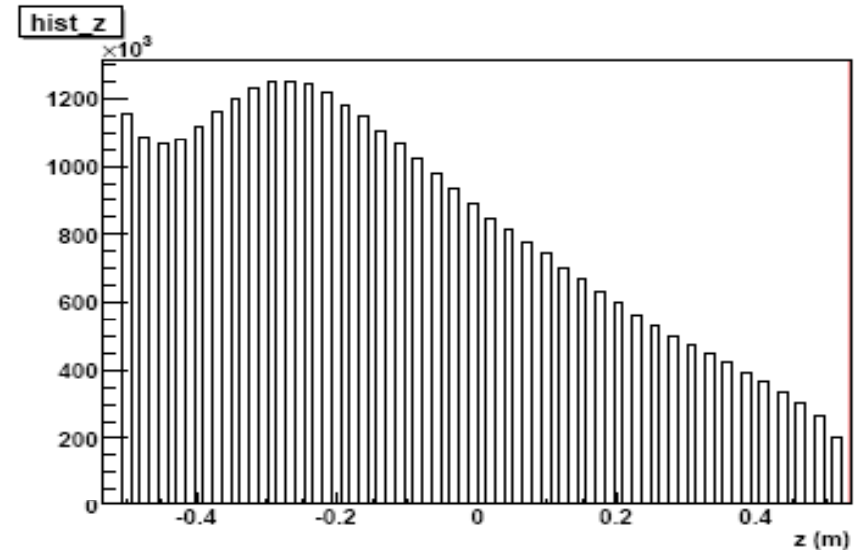


Which dimensions for the prototype?



Longitudinal and transverse develop.
of hadronic showers associated to
100 GeV pion in **DHCAL(4,5 λ)**
behind **ECAL (24 X₀)**

Preliminary :
95% of the showers are included in 70X10cm Cal



Toward the 1M³ prototype

Although 70X70 X 100 cm³ prototype is ok for hadronic shower studies with GRPCs, we think to go to 100X100 X 100 cm³ one if the additional cost is not too high.

In any case this will be subject to results obtained with the 1M² detectors (GRPC/MICROMEAS)

Conclusion

- A mini DHCAL/GRPC was built and successfully operated using the new generation of readout electronics
- New design GRPC detectors were tested and interesting results obtained
- The GRPC 1M² is almost completed and beam test is expected before the end of 2008.
- The EuDHCAL is enriched by new comers (Bologna-Italy)
- Important work was done for DHCAL/GRPC for ILD (M.Anduze) but more work is expected soon

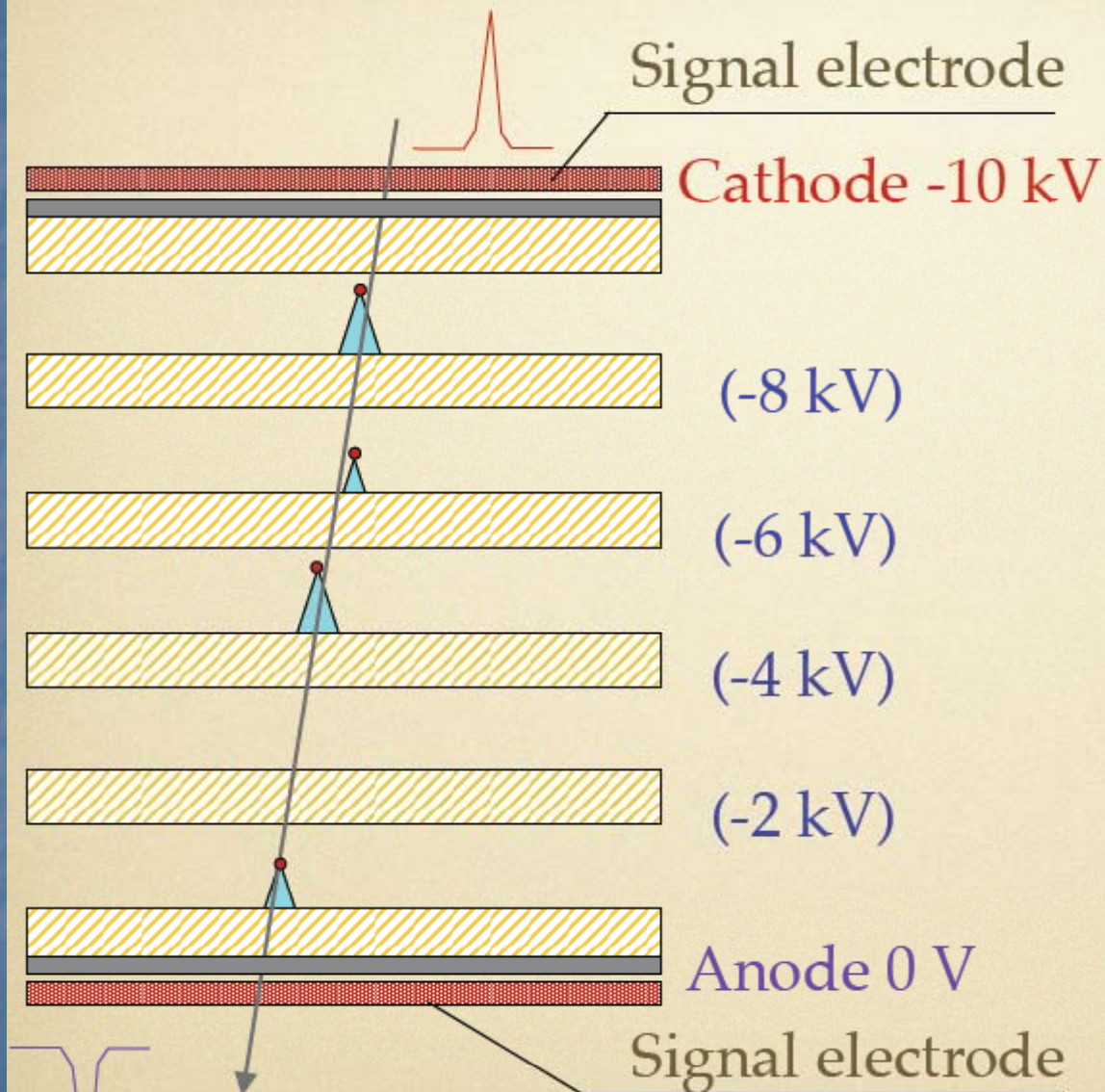
Multigap GRPC

Advantages :

- 1 mip spectrum is less spread
(very good for semi-digital readout)
- Higher efficiency

We would like to test it....

MULTIGAP RESISTIVE PLATE CHAMBER



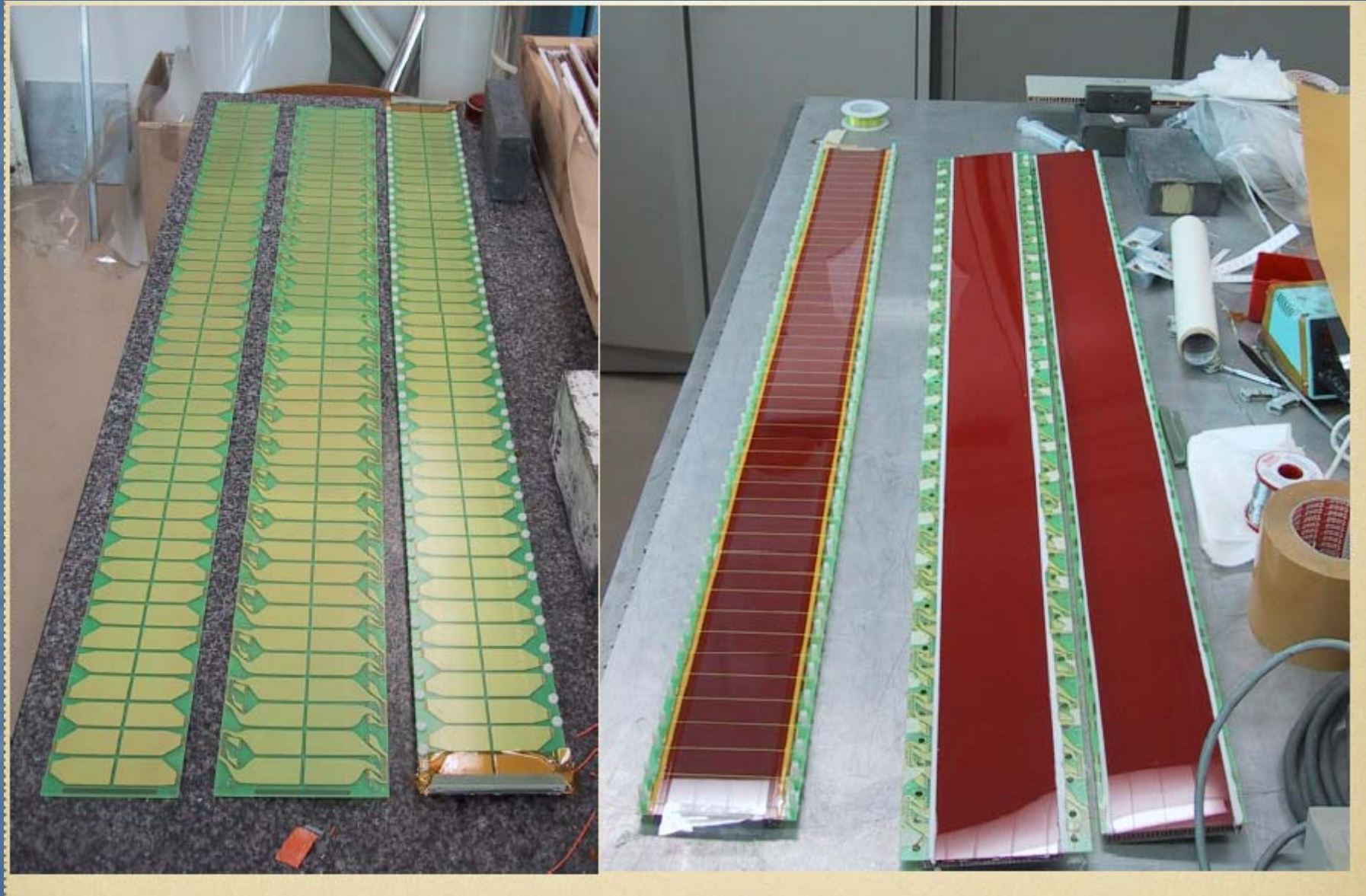
Stack of equally-spaced resistive plates with voltage applied to external surfaces (all internal plates electrically floating)

Pickup electrodes on external surfaces (resistive plates transparent to fast signal)

Internal plates take correct voltage - initially due to electrostatics but kept at correct voltage by flow of electrons and positive ions - feedback principle that dictates equal gain in all gas gaps

Courtesy C. Williams

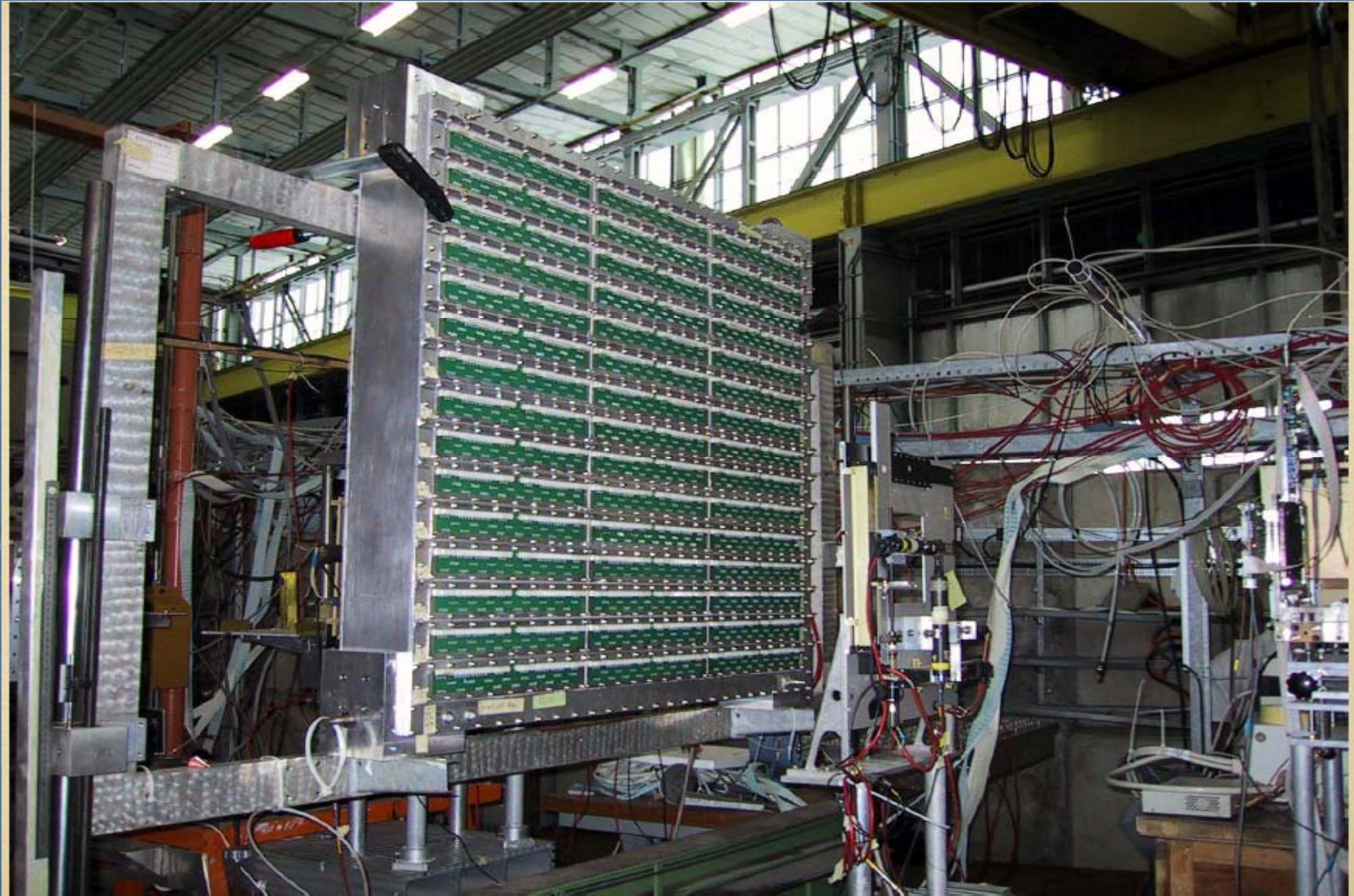
Alice TOF



Courtesy C. Williams

I. Laktineh Calice-Manchester

Alice TOF



Courtesy C. Williams

I. Laktineh Calice-Manchester