

Technical

Meetings on electronics, mechanics, and ILD integration

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Minutes of the “short meetings on electronics”

June 6, 18, 24

July 4, 29

June 6 : List of modules that could be shared

[Http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2809](http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2809)

Identify common blocs with links on documentation

Check the interfaces

Proposal from developers themselves:

Component name	Contact person	status	schedule	description
USB	Julie	V0 tested		
Analogue RO	Julie	Not tested		
RO itf	Clement	Working with		
DIF-SLAB itf	LPC ? or LAPP	old ROCs		
LDA-DIF itf	Marc			
LDA-ethernet	Marc			
USB debug sw	Clement			

Could become more “official” within CALICE

June 18 : USB module

<http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2798>

- Review of the existing USB module from Julie Prast, Clement Jauffret and Christophe Combaret
- CALICE “standard”
- Extensively used for the DHCAL TB this summer
- Links on FW/SW code (see indico)

June 24 :DAQ and CCC

<http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2817>

- First discussion on “Running Modes”
 - Demonstrator : thermal tests, low pulsed power,... = technological studies based on ILC constraints
 - Test Beam/Physics : detector performance based on TB properties (structure, rate, ...)
- Clear definition of what we expect from EUDET
- See Yesterday Christophe’s Talk
- Definition of “Very Fast Commands” and “Commands”
- CCC timing, latencies, etc...
- BUSY signal

July 4 : Demonstrator mode, DCC, DIF

<http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2839>

- Discussion on consequences of the technological studies on electronics design
 - Low power configuration of electronics
 - TB structure and compatibility with electronics optimized for ILC constraints
 - Data rate
 - No ext trig : noise!
- Data concentrator card status
 - Impact on DIF-LDA protocol

Background question is the ratio physics/techno

100 evt/s ?

EUDET meeting, LAL, June 2nd 2008

- Assuming : **4 chips full** every times on the highly occupied layer, **64 ch/chip, 16 evt buffer**

Chips become full because of the common triggering scheme and particles rate of the beam

 - Data = $4 * (16 \text{ ID} + 16 * 16 \text{ time} + 16 * 64 * 16) = 16656 \text{ bits}$
- Assuming **5 MHz read-out clock** and no partitions
 - $16565/5E6 = 3.4 \text{ ms}$ (for 16 evt)
- Number of events that could be acquired in one spill
 - $10\text{s}/3.4 \text{ ms} = 2.9 \text{ k}$
 - To be divided by $N/4$ if **N** chips are full (max is $N=16$ in the tower)
 - To be multiplied by **P**, the number of partitions **read-out in //**
- Actual rate : 1 spill every **2 mn (could be 1 mn)**
 - $2.9 \text{ k} / 120\text{s} = 24 \text{ Hz}$ (50 Hz) But not all are interesting events ! = time aligned over the detector


 EUDET specific



P=4, data rate at the output of a DIF = 20 Mb/s

Event rate, limiting factors

- Read-out time
 - Read partitions in //
 - Store in buffers only interesting events
 - Ext trig (but rate of ext trig?)
 - Increase int trig threshold
 - Increase SlowCLK frequency (short SLABs only)
- BEAM structure
- EXT trig

EUDET : 2 aims = 2 major modes ?

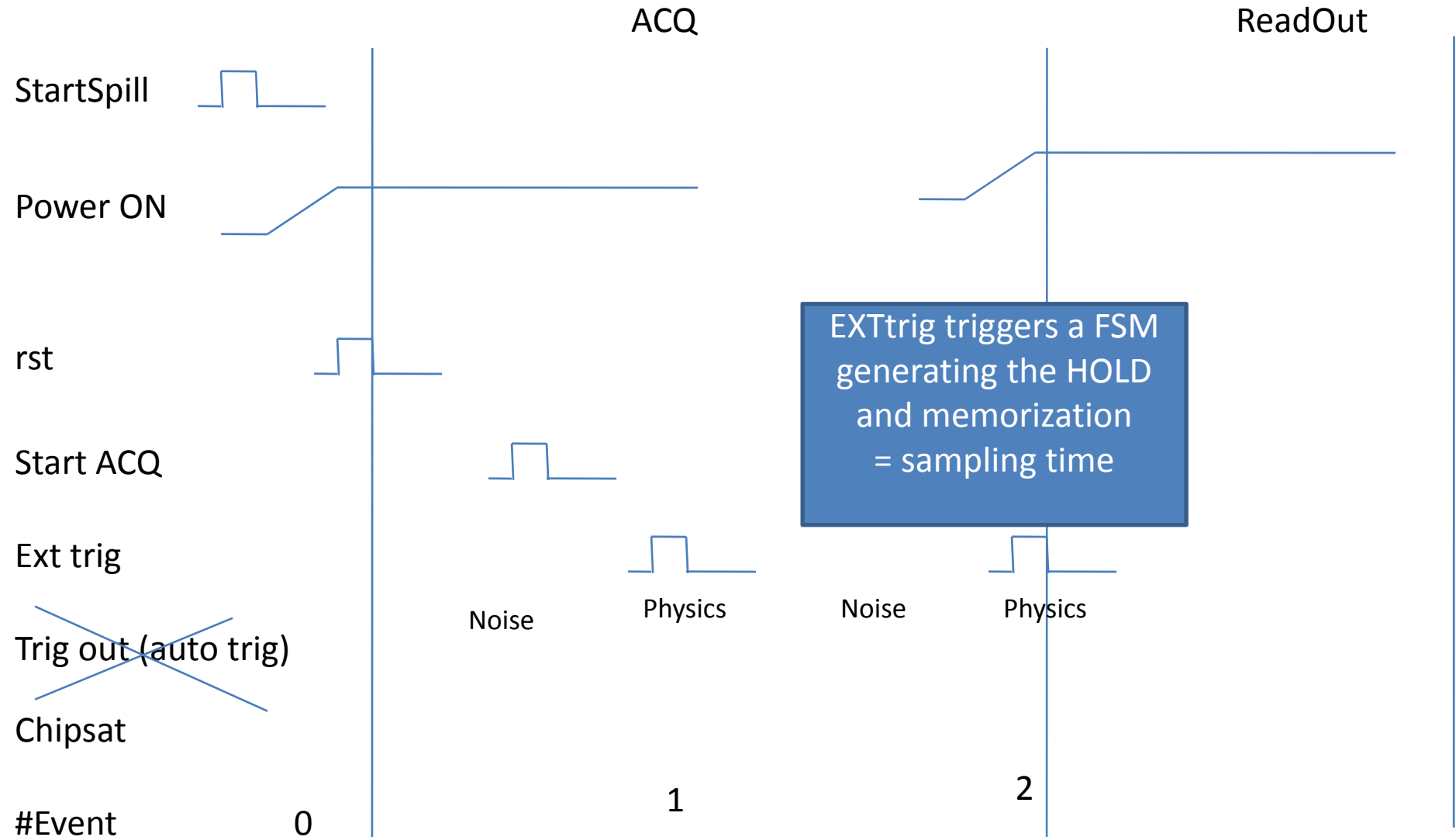
- Calibration / Noise / Test beam

The aim of the calibration mode is data taking in order to perform the calibration of the detector and physics studies about properties and performance of the detector. The detector and the electronic systems are configured to ensure the highest rate for the data taking.

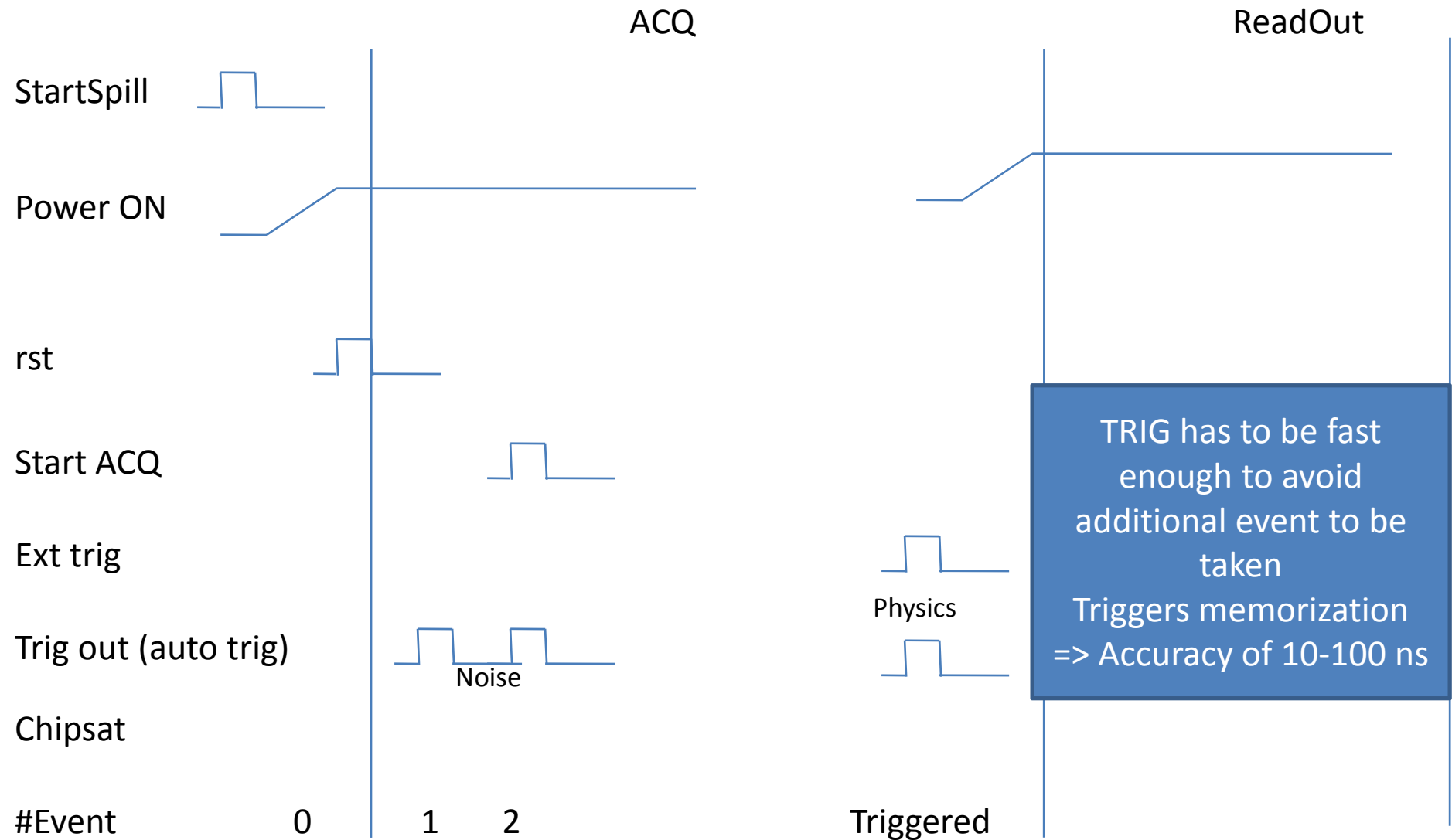
- Demonstrator (=EUDET)

The demonstrator mode is intended to run the detector as close as possible to ILC functioning in order to perform engineering studies on power pulsing, power supply, thermal dissipation. It is under the scope of the EUDET contract for which technical solutions must be tested and engineering feasibility must be proven.

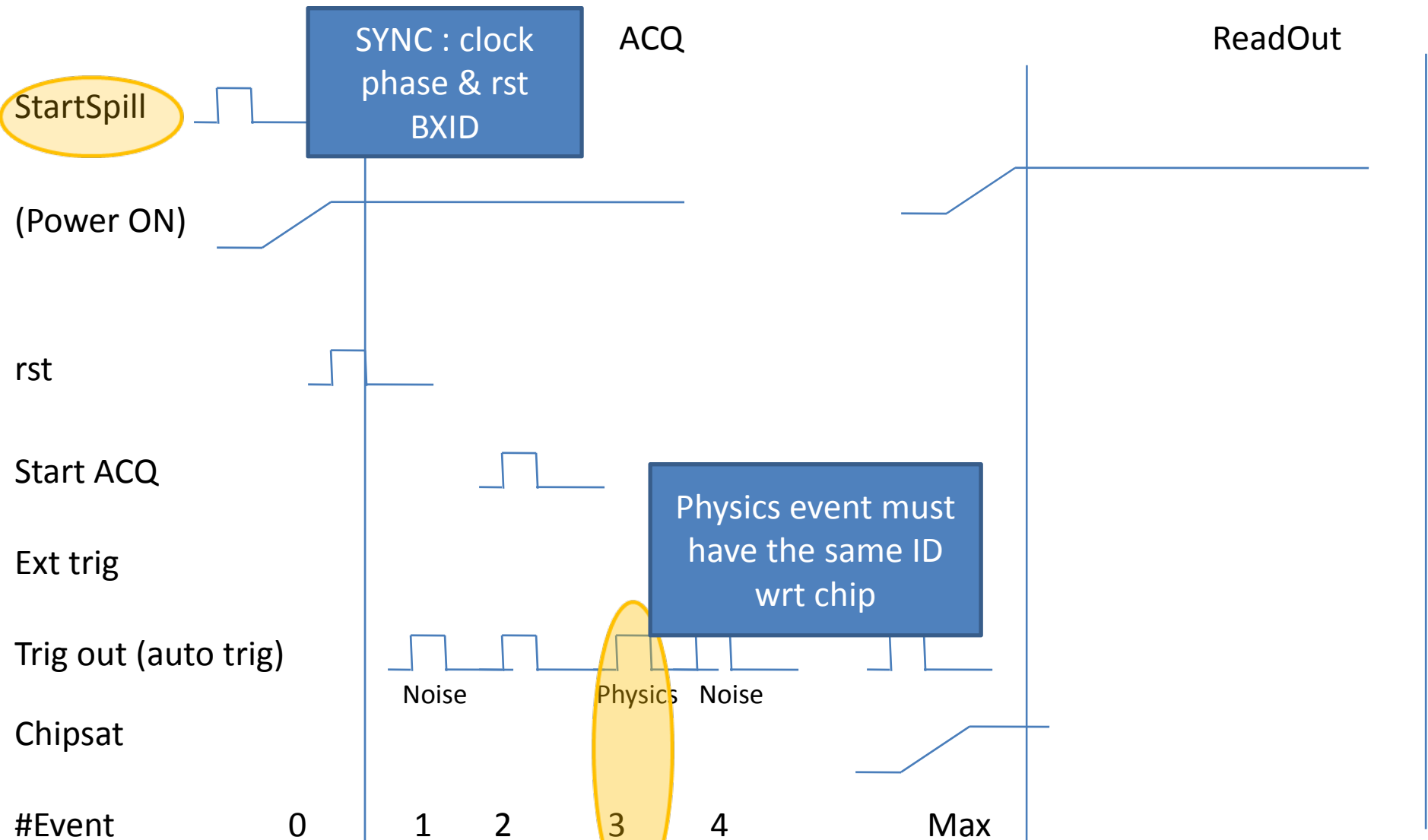
Typical cycle (triggered event)



Typical cycle (single event)



Typical cycle (burst)



July 29 : Meeting at LLR

<http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2890>

- First part dedicated to Si-W ECAL
- Second half about CCC and DAQ
 - LDA-DIF links
 - FASTin/out : BUSY/TRIG/STOP
 - Commands
 - Latency and phase adjustments
 - Machine signals : “Start Spill”, “TrainSync”
 - Resets, hardware reset?

Find common vocabulary !

Do we need to continue ?

- (Common) Pending questions
 - Magnetic field
 - Signal integrity (buffer strength, PCB traces,...)
 - Grounding
 - Power supplies (On/OFF procedure, decoupling, ...)
 - TB installation
 - ...
- Feedback on designer's experience, sharing
- Speed up communication : convergence on specifications
- Would need written document : CIN
- Meetings on the web cannot replace meetings with people physically present

Conclusion

- Minutes are on the web
 - <http://ilcagenda.linearcollider.org/categoryDisplay.py?categId=156>
 - ~ 30 pages
- Written documents (should be) in preparation
 - LDA-DIF link
 - LDA protocols
 - Running modes

Next ? : EUDET event rate(use of running modes), Power supplies, Grounding, TB installation...

How ? EVO? T?