Testbeam issues for CALICE/EUDET technological prototypes

8 September, 2008

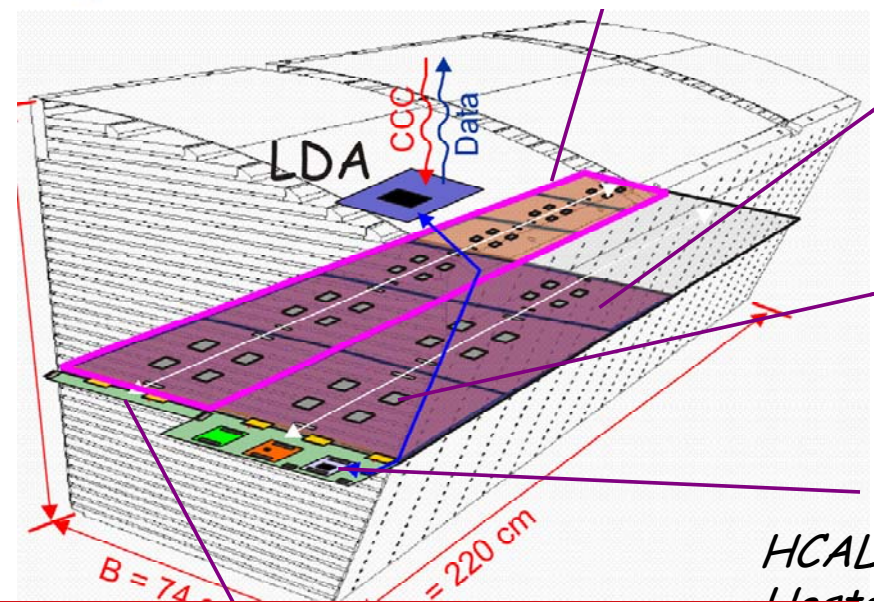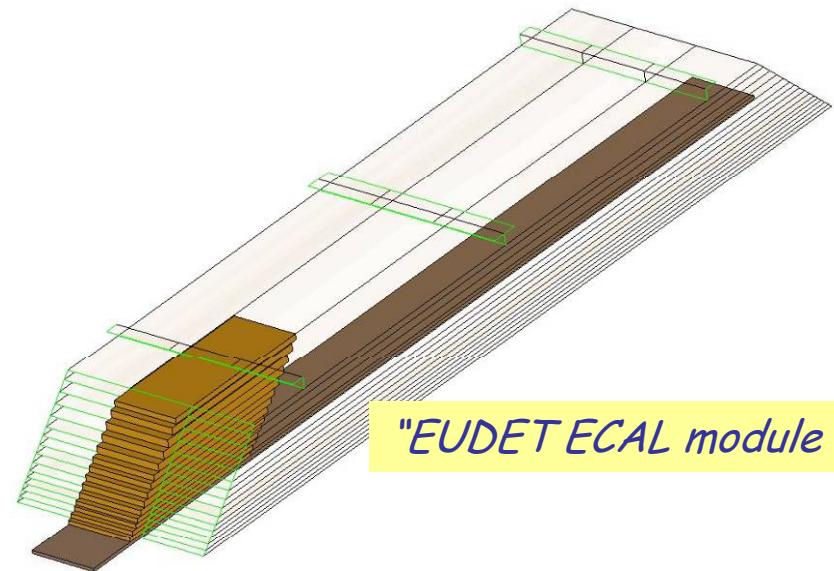- **Technical prototype**

- Test many technical issues
  - "stictchable" motherboards
  - Minimize connections between boards
  - Reduce PCB thickness to <1mm
  - Internal supplies decoupling
  - Mixed signal issues
  - Digital activity with sensistive analog front-end
  - Pulsed power issues
  - Electronics stability
  - Thermal effects
  - To be validated in beam
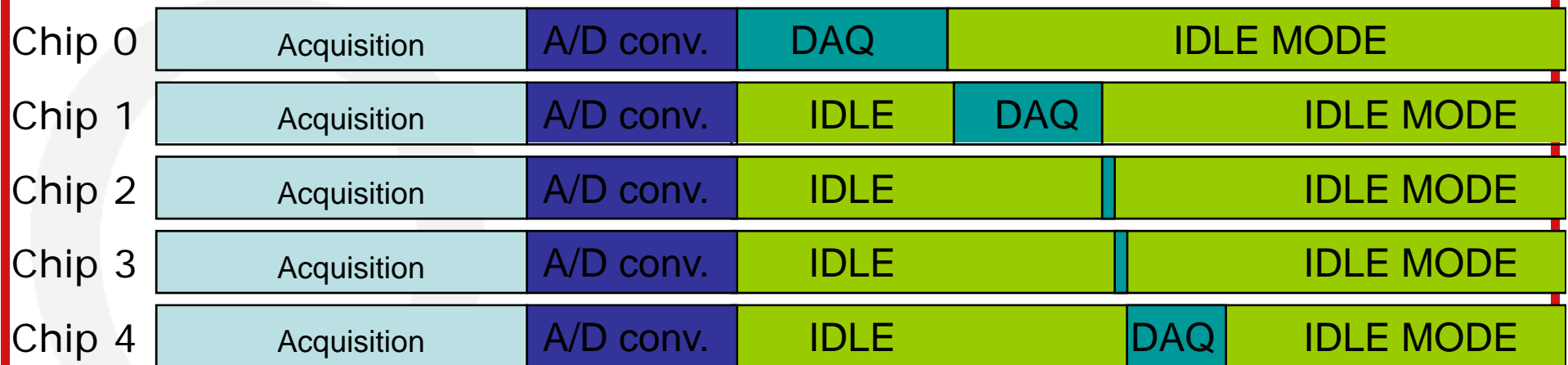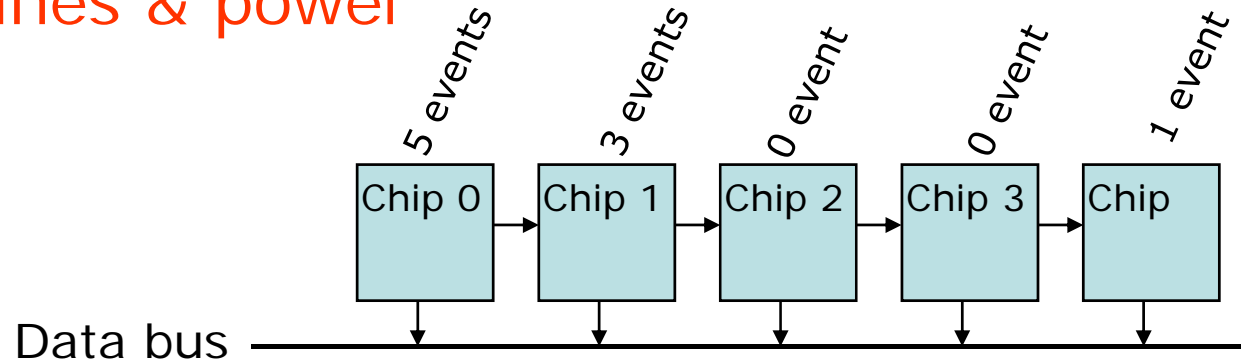

"EUDET ECAL module

ECAL boards

- ## Front end boards (FEV7)
  - 18cm*18cm PCB with 6-inch wafers (4 wafers of 9*9cm)
  - 0.5*0.5cm² pads → 324 pads/wafer → 1296 channels/PCB
  - 16 redout chips (first SPIROC2 then SKIROC2)
  - 2 (duplicated) readout lines => 8 chips/line
  - 16 events*(32 or 64 channels)*16bits/chip=8-16kbits/chip

SKIROC2
or
SPIROC2

Data

Data

PCB

WAFER

18cm

18cm
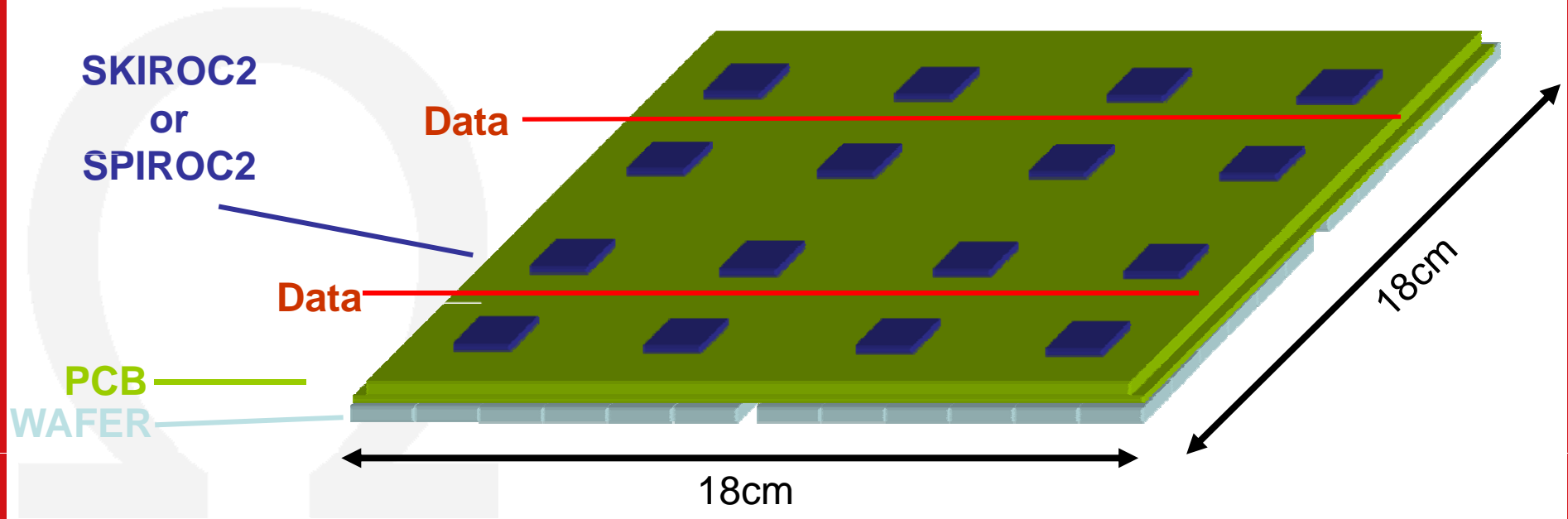
ECAL readout rate

- ## Readout rate : 1 to 5 MHz
  - 8 chips/ data line * 16 kbit/chip = 128 kbit/data line
  - Readout time : 25 to 128 ms
  - Acquisition and digitization time negligible (~2 ms)
  - Readout sequences per second : 8 to 40
  - Events per second : 128 to 640
  - 5 MHz with only one board on the slab should be feasible

- ## « Add » 1% duty cycle
  - Need that digital power pulsing efficient, ie reduced power during readout
  - otherwise 1% ON during 10s beam means OFF during 16mn !!

Read out : token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power

5 events	3 events	0 event	0 event	1 event
Chip 0	Chip 1	Chip 2	Chip 3	Chip

Data bus

Chip 0	Acquisition	A/D conv.	DAQ	IDLE MODE
Chip 1	Acquisition	A/D conv.	IDLE	DAQ	IDLE MODE
Chip 2	Acquisition	A/D conv.	IDLE	IDLE MODE
Chip 3	Acquisition	A/D conv.	IDLE	IDLE MODE
Chip 4	Acquisition	A/D conv.	IDLE	DAQ	IDLE MODE

1ms (.5%)   .5ms (.25%)   .5ms (.25%)   199ms (99%)

1% duty cycle   99% duty cycle

Discussion

- Figures to be checked and discussed
- Data taking rate: 128 to 640 Hz
- Power pulsing 1%
- Readout time (~100ms) dominates acquisition time
- Cycle similar to ILC (ms)
- Much higher occupancy (16)
- Very pessimistic : assumes all 8 chips full
- What power dissipation during readout ?