TRK/VTX summary

Summary of the Silicon sessions of the tracker and vertex detector R&D groups
(gaseous tracking covered separately)

Marcel Vos
IFIC, centre mixte U. València/CSIC

Thanks to my fellow tracking conveners (K. Dehmelt, M. Stanitzki) and the vertexing convenors (L. Andricek, M. Campbell, M. Winter)

TRK/VTX group

7 ½ Sessions:

Tuesday	-	13:00 – 14:00 LC tracking discussion (S. Aplin, M. Battaglia)
	-	14:00 – 15:30
Wednesday	-	09:00 – 10:30 TPC/VXD
	-	11:00 – 12:30 VXD/SiTRK
	-	16:00 – 18:30 TPC/VXD
Thursday	-	09:00 – 10:30
	-	14:00 – 16:00

25 Contributions:

SiLC update, A. Savoy-Navarro, LPNHE
SiTra FE design, R. Sefri, LPNHE, by A. Savoy-Navarro
Transparent Si sensors, M. Fernandez, IFCA Santander
The Silicon Pixel Tracker, Ch. Damerell, RAL

Bump bonding hybrid pixel detectors, Sami Vaehaenen,
3D chip development, R. Lipton, Fermilab
SOI pixel sensors, M. Battaglia, CERN/UCSC/LBNL
Read-out system for FPCCD, T. Saito, Tohoku U.

Progress in Spider, S. Worm, RAL
LePix, W. Snoeys, CERN
HV CMOS pixel detectors, I Peric, Heidelberg U.
CMOS pixel sensors, J. Baudot, IPHC Strasbourg

Thanks to all speakers + apologies, as I cannot possibly present a complete and balanced summary in 15 minutes

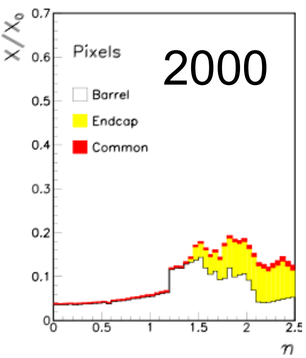
UCSC μ-strip R&D, B. Schumm, UCSC
ILD forward tracking, W. Mitaroff, HEPHY Vienna
Cherwell: intelligent tracking, J. Goldstein, Bristol U.

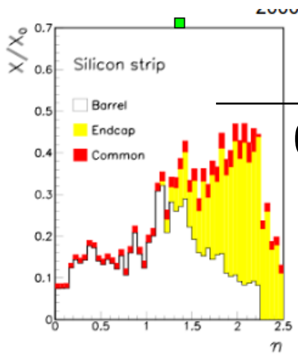
DEPFET, J. Ninkovic, MPI
Low mass VXD structures, J. Goldstein, Bristol U.
Ultra-light ladders, I. Gregor, DESY
Monitoring, I. Vila, IFCA Santander, by D. Moyà
Layout optimisation for CLIC, D. Dannheim, CERN

CLIC-SiD performance, B. Pie, U. Barcelona
Tracking simulation, A. Charpy, LPNHE
DAQ, E. Corrin, U. Geneva + discussion

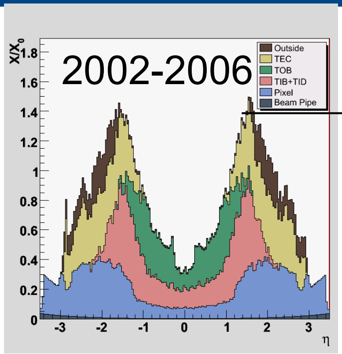
The CMS all-silicon tracker, D. Abbaneo, CERN
Testbeam, M. Winter, Strasbourg + discussion

Lessons learnt at the LHC



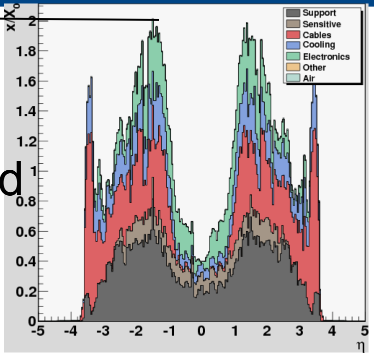


0.5 X/X_0



1.4 X/X_0

2 X/X_0
2010
measured



The least glorious part of the story: CMS tracker material budget estimate vs. time

The protocol that is known to lead to the wrong material budget estimate

- Start from an empty file
- Add the elements that you know, with optimistic assumptions
- Use theoretical values for services
- Ignore everything that you don't know how to estimate
- Don't add any contingency for elements to be added along the way

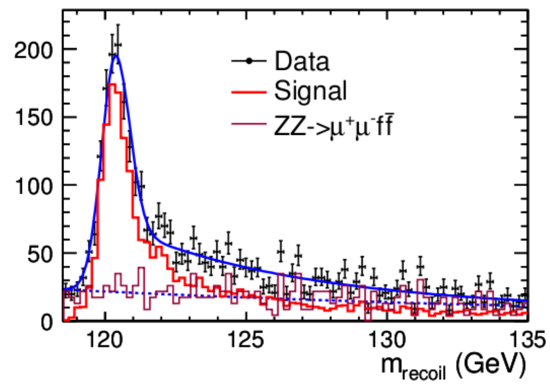
The CMS upgrade protocol: "guilty until proven innocent"

- Start from an existing detector (in our case, the CMS Tracker)
- Remove/reduce material only where justified by a reasonably understood ongoing development
- Aspects not yet "reviewed" should serve as contingency for the uncertainties on the new developments
- Invest a lot in modelling studies
- Keep in mind: detectors that are not built tend to be lighter than detectors that are built!

We are not exactly following the first protocol.
The second is not applicable in exactly the way CMS uses it.

D. Abbaneo (CERN)

TRK/VTX Requirements



Canonical tracking resolution:

$\Delta\ (1/p_{(T)})$ = few times 10^{-5}

Driven by recoil mass analysis and SUSY end-point analyses. Figure: reconstructed Higgs mass in ILD LOI

Canonical vertexing resolution:

$\Delta\ (d_0) = 5 \oplus 10\ /\ p \sin^{3/2}\theta$

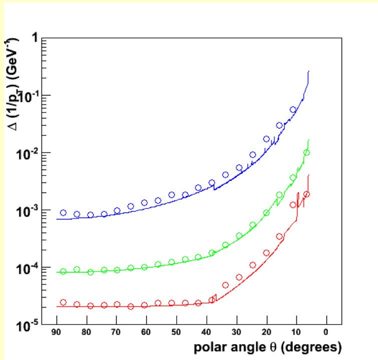
	a (μm)	b (μm GeV)
LEP	25	70
SLD	8	33
LHC	12	70
ILC	5	10

$$\sigma_{IP} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

Do all this with material budget → 0!!!

CAVEATs

SiD specifies (1/p), ILD ($1/p_T$). Actually, that "T" makes a difference...



Specs are not met for all momenta and all angles. Do we limit ourselves to complete polar angle coverage, or do we require uniform performance?

....

There are other (equally important) specifications that are harder to quantify, the robustness of track finding (pattern recognition)

tools are being completed to address this type of questions. Interesting Talks by A. Charpy, W. Mitaroff

ILC vs. CLIC

Talks by D. Dannheim, B. Pie

ILC vs. CLIC: New benchmarks

Example: Higgs-strahlung process and recoil mass analysis not likely to be relevant at a multi-TeV machine. A strong tracking requirement can be derived from $H \rightarrow \mu\mu$

Example: relevance of forward b-tagging

ILC vs. CLIC: New specifications

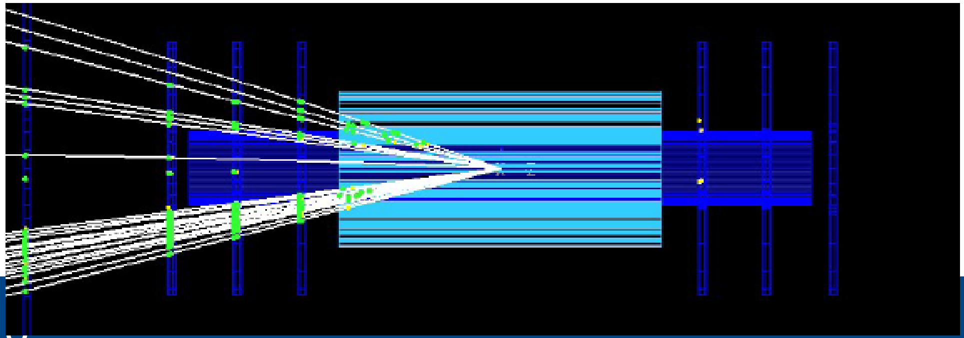
Example: CLIC VXD forced out to R = 3 cm by machine background. Affects what's feasible (especially when required to identify BCID)

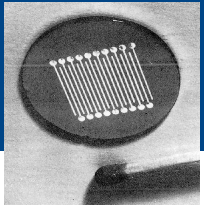
ILC vs. CLIC: New detector design

Obvious example: HCAL thickness

Example II: at R = 3 cm, the long barrel vertex detector either becomes a "very long barrel", or has inadequate coverage,

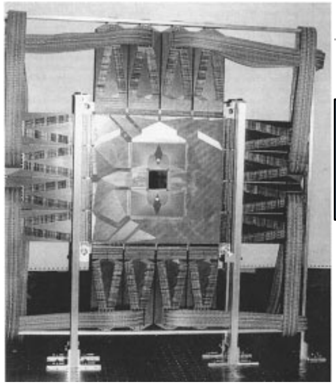
Simulated event in new CLIC forward vertex disks
$e+e- \rightarrow nnH(185) \rightarrow nnbb$
Courtey of M. Battaglia





1980s: μ-strip detector is mature: < 5μm resolution

Si μ-strips



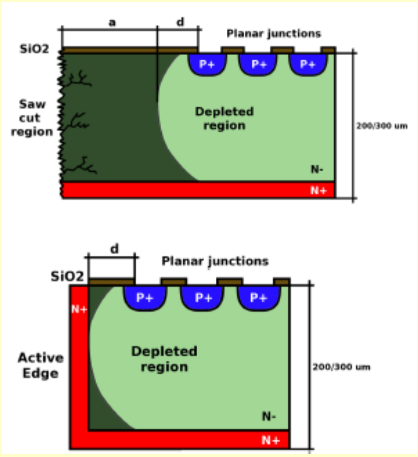
Since then, struggling with 4π geometry!

Measure coordinate along strip using charge division.
UCSC find 6 mm precision is feasible,
in agreement with the old claim by Radeka et al. (B. Schumm)

And challenges some of our prejudice about long ladders

$$Q^2 = F_i \tau \left(2eI_d + \frac{4kT}{R_B} + {i_{na}}^2\right) + \frac{F_v C^2}{\tau}\left(4kTR_s + {e_{na}}^2\right) + 4F_v A_f C^2$$

A very dynamic market, new vendors and new products

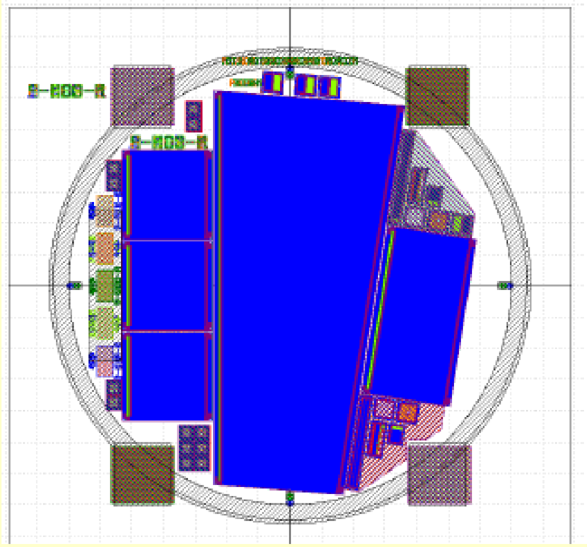


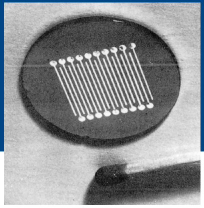
DSSD (out of fashion for a long time) available from Micron / HPK / Canberra / SINTEF / ETRI

Active edge-buttable sensors

(A. Savoy Navarro)

Trapezoidal sensor with test structures





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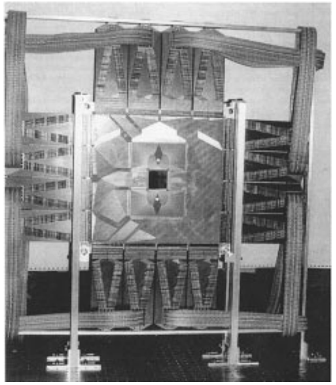
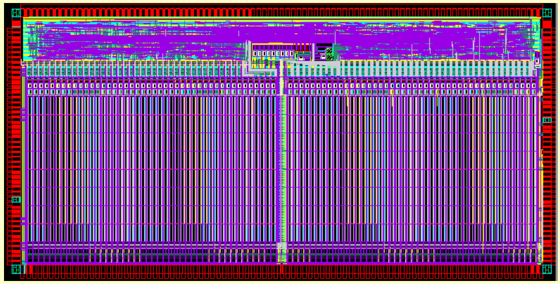
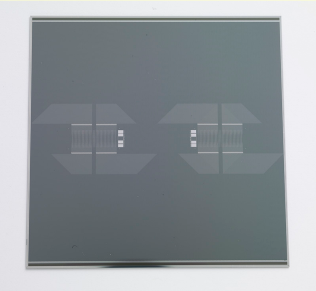


Since then, struggling with 4π geometry!

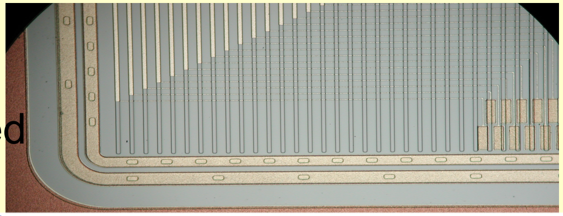


SiTra FE,
ILC read-out,
500 μW/channel

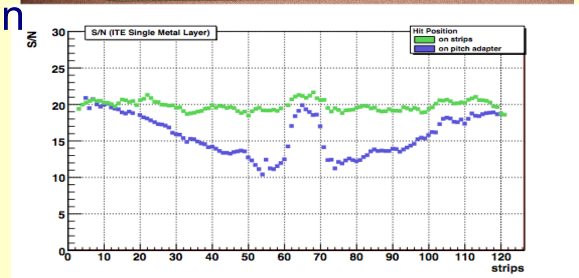
Presentation by R. Sefri



Both SiD and SiLC pursue
hybrid-less modules:
direct integration of FE on sensitive material. Additoinal metal layer incoroporates pitch adapter

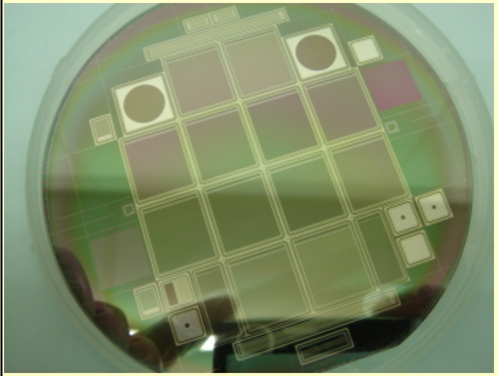


Signal loss observed by HEPHY for particles incident on PA, compared to other areas of the sensor



A. Savoy Navarro

IFCA/CNM: IR transparent sensor provides no-added-material alignment system a la AMS (M. Fernandez)

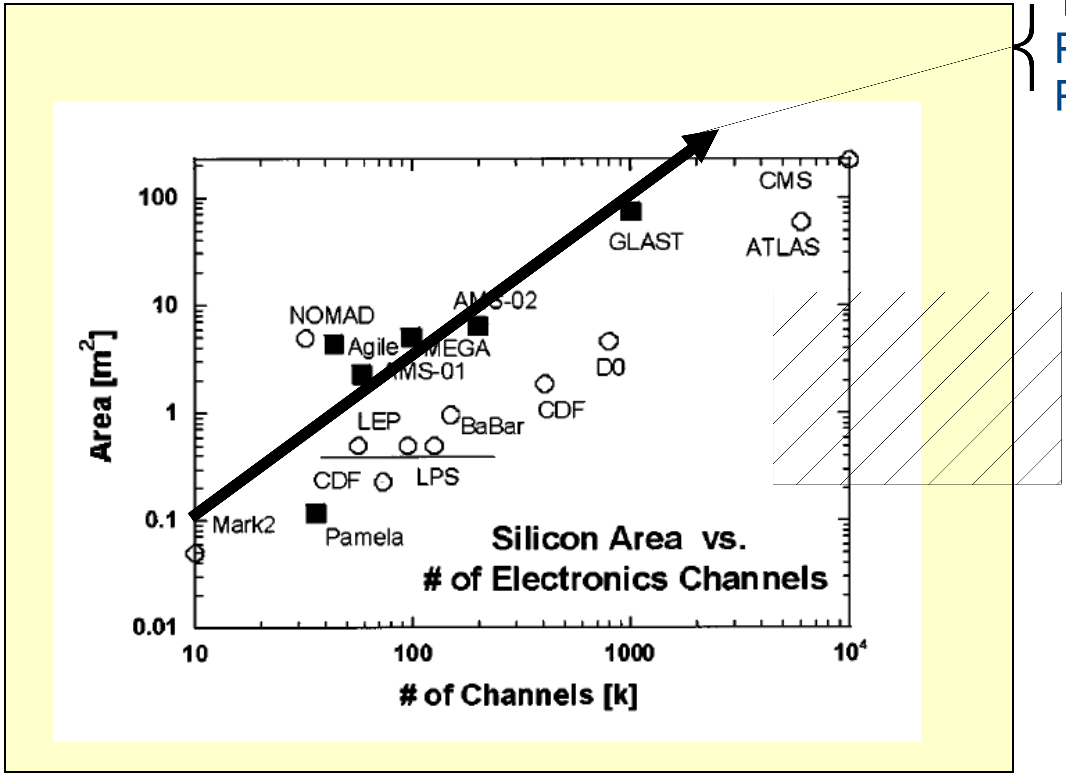


T= 55%

See EUDET Annual MEMO
Next step: Bragg Fibers monitoring?
(I Vila, D. Moyà)

Strips vs. pixels

Trend for μ-strips is towards larger systems with moderate performance in terms of spatial resolution



The micro-strip line:
Power ~ 500 μW/channel (SiTra FE chip)
Power densit-y ~ 5 mW/cm² (instantaneous)

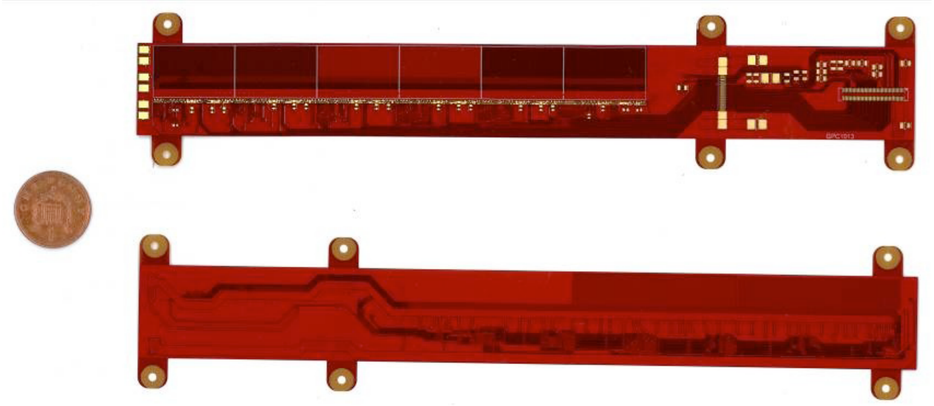
Consensuated niche for highly granular devices. # channels/area increases by up to 4 orders of magnitude wrt μ-strips.

More daring ideas about the role of pixel technology in the inner detector of an LC experiment exist
- trading off spatial granularity and time resolution - see Silicon Pixel Tracker presentation by Ch. Damerell and talks by J. Goldstein/S. Worm)

The challenge is NOT to reach a few micron precision OR good time resolution/read-out speed, but to develop a device that balances both AND has acceptable power/material budget

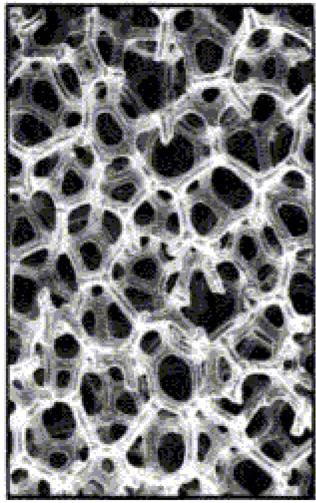
Mature technogies

Proof of maturity: several groups have dedicated considerable effort to services: support concepts for ultra-thin sensors (PLUME/SERWIETTE, DEPFET), stitching, buttable sensors (several, notably STFC), air cooling (MIMOSA for FIRST/STAR/CBM-MVD, DEPFET for Belle-II)

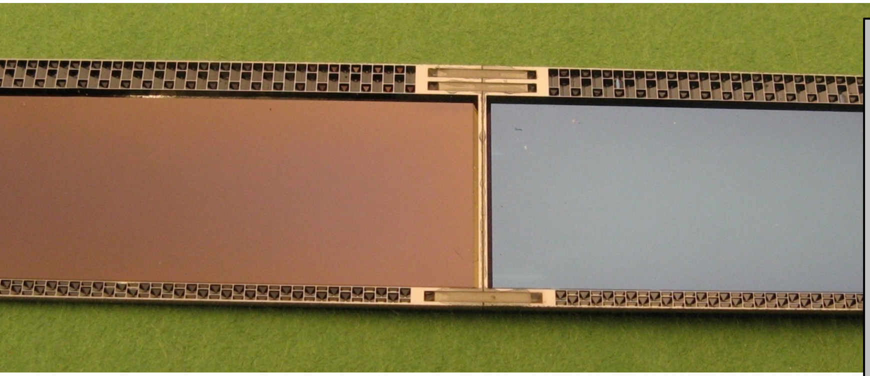


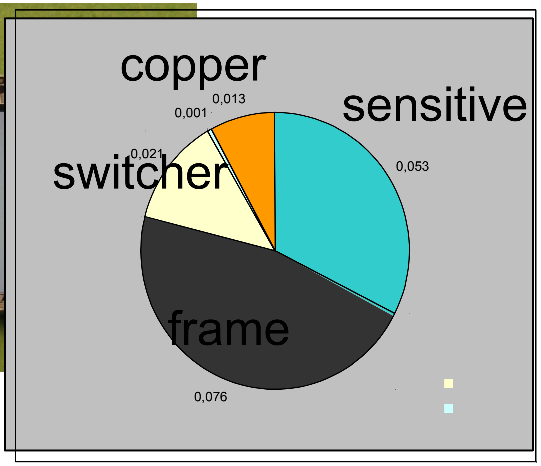
Double sided ladder with SiC foam support
2010: 2x6 MIMOSA-26, 0.65% X_0
2011: 2x6 MIMOSA-26, 0.4% X_0
2012: 2x6 optimized MIMOSA's, 0.3% X_0

Baudot/Goldstein/Gregor



Belle-II DEPFET sensors: 0.18 % X_0



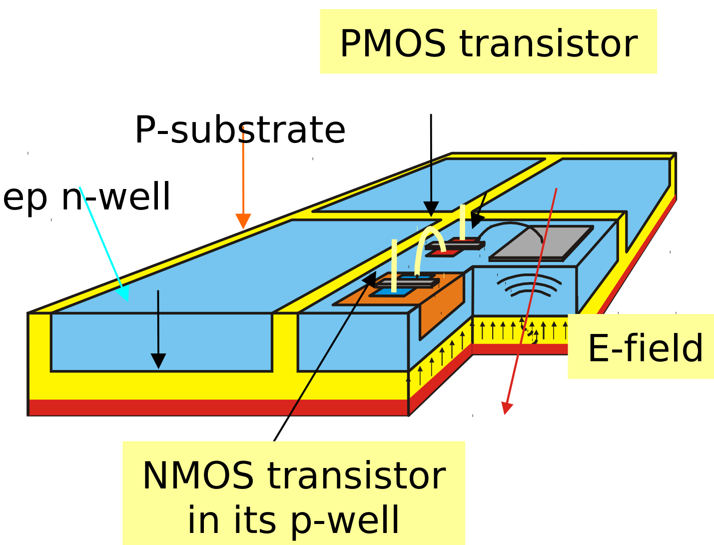


Promising technologies

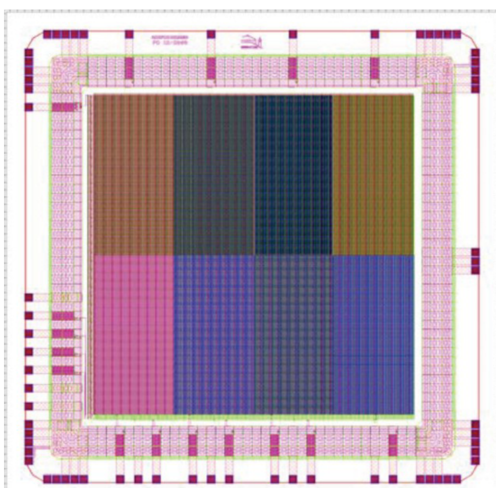
Many different flavours in the monolithic pixel family, with degrees of maturity ranges from “promising idea” to “ready to demonstrate ILC specs before 2012”

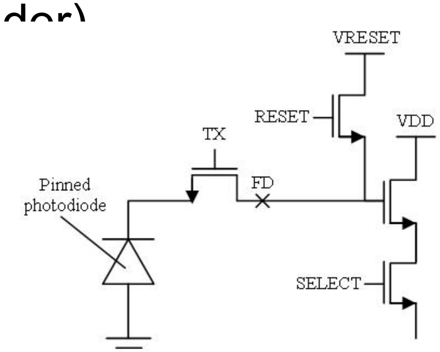
W. Snoeys, LePIX, 90 nm CMOS on moderate resisitivity substrate

HV CMOS pixels reach S/N~100, I. Peric



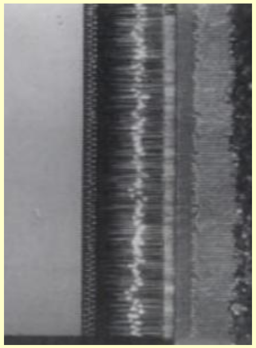
INMAPs pixels with 4T FE reach S/N~100, S. Worm (Spider)



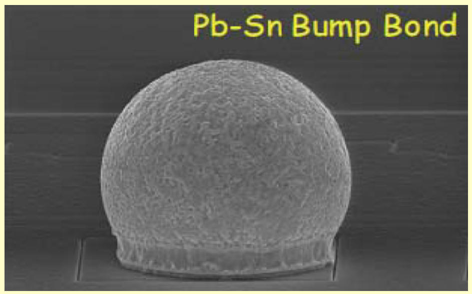


Preliminary results by M. Battaglia show SOI pixels are close to joining the “1 μm” club

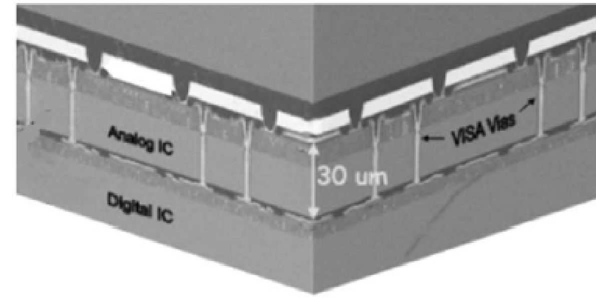
In the long run...



From 1D to 2D... (1990s)

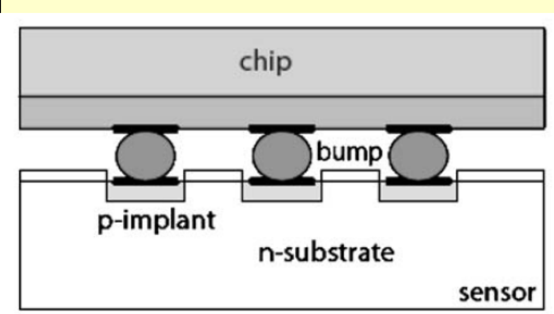


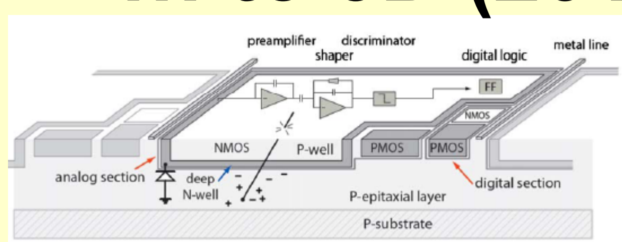
Coarse, bumps diameter is 10s of μm
(but, see talk by Sami Vaehaenen)

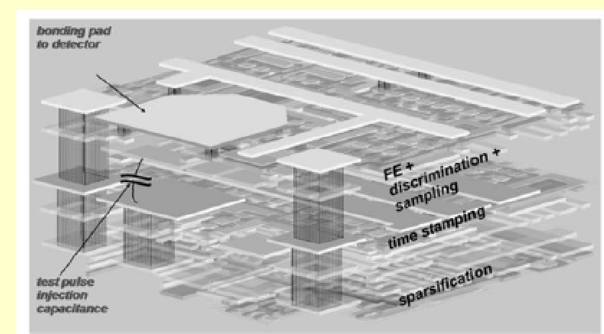


A reality in industry/research labs, but not yet quite in HEP...

… to 3D (2010s)





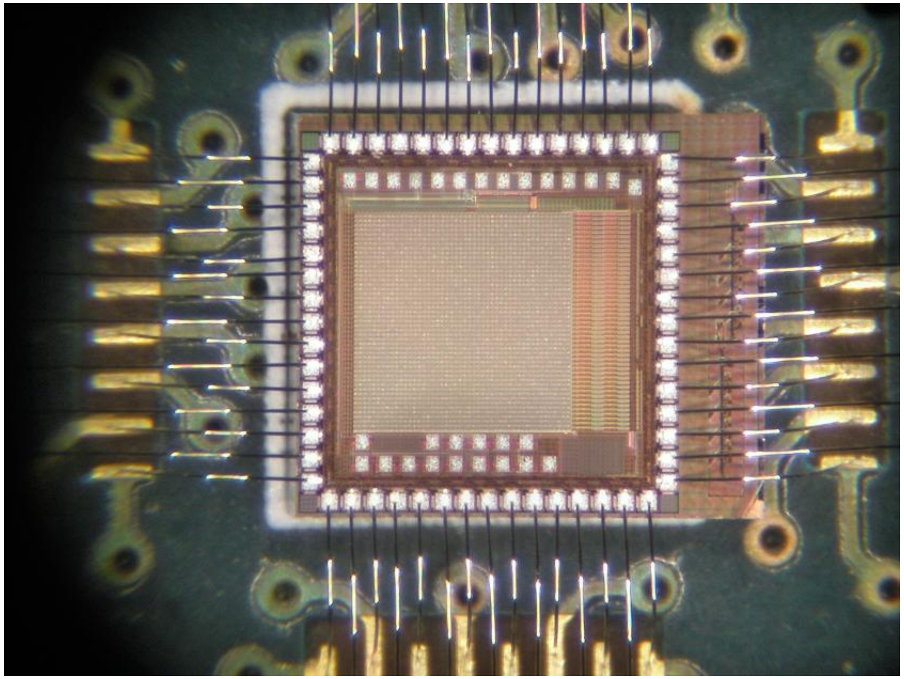


Sensor on “detector-grade” material. Coarse integration.

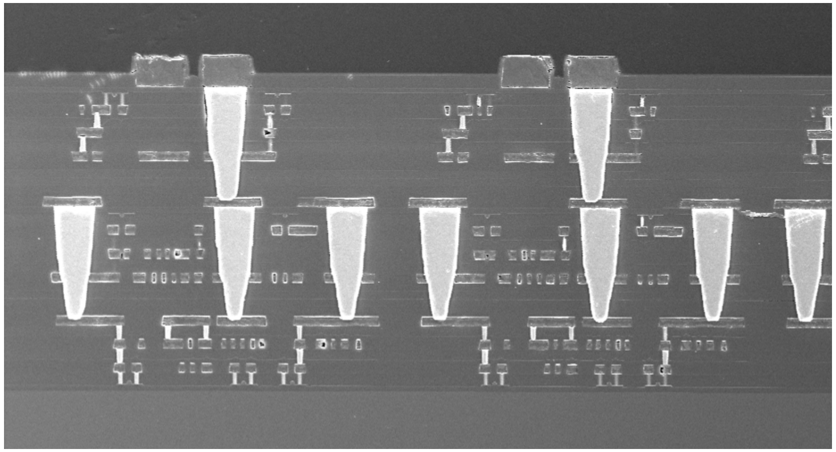
Put FE in sensor (APS, DEPFET) or sensor in FE (Monolithic APs)

More tiers. Finer integration

The future starts today...



progress of two lines (R&D process on SOI through MIT-LL) and commercial, “mainstream process” (Tezzaron/Chartered)



FNAL managed to build a working chip using vertical interconnects 2 years ago
Several other groups (INFN, Strasbourg) access MPW runs through 3DIC consortium FNAL
AIDA WP3 to serve as a platform to provide access to vertical interconnects in Europe
Revolutions come with a learning curve

Ron Lipton:
An established CMOS process is preferable to the MIT-LL process which is run on an R&D line. Development of the Tezzaron process and multiproject run has been a “learning experience” […]

Summary of the summary

Detector R&D for tracking/vertexing at the next energy-frontier experiment remains a very active field. Some success applying formulae to deal with lack of funding, varying from "generic R&D" to building detectors for intermediate time-scale projects (but also loosing time/missing some very good opportunities!).

Detector R&D is successful in improving the performance

- unprecedented S/N (i.e. 10-20 electrons noise in monolithic pixel detectors)
- increased functionality (smarter detectors output less data)
- reduced material (integrated PA, much of the monolithic pixel developments)

TRK/VTX R&D for LC becomes more coordinated; discussed DAQ (talk by E. Corrin, EUDAQ) and TB plans (better coordination of requests, the 2012 gap, M. Winter)

We have reached the point where we can be quite confident that ILC-grade demonstrators will exist soon.