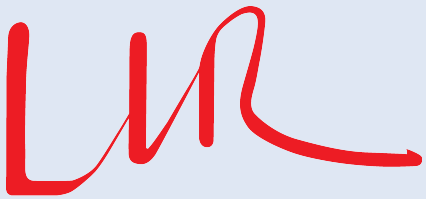
DAQ summary

Vincent Boudry
LLR, École polytechnique



IWLC'2010
CICG, Geneva
20/10/2010

DAQ activities

- Front-end electronics
  - Addressed in specifics talks
    ... or deeply embedded...
- DAQs for beams tests
  - Many systems
  - Integration to be started.... AIDA
    - VTX : EUDAQ (EUDET DAQ for the telescope)
    - Calo: CALICE DAQv2 (digital readout of technological prototypes of CALICE)
    - FCAL
    - LC TPC
    - SiLC
- Large Detectors
  - ILD
  - SiD
  - CLIC options (not yet)

"Virtual DAQ session"
Many scaterred talks (~25) in :
ECFA parallel sessions:
VTX, Tracker, Calo
+ AIDA DAQ working session
+ 1 discussion in VTX session

Thanks to G. Eckerlin

Selection for mainstream
Apologies for forgotten R&D

- Individual TB → technological prototypes
- Combined TB

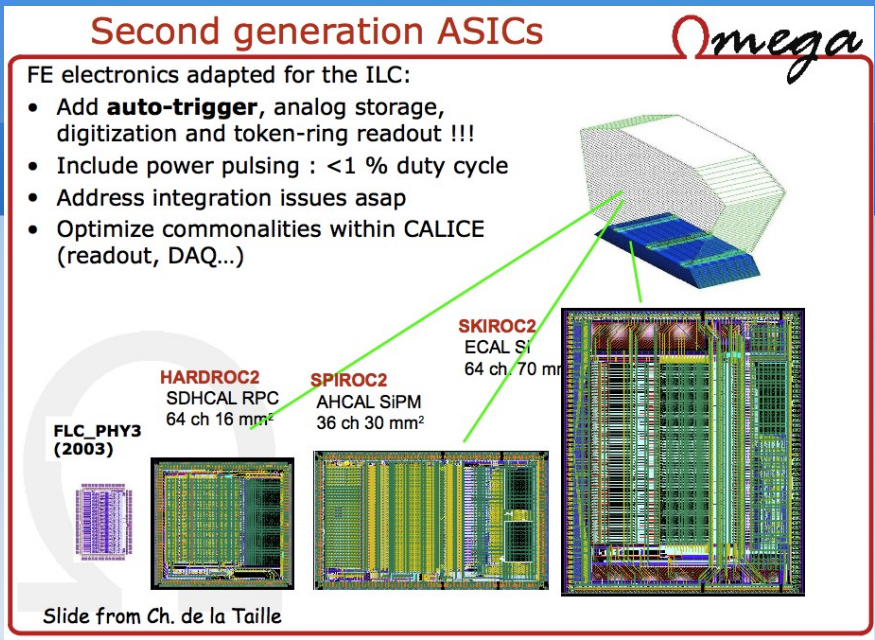
CALO Readout ASICs

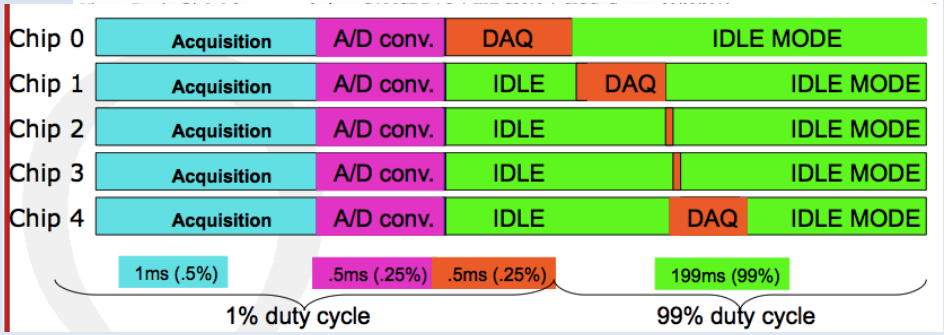
CALICE

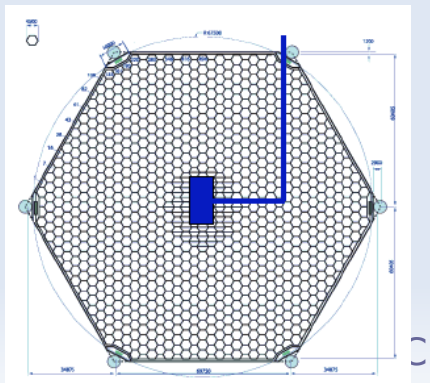
- Omega *ROC chips [CALICE]
  - SPIROC (36 ch SiPM AHCAL)
  - SKYROC2 (64 ch Si-W / ECAL)
  - HARDROC (64 ch SDHCAL RPC)
  - MICROROC (64 ch SDHCAL µMegas or GEM)
- FNAL & ANL DCAL chips
  - DCALv8 (64 ch RPC & GEM DHCAL)
- SLAC KPiX chips
  - KPiXv7 64 ch
  - KPiXv9 512 ch

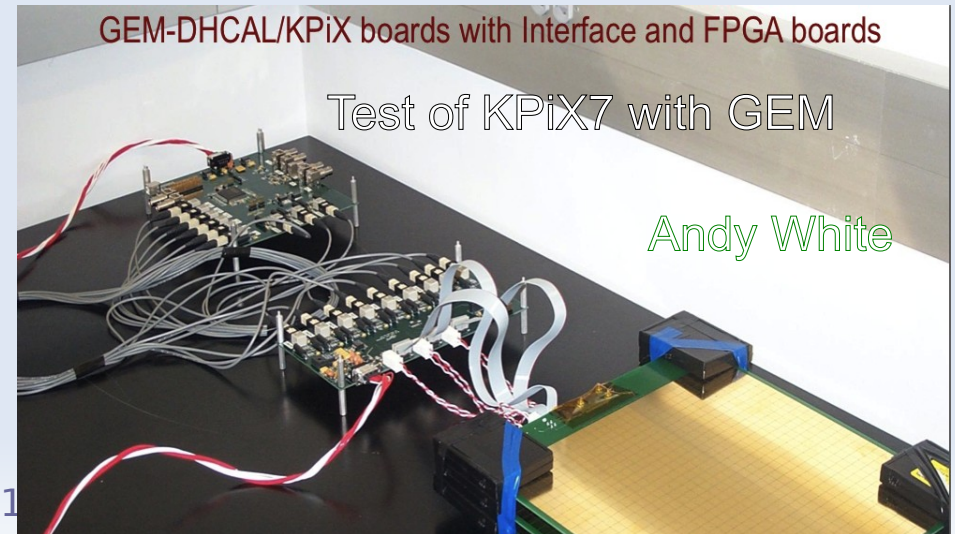
    → 1024 ch

- SiD Si-W ECAL
- GEM DHCAL
- SiD tracking
- SiD Muons





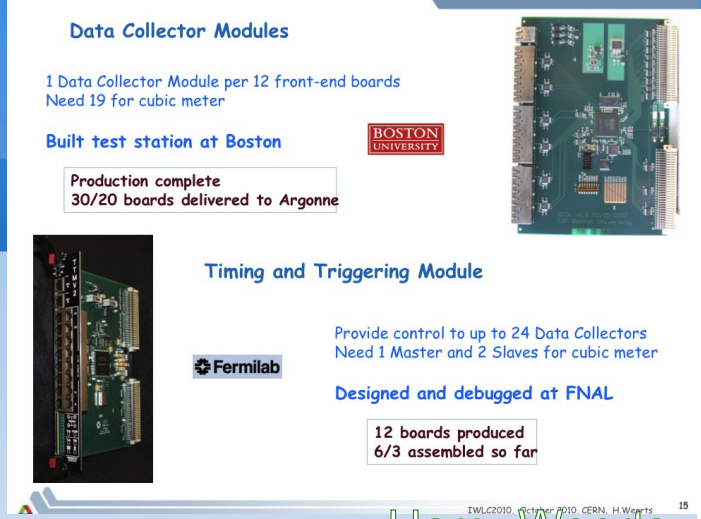


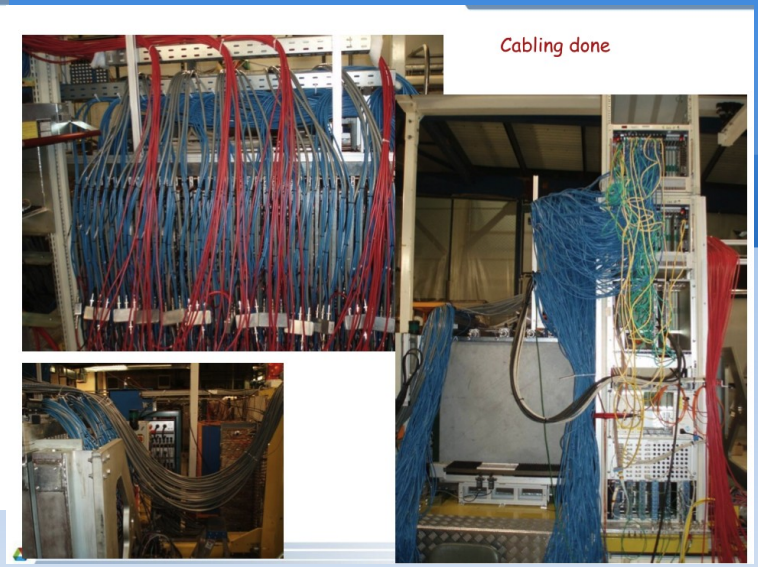


CALICE DAQs

Analogue version DAQv1

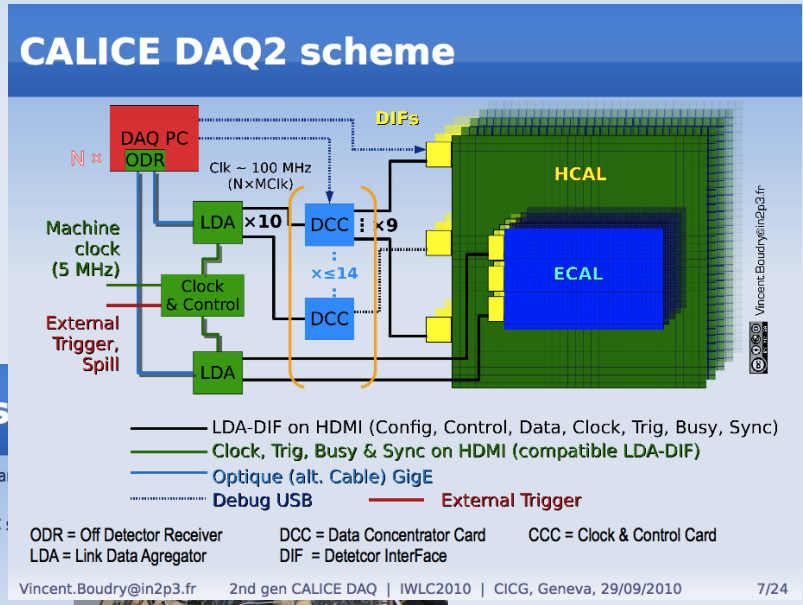
- Used for ECAL, AHCAL, TCMT combined test since 2006...
- In use for 1 m³ DHCAL prototype cosmics & TB @ FNAL
  - With specific cards + r/o of ~5000 DCAL chips
    - ~400 000 channels!
- In use for W-HCAL TB @ CERN
  - AHCAL + µMegas

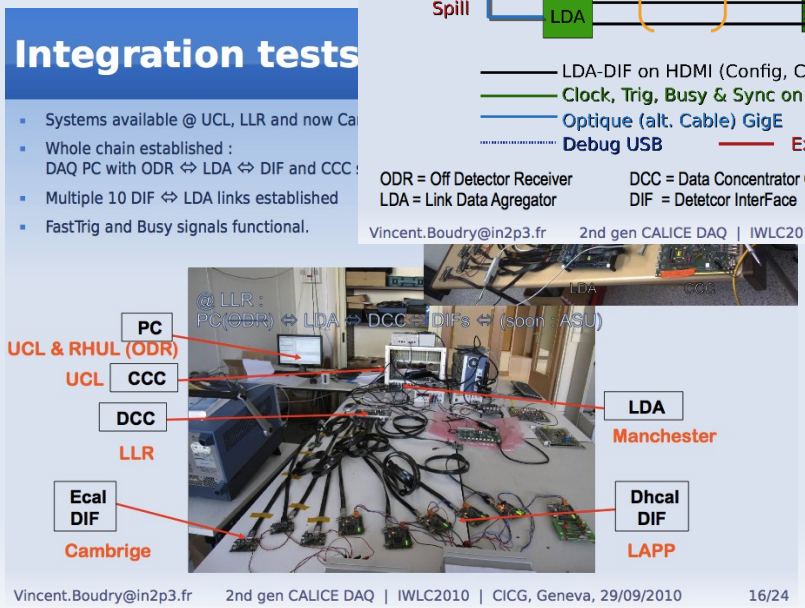




Digital version DAQv2

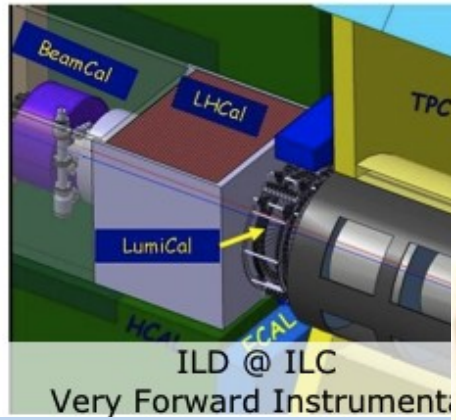
- for the technological prototypes
- Tree topology
- SW framework = XDAQ
- Ready → end 2010.
  - Extensive TB in 2011

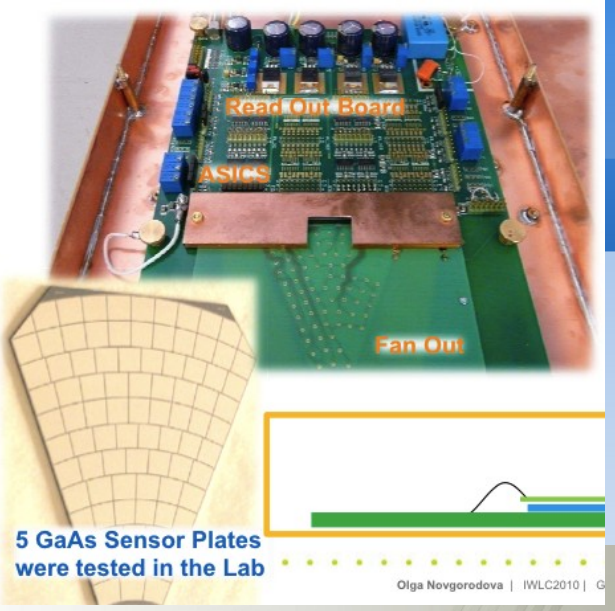




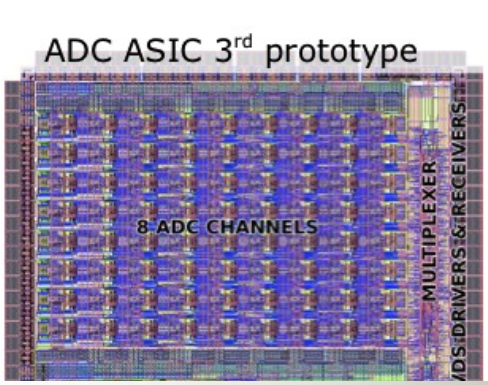
FCAL

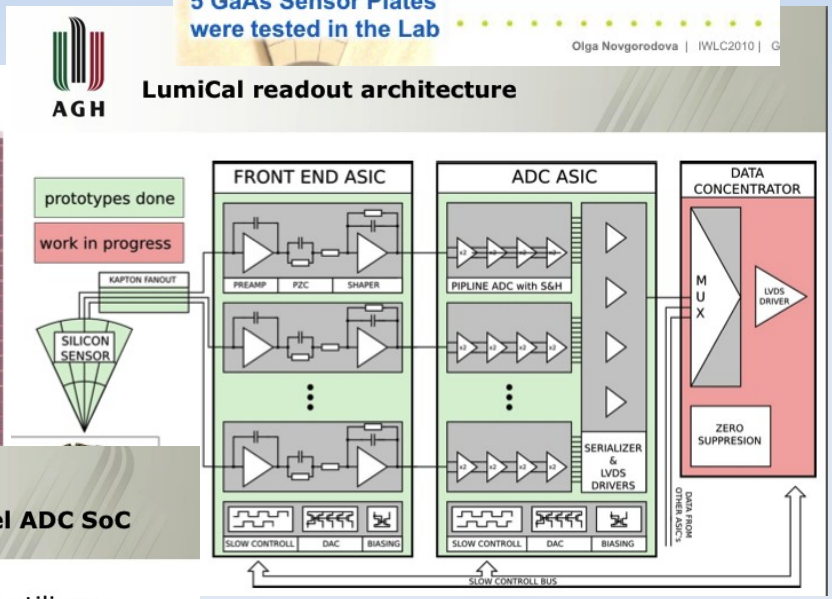
Olga Novgorodova; Szymon Kulis

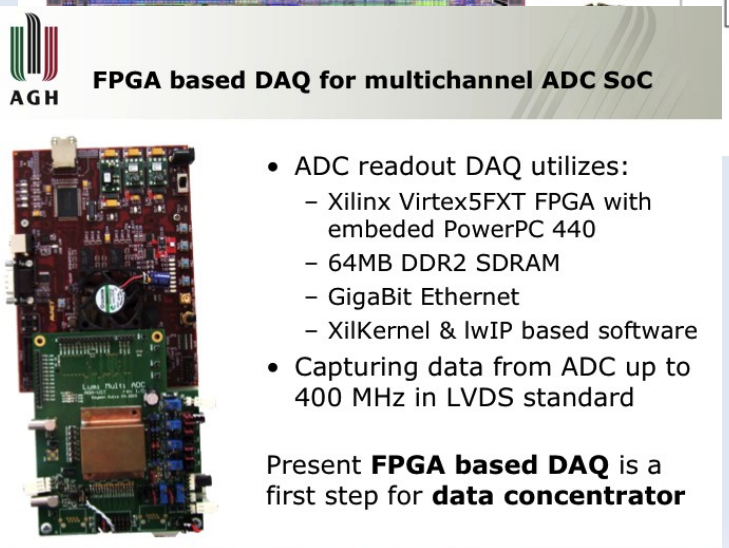




- FE electronics
  - GaAs (BeamCal)
  - Si (LumiCal)
- 2 prototype ADCs (10bit ; ~ 8mW / MHz)
  - 3 prototypes en route
  - EUDET
- Multi-ch ADC SoC (AGH)
  - 8 ch
  - 1 GHz LVDS driver
- Readout
  - ZEUS telescope for TB
  - CALICE DAQ later ?



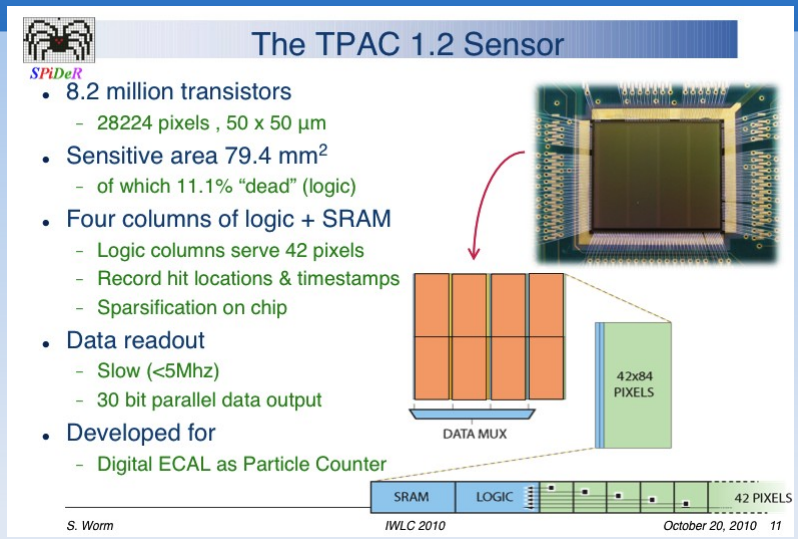




Spider (Silicon Pixel Detector R&D)

Steven Worm (RAL)

- "MAPS"
  → Calo (DECAL) & tracker (CHERWELL/2)
- TPAC SENSOR
  - 28K Pixels 50×50 µm²
  - R/O @ 5 MHz, 30 bits in //
  - Readout by custom HW
    + EUDAQ
    - Funding...



VTX FPCCD readout

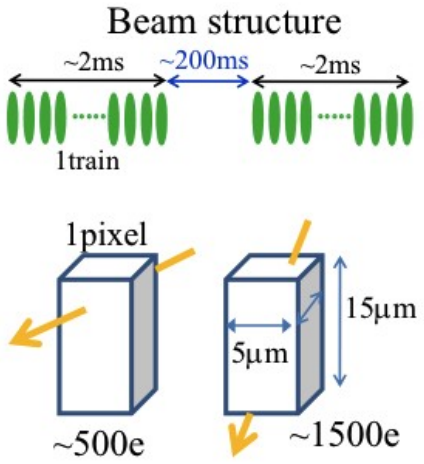
Tomoyuki Saito (Tohoku U.)

- FPCCD (Fine Pixel CCD): 5µm× 5µm

- ILC compatible readout chip designed & tested
- Low noise ✔
- Readout speed → in next vers.

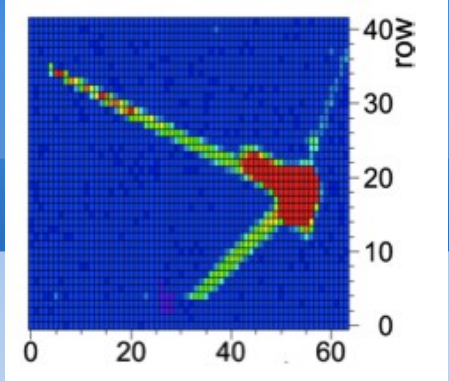
Requirements for FPCCD

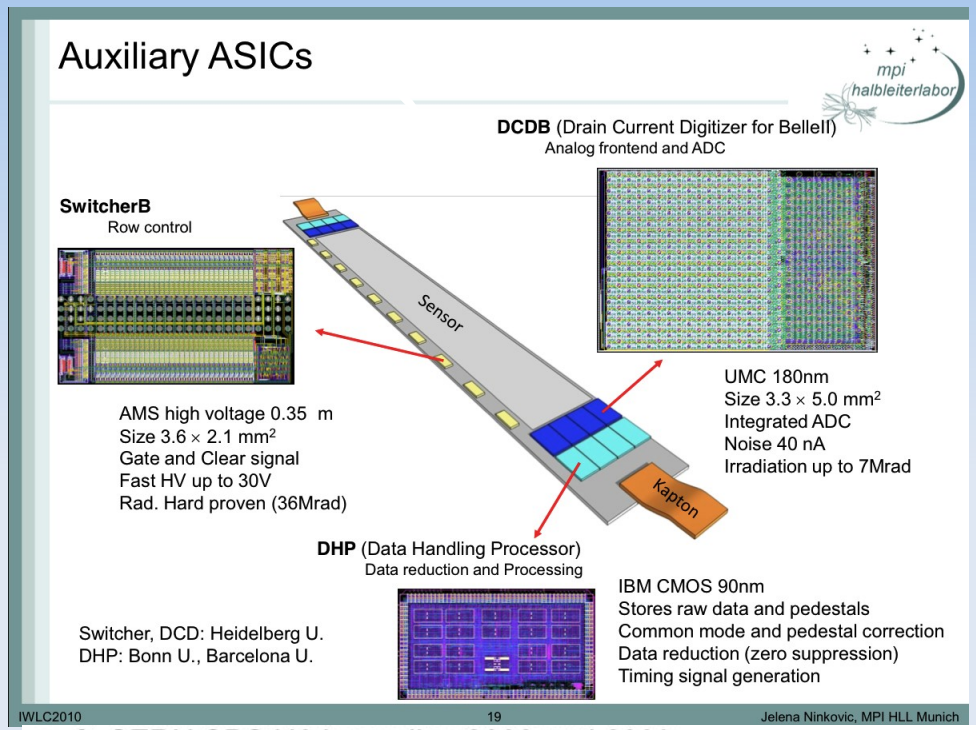
- Readout speed > 10Mpix/s
  - ☛ All pixels is read out in the inter-train time.
- Noise level < 50 electrons
  - ☛ Signal level is ~500e.
- Power Consumption < 100 W (16mW/ch)
  - ☛ VTX is put in cryostat.



VTX: DEPFET collaboration

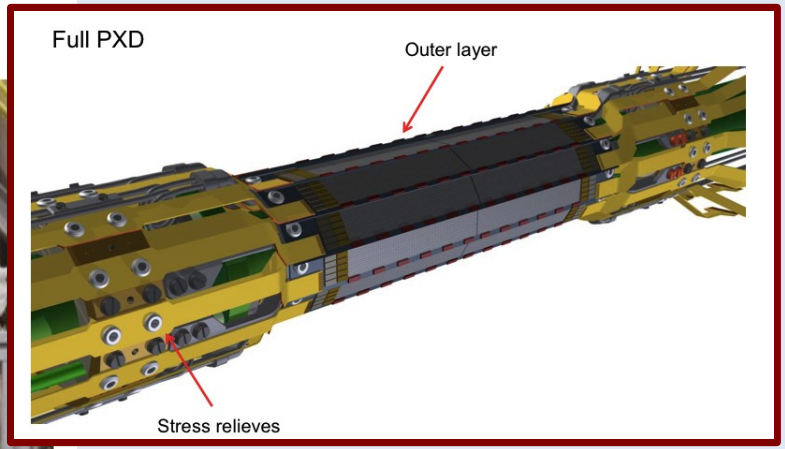
Jelena Ninkovic *for the DEPFET Collaboration (www.depfet.org)*





- DEPFET collaboration
- Build for PXD for Belle-II
- Uses “auxiliary ASICs”
- **Has a WP on DAQ**
  (not described here)
- Many technique applicable for LC.

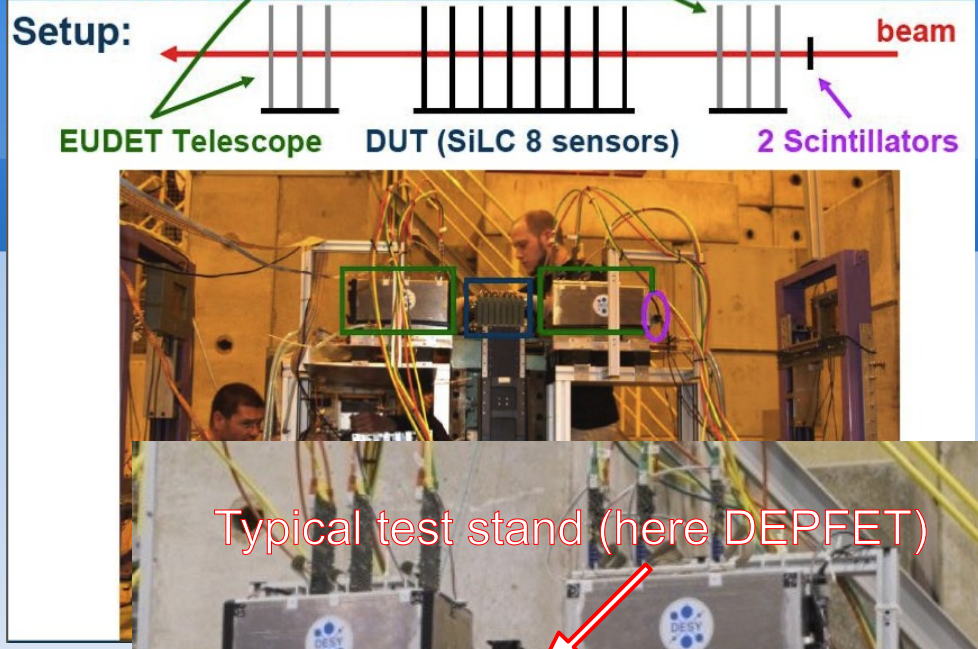
- → CERN SPS H6 beam line 2008 and 2009
- stand alone DEPFET telescope and integration as a DUT in the EUDET telescope

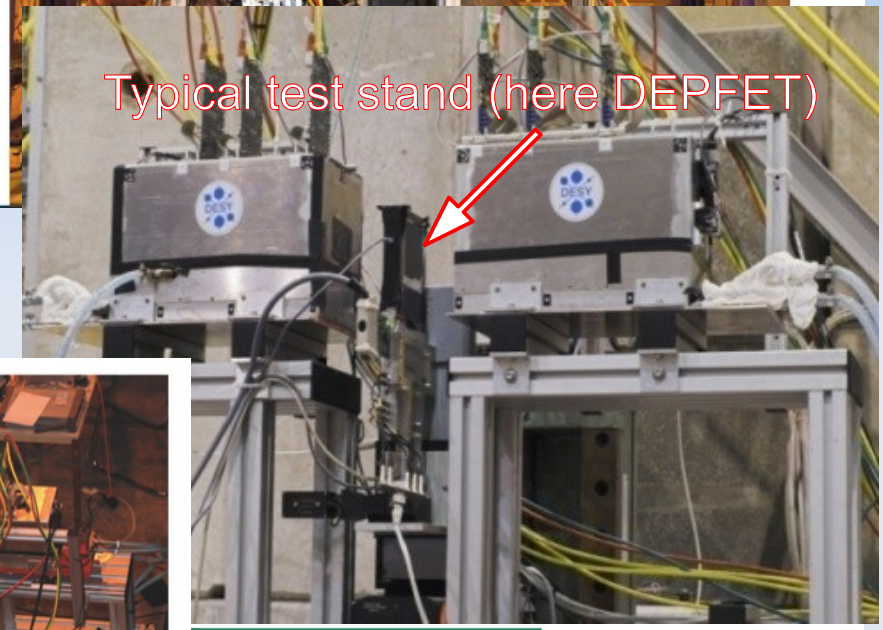


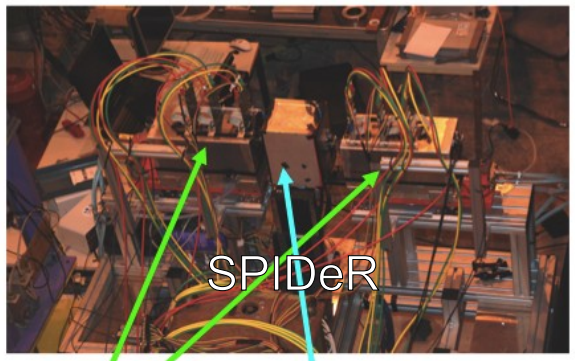
EUDAQ

Emlyn Corrin (U. Geneva)

- a DAQ for EUDET telescope + *YourDevice*
  - Readout of Mimosa [IPHC] sensors
    - V22, 26,
  - Plus plug-in for in test devices
    - Many (≥29) user groups: Calorimeters, DEPFET chips, …
    - Data collector as plug-in
- Nearing EUDET completion
  - Stability & Usability
  - User manuel
- Future:
  - Monitoring via plug-ins
  - JTAG Programming Sensors
  - Better Data Collector
  - …







Emlyn Corrin, EUDET Annual Meeting, Hamburg, 29 Sept 2010 FACULTÉ DES SCIENCES UNIVERSITÉ DE GENÈVE

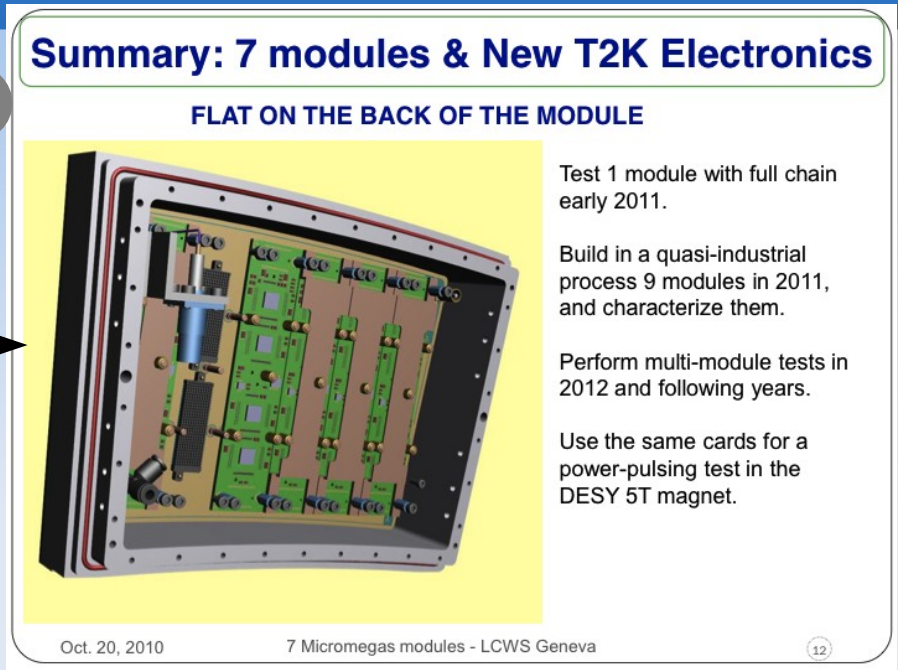
User Manual

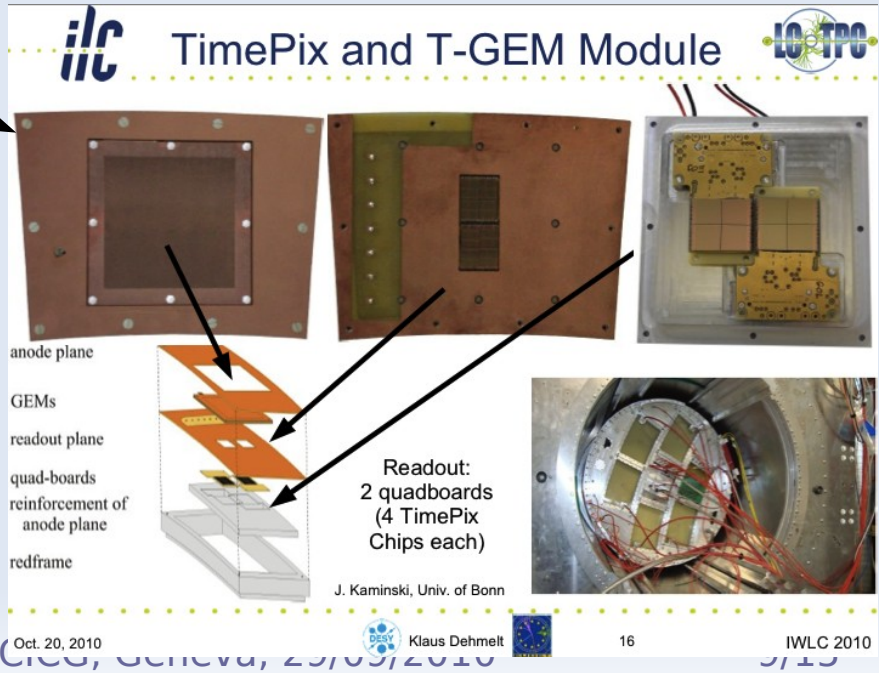
- Finished (at last) early this year
- Recommended reading for anyone interested in EUDAQ
- EUDET Memo 2010-01
- http://www.eudet.org/e26/e28/e86887/e86890/EUDET-Memo-2010-01.pdf

LC TPC Front-End readout

3 different DAQs

- 3 existing readout ASICs
  - T2K AFTER chip (Saclay)
    - 5 modules µMegas
    - On going: 7 modules in Large MicroMegas TPC with better integrated electronics
  - ALTRO (EUDET, Lund, CERN) : 16 ch
    - 3 modules “Double JGEM”
  - TimePix (EUDET)
    - Triple GEM
- In devt
  - S-Altro16 demonstrator chip (P. Aspell): 16 ch, “100µs @ 10 MHz” for ILC & CLIC→ end 2010
    - → S-Altro 64 for GEM & µMegas [in AIDA]
  - Timepix2 (X.Llopart) → end 2011
    - HEP & non-HEP; 256×256 array; 1.5 ns resol
  - LePix (W. Snoeys): ⊃ detector and readout: proof of principle in 2011 ?
    - Submicron CMOS (speed, rad hard, cost, low W, ...)





SiLC

A. Savoy-Navarro (LPNHE)
A. Charpy

- Front-End readout chip
  - 2 existing
  - 1 in dev spec. for ILC
  - Reflexion for CLIC
- DAQ HW:
  - DAQ Hardware ToolKit (part of EUDET)
- DAQ SW: NARVAL for new ASICs
  - ADA + C/C++

F.E.E. General description

Baseline: Full readout chain integrated in one chip developed in two steps

EUDET BASELINE
- Preamp-shaper
- Sparsification analogue sums : Trigger decision on
- Sampling pipe-line : 8-deep sampling analogue
- Analogue event buffering: : Occupancy: 8 deep event buffer
- On-chip digitization : 8-bit ADC
- Calibration and calibration management

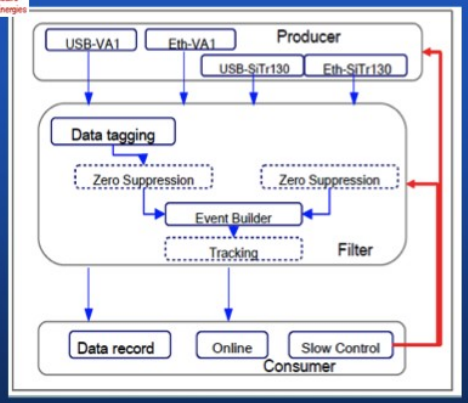
BEYOND
- *Full digital handling of the chip running operation*
- *Power switching (ILC duty cycle)*
- *Fault tolerance*

In addition: two "conventional" FE ASIC: VA1' and APV25

Developed up to now: the ILC case (slow machine) starting the work on the fast cycle case (see later)

DAQ software (new for new FEE readout system)

LPNHE Laboratoire de Physique Nucléaire et des Hautes Energies

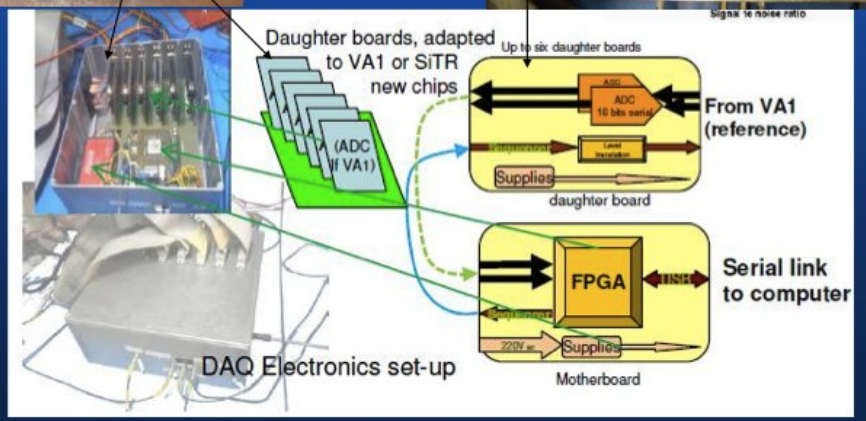


NARVAL:
- o Distributed DAQ written in ADA language
- o Divide the acquisition into activities called actors (ADA)
- o 3 basic actors:
  - Producers
  - Filters
  - Consumers
- o Dedicated Libraries in C/C++/ADA
- o High Flexibility with very simple scripts & xml files

2 other DAQ lines used by SiLC based on system were developed by other experiments (synergy)
- **APV25 based** => hardware & software developed forCMS & also BELLE application.
- **ALIBAVA** developed by Liverpool, CNM-Barcelone and IFIC Valencia (ATLAS et al..)

DAQ Electronics

VA1' ASIC used as reference devices



DAQ Electronics set-up

DAQ merging in AIDA (FP7)

- Combined beam tests ≥ 2013
  - VTX + TPC + SiTR + FCAL and/or CALOs
  - AIDA DAQ session + discussion on VTX session
- "merge" of
  - EUDAQ
  - CALICE DAQv2
- Interface the others
- Extend functionalities
  - EUDAQ TLU2
  - Beam Interface (HW and **SW**)
    - **CERN, DESY**
  - Speed
    - ACTA testing
    - FW Event Builder

• Exercise for large detectors (ILD)
• Synergies (manpower is scarce)

WP8.6.2: Common DAQ for combined TB

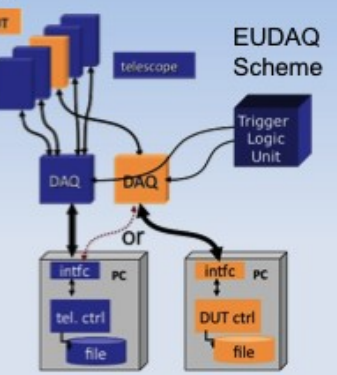
Task leader: V Boudry (LLR), E. Corrin (U. Geneva)

Provide a uniform control and acquisition framework allowing for the integration of most ILC R&D components in a combined beam test

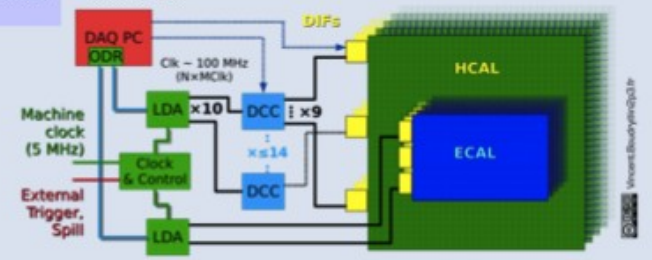
Main components are
- EUDET telescope
- CALICE prototypes
- FCAL calorimeters
- Silicon trackers
- TPC readout units

Deliverables :
T0+20 : specification documents (common interfaces/infrastructure To LC beam tests
T0+46 : Report on performance & use in beam test

The integration will includes SW and HW (sync) components and the beam line Interfaces based on EUDAQ and CALICE DAQv2.



CALICE Scheme

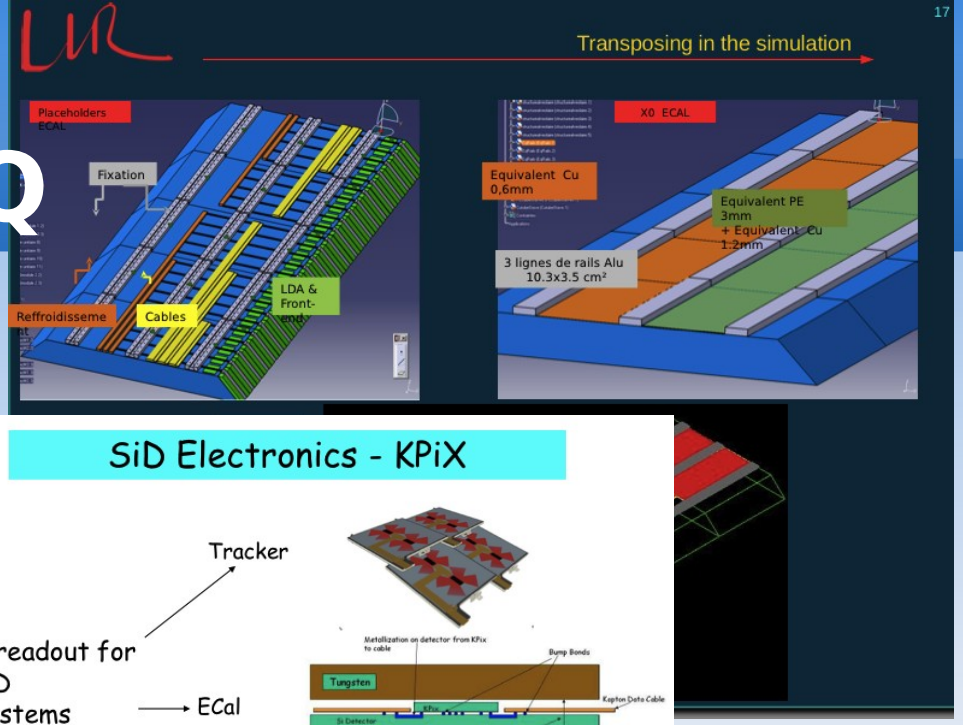


EUDAQ Trigger and Logic Unit

Main users: all devices needing integrated tests
WP9.5 (set-up for High Granular Calorimeters)

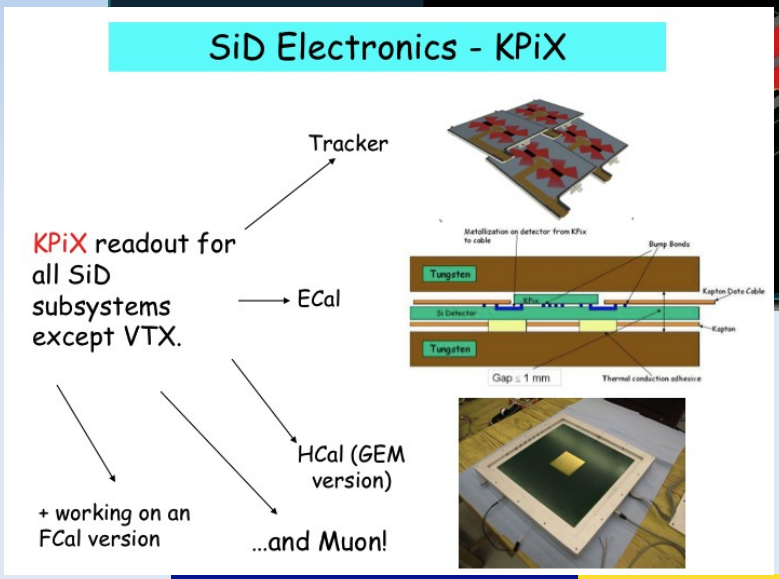
Vincent. | CERN (and elsewhere) 15

Experiments
FE integration & DAQ



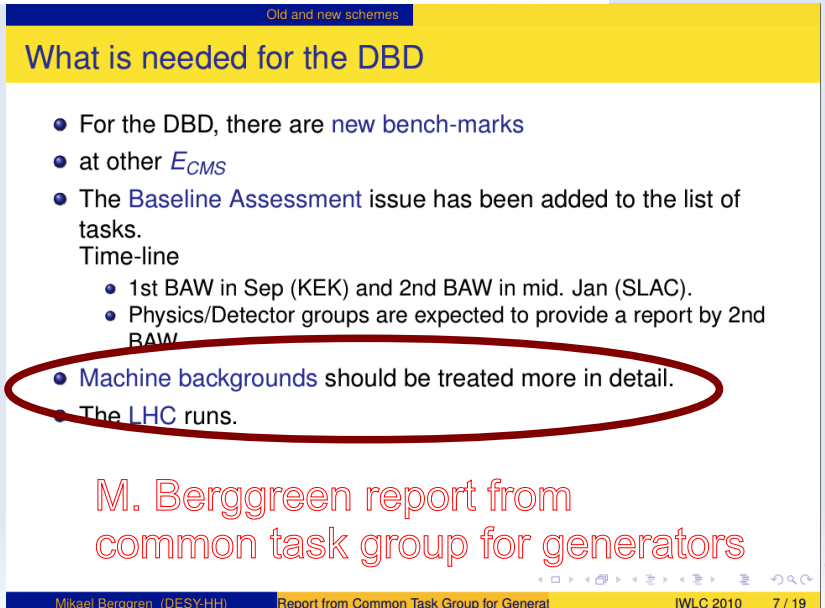
DAQ Front-End integration

- ILD
  - Calo well advanced (easiest ?)
  - SiLC → scheme in progress
  - LC TPC in progress during the last months (FE integration)
  - VTX (& FCAL) needs efforts
- SiD (personal impression)
  - (almost) Achieved VFE grand unification!!
  - R&D going on but integration needs efforts



Rate estimations

- Waiting for updated physics, machine and beam background
- Work on-going (for the DBD and CLIC CDR)



Lessons from CMS

Duccio Abbaneo (CERN)

- FE system
  - Hard coded ID → channel mis-ID ↘
  - Aim “spatial” quality
  - Discussion:
    - Optical links “perfect”
- Continuous data checking (10Mch)
- Connectivity is devil!!!
  - More integration ↔ Less flexibility ?
- Lot of lessons!!!
  - No more ring !!
    - Chip And Connection reliability
  - More slow control !!!
    - Never enough data O(10^5)

Reminder: ILD & SiD ~ 10^8 channels
Self triggering embedded electronics with local memory → uncontrolled electronics as good as dead

Beware of low-tech stuff

- High-tech stuff (silicon sensors, microelectronics, optoelectronics…) is appealing and receives a lot of attention
- A lot of problems come from low-tech stuff
  - For the CMS TK:
    - Problems during production of FE hybrids and several PCBs
    - Most of missing channels come from
      - Faulty electrical connections
      - Leaking cooling pipes
- Anything that goes into the detector requires a high level of attention
  - Design, evaluation of components, even R&D
  - Strict quality control during production

Connectivity vs integration

- Connectivity is the devil
  - Connections are by far the major source of lost channels
  - A functional test is in most cases not enough
    - And it is in most cases all what can be done…
    - Expect to loose channels later
- Connectivity in a complex architecture is a bigger devil
  - E.g. the ring architecture of our controls
    - Despite the “redundancy” (option to skip a faulty node)
  - No more “rings” in the upgrade
    - Ring architecture abandoned for controls
    - DC-DC converters preferred over serial powering
- A more integrated design can be the cure
  - But much less flexibility to implement solutions late in the game
  - More emphasis on early “system testing”
    - Need to freeze the system design earlier
    - Reduce opportunities to profit from late developments

10/21/2010 D. Abbaneo 53

Spy channel

- Provides direct access to the front-end raw data stream for a fraction of events during normal data taking (physics runs)
- Snapshots of events at ~ 0.3 Hz
- Full information available: raw data from all 9 M channels
- Used to monitor calibration under real conditions
- “Goldmine of possibilities for monitoring and debugging”

Conclusions

- Many R&D on sensors and associated Front-End readout
  - Merging in ASICs + FPGA for readout
  - Most adapted or ILC; Some work started for the CLIC conditions
- DAQs
  - EUDAQ for many VTX test (but not only): big success!!
  - CALICE DAQv1 & v2 → ~½ Mch
  - Manpower is scarce for online SW
    - Synergy needs action
  - Merging of (mostly ILD) DAQ in AIDA
    - EUDET + CALICE DAQ + … → devt of utilities (↔ machine interface)
    - “exercise” for HW & SW integration of ILD
- Large detectors
  - CMS: “Think very high reliability (almost spatial) & precise monitoring”
  - Update numbers (main uncertainty : machine bgd)

R&D test beams with add-hoc systems

UCSC, LBNL, CERN collab KEK and SOIPIX collab

SiD VTX: Chronopix

Specifications:

Detector sensitivity
10 μV/e (eq. to 16 fF)
Detector noise
25 electrons
Comparator accuracy
0.2 mV rms (cal in each pixel)
Memory/pixel
2 x 14 (will be 4 x 14)
Designed for scalability
eg. No caps in signal paths
Provisionally use limited pixel active area
use processes without deep-p well

Status: First prototype (SARNOFF) tested, validates general concept, but improvements needed.

Second prototype: February 2011 after more design evolution and simulation – changes agreed with Sarnoff.

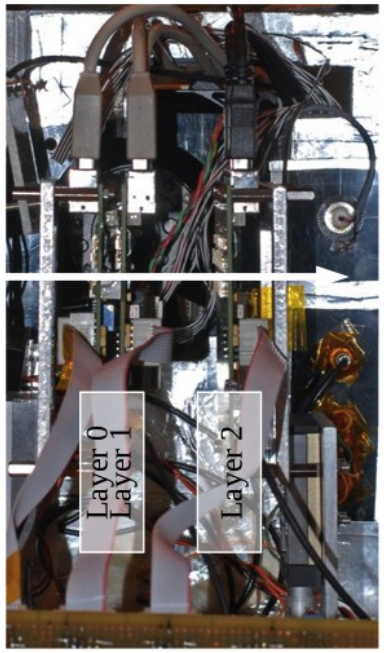
General idea (Sarnoff): get rid of n-wells absorbing signal electrons; build all electronics inside pixel only from nmos transistors sitting in shallow p-wells.

Oregon, Yale

Marco Battaglia

Tracking with Monolithic Pixel Sensors in SOI Technology

CERN Beam Test Setup



Beam test at SPS on H4 with 200 GeV π- at beginning of September 2010;

Small telescope made of three planes of SOImager2 to study charge collection, single point resolution and efficiency as function of depletion voltage, one plane mounted on motorised rotation stage to study charge collection for inclined tracks;

Data acquisition performed using custom ADC+FPGA board, online cluster search using ROOT-based COOL program, tuple output converted to lcio, offline analysis performed with custom processors in Marlin;

Readout at 12.5 MHz corresponding to ~1500 frames/spill, operation at constant temperature (20+/-1)°

LCIO output