The SiD Detector Concept

On behalf of the SiD Concept Group

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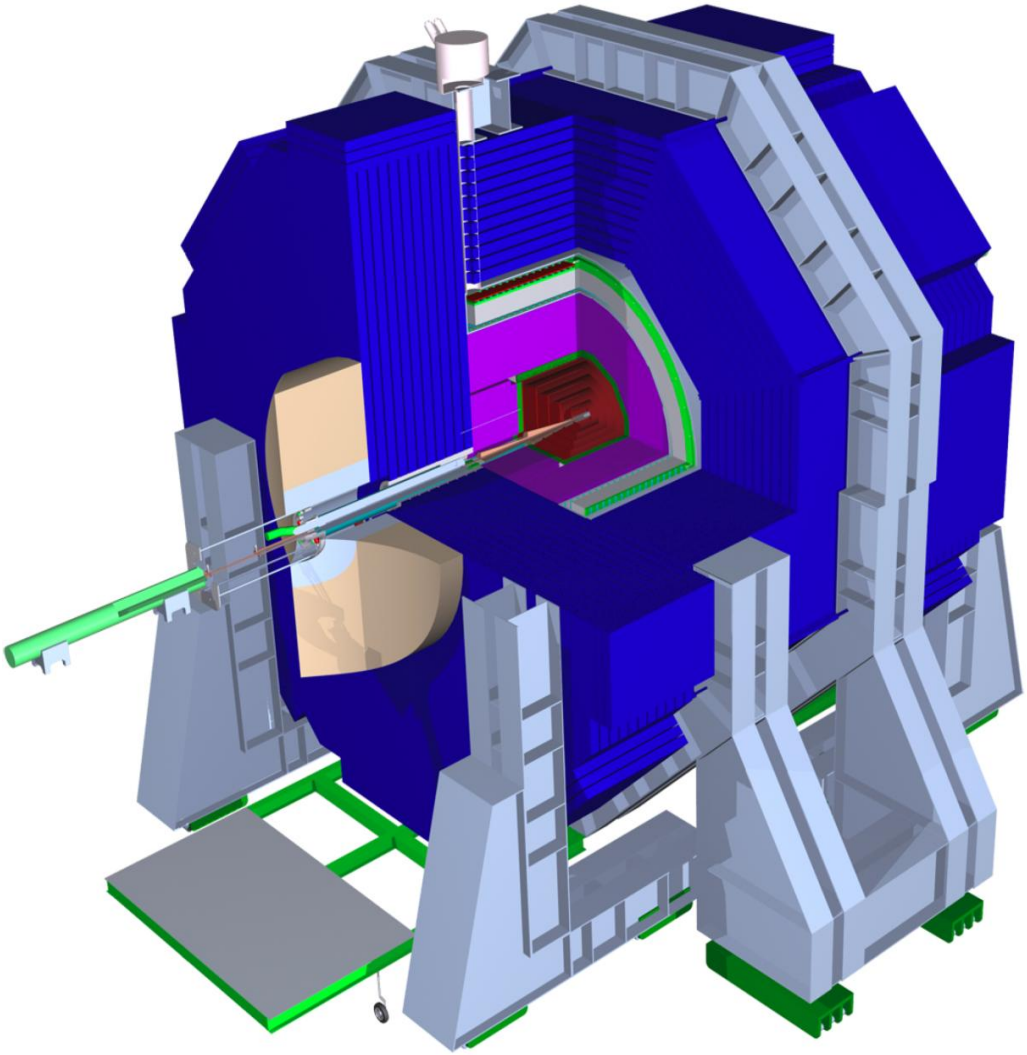
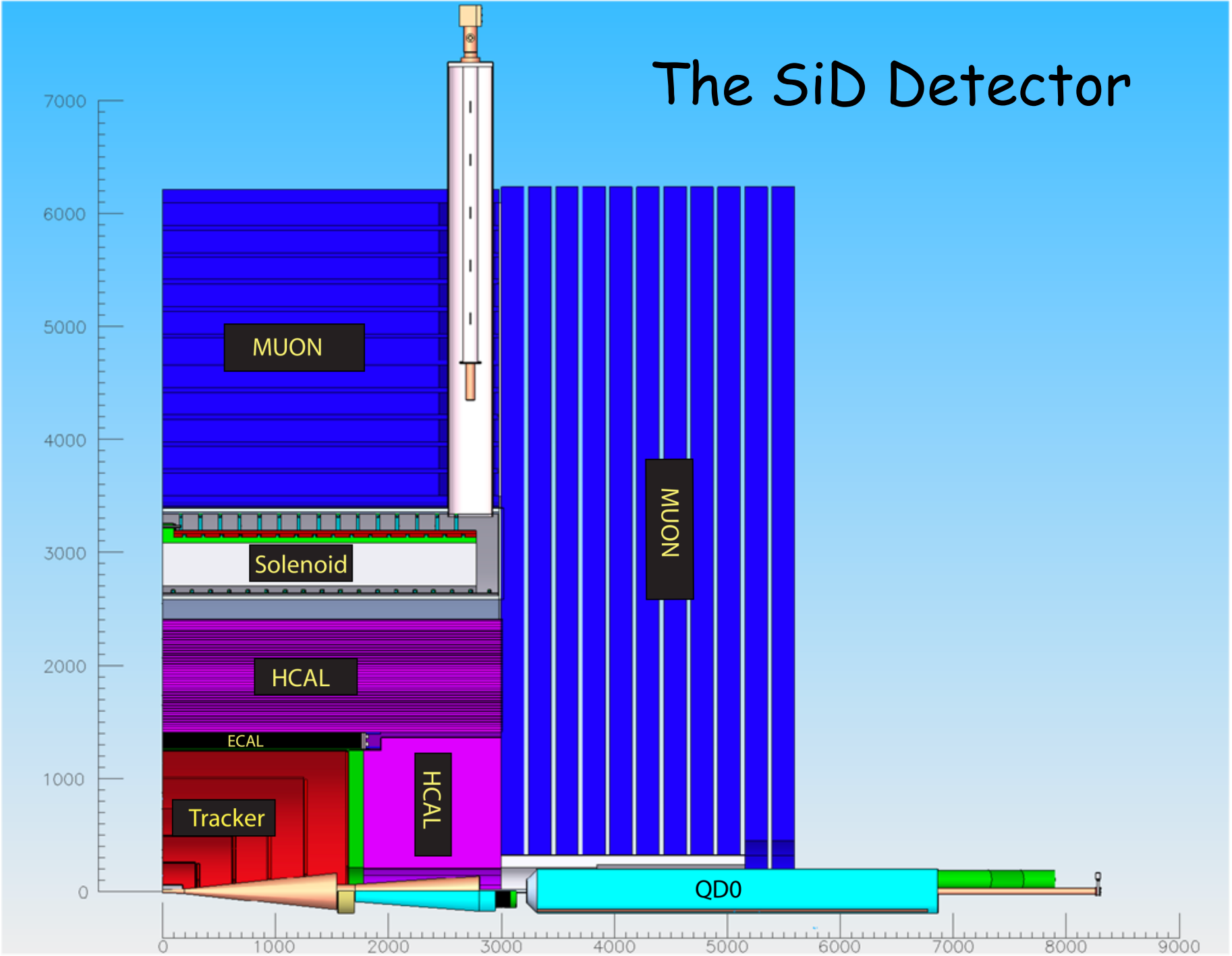
University of Texas at Arlington



Contents

- The SiD Detector design – an overview.
- The SiD Work Plan: from LOI to DBD in 2012.
- Developments in subsystems R&D including critical areas of R&D for SiD.

The SiD Detector



The SiD Design

A compact, cost-constrained detector designed to make precision measurements and be sensitive to a wide range of new phenomena.

-> Compact design with 5T field.

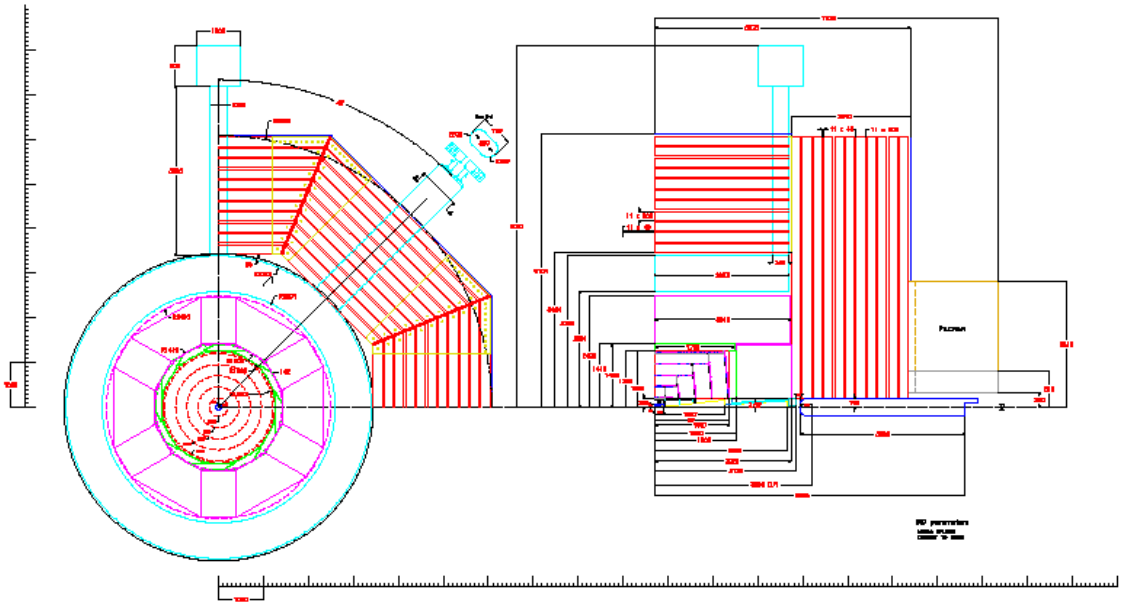
-> Robust silicon vertexing and tracking system – excellent momentum resolution, live for single bunch crossings.

-> Calorimetry optimized for jet energy resolution, based on a Particle Flow approach, "tracking calorimeters", compact showers in ECal, highly segmented (longitudinally and transversely) ECal and HCal.

-> Iron flux return/muon identifier – component of SiD self-shielding.

-> Detector is designed for rapid push-pull operation.

SiD Global Parameters



Detector	Technology	Radius (m)		Axial (z) (m)	
		Min	*Max*	*Min*	*Max*
Vertex Detector	Pixels	0.014	0.06		0.18
Central Tracking	Strips	0.206	1.25		1.607
Endcap Tracker	Strips	0.207	0.492	0.85	1.637
Barrel Ecal	Silicon-W	1.265	1.409		1.765
Endcap Ecal	Silicon-W	0.206	1.25	1.657	1.8
Barrel Hcal	RPCs	1.419	2.493		3.018
Endcap Hcal	RPCs	0.206	1.404	1.806	3.028
Coil	5 tesla	2.591	3.392		3.028
Barrel Iron	RPCs	3.442	6.082		3.033
Endcap Iron	RPCs	0.206	6.082	3.033	5.673

Kurt Krempetz/Marco Oriunno

The Path to 2012: SiD Work Plan

- Focus and goal for SiD is the Detailed Baseline Design of the Detector for 2012.

- The LOI was a significant milestone last year. Since then we have continued R&D and worked on the definition of a Work Plan for all subsystems until 2012.

- Status: ongoing work in all subsystems, but each on its own timeline – aiming for convergence by 2012, but it is clear that R&D will continue beyond this point.

- Developing more realistic detector description – folding in increasing realism in subsystem elements.

- Mutually beneficial interworking with CLIC detector group on SiD'

The Detailed Baseline Design

"DBD"

- Recognition by Research Director that LOI was a substantial milestone/result of a large body of work.

- We should not repeat the LOI within the DBD.

- DBD should "make a compelling case that detectors capable of fully exploiting the physics potential of the ILC are feasible, cost effective, and based on demonstrated detector technologies."

- Recognition that resources are/will be limited.
  e.g. select a few key benchmark processes,

The Detailed Baseline Design

"DBD"

From SiD Work Plan, Oct 2009:

"…doesn't attempt to produce full engineering designs of all the detector components, nor does it include production and testing of full detector prototypes. These are not imaginable with the present level of support. Rather it attempts to establish technical feasibility for key detector systems, conceptually engineered designs of detector subsystems, and proofs of principle of key engineering assumptions, in addition to an accurate rendition of detector and physics performance with a level of simulation detail previously unmatched in high energy physics proposals. "

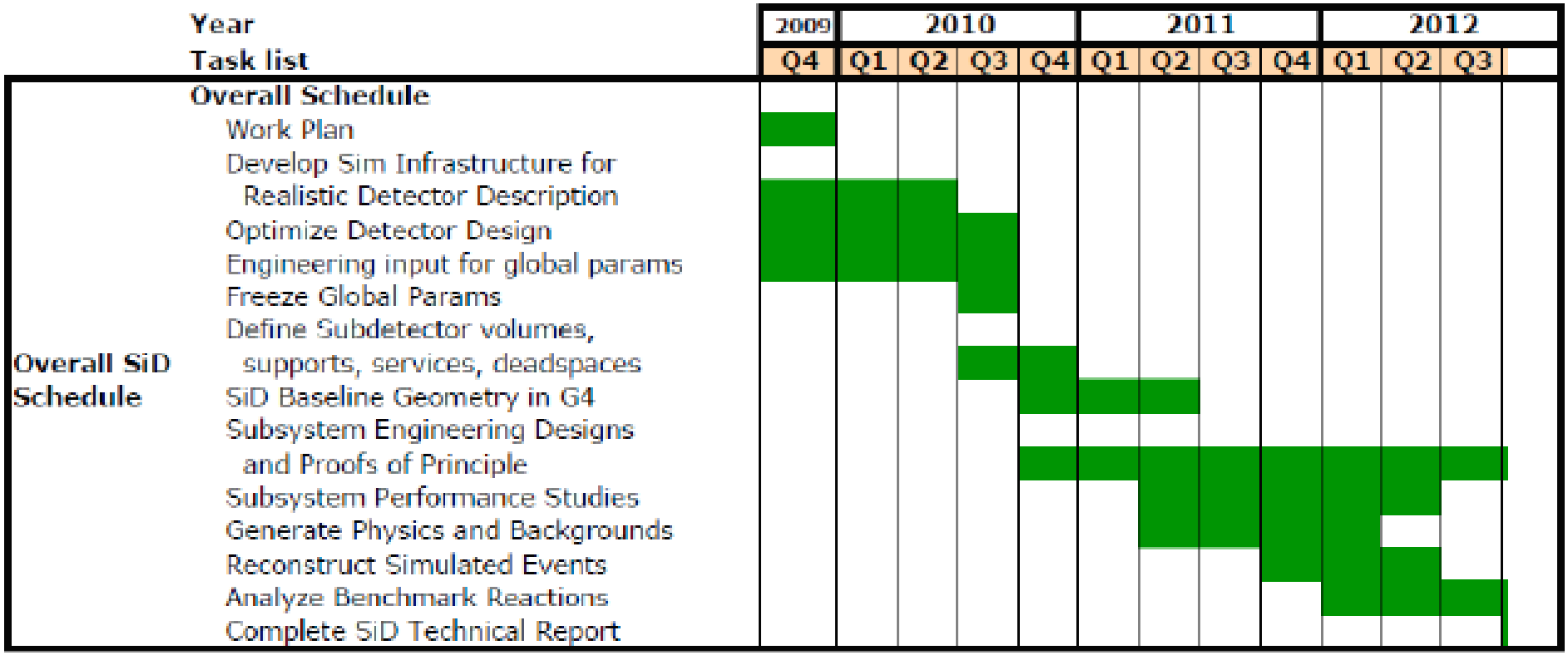
The Detailed Baseline Design

"DBD"

- Expect further discussions on DBD with RD and IDAG at this meeting.

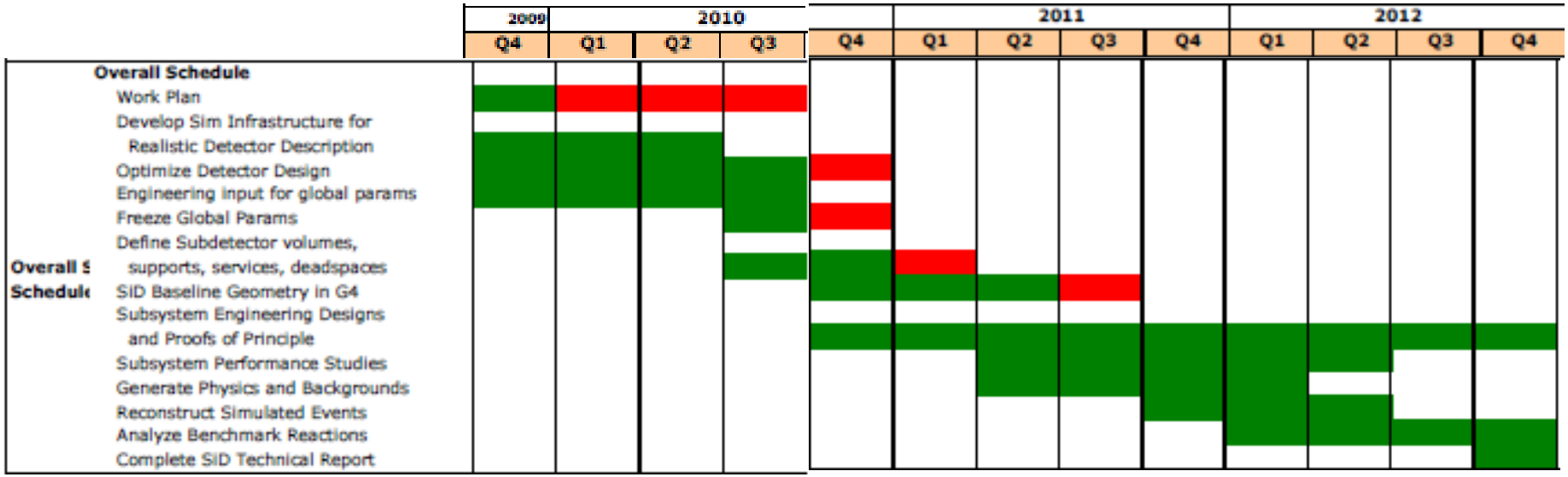
- Also with GDE on TDR + DBD package.

The Path to 2012: SiD Work Plan

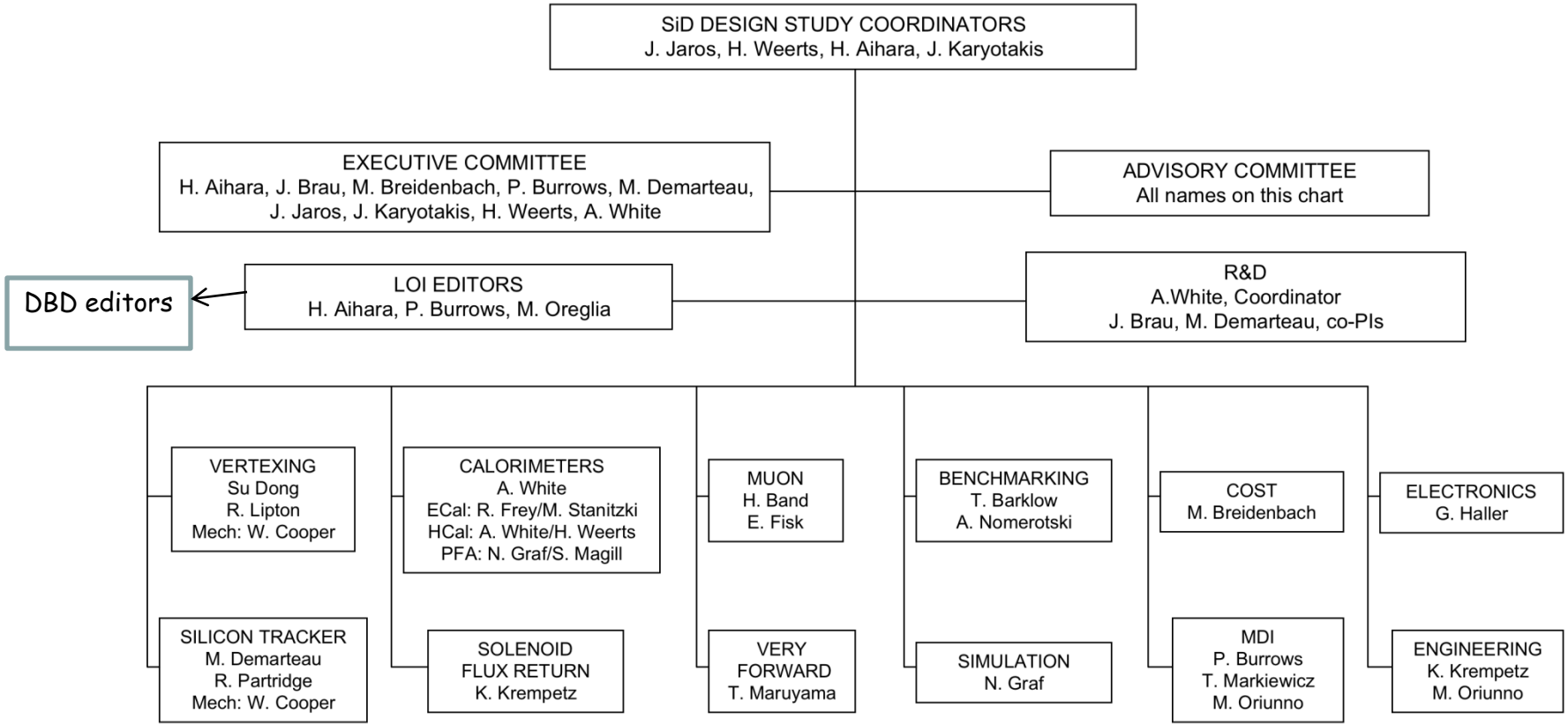


Work Plan for SiD and all subsystems - completed and submitted to Research Director, Oct 09. Updated with realities of subsystem progress, available resources,…

SiD Work Plan - updated



SiD Organization



-> Alternating SiD Executive Committee and SiD Advisory Board meetings.

-> Current focus on preparation/organization for DBD and CDR.

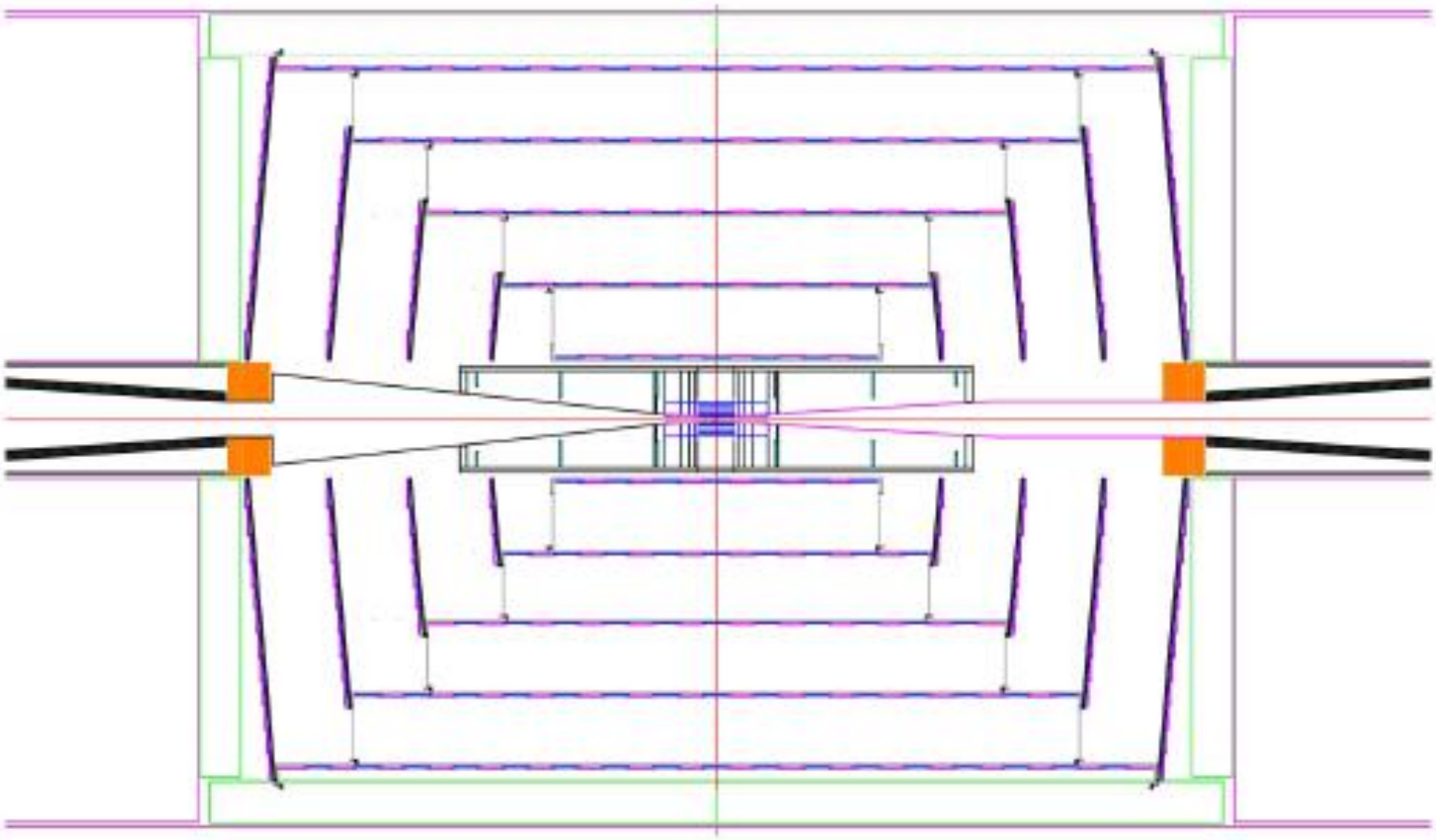
-> Next SiD Workshop: November 15-17, University of Oregon.

Progress on SiD Detector Subsystems

Recent R&D Results and Plans

- An overview of MANY areas of detector R&D
- Not possible to cover every project
- Projects move at different rates
- Many excellent projects moving the whole field of detector R&D forward.
- Some projects are SiD specific, others we follow as SiD technology options.

SiD Beam Pipe and Tracking system



SiD Critical R&D

During the LOI process we identified areas of Critical R&D for each SiD subsystem – review and update where appropriate in this talk.

2) Vertex Detector.
No ILC-ready vertex detector sensor yet exists. The main needs are to develop one or more solutions for the sensors, a demonstrably stable and low mass mechanical support, and pulsed power/cooling solutions. Sensor technologies are being developed, as well as mechanical support materials, designs, pulsed power, and cooling.

3) Tracking Detector.
The priorities for tracking are testing a multi-sensor prototype in the absence of a magnetic field and at 5T, refining the track finding and fitting performance, understanding the optimal forward sensor configuration, and developing more detailed understanding of the mechanical stability and required alignment. Work is underway in all of these areas…

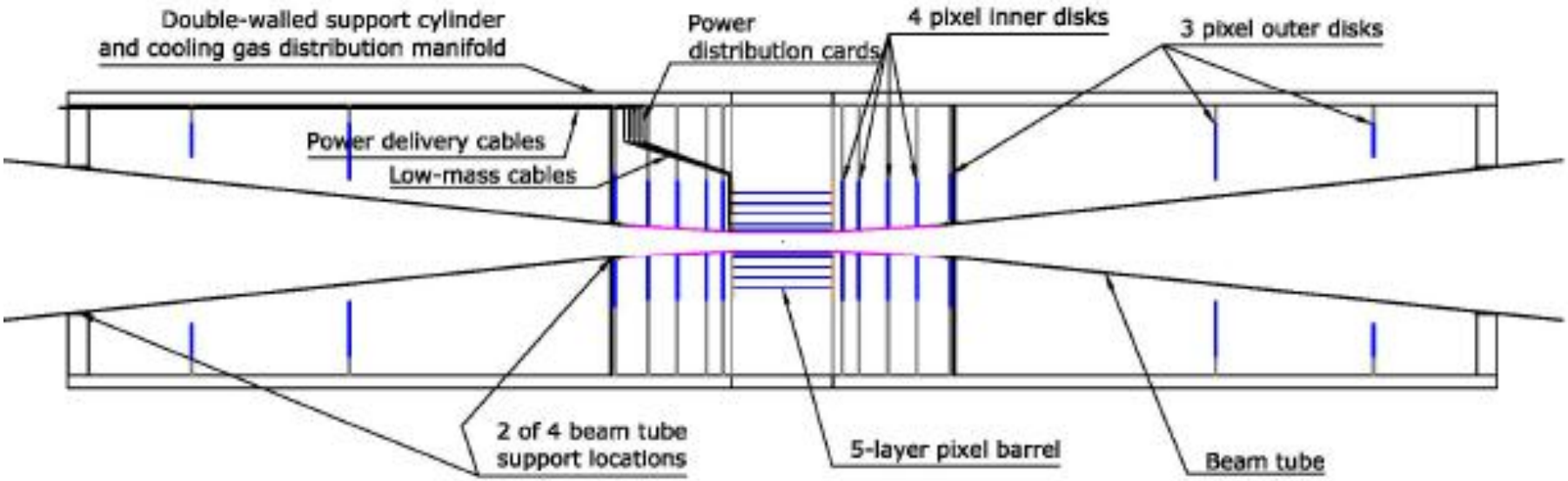
Vertex Detector

-Sensor technology to be decided: Chronopix, 3D, DEPFET,…

- Sensors glued on edges to form cylinders

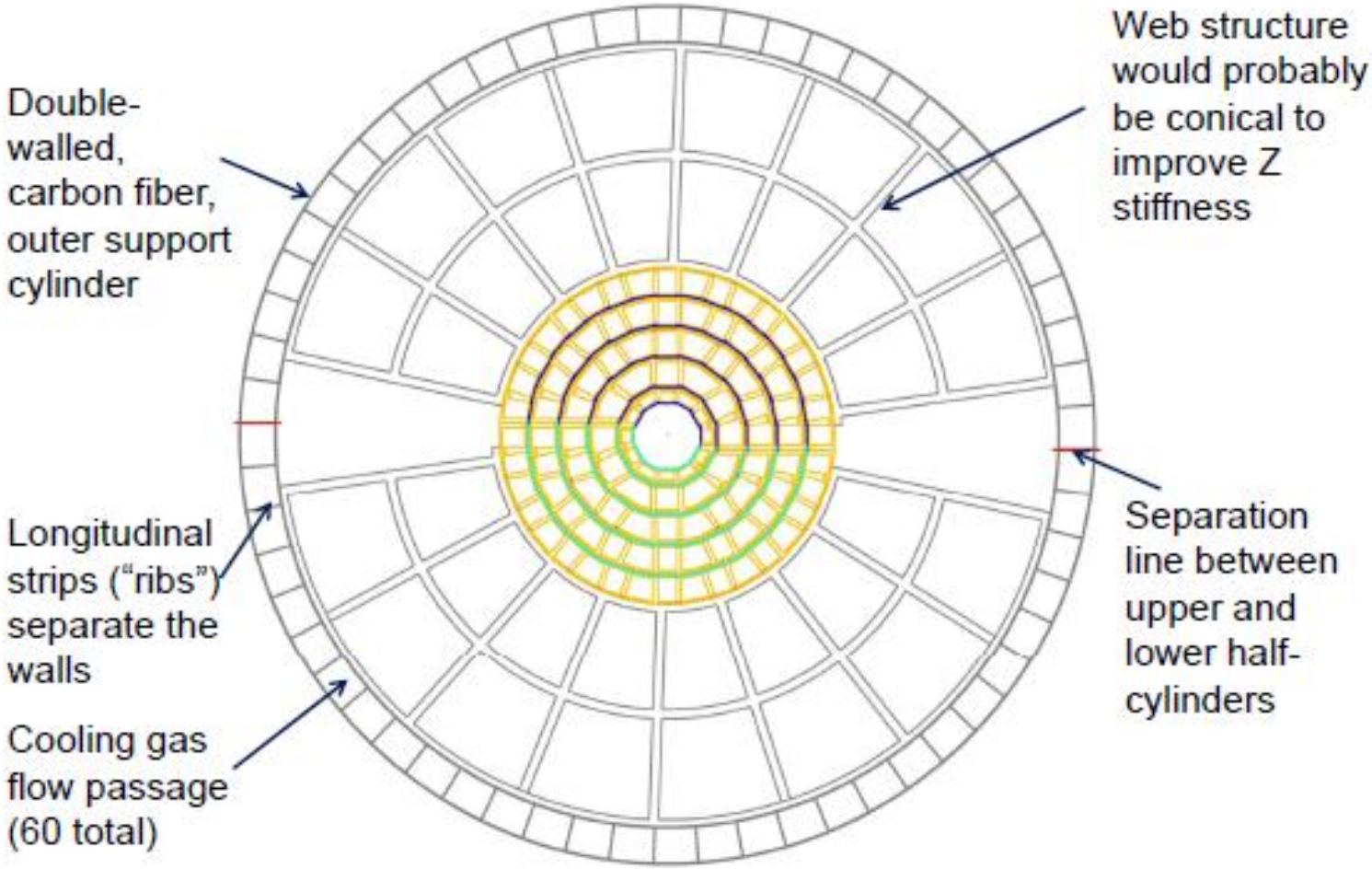
- Gas cooled, power pulsed, low mass

- Pixel outer disks match coverage of outer tracker



Bill Cooper (Fermilab)

Vertex Detector

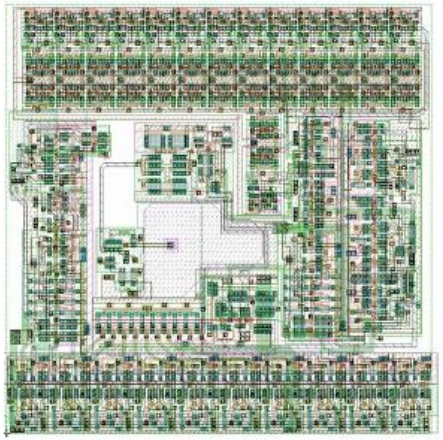


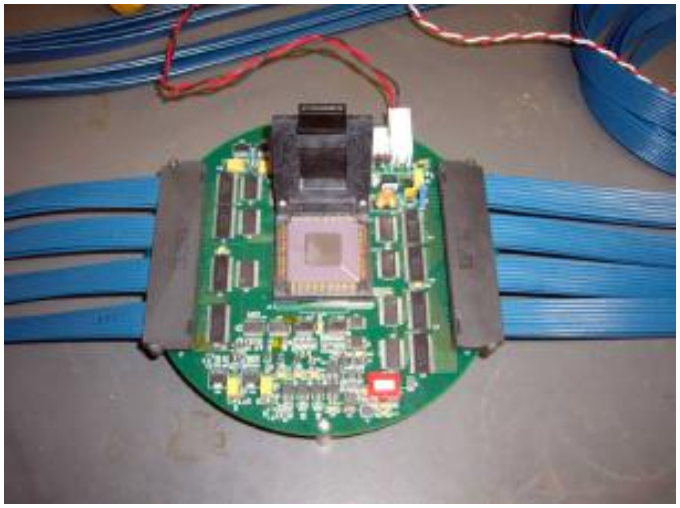
Bill Cooper (Fermilab)

SiD VTX: Chronopix

Specifications:

Detector sensitivity
10 μV/e (eq. to 16 fF)
Detector noise
25 electrons
Comparator accuracy
0.2 mV rms (cal in each pixel)
Memory/pixel
2 x 14 (will be 4 x 14)
Designed for scalability
eg. No caps in signal paths
Provisionally use limited pixel active area
use processes without deep-p well





Status: First prototype (SARNOFF) tested, validates general concept, but improvements needed.

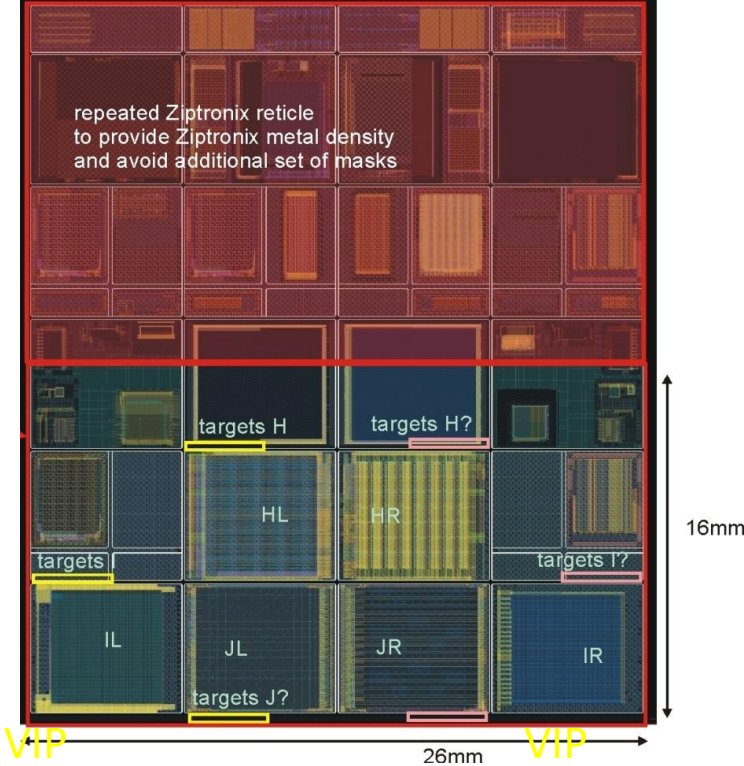
Second prototype: February 2011 after more design evolution and simulation – changes agreed with Sarnoff.

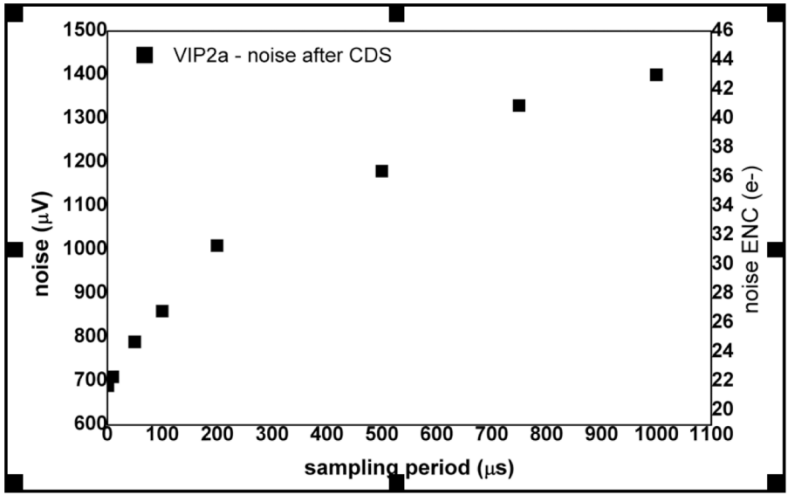
General idea (Sarnoff): get rid of n-wells absorbing signal electrons; build all electronics inside pixel only from nmos transistors sitting in shallow p-wells.

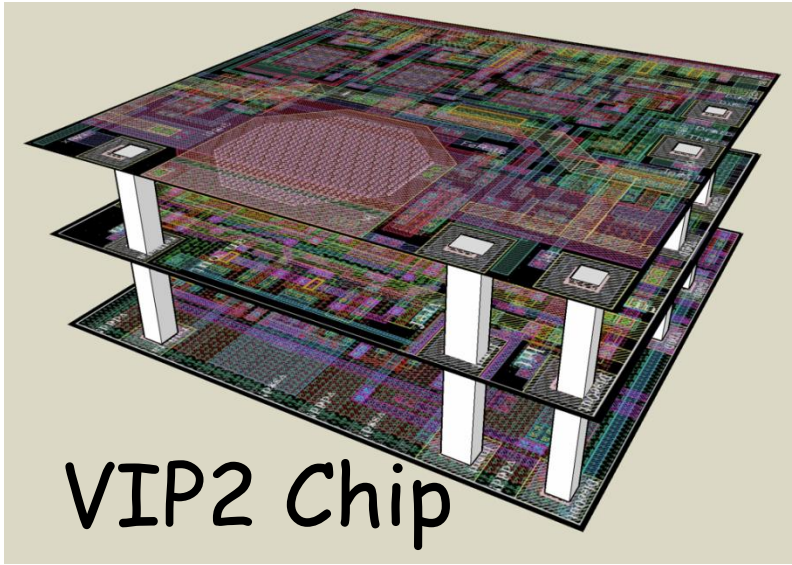
Oregon, Yale

Vertex Detector: 3D

- 3D Sensors and electronics
  - VIP1 three tier chip from MIT-LL received and tested last year
  - Two-tier version of VIP(2b) in Tezzaron/Chartered 3D process
  - VIP2A (three tier) chip received Sept. 2010 from MIT-LL. Initial tests…

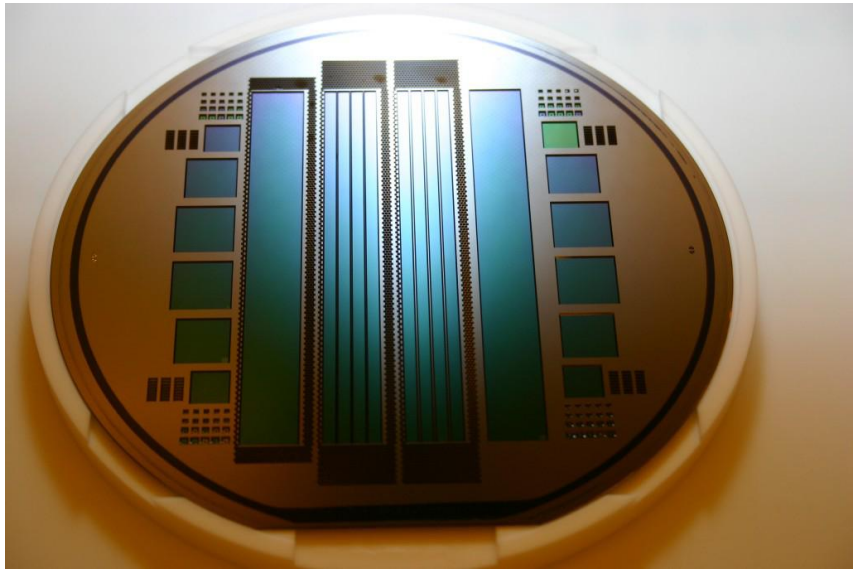






SiD VTX: DEPFET

- Demonstrated SOI-based wafer thinning
- Building DEPFET-based Belle vertex detector – many similarities to ILC design

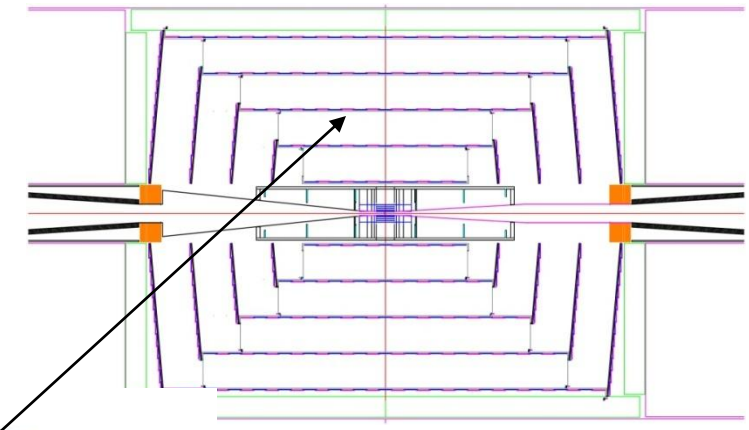


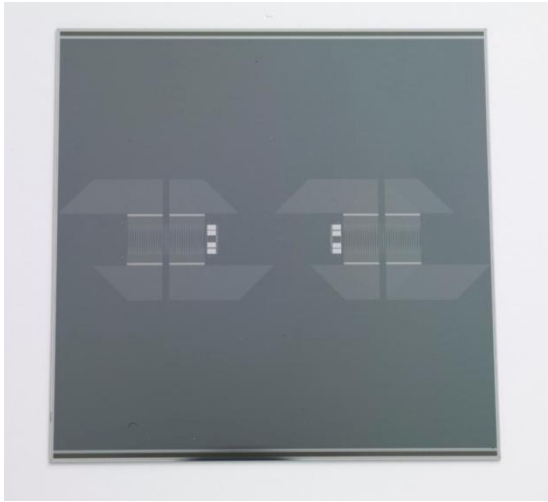
	ILC	Belle 2
occupancy	0.13 hits/μm^2/s	0.4 hits/μm^2/s
Frame time	25-100 μs	10 μs
Duty cycle	1/200	1
	Excellent spatial resolution (3- 5 μm) AND material budget (0.12 % X_0/layer)	Lowest possible material budget (0.15 % X_0/layer) Moderate pixel size (50 x 75 μm^2)

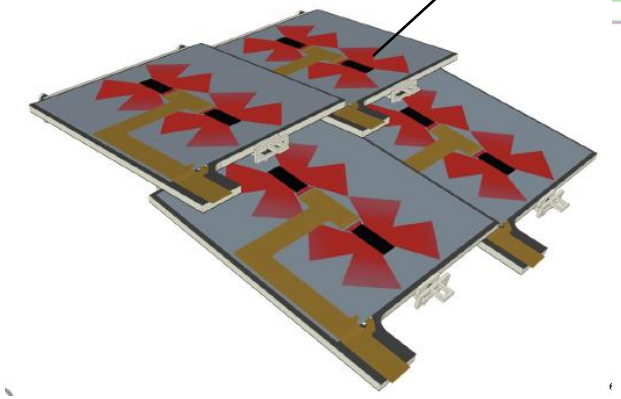
Belle-II presents a more severe challenge than the ILC in several aspects (Vos)

SiD Tracking – Silicon strips

- SiD has an all-Silicon Tracker
- 5 barrel + 7 disk pixel inner vertex detector
- 5 barrel (axial strip) + 4 disk (stereo strip) outer detector. ~10 precision hits per track.







Tiling of tracking layer with Si sensors and on-board KPiX chips

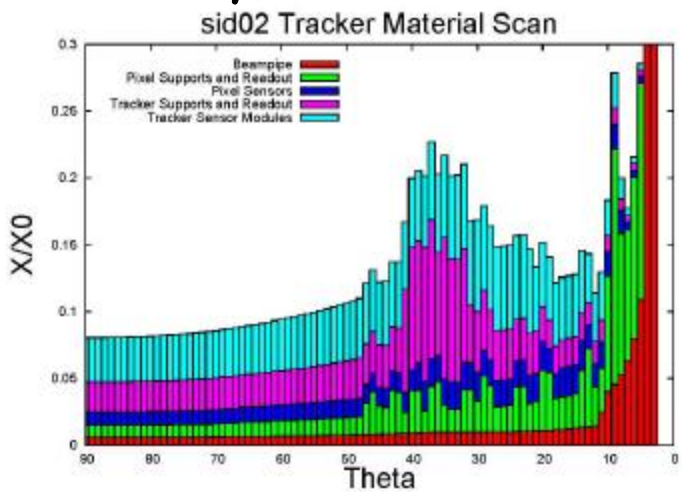
Sensor testing: UCSC/SLAC

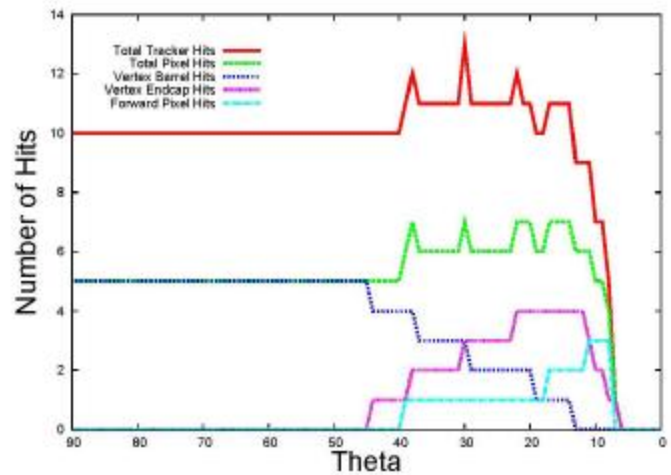
KPiX7 bonded to smaller sensor prototype – under test.

Extension of work to KPiX9 (512 ch.)

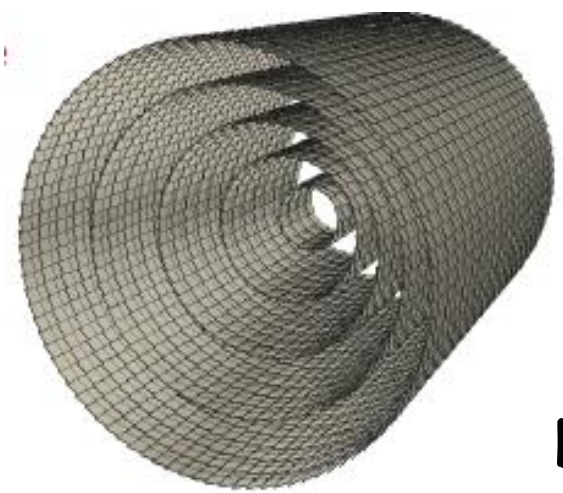
SiD Tracking System

Material/hit layers:



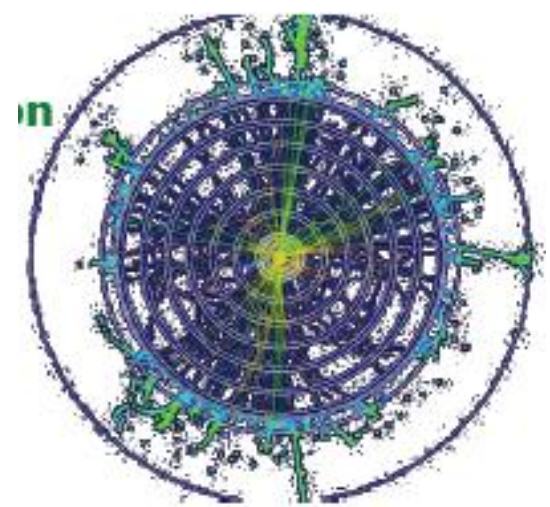


Simulation



Fully segmented detector with individual sensors, overlap and dead material. Allows for detailed tracking and alignment studies

Digitization

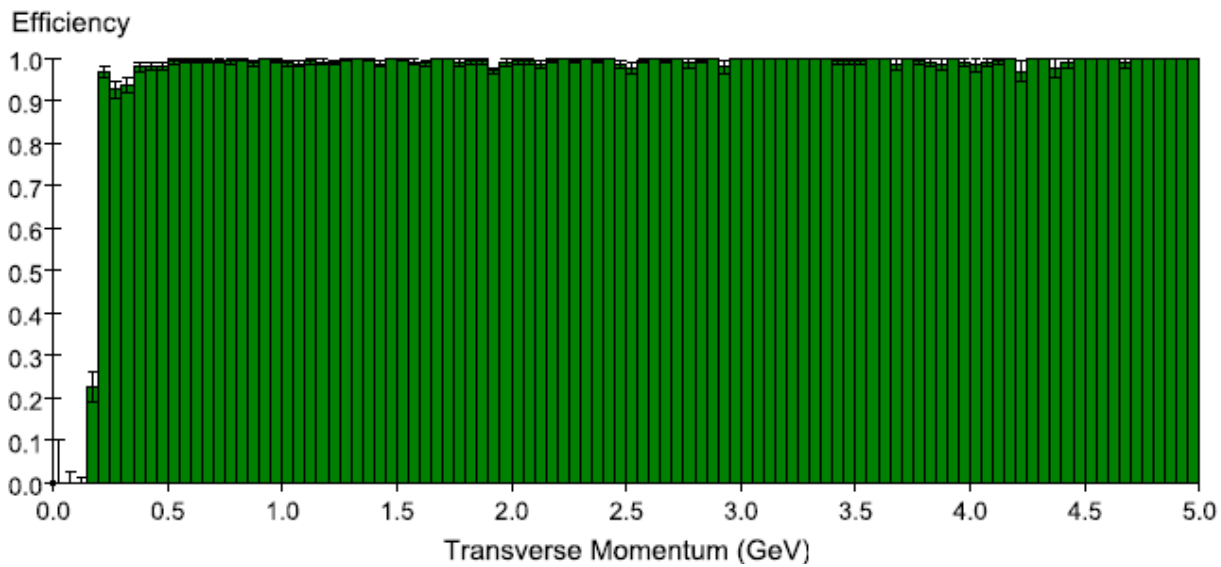


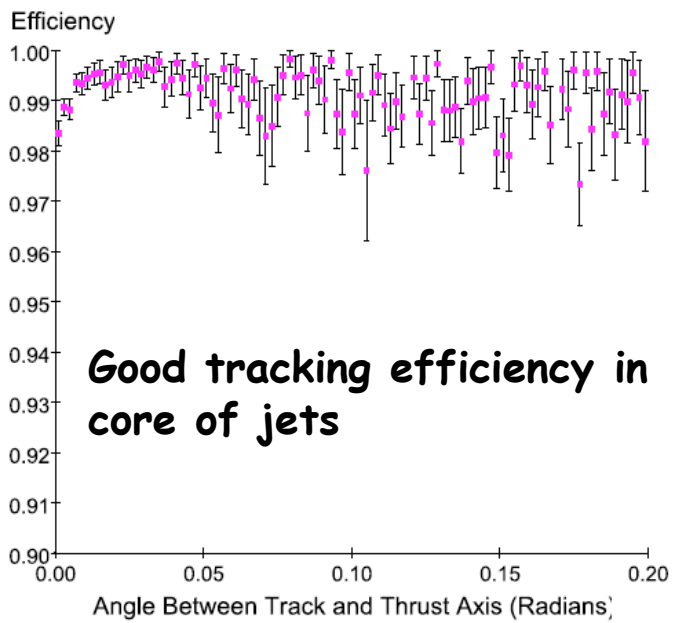
Tracking system performance

Generally find high tracking efficiency for tracks with:

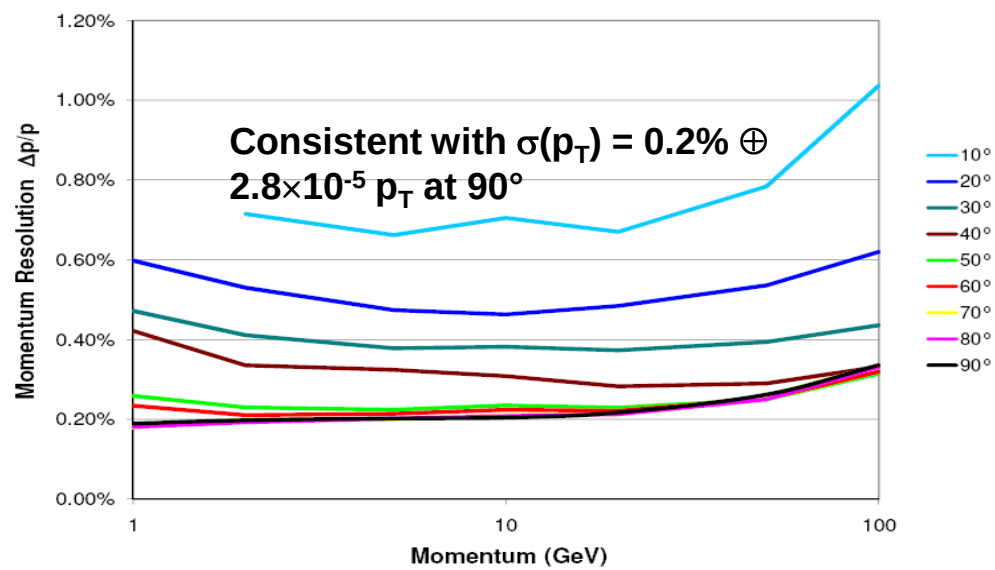
pT > 0.2 GeV

|cos(θ)| < 0.99





Good tracking efficiency in core of jets



Residual issue; tracking across barrel/endcap overlap region.

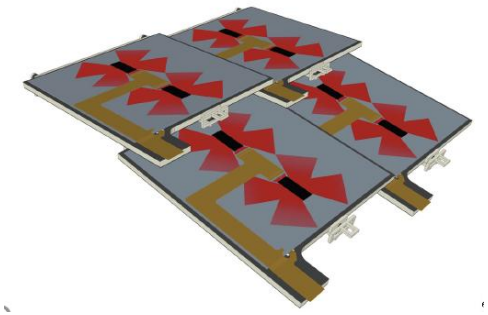
SiD Critical R&D: Electronics

6) Electronics.
One critical item on electronics is a demonstration of the operation of 1024 channel version of the baseline KPiX chip. Another is to develop power distribution schemes for the vertex detector and tracker with DC-DC conversion or serial powering. Adapting and testing KPiX readout to the tracker, calorimeters, and muon systems must also be continued and perfected.

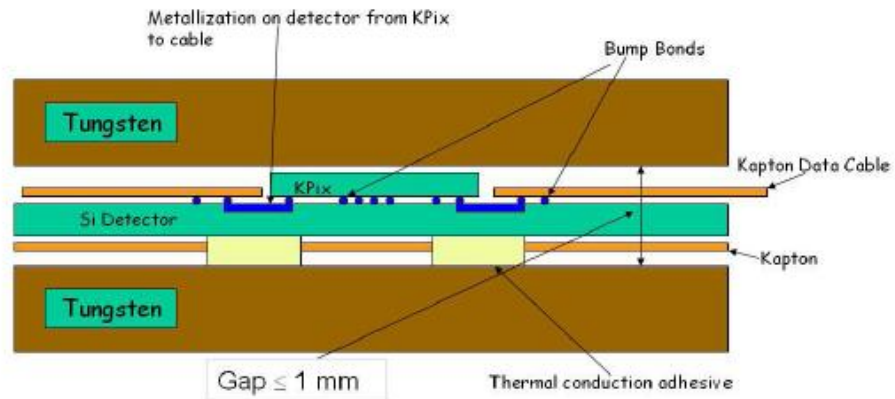
SiD Electronics - KPiX

KPiX readout for all SiD subsystems except VTX.

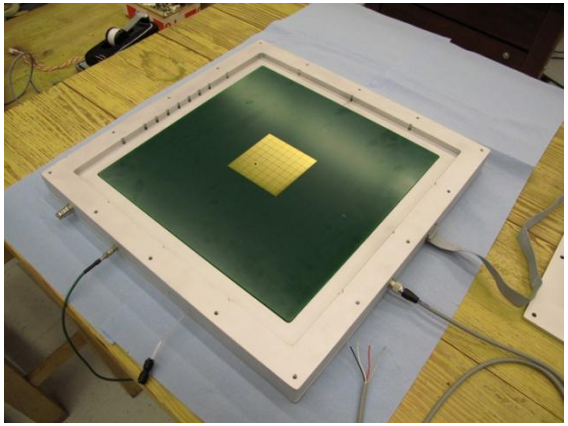
Tracker



ECal



HCal (GEM version)



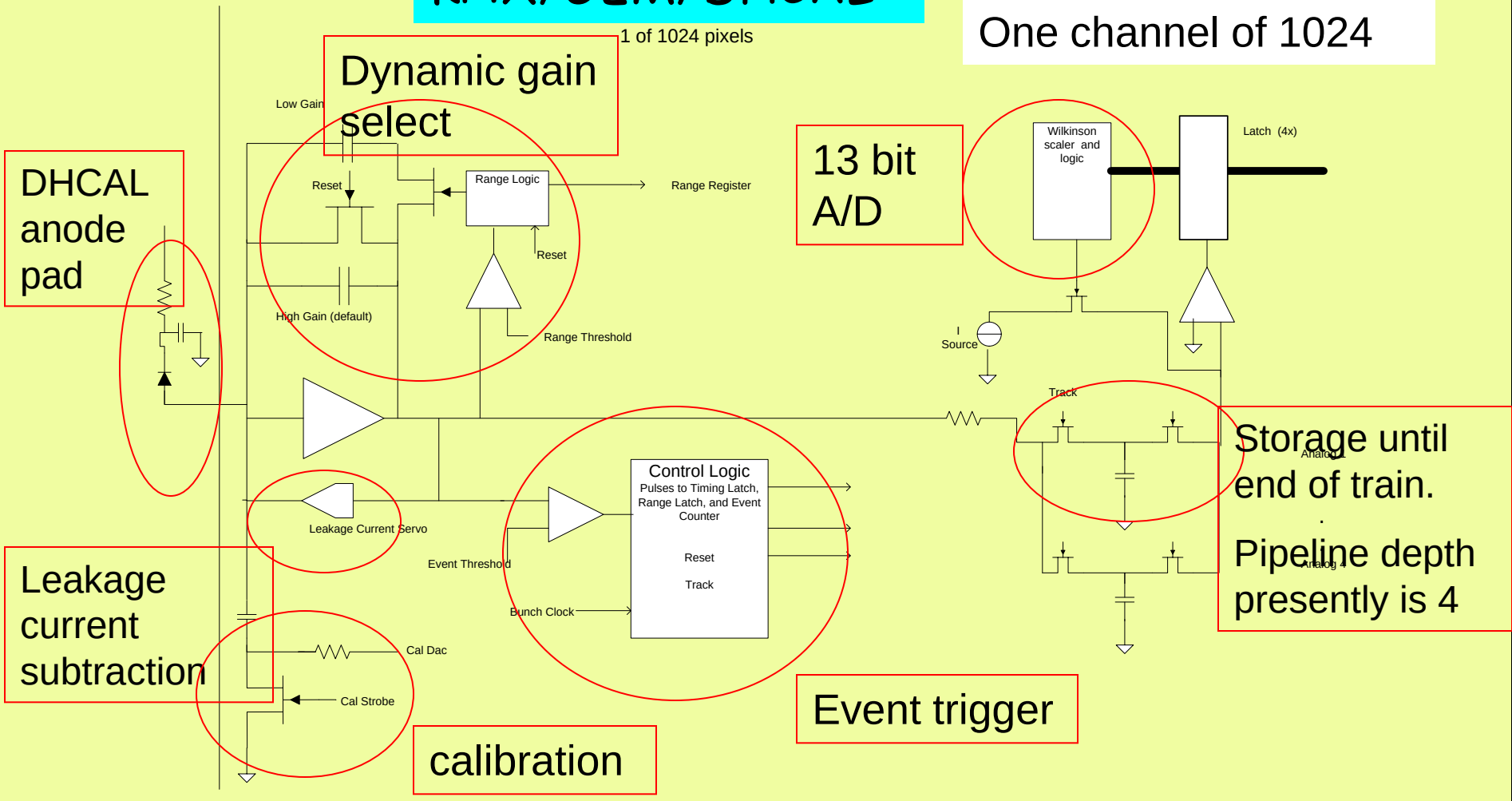
+ working on an FCal version

...and Muon!

KPiX/GEM/DHCAL

KPiX chip

One channel of 1024



Simplified Timing:

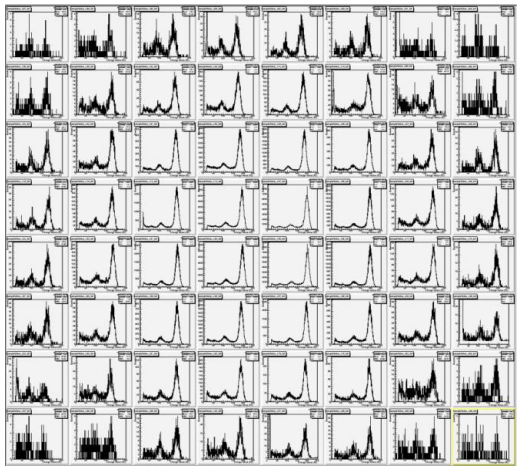
There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

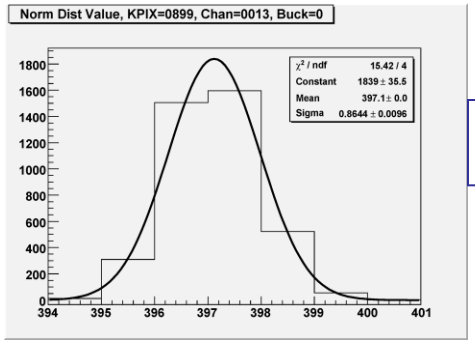
SiD Electronics - KPiX

- Many tests with KPiX 7 (64-channel):

- DHCAL



Noise measurement



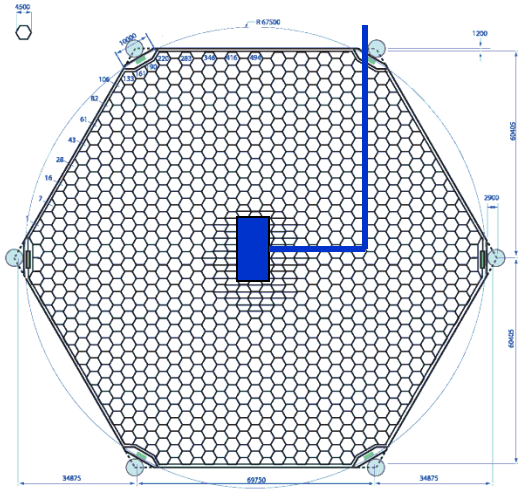
1300 e rms

- Version 9: 512 channels – under test.

SiD ECal

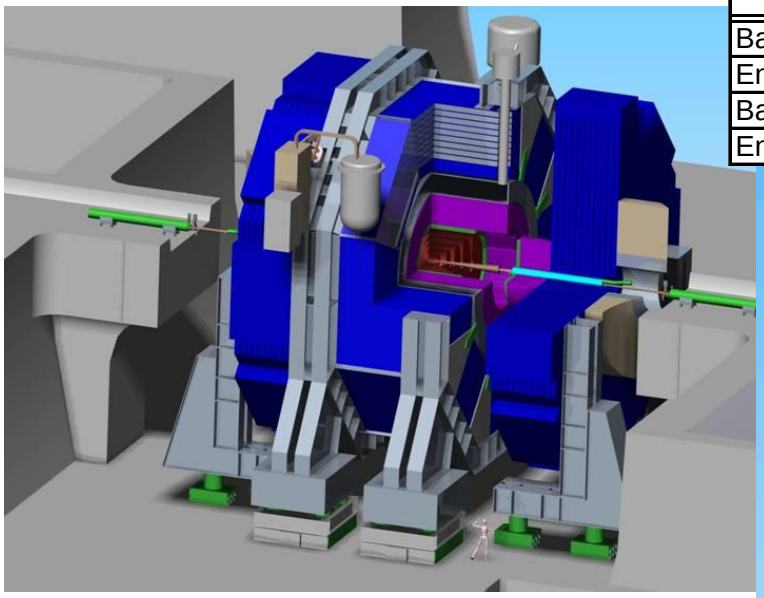
With a 512-channel KPiX-9 bump-bonded to a sensor, can get noise measurements for the full range of input capacitances and resistances. Some bonding issues.

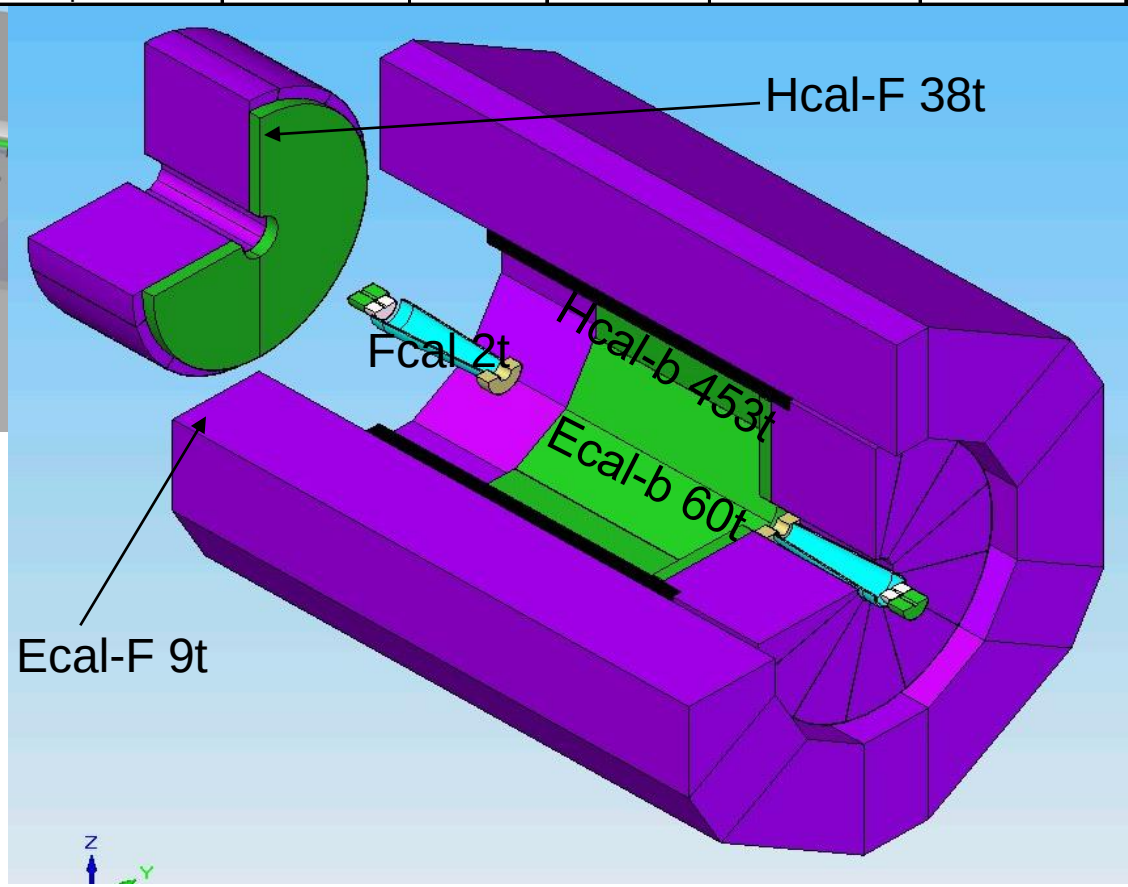
1024-channel KPiX about to be submitted

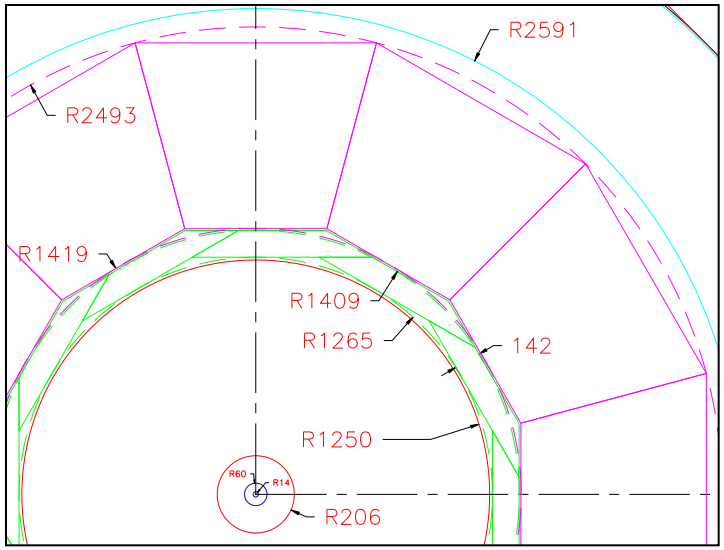


SiD Calorimeter System

	Technology	Xo / λ	Absorbers	Weight (tons)	Area (m^2)
Barrel Ecal	Silicon-W	26	Tungsten	60	80
Endcap Ecal	Silicon-W	26	Tungsten	2 x 9	2 x 143
Barrel Hcal	RPCs	4.5	Stainless	453	3000
Endcap Hcal	RPCs	4.5	Stainless	2 x 38	2 x 247





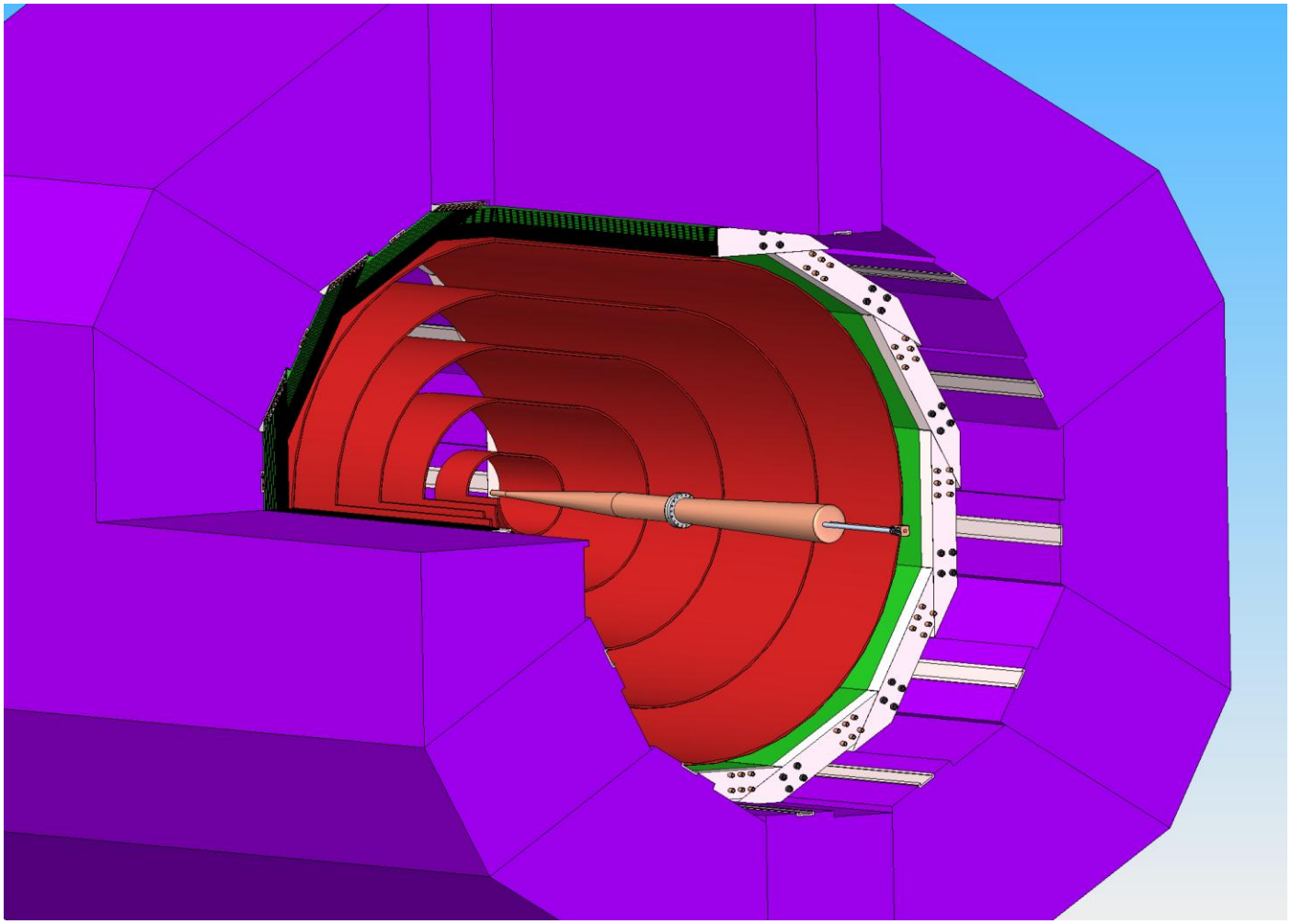


For FCal we follow the work of the FCal Collaboration.

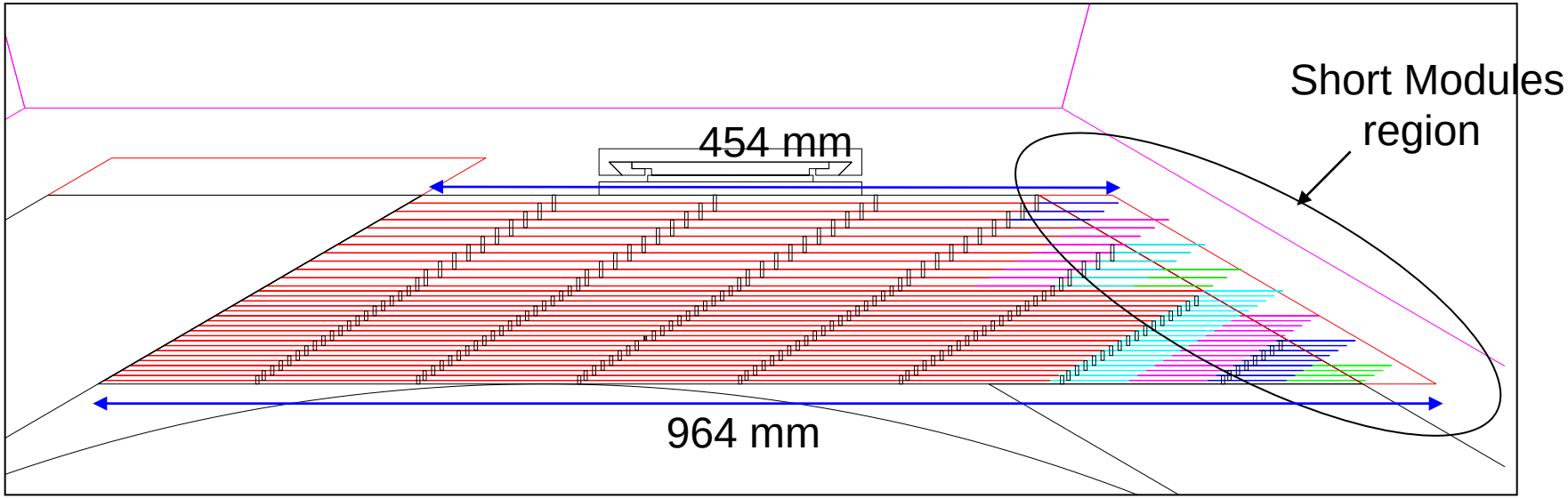
SiD Critical R&D: ECal

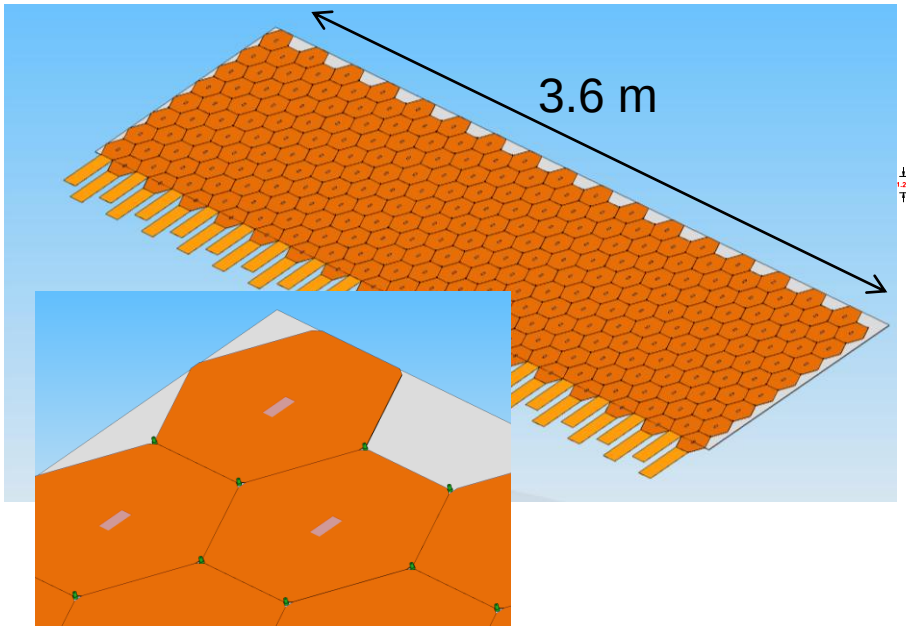
4) Electromagnetic Calorimetry.
For the baseline silicon-tungsten Ecal design, the operability of a fully integrated active layer inside the projected 1.25mm gap between absorber plates must be demonstrated. Sufficient S/N, successful signal extraction, pulse powering, and adequate cooling must be shown as well. Mechanical prototypes with steel rather than tungsten will first be built, followed by a full depth tower appropriate for beam tests. For the alternative MAPS technology being investigated in the U.K., a key need is production of large sensors with sufficient yield.

Si-W sampling/imaging ECAL



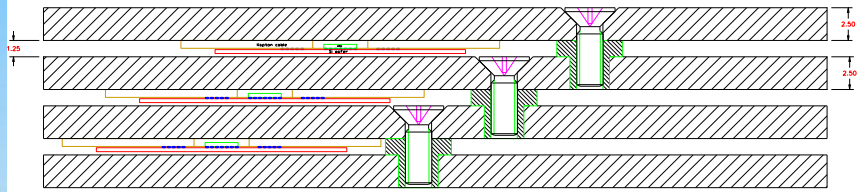
SiD Electromagnetic Calorimeter

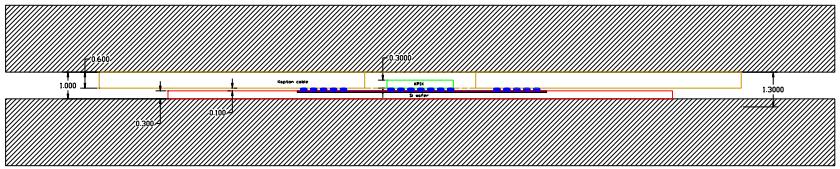




Staggered layout

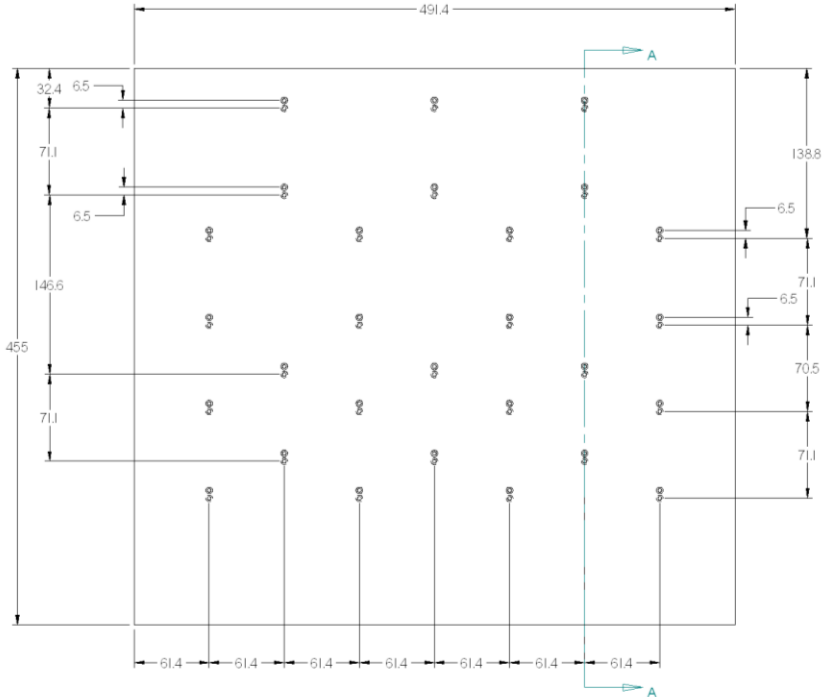
Only 2 masks for the wafer and 8 for the kapton

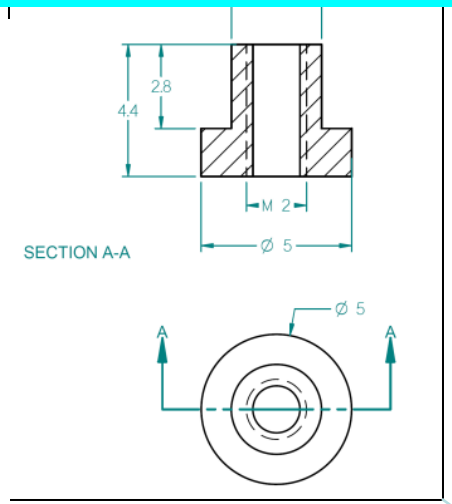


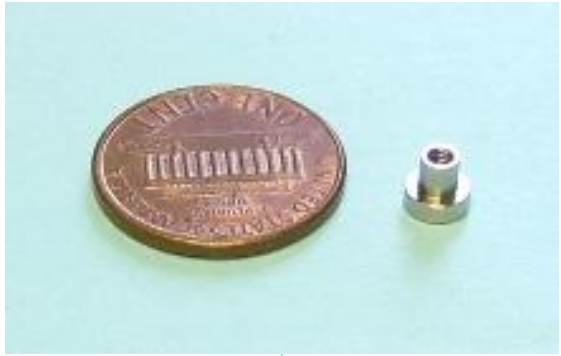


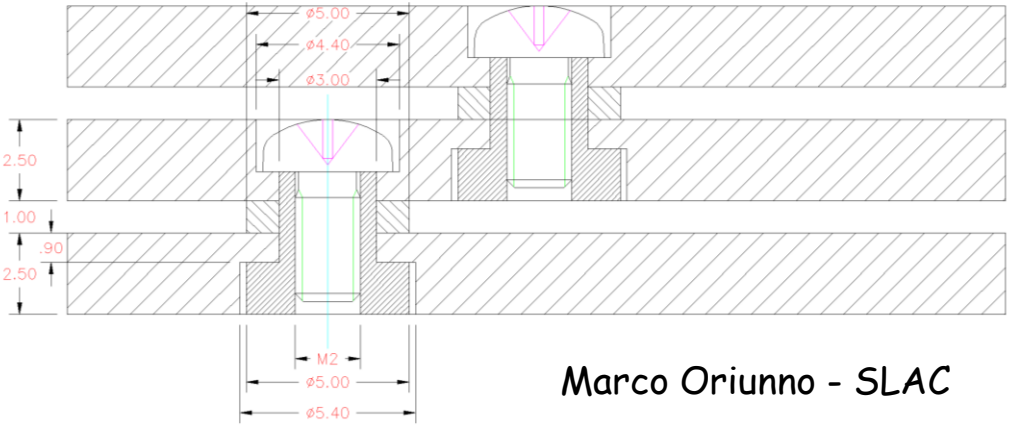
SiD Electromagnetic Calorimeter

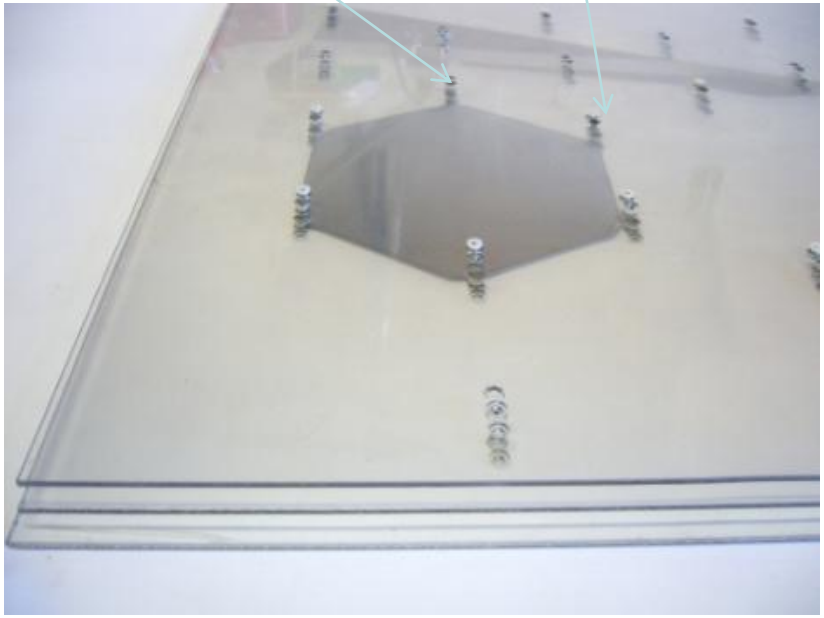
- mock-up with Lexan plates





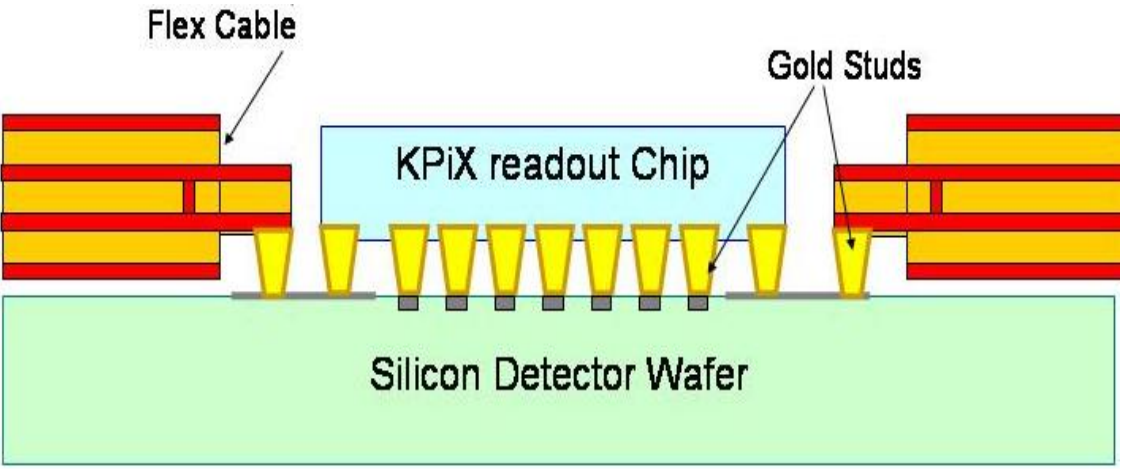




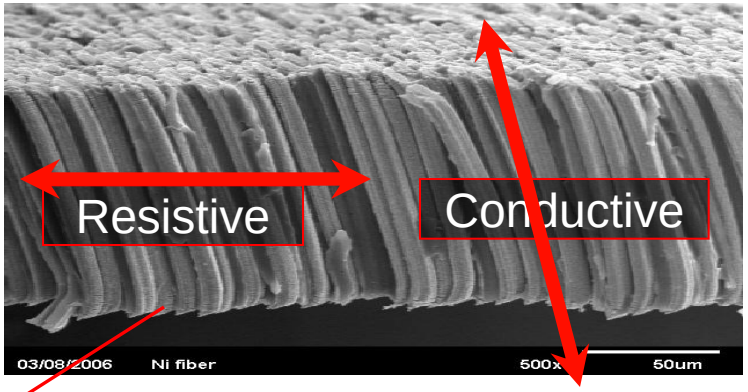


Marco Oriunno - SLAC

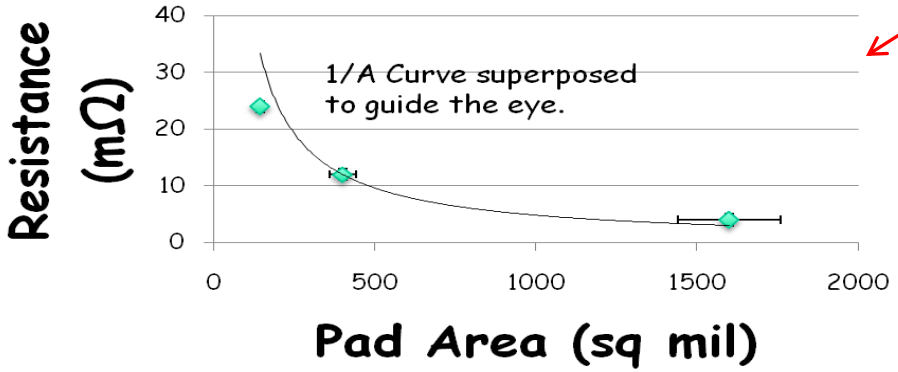
SiD Electromagnetic Calorimeter



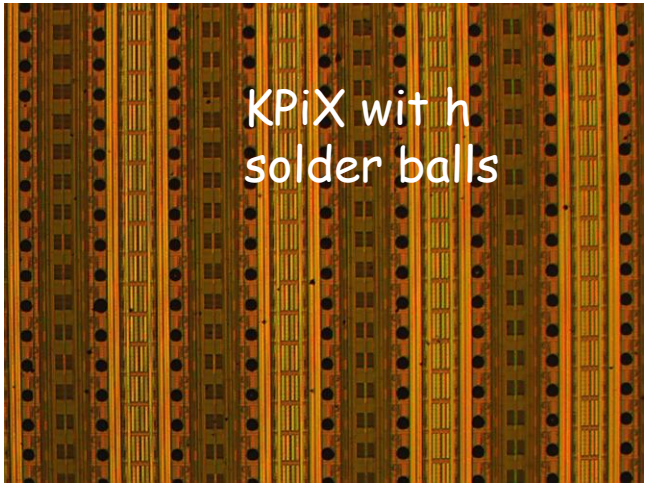
Anisotropic Conducting Film



Gold-stud bonding for prototypes – issues (shorts) with wafers -> solder bumps on created Ni-Au surface.

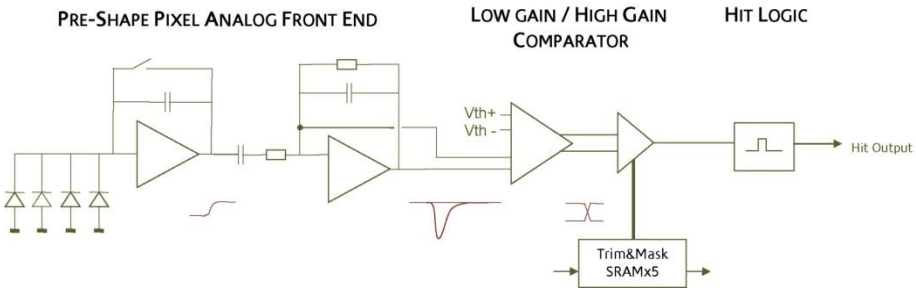


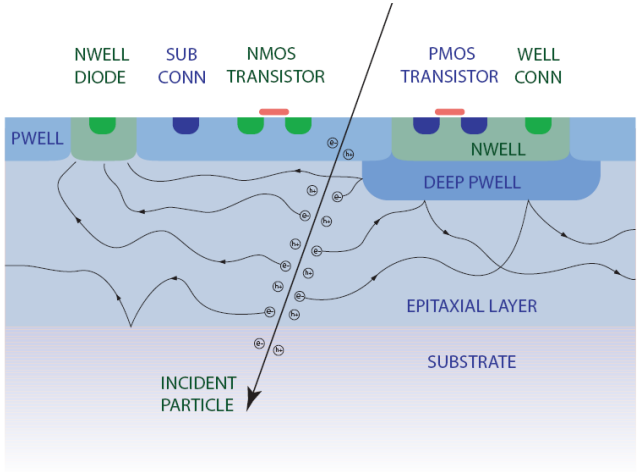
Initial results are promising. Goal for Flex Cable pads (100 sq mil) is ~100 mΩ, which is achievable. Also studying solder ball

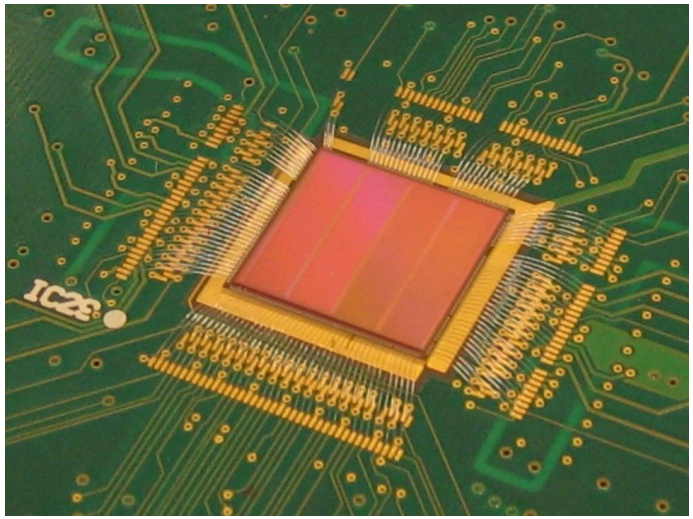


New Bump Bonding Equipment Installed at UC Davis

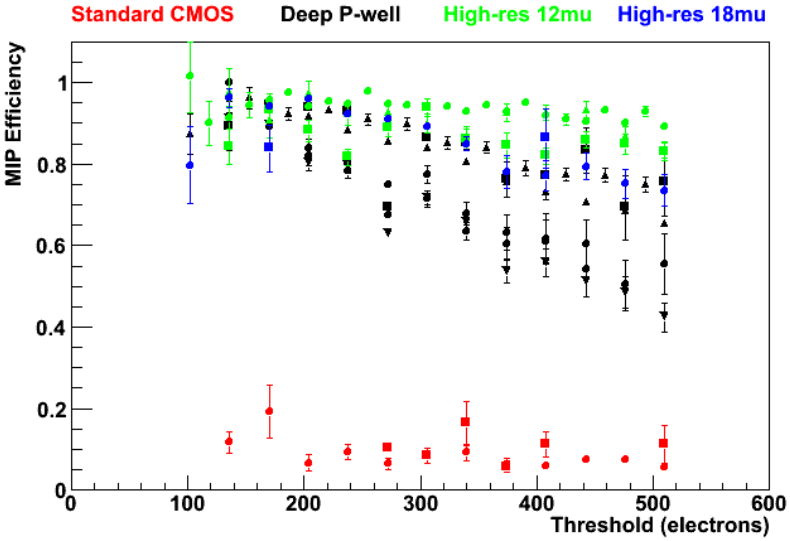
MAPS Electromagnetic Calorimetry







TPAC 1.2. Four variants made in 0.18μm INMAPS CMOS, 50μm pixels. 168x168 array



Beam tests at CERN and DESY: significant efficiency gain with INMAPS over standard CMOS.

Next steps

Calorimetry: ECal

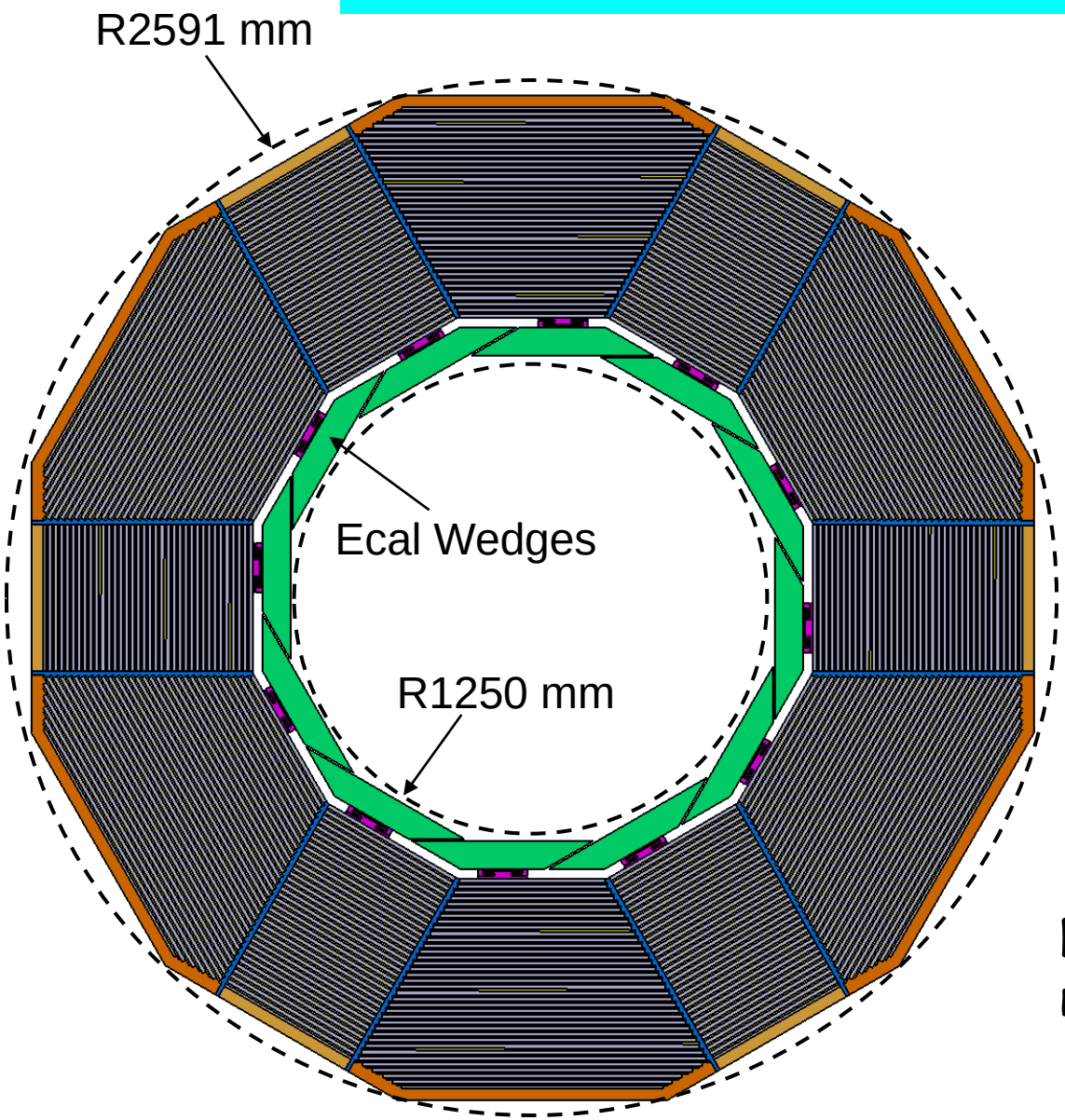
- Si-W ECal: anticipate that, once bonding issues are resolved, the test-beam related data taking and analysis begins and will continue well into 2011.

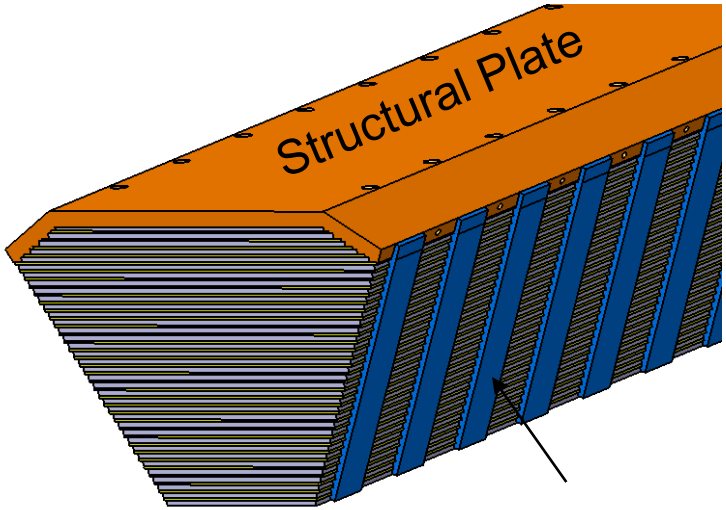
- First the module will be tested in an electron beam (possibly at SLAC – new ESTA beam), followed later by a beam test with hadrons and in combination with hadronic stack.

- Completion of this R&D is expected by 2012.

- MAPS ECal: the goal is to make a second generation chip which is sufficiently large to make an ECAL stack to study digital electromagnetic calorimetry in detail.

SiD HCal – an example design

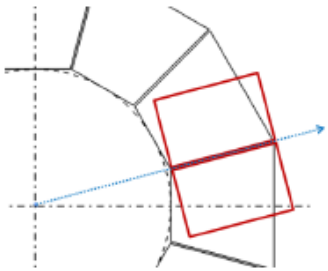




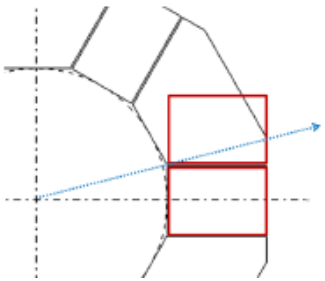
Non-projective version – not yet in SiD simulation

Nicolas Geoffroy - LAPP

SiD HCal – study of effect of cracks

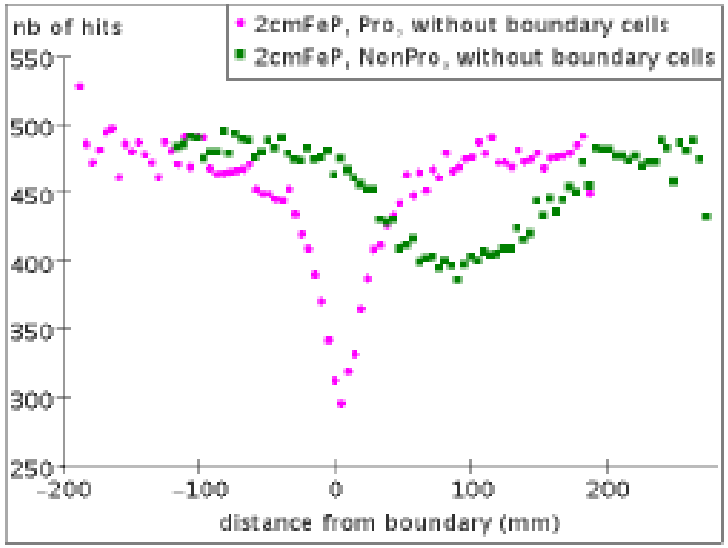


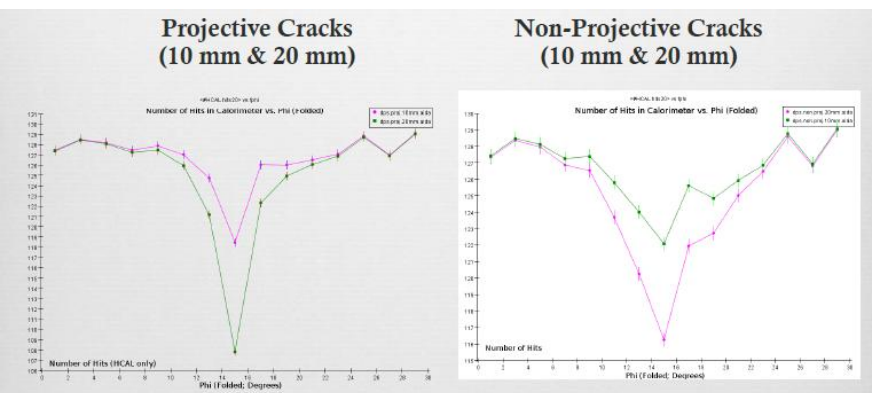
Projective Geometry



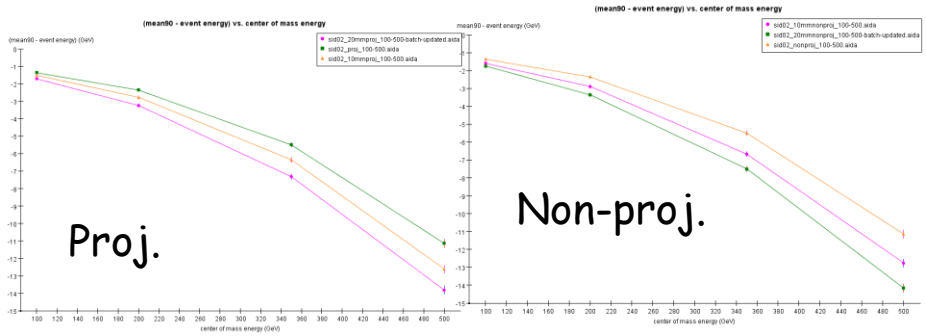
Non Projective Geometry

Jan Blaha – analysis note soon.





sid02 qqbar events



Effect(s) on physics studies (parameter measurements) to be studied.

Lauren Gilbert (Caltech)

SiD Critical R&D: HCal

5) Hadronic Calorimetry.
The priority for hadronic calorimetry is to demonstrate the feasibility of assembling a fully integrated, full-size active layer within a ~8mm gap between absorber plates. Several technologies are being investigated: RPC's, GEM's, Micromegas, and scintillating tiles/SiPM's. All of this work is being carried in conjunction with the CALICE Collaboration, and the results will form a critical component of SiD's future technology selection. An alternative approach, using homogeneous crystal calorimetry with dual readout, is also being studied. This effort needs to demonstrate good hadronic energy linearity and resolution in a test beam, to develop suitable crystals, to produce a realistic conceptual design, and to simulate physics performance.

RPC DHCAL

Argonne NATIONAL LABORATORY

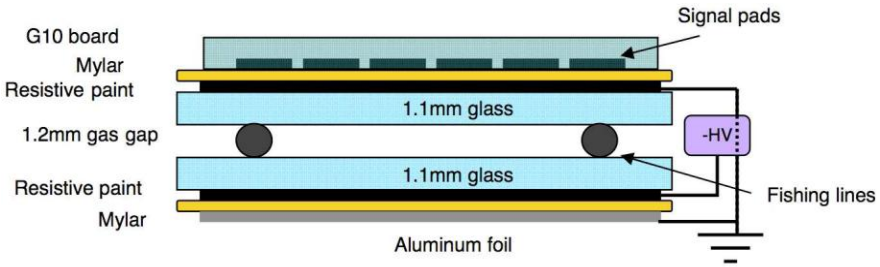
THE UNIVERSITY OF IOWA

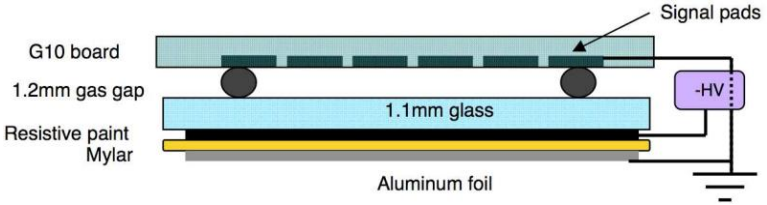
Boston University

CALICE Calorimeter for ILC

Construction of 1m^3 prototype RPC stack:

- 114 chambers + spares
- Essentially all materials in hand
- 2 man-days/chamber
- 3 assembly lines
- Start tests at Fermilab in October (after shutdown)



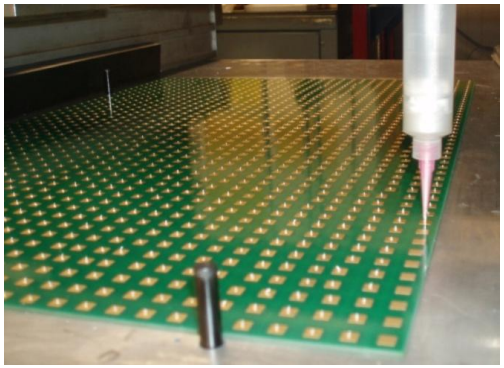


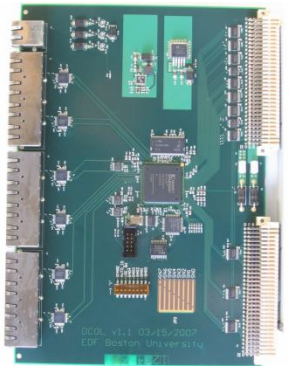
Five publications from earlier Vertical Slice Test !

RPC chamber construction/services for 1m^3 stack

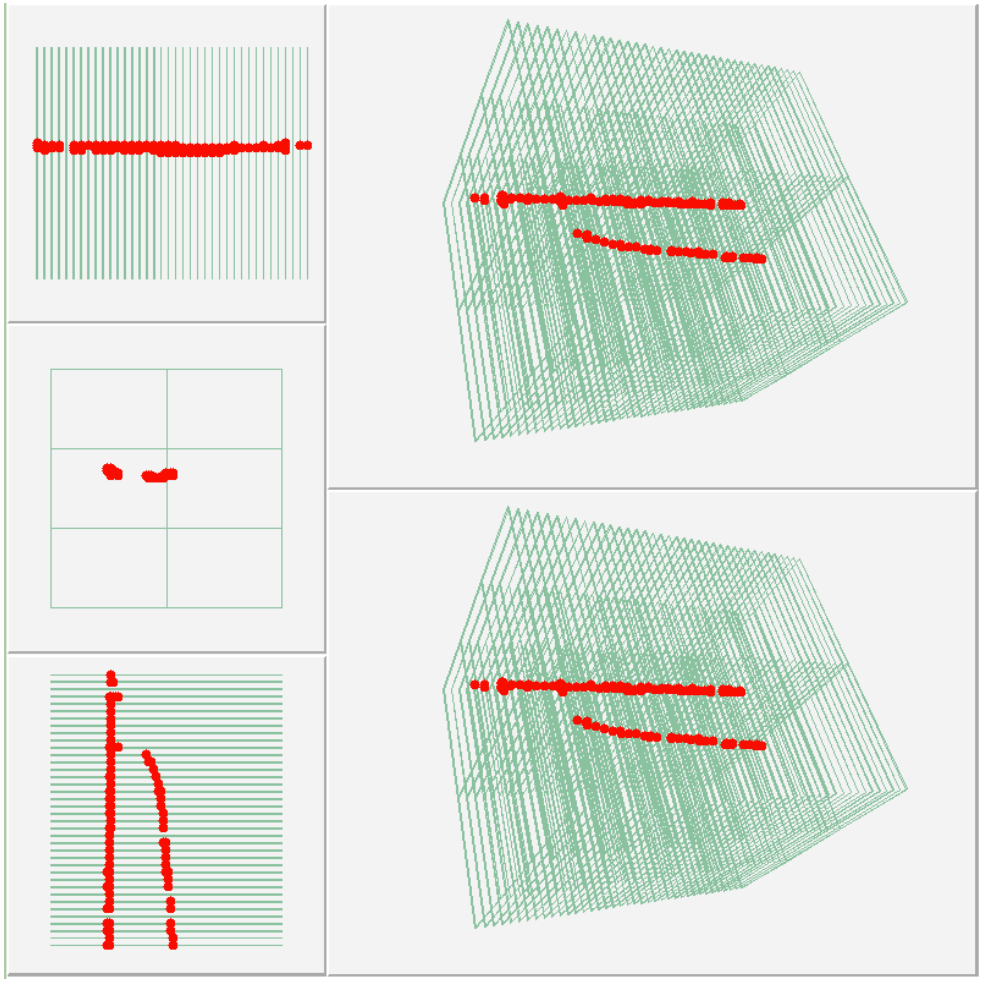
Very large effort underway on Chamber construction, Electronics, Cassette production, High Voltage, Gas System.

DHCAL Collaboration	Heads
Engineers/Technicians	22
Students/Postdocs	8
Physicists	9
Total	**39**



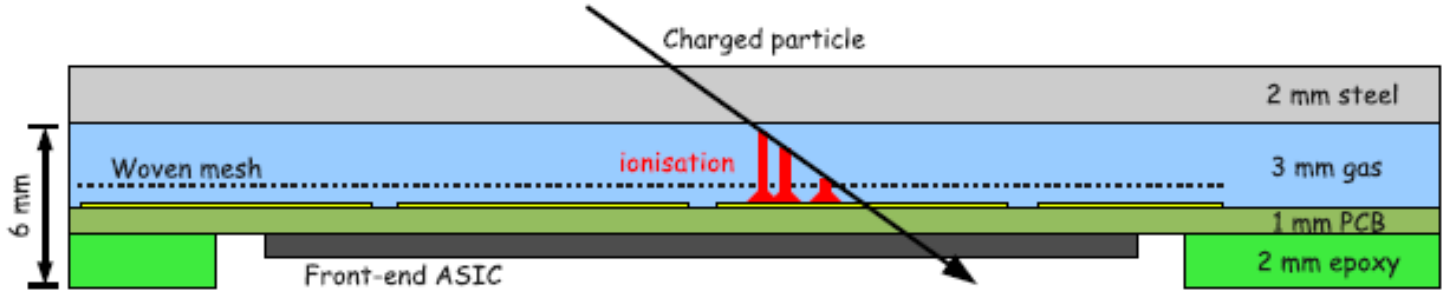


RPC DHCAL

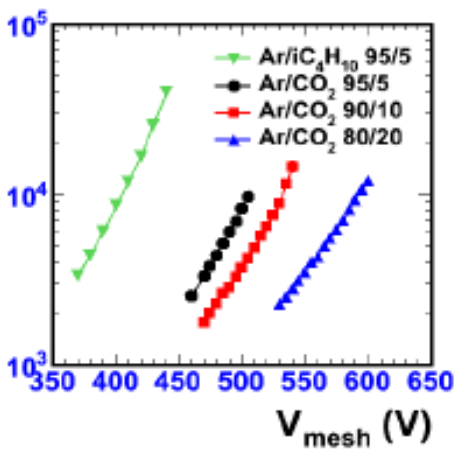


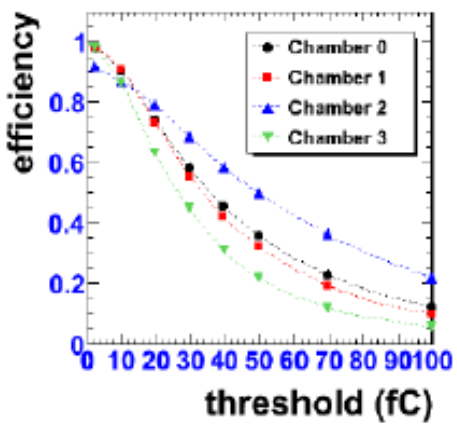
First muon tracks through RPC 38-layer DHCAL at Fermilab.
J. Repond et al. ANL

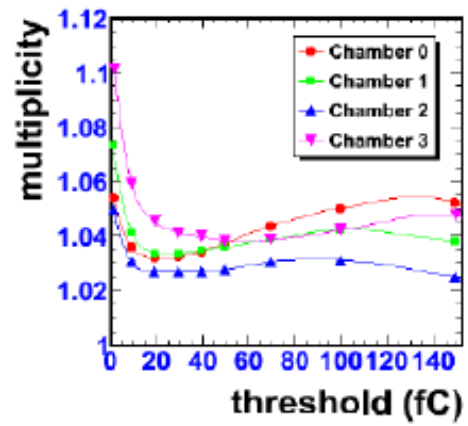
Micromegas-DHCAL



- MICROMEGAS for a DHCAL:
  - fast, radiation hard, good aging properties, robust, large area, high gas gain, spark proof, standard gas mixture (Ar, iC_4H_{10}, CO_2)
  - small avalanche charge → sensitive front-end electronics

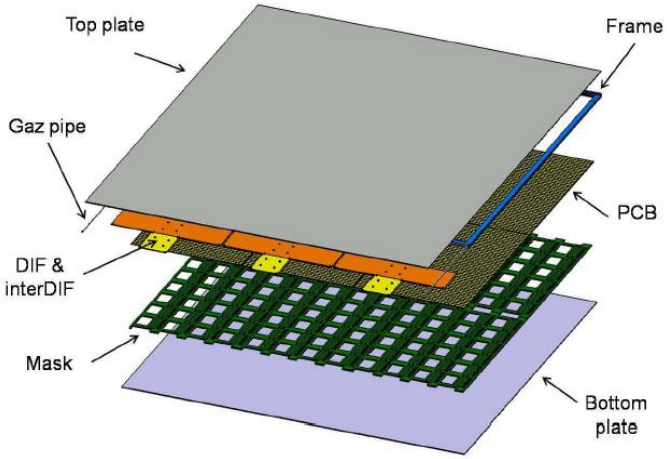


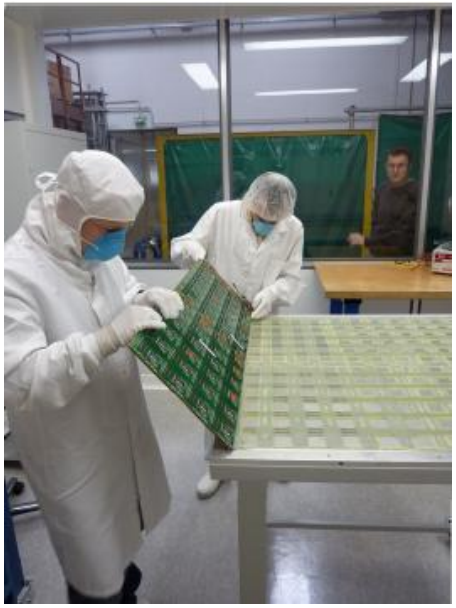




Jan Blaha

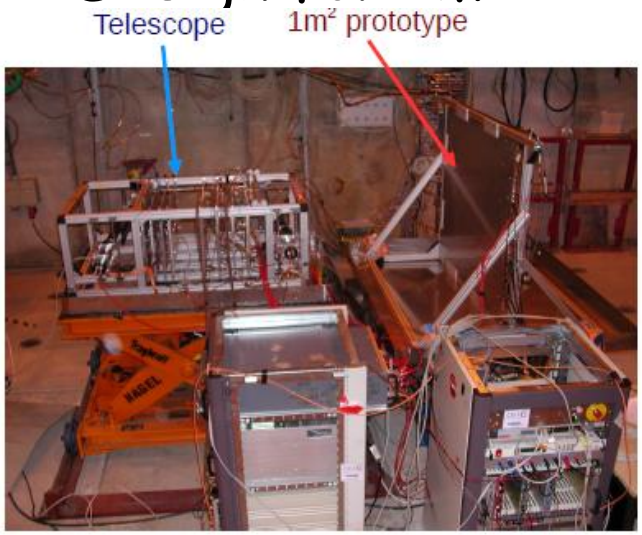
Micromegas-DHCAL





After 1 week the 1 m² is fully assembled!

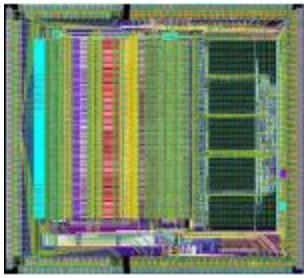
Design for 1m²

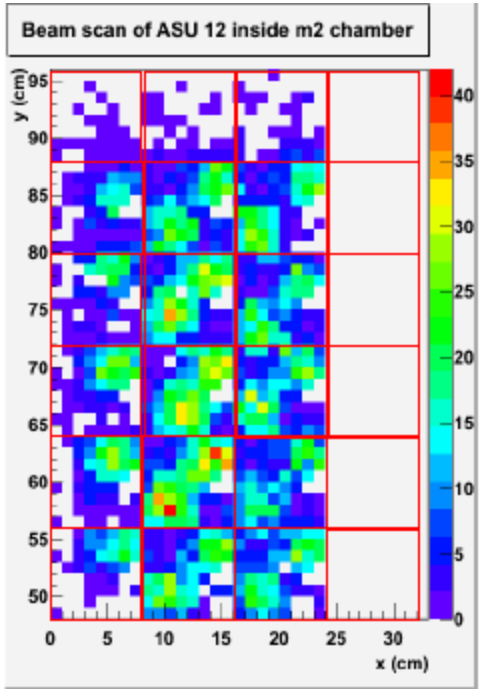


SPS/H4 beam

- 4 weeks in June/July 2010
- 150 GeV/c muons and pions

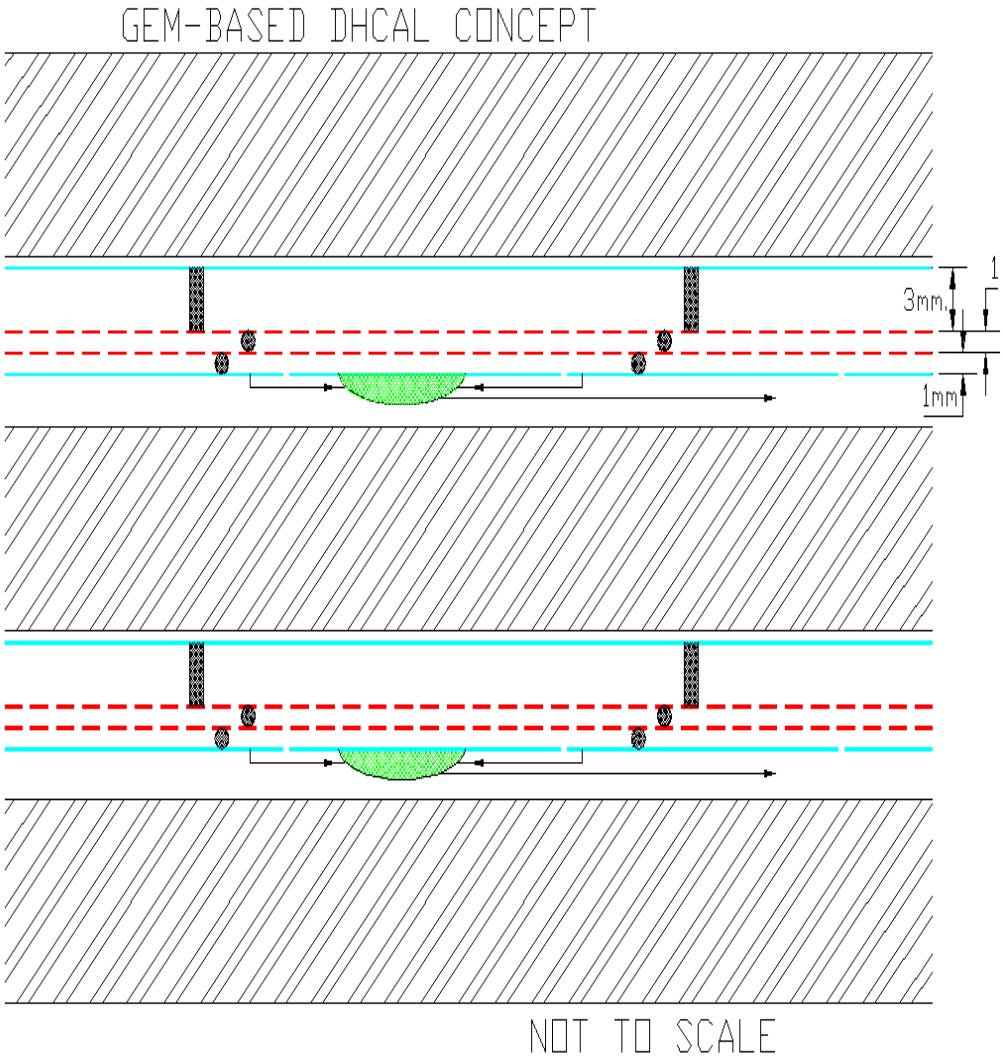
Low efficiency – non-optimal electronics

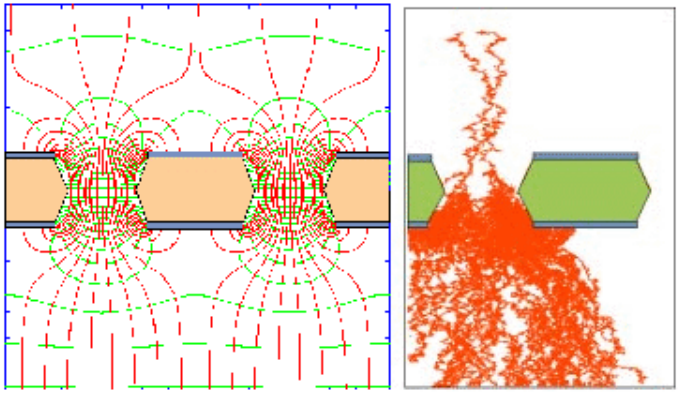




New readout chip MICROROC
Development with LAL/OMEGA
Shaping time matching the detector signal duration

GEM/DHCAL active layer concept





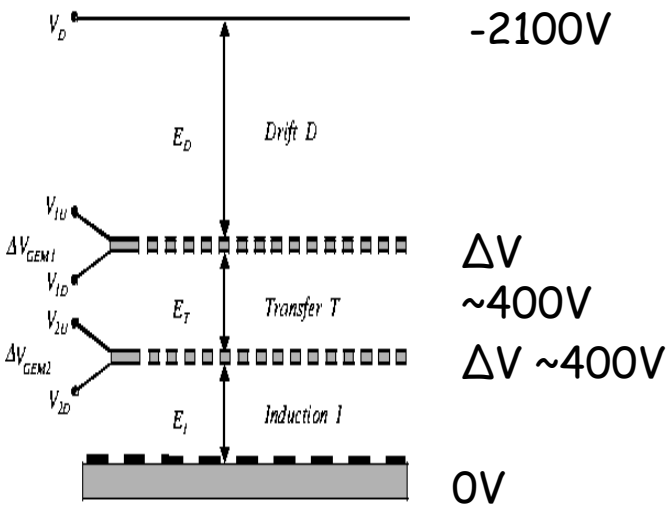
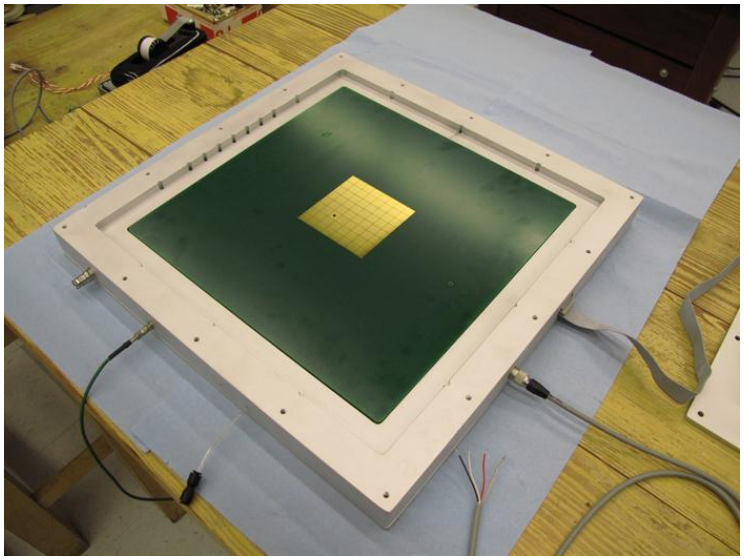
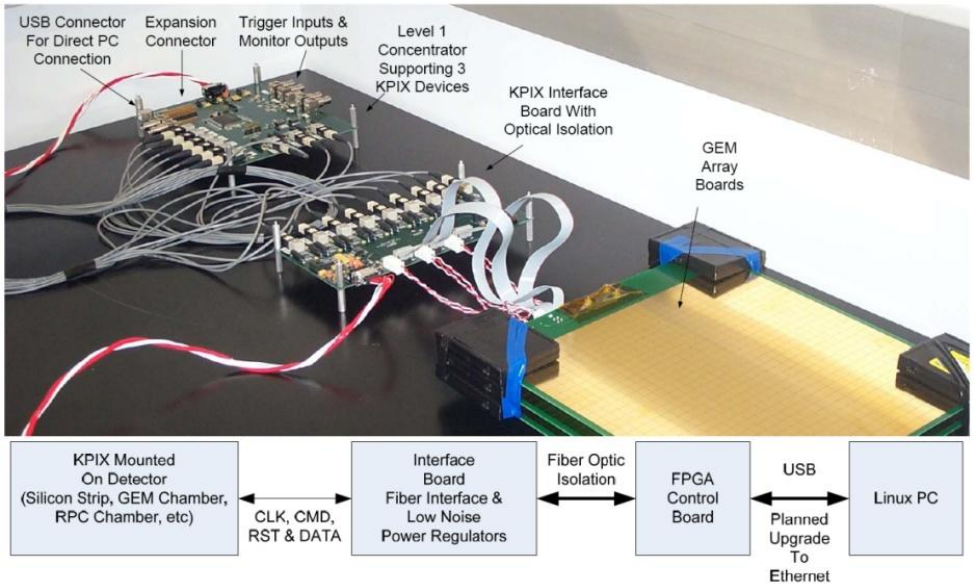


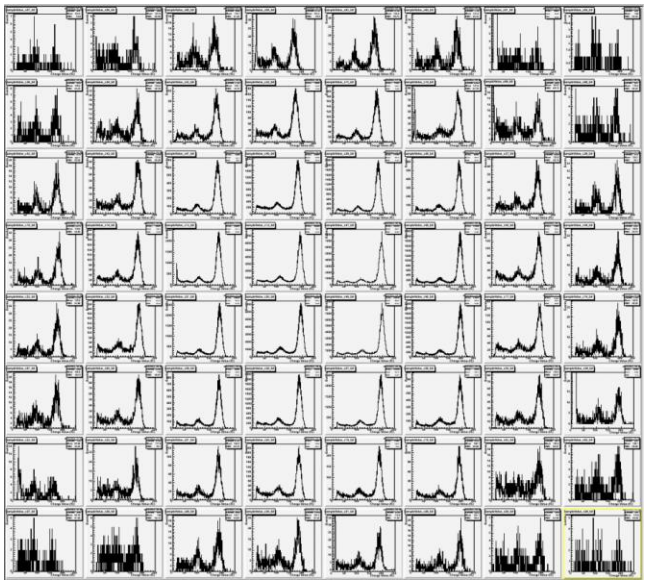
Fig. 1: Schematics of a double-GEM detector.

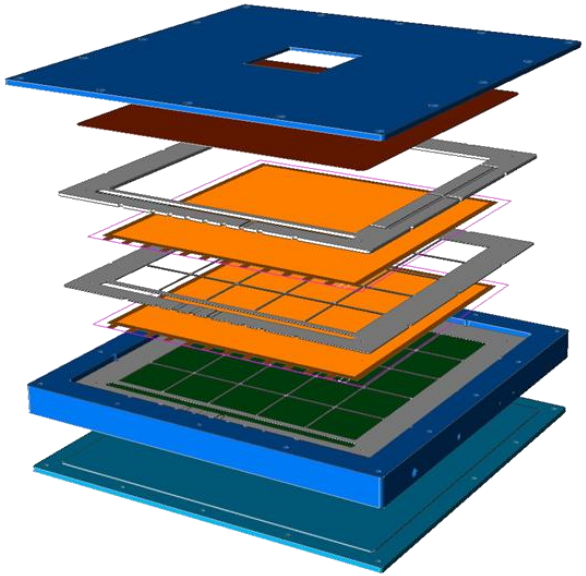
SiD GEM-DHCAL





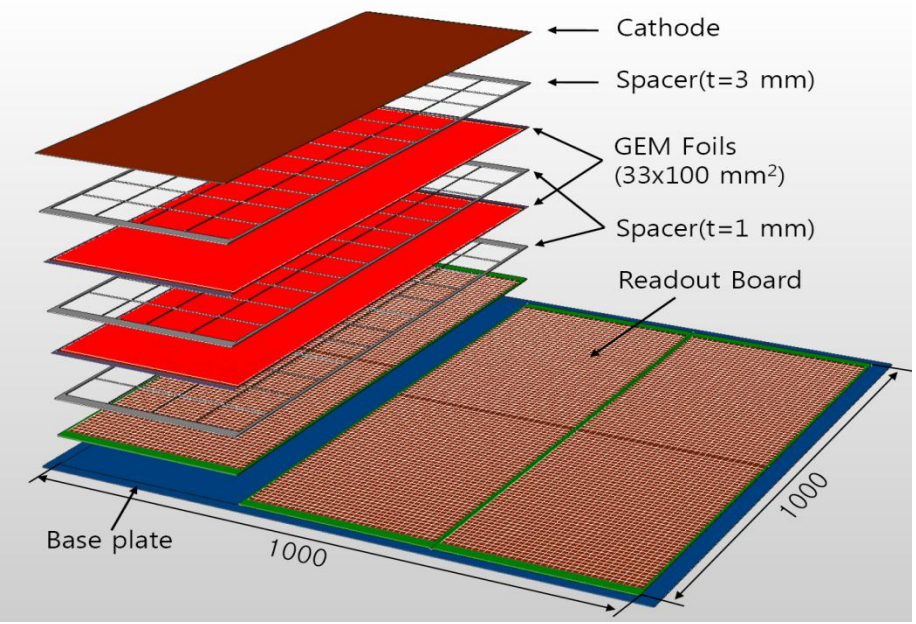
30cm x 30cm GEM-DHCAL prototype





UTA's 100cm x 100cm Digital Hadron Calorimeter Plane

First 5 of 33cmx100cm GEM foils delivered early July, 2010



Phase II ➔ 33cm x 100cm unit chamber characterization

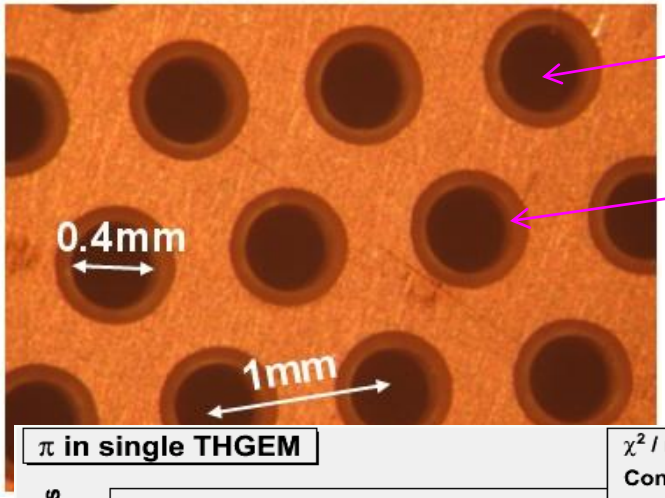
Early 2011 at MTBF: Using available KPiX chips and DCAL chips

Phase III ➔ 100cm x 100cm plane GEM DHCAL performances in the CALICE stack

Early 2011 – Late 2011 at Fermilab's MTBF *or CERN*

Five 100cm x 100cm planes inserted into existing CALICE calorimeter stack and run with either Si/W or Sci/W ECALs, and RPC planes in the remaining HCAL

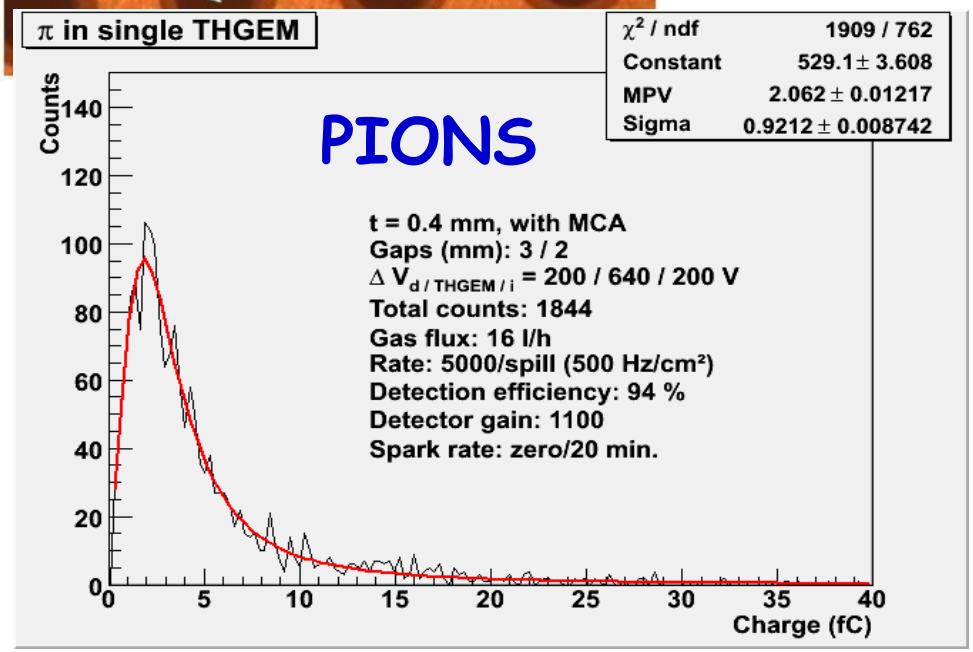
SiD thick-GEM-DHCAL

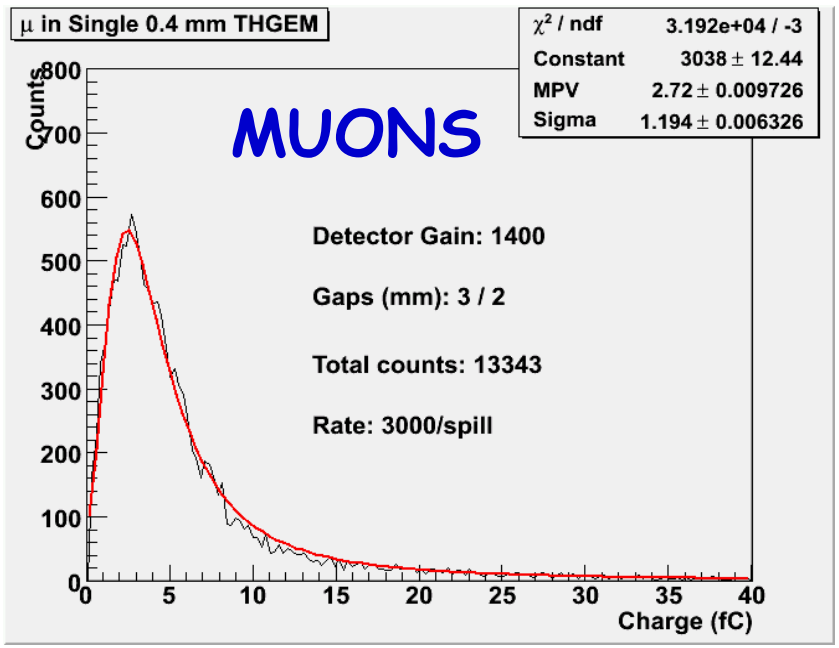


drilled

etched

- PCB Based GEM ➔ Cost effective
- 0.5 – 1mm thick PCBs
- Drilled 0.4mm holes with 1mm pitch
- Expected to have higher gain per GEM
- 10cmx10cm tested, up to 30cmx30cm produced





Measured very low discharge rates even with pions

Next steps

Calorimetry: HCal

- RPC option -> continue with testing the $1m^3$ stack. beyond the first year. Calorimeter will be exposed to muons and pions and positrons of various energies. The response and energy resolution will be measured together with characteristics of hadronic showers, for Particle Flow Algorithms. R&D for Technical Prototype – 2010-2012.

- GEM option will test its $1m^2$ layers as part of the CALICE hadron calorimeter prototype (2010-2011), and will design and build a complete, integrated layer with minimal thickness and full services. Thick GEM prototypes will also be assembled and tested as large sections of thick GEMs become available. Gas studies for thick GEMs will also continue.

Next steps

Micromegas option -> Test of the 1m^2 chamber in the W-structure with AHCAL: • ~3 weeks (from 3rd Nov 2010) CERN PS T9. • Objective: – First comparison between 1cm^2 pad Micromegas and 3cm^2 scintillating tile layers

- Scintillator/SiPM option -> insertion of the integrated readout layer planes fabricated with the CALICE/EUDET electronics into the CALICE absorber stack. This installation will be followed by the commissioning and exposure of this prototype to a test beam. 2010-2011?

- Homogeneous dual-readout calorimetry -> development of suitable crystals, photodetectors, and associated readout electronics, all in preparation for a demonstration of linearity and energy resolution for hadrons in a test beam, while developing a conceptual design for inclusion of this technology into SiD. 2010-2012?

SiD PFA Development

- Ongoing development of SiD (Iowa/SLAC/MIT) PFA.

- Taking the algorithm apart, checking performance at each step, re-assemble, test.

- Developed more diagnostic tools, performance metrics at each stage -> ready to use.

- Specific study items:

    - Use of first, second cone algorithms

    - Use of E/p matching

    - Improve showering point determination

    - Improved muon finder

    - Improve electron finder for lower energies

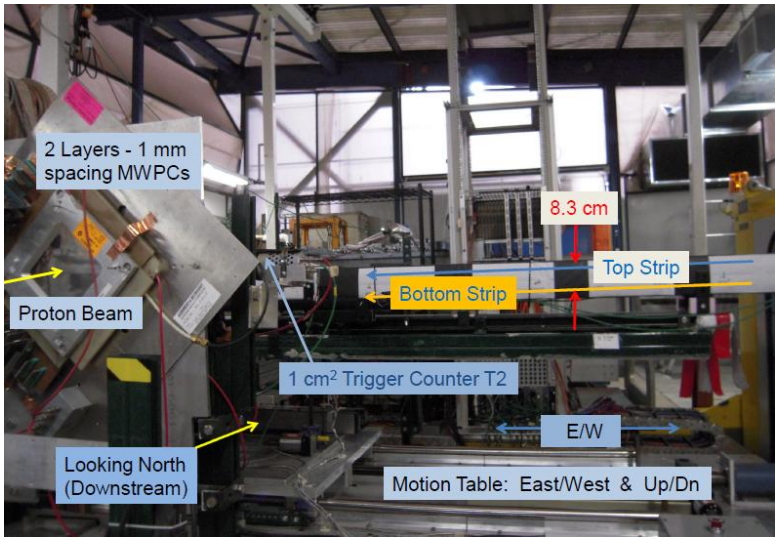
    - Cluster sharing

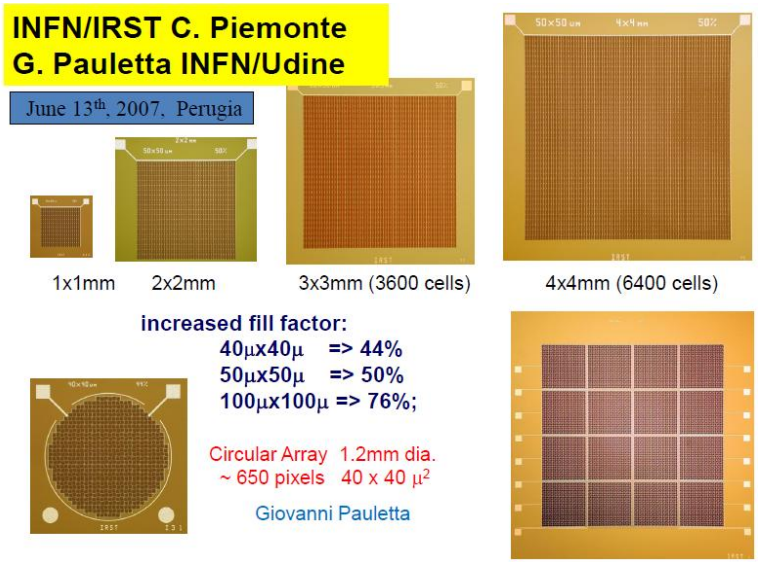
    - ....

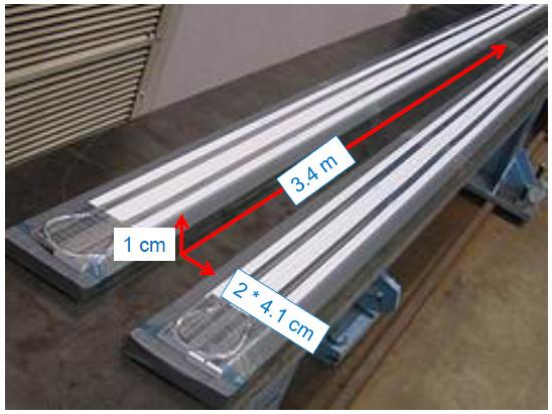
- Timeline for new version – new benchmark studies.

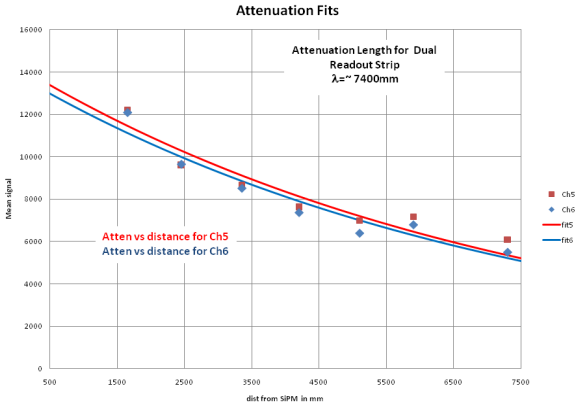
SiD Muon – Scintillator Strips/MPPCs

T-995 Beam Tests at Fermilab MTBF

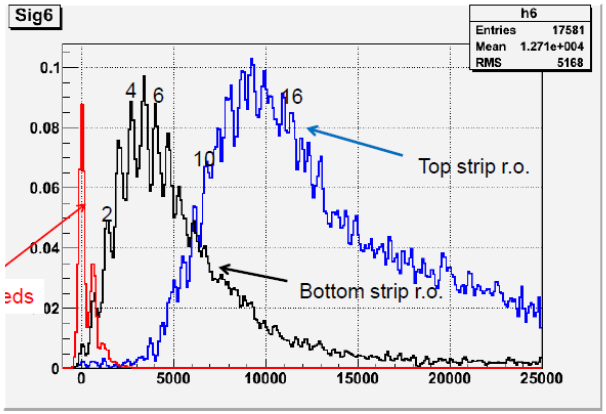








cam in the top strip 10 cm from readout end.



Runs 5045 and 5046 2/20/2010

New double strip with sputtered Al on far end - tested in Sept. – results under study

SiD Muon – Bakelite RPC R&D

- Babar Forward Endcap RPCs – H. Band, U. Wisconsin
  - Similar construction to Atlas/CMS RPCs
  - Wide range of rates/current accumulated over ~ 6 years
- Good overall efficiency but clear signs of aging

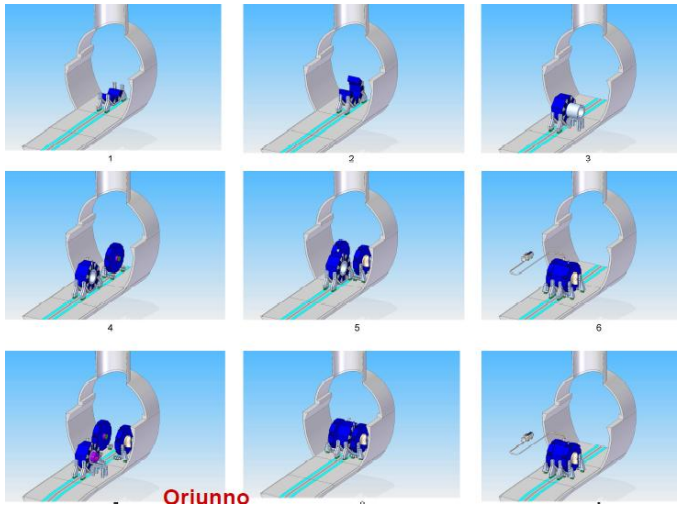
- RPC readout with KPiX chip - previously reported

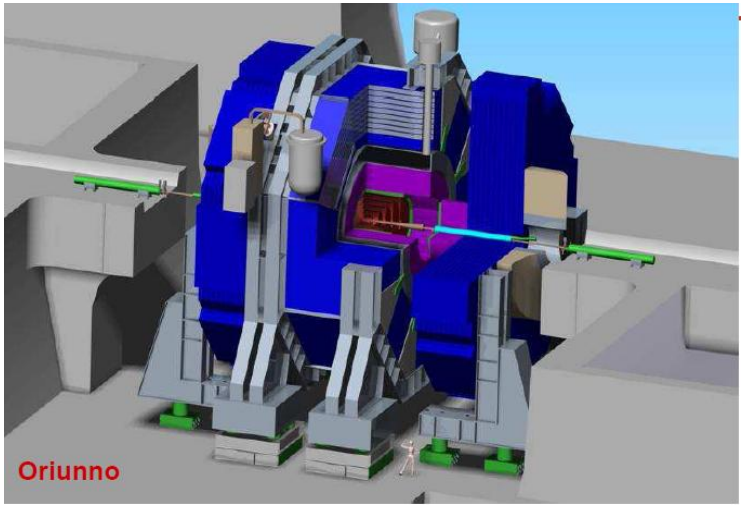
- BESIII/Daya Bay RPCs - C. Lu Princeton U.
  - No linseed oil
  - Accelerated aging studies with ^{60}Co equivalent to many years of cosmic ray rate
  - Sizable eff. losses
  - HV surfaces are vulnerable to HF produced in gas
  - Testing linseed oil impregnated Bakelite
  - Developing thin Bakelite for possible HCAL application

SiD MDI Issues

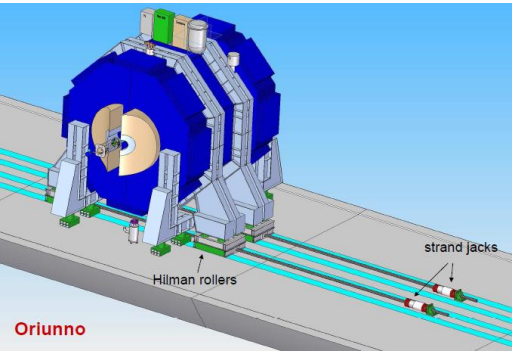
- SiD participates in MDI Common Task Group and works closely with ILD colleagues on push-pull issues.

- Detector assembly and roll-in strategies defined:





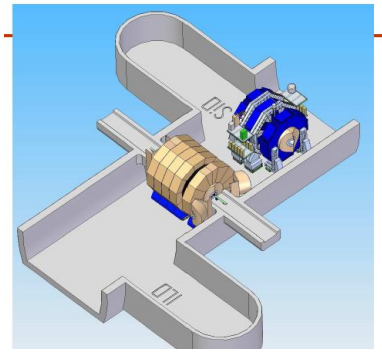
SiD moves into beam position on multi-rollers – position accuracy +/-1 mm



Main issues:

- Height difference
- Preferred detector support mechanism
- Preferred detector motion mechanism
- Interface to machine tunnel
- ...

3) Both detectors on legs?



LCWS10: New results on vibrations, radiation simulations, and magnet studies.

SiD MDI Issues

Vibration Studies in Progress :

FEM model of QD0 on the door
Stability requirements SiD on longer feet
Effect of SiD on Platform

Benchmarking with vibrations measurements on the CMS platform (in progress)

Other benchmarks with vibration measurements on reinforced concrete structures at SLAC. (US-ILC MDI)

Cost estimation of the full push-pull system in progress : w&w/o platform, rollers, jacks, alignment system

MDI Common Tasks WG (ILD+SiD+BDS)

Discussion with ILD of the implications for ILD moving without a platform
Working on the "Push-pull technical specifications", to be finalized in a document for ILC2011 Eugene

Continuation of the studies on the simulation of Radiation dose in the cavern (beam loss). Comparison with Radiation Protection rules for different sites

RF analysis of the SiD experimental beampipe: heat deposition, HO trapped mode, etc.

SiD Detector - Summary

- Moved on from LOI.

- Goal is DBD by 2012.

- DBD is still being defined – this meeting…

- Comprehensive Work Plan defined – completion depends on human and financial resources.

- Ongoing R&D in all subsystems.

- Productive and developing cooperation with CLIC on SiD' for CDR – detector(s) design, benchmarks/physics,…

- DBD and CDR planning and Review of R&D activity at SiD Workshop, University of Oregon, November 15-17, 2010.

- What happens after DBD/2012?