MICROMEGAS sDHCAL status report

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SiD meeting, 16th Nov. 2010

Overview

- MICROMEGAS for hadronic calorimetry
- Expected performance of a 1 m3 calorimeter
- 1 m2 chamber design, assembly and test
- New ASIC, MICROROC
- Plans for 2011

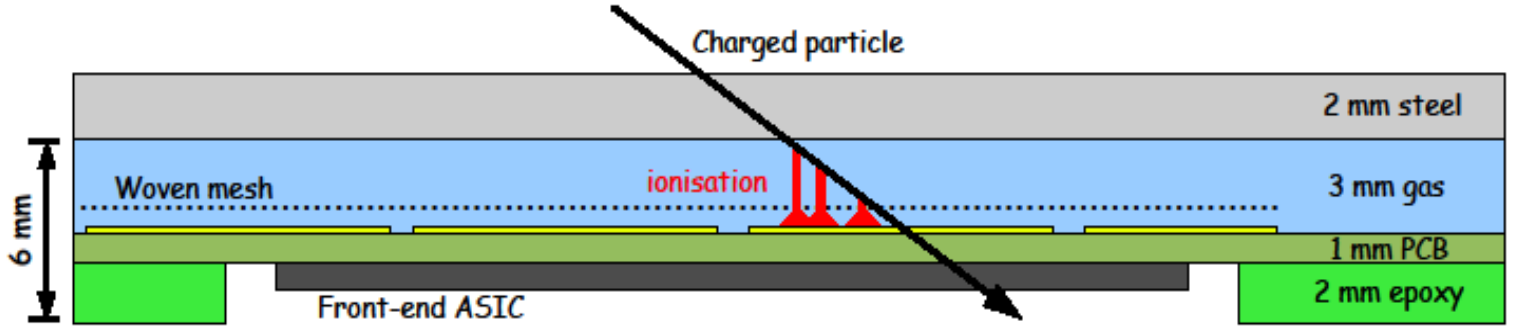
MICROMEGAS for DHCAL

- Bulk technology: robust, large area, CERN workshop, production capability, 10% signal uniformity over 100 cm2
- Non flammable gas mixtures
- Working voltage < 500 V
- Good time resolution (5-10 ns)
- Fast signal and high rate capability
- P/T effects known and real time correction of mesh voltage possible

Advantages for a semi-DHCAL

- Proportional mode: info on N particle crossing a pad useful for semi-DHCAL → improve resolution and linearity @ high energy
- High efficiency with low noise electronics (97% +/- 1%) @ 1.5 fC thr.
- Little diffusion in gas: no crosstalk and multiplicity below 1.1

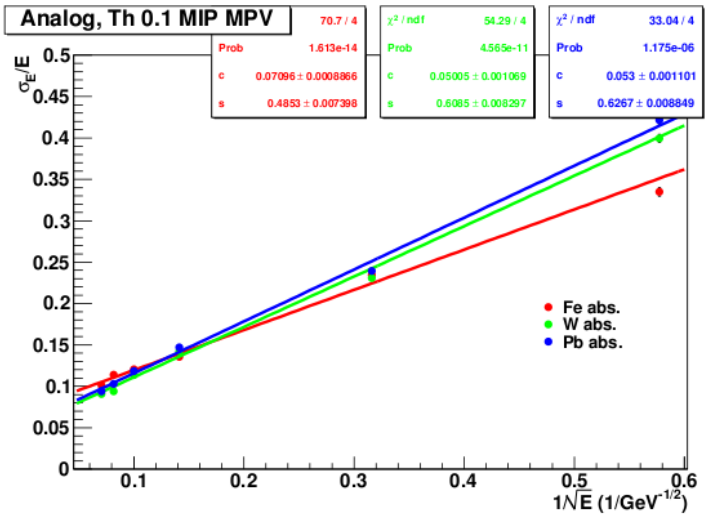
2009 JINST 4 P11023

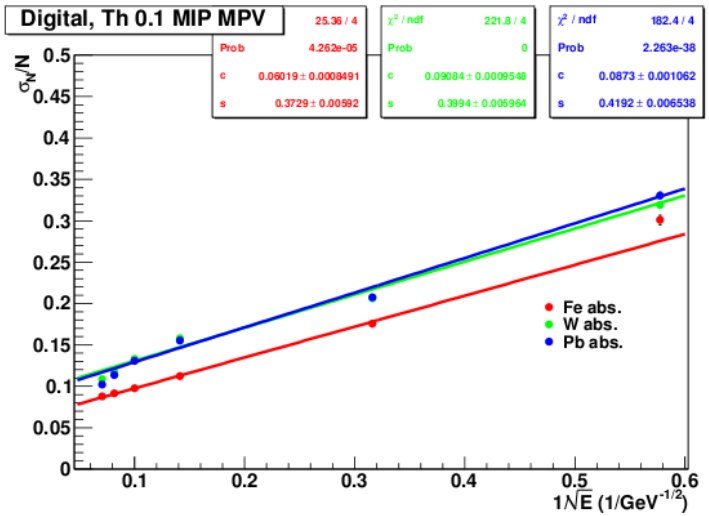


Expected performance

- GEANT4 simulation of a MICROMEGAS DHCAL of 1 m3 (40 layers)
  - Digital readout of gas shows slightly better resolution @ low energy
  - Better linearity of analogue @ high energy (not affected by saturation effects)
  - Similar shower profiles in various absorbers (JINST 4 P11009 (2009))
- For instance, 23% resolution for 20 GeV/c pions in Fe *VS* 30% with analogue

  Non-linearity of 3% at 200 GeV/c in Fe for digital readout
- On-going work: digitization and multi-threshold study





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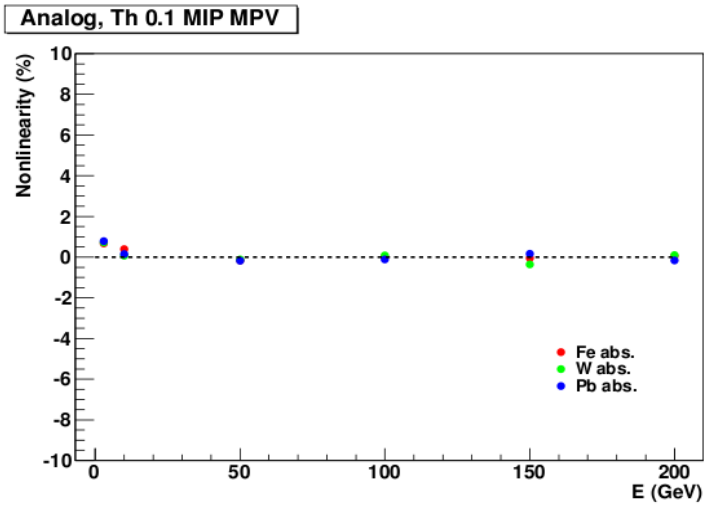
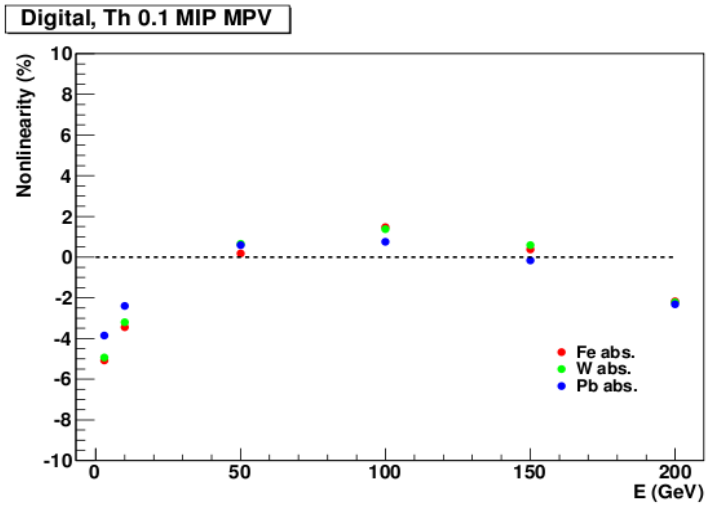
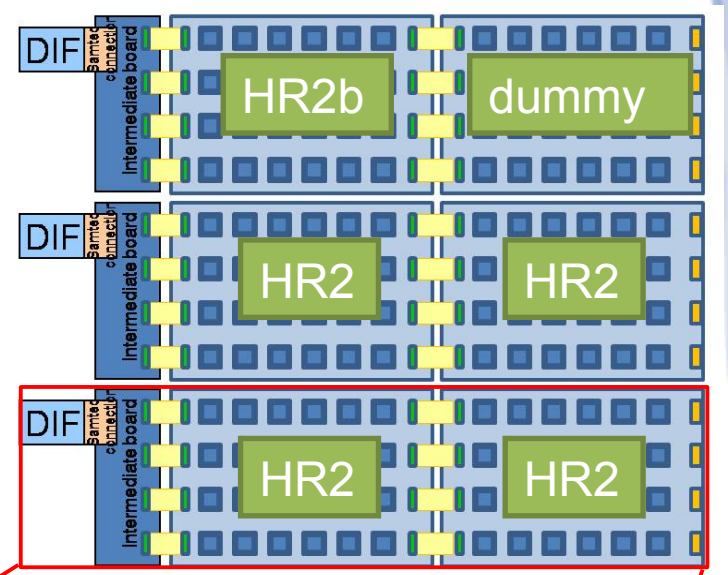
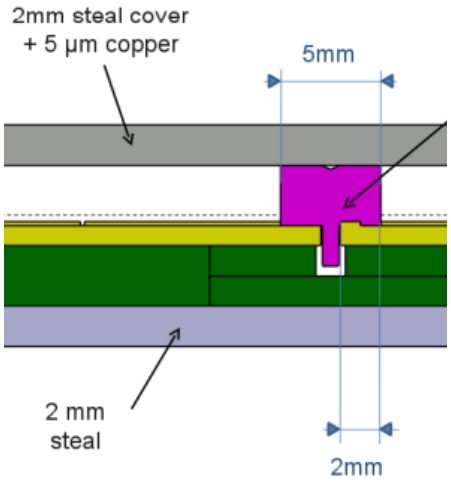


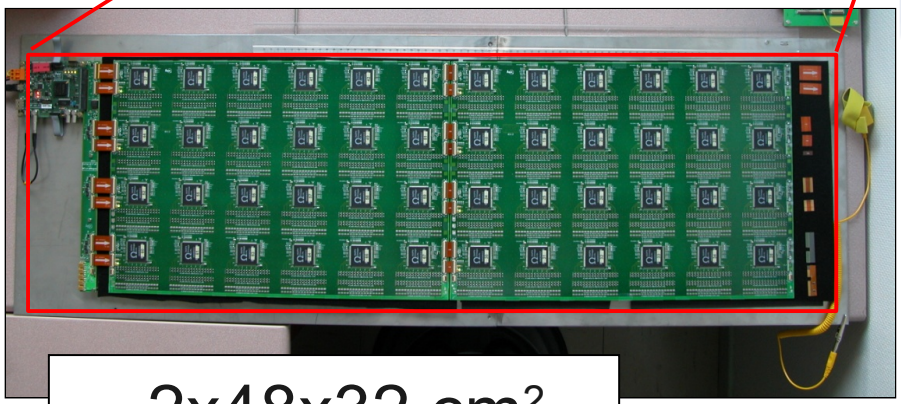


Prototype of 1 m2 - design

- Basic Unit: Active sensor Units of 32x48 cm2
  - 24 HARDROC2 chips (LAL/Omega)
    2-bit readout, power-pulsing capability, fast shaping
  - Spark protections (resistances, diodes)
  - 1 Bulk (mesh) with 1 cm2 pads
- Design of the 1 m2 prototype: 3 SLAB of 2 ASU
  - Minimal dead regions (2%) between ASU
  - Total thickness of 8 mm + 2*2mm steel covers
- Assembly validated with a mechanical prototype early 2010
- Assembly with 5 ASU in May 2010

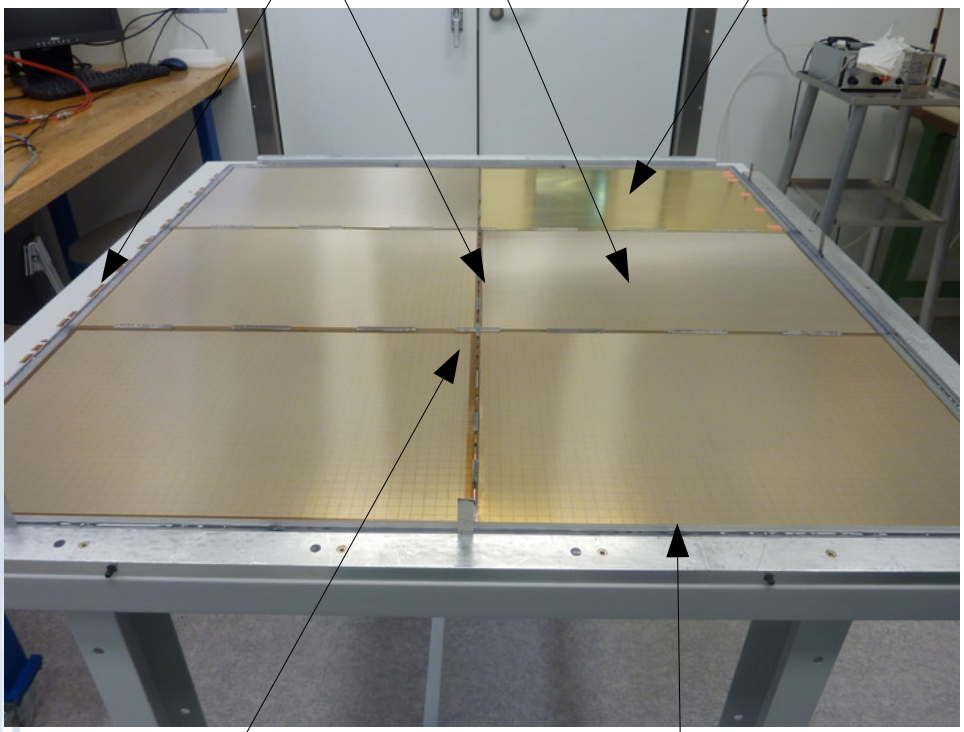


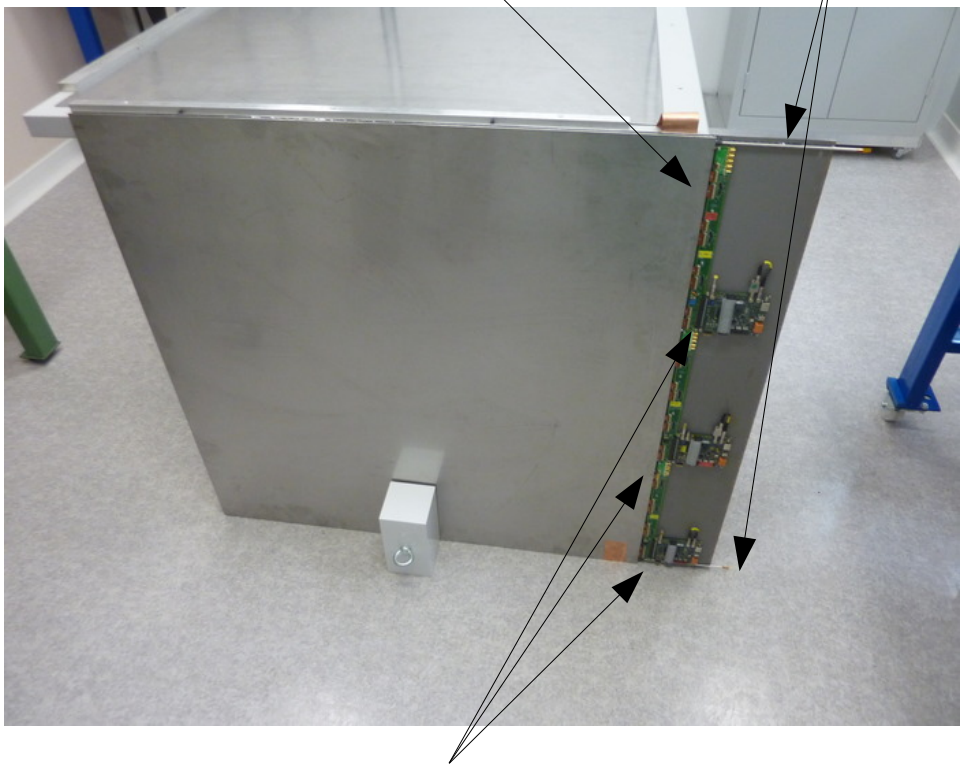




2x48x32 cm^2

Prototype assembly

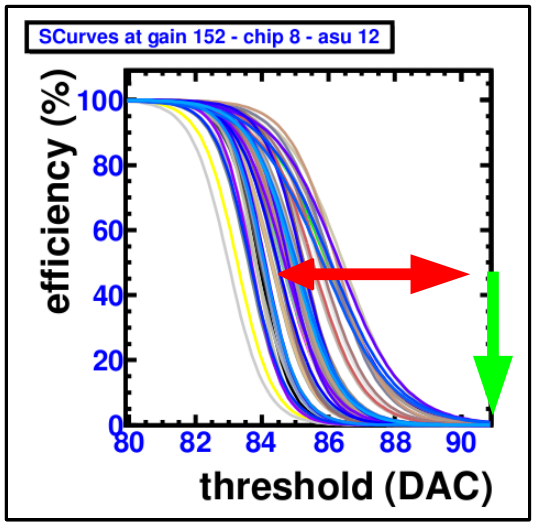


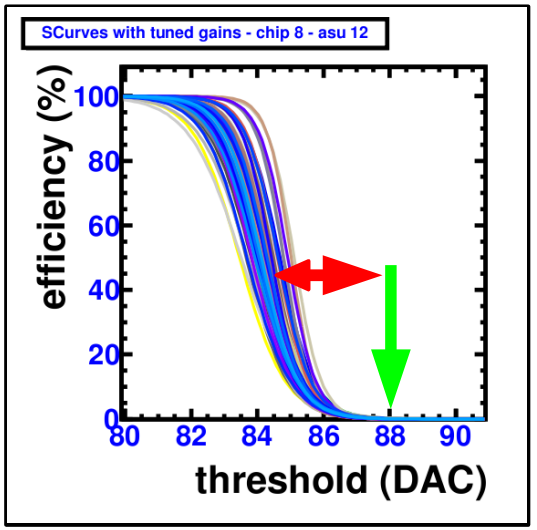


HARDROC2 chip settings

- Fast shaping of HARDROC2 chip (80% of signal wasted)
- Set thresholds as low as possible
  - Shift channel pedestals by varying individual preamp gains
  - Increase non-uniformity BUT reduces individual thresholds
- Eventually, thresholds about 5 fC (still to be worked out precisely)
  To be compared to 20 fC * 20% (= MIP MPV * shaped signal fraction)
  = 4 fC at maximum mesh voltage

Minimum global threshold of 7 DAC ~ 10 fC

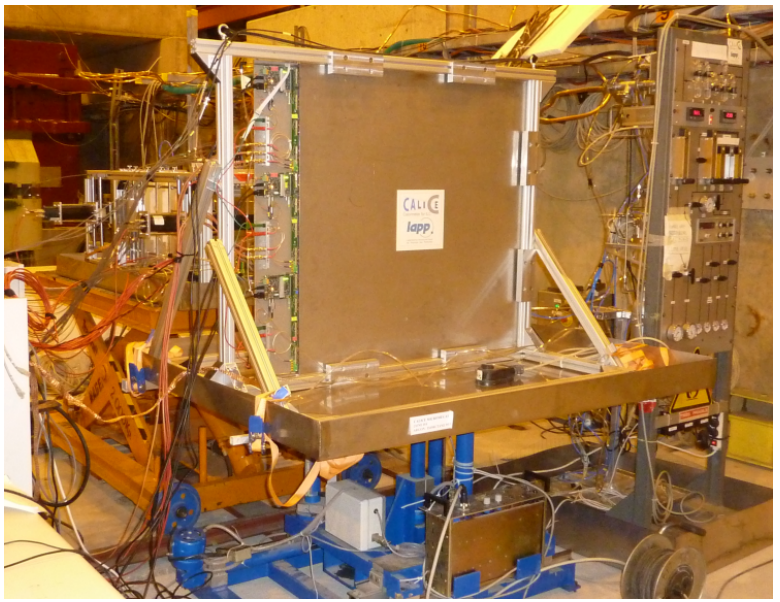




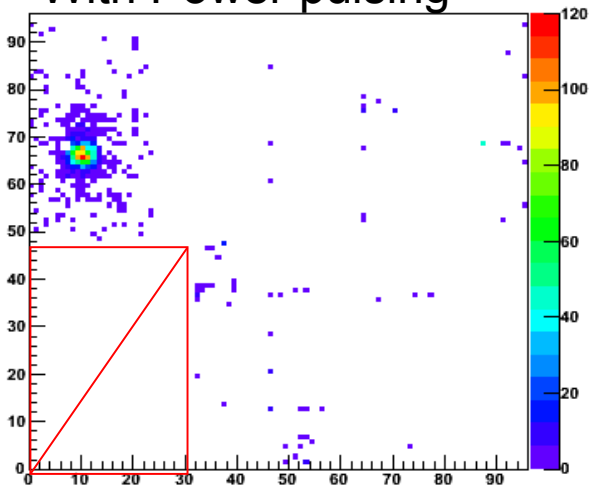
Minimum global threshold of 3 DAC ~ 5 fC

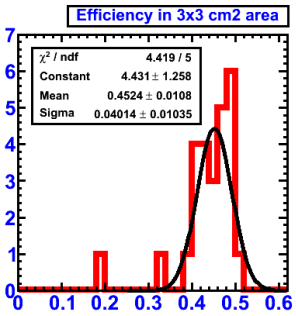
Prototype test in beam (I)

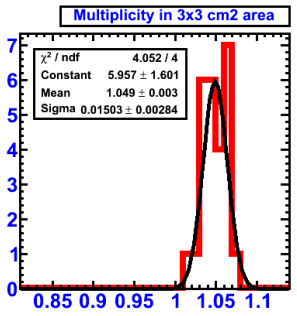
- SPS/H4, 150 GeV muons, low intensity < 1kHz over 5x5 cm2, June/July 2010
- Telescope with small GASSIPLEX chambers
- Acquisition rate ~ 100 Hz
- Time-stamping with 200 ns clock, use time to trigger to suppress noise hits
- Efficiency of 45 % with 5 % variations over a chip
- Multiplicity of 1.05 with 0.02 variations
- Lot of data collected with beam impinging on several chips
- Power-pulsing of the analogue part all chips (~3 A)
- Several technical choices validated
- Potential improvements for next prototype found



With Power pulsing



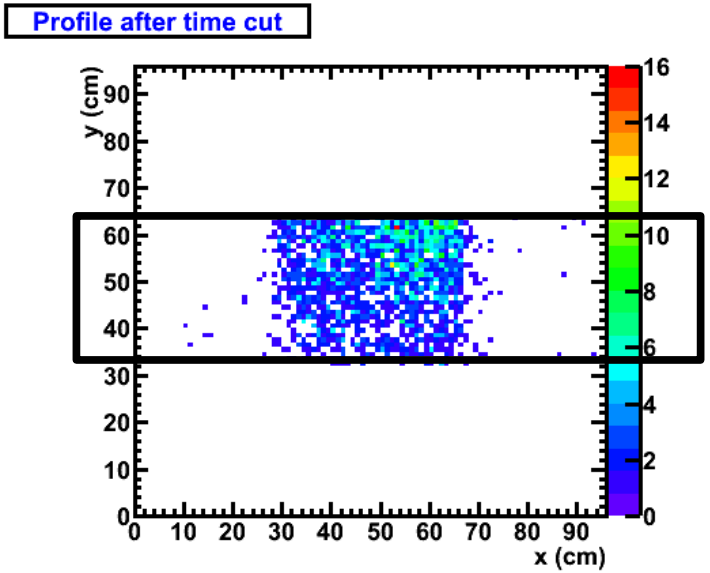




Prototype test in beam (II)

- Insertion of the prototype inside the W-CLIC structure
  - 30 layers of scintillators (AHCAL)
  - MICROMEGAS acts as last layer
  - Started mid October in PS/T7 (muons)
  - Recently shifted to PS/T9 (hadrons)

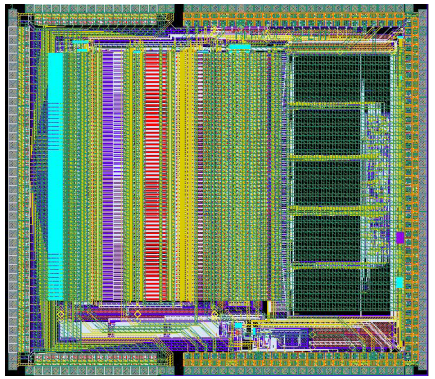
- Goals
  - Detect shower tails
  - Use info. From AHCAL
    → synchronization between 2 DAQ for common event numbering and off-line reconstruction (P. Dauncey, G.Vouters)
  - Synchronization with other detectors (GRPC) will be useful for test in steel or tungsten m3 structure next year



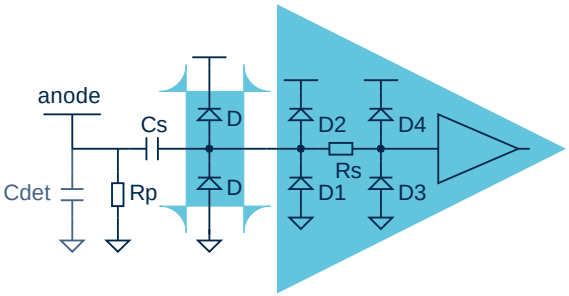
Muon beam profile on center slab recorded shortly after installation in T7(other slab off, scintillator geometry visible)

New ASIC, MICROROC

- Modify input stage of HARDROC2 while keeping the digital part the same: Micromegas Readout Chip
  - Longer shaping time
  - On-chip spark protection
  - Pin-to-pin compatible with HR2
  - Collaboration with LAL/Omega group
  - (could be interesting for GEM DHCAL)



- Features: charge preamp., variable shaping time up to 200 ns, 3 thresholds, 400 fC dynamic range, noise rms of 0.24 fC



- Multi-project wafer run → 360 chips available
  - 25 chips ordered so far
  - Very low noise on test board (1 fC input charge detected)
  - More characterisation test on-going

Future plans

- Assembly of new chambers with MICROROC
  - Order and test all available MICROROC
  - Produce 12 ASU with 24 chips each
  - Assemble 2 chambers of 1 m2
- Depending on funding for 2011(to be decided very soon)
  - Order more chips (2 multi project wafer runs)
  - Build 3 more plans → would make 5 in total
  - Uncertain today...
- Beam request in 2011
  - 1 month at SPS/H4 in July/August (RD51 and CALICE requests)
  - At least 2 weeks inside steel and tungsten m3 structure at the end of the year (CALICE request)
- Maintain efforts towards development of CALICE DAQ