Cosmic-ray measurements of scintillator tiles with SMD SiPMs

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Outline

- Cosmic-ray measurements for SMD design
 - Aim: SMD SiPM response to MIPs
 - Hamburg tile as a reference
 - SiPM: side-surface mounted
 - Dimpled tiles produced in Uni-Mainz
 - SMD SiPM: bottom-surface mounted

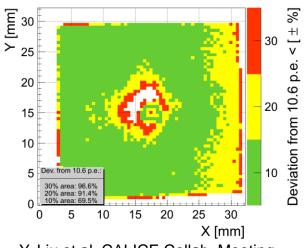
Summary and discussions



HBU in SMD SiPM design

Motivations

- Much easier to solder on HBU (feasible for mass assembly)
- Uniformity in SMD design
 - Scan in MPI Munich shows promising results
 - Updated dimple design
 - Suitable for various SiPM packages
 - Updated Geant4-based simulation
 - shows good uniformity



Y. Liu et al, CALICE Collab. Meeting, LAPP, Annecy, Sep 2013

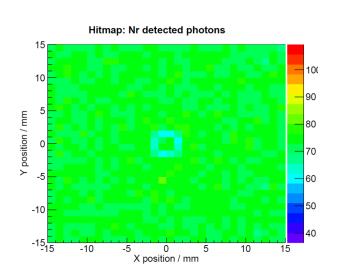


Simulation: cosmic-ray response & uniformity (1)

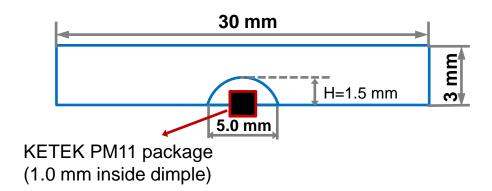
Scintillator: BC408

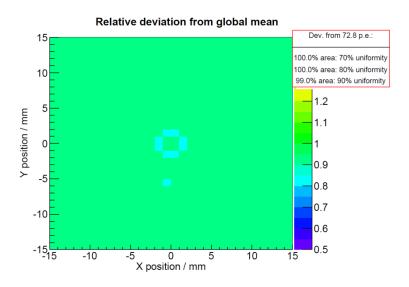
 SiPM: KETEK PM1150NT (1.2x1.2mm², 50µm pixel pitch)

SiPM Vop: 15% overvoltage



Mean 72.8 p.e.



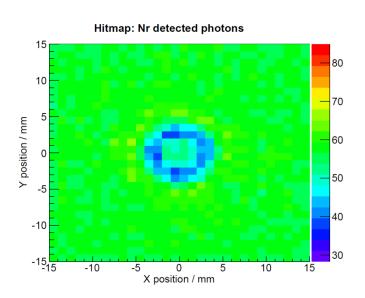


99.0% area within 10% deviation

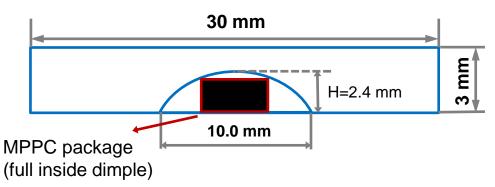


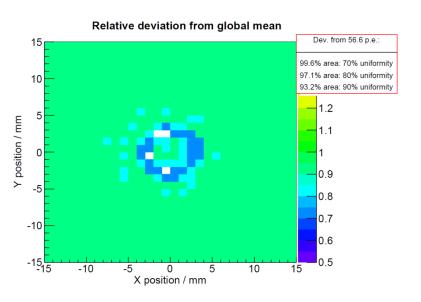
Simulation: cosmic-ray response & uniformity (2)

- Scintillator: Polystyrene (for NA62 MUV)
- SiPM: MPPC S10931-50P (3x3mm², 50µm pixel pitch)
- SiPM Vop: 72.61V (suggested)



Mean 56.6 p.e.





93.2% area within 10% deviation

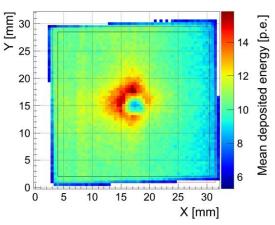


SiPM response to MIP

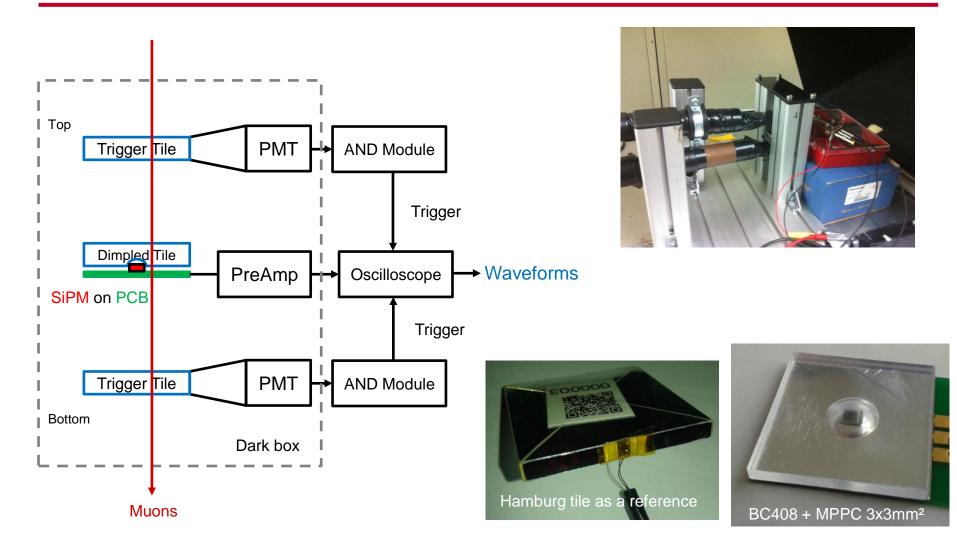
- SiPM response in uniformity scan in MPI, Munich
 - Low level: mean 11 p.e.
- Cosmic-ray teststand in Uni-Mainz
 - Measure mean N(p.e.) for MIPs
 - More scintillator options
 - Polystyrene for NA62: easy to handle
 - BC408: ~1.6 times higher intrinsic light yield



- Will be ready for next round of cosmic-ray measuremnt
- Foils for this round
 - Pieces of 3x3cm²: precisely cut by (mechanical engineer) Karl-Heinz in Uni-Mainz

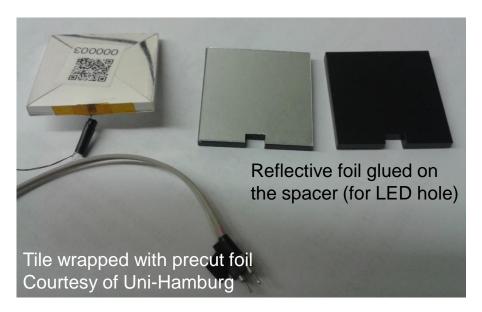


Cosmic-ray setup

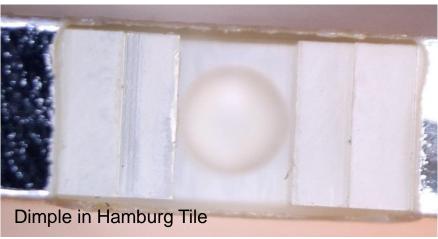


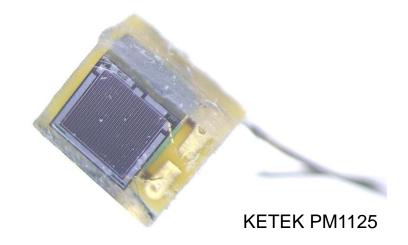


Hamburg tile + KETEK PM1125



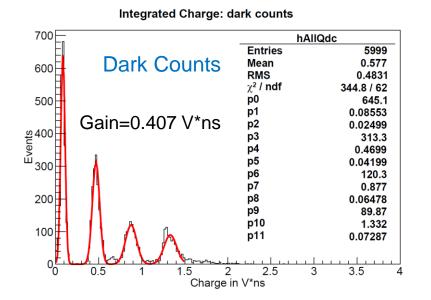
- Use Hamburg tile wrapped with pre-cut foil as reference
- Latter SMD design can be directly compared: less or more Npe?

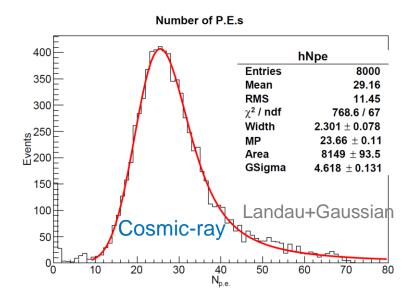




Cosmic-ray: Hamburg tile+KETEK 1.2x1.2mm²

Operational voltage: 31.0 V (~15% overvoltage)





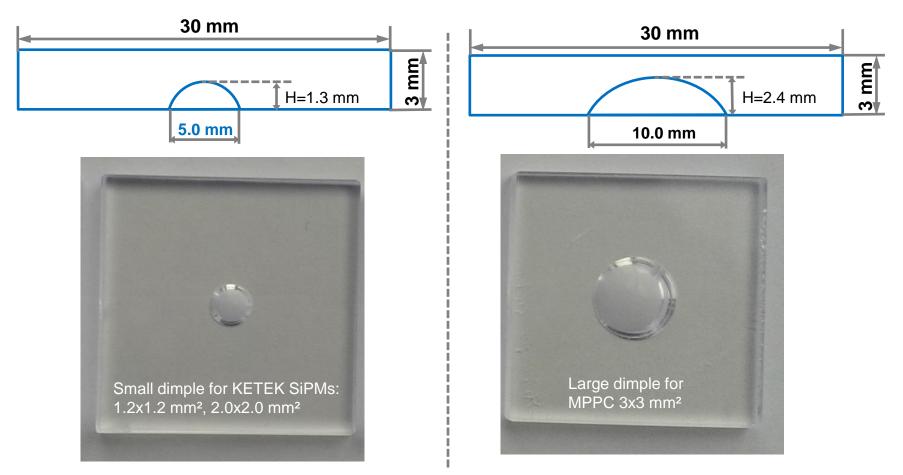
- Side-surface design: mean 23.7 pe in cosmic ray
- Consistent with Uni-Hamburg measurement (reponse to MIP)

Ref: M. Ramilli et al, Tile test and production at Hamburg, AHCAL Meeting, Dec. 2013



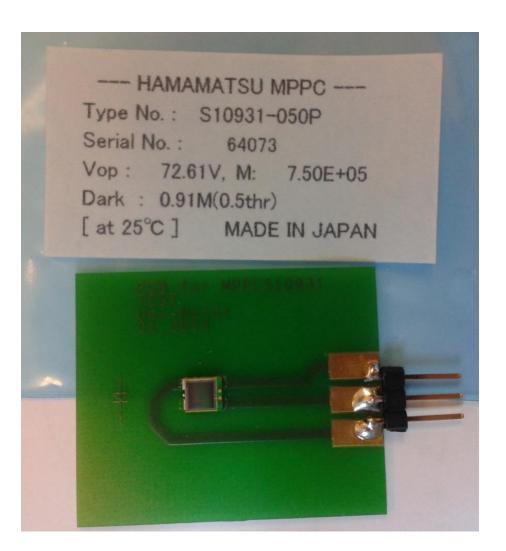
Design of dimpled tiles

- 2 scintillator materials: BC408, Polystyrene for NA62
- Machined by mechanical engineer Karl-Heinz in Uni-Mainz





PCB with SMD SiPM soldered on(1)

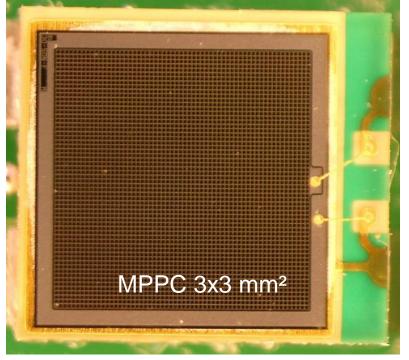


MPPC S10931-50P

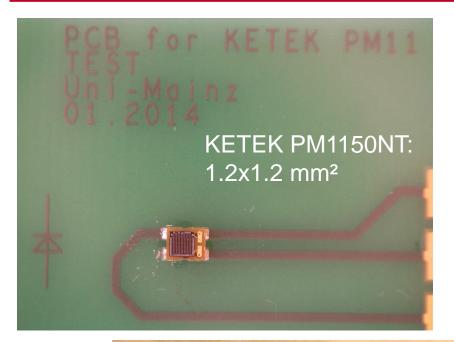
Pixels: 3600

Pixel size: 50x50 µm

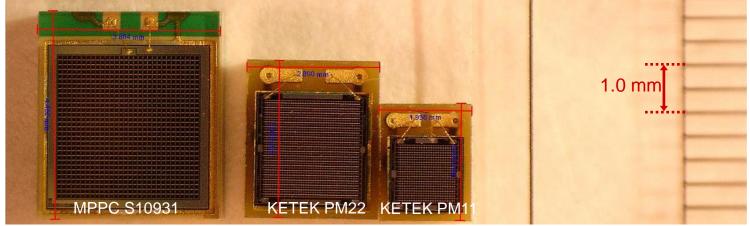
Fill Factor: 61.5 %



PCB with SMD SiPM soldered on (2)

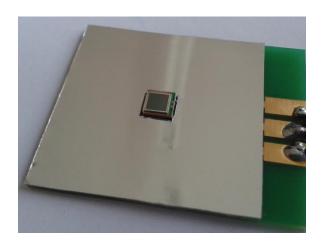




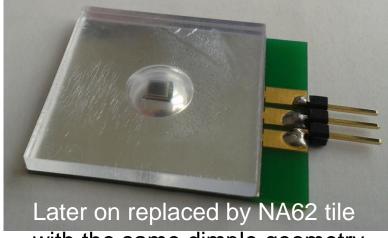


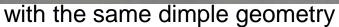


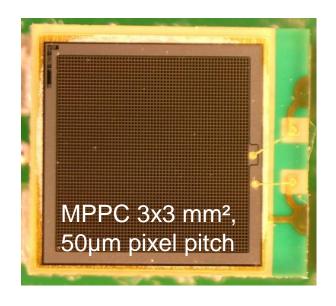
Setup: Dimpled tile with MPPC 3x3mm²

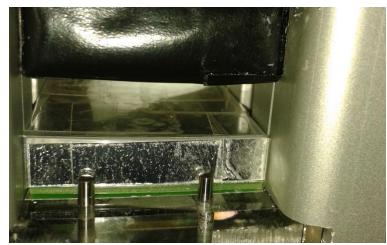


Dimpled tile: BC408



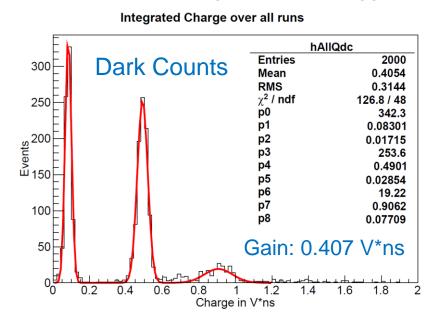


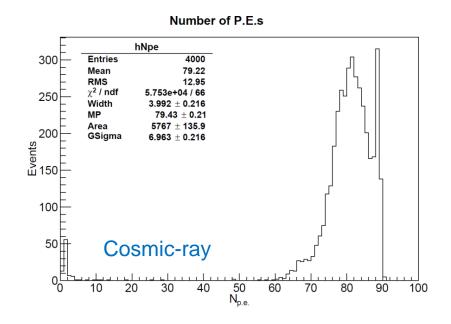




Measurements: BC408 with MPPC 3x3mm²

Operational voltage: 72.61 V (suggested)



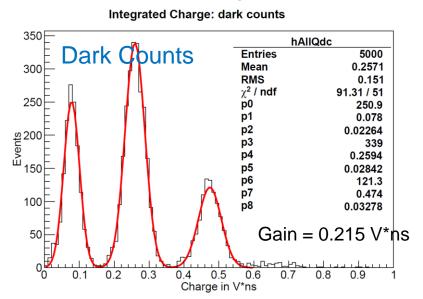


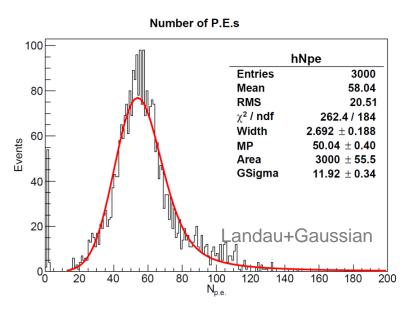
- Saturation observed
 - Too many p.e.s: SiPM pulse higher than output range of preamplifier
- Mean ~80 p.e., high enough reponse to MIP
- SMD MPPC package can be completely placed inside dimple
 - Perfect for mass assembly



Measurements: NA62 tile with MPPC 3x3mm²

Operational voltage: 71.8 V

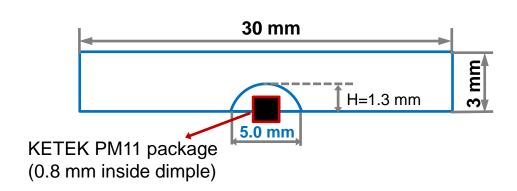




- For less saturation with the given preamplifier
 - Decrease operation voltage by 0.61V
 - Change to scintillator with lower light yield
- Mean ~50 p.e., MIP response still high enough
- SMD MPPC package can be completely placed inside dimple
 - Perfect for mass assembly

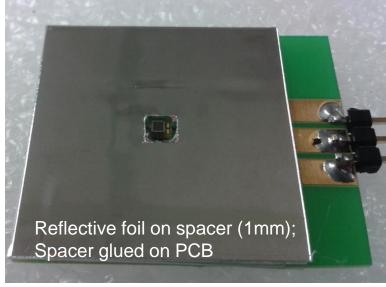


Setup: BC408+KETEK PM11



- KETEK Package thickess: 1.8mm
 - Too thick for 3mm thick tile
- Spacer (1mm thick) used to keep part of SiPM package ouside dimple
 - For better uniformity and higher reponse, suggested by simulation
- Window in foil cut by knife
 - Will be improved by better stamp tool

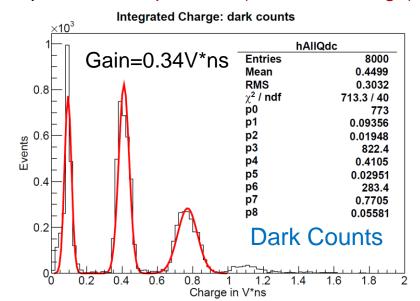


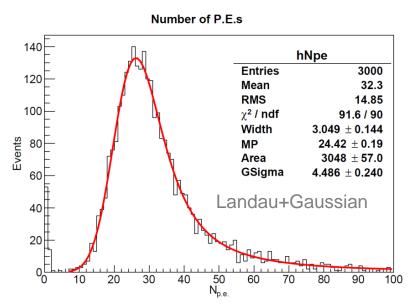




Results: BC408+KETEK PM1150NT

Operational Vop=30.0V (~6% overvoltage)





- For less saturation: only use ~6% overvoltage
- Mean 24.4 p.e. measured in cosmic ray
 - ~33.5 p.e. can be foreseen at 15% overvoltage (based on KETEK PDE vs overvoltage)
 - Side-surface design: 23.7 p.e.
- Similar scintillator and SiPM sensitive area
 - SMD design yield higher reponse to MIP than side-surface design



Summary

- Uniformity of SMD design
 - Measurements show promising uniformity
 - Geant4 simulation suggest great uniformity
 - At least 93% area within 10% deviation
- Responses of SMD design to cosmic ray
 - At least 50 p.e. when MPPC 3x3mm² is used
 - Higher reponse (>24.4 p.e.) to MIP than side-surface design (23.7 p.e.)
- Mainz group will proceed to design and build prototype of HBU with SMD SiPMs



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Discussions

- HBU in SMD design
 - Dependent on SiPM package size
 - KETEK
 - Too thick (1.8mm); not possible to be placed in the dimple made for 3mm thick tile
 - Need to discuss packaging with KETEK
 - Hamammatsu
 - Thin enough to be soldered on HBU and placed inside dimple
- What N(p.e.) should we design for?
 - 1.2x1.2mm² SiPM: 24.4 p.e. at 6% ov
 - (35.5 p.e. estimated at 15% ov)
 - 3x3mm² SiPM: ~80 p.e.



Thank you!







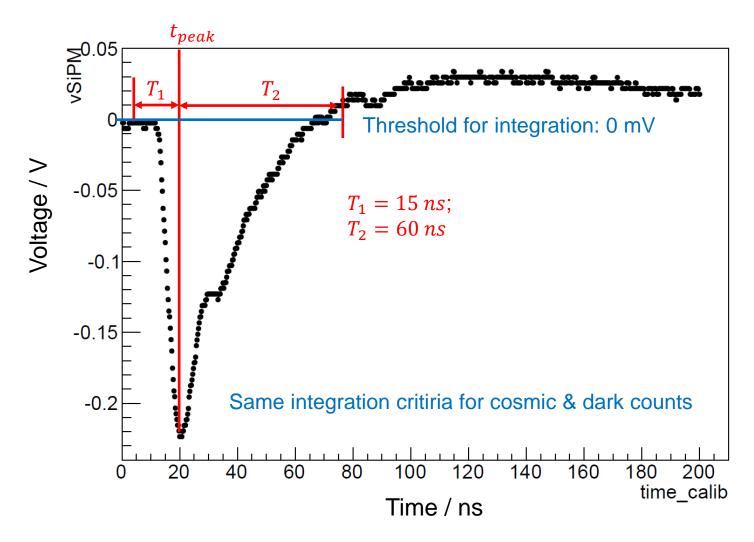
Backup slides







Analysis of SiPM waveform in osciloscope

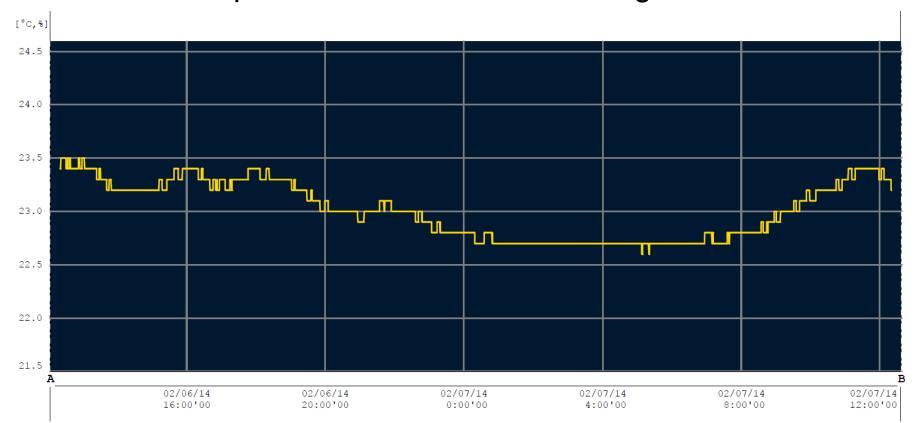






Temperature fluctuations

- Within 1 degree during 24 hours
 - Several percent flucturation in SiPM gain



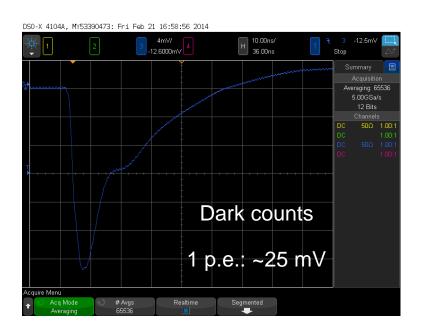


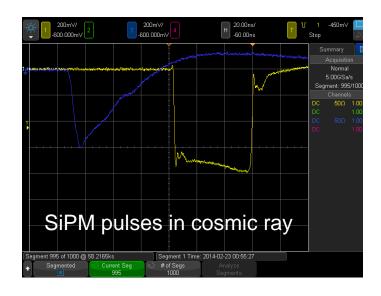
Status: Hamburg tile with KETEK PM1125

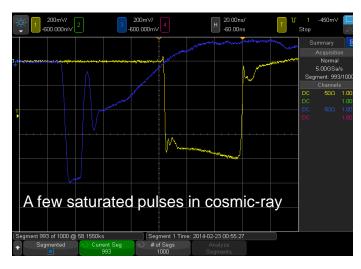
Dimpled tile with KETEK PM1125

Vop=31.0 V (~15% overvoltage)

Breakdown voltage: ~27V Amplification Rf=5.1k Ohm









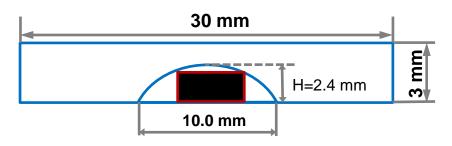
Status: BC408 with MPPC 3x3mm

Dimpled tile with MPPC S10931

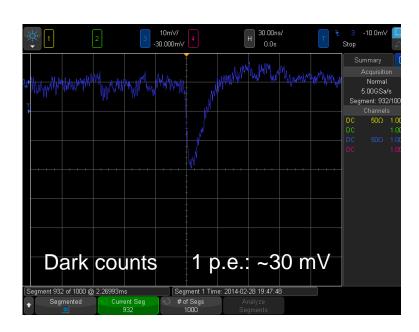
Vop=72.61V (suggested)

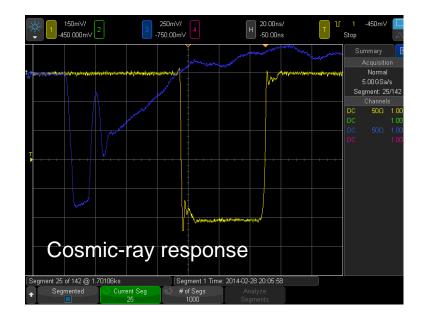
Breakdown voltage: not yet tested

Amplification Rf=5.1k Ohm



Driller Diameter: 13.0 mm







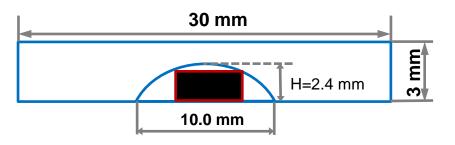
Status: NA62 tile with MPPC 3x3mm

Dimpled tile with MPPC S10931

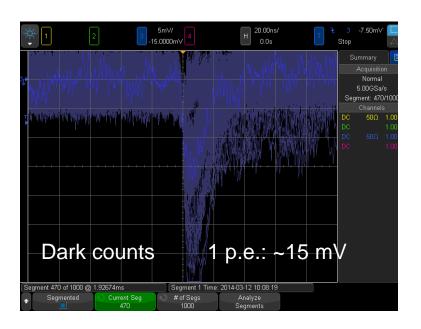
Vop=71.8V (0.81V lower than suggested)

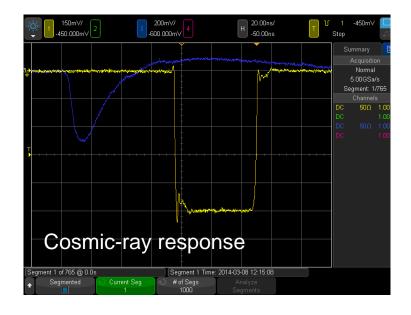
Breakdown voltage: not yet tested

Amplification Rf=5.1k Ohm



Driller Diameter: 13.0 mm







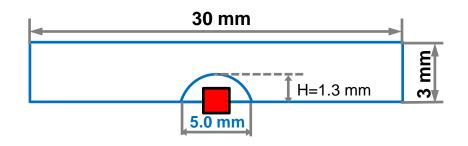
Status: BC408 + KETEK PM1150NT

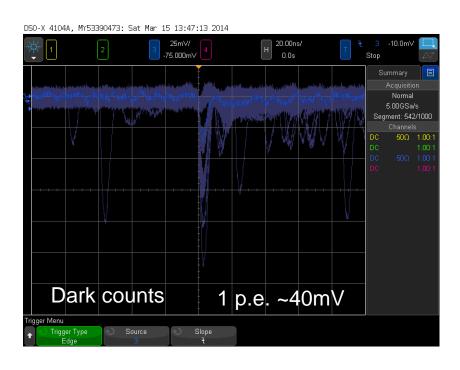
Dimpled tile with KETEK PM1150

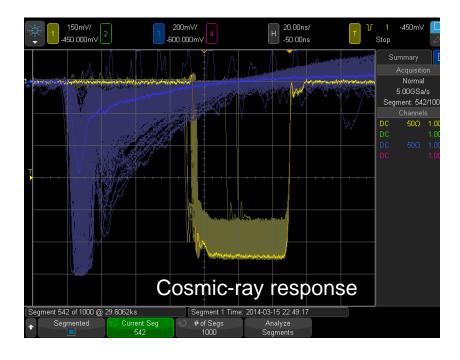
Operational Vop=30.0V (6% overvoltage)

Breakdown voltage: Vbr = ~28.3 V

Amplification Rf=2.4k Ohm (modified)



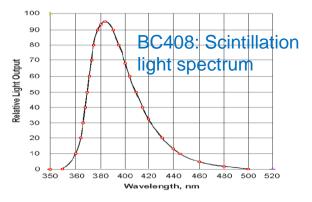






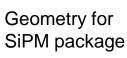
Details on Simulation (1)

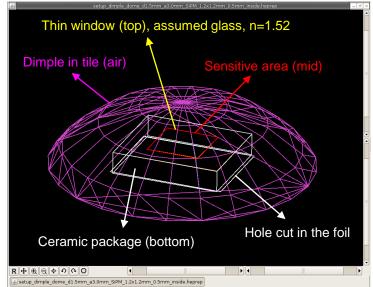
Simulation: scintillator tile, dimple and surface



Optical boundary model: polished in UNIFIED Model

Measured curve:





ESR reflectivity vs wavelength

CRESST experiment

CRESST experiment

or scintillating side VM2000

or scintillating side VM2000

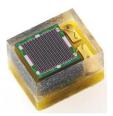
wavelength [nm] Plot courtesy of Frank Simon



Details on Simulation (2)

Simulation of SiPM PDE





KETEK PM1150NT SMD: 1.2x1.2 mm² Pixel size: 50x50 µm² 576 pixels (24x24)

