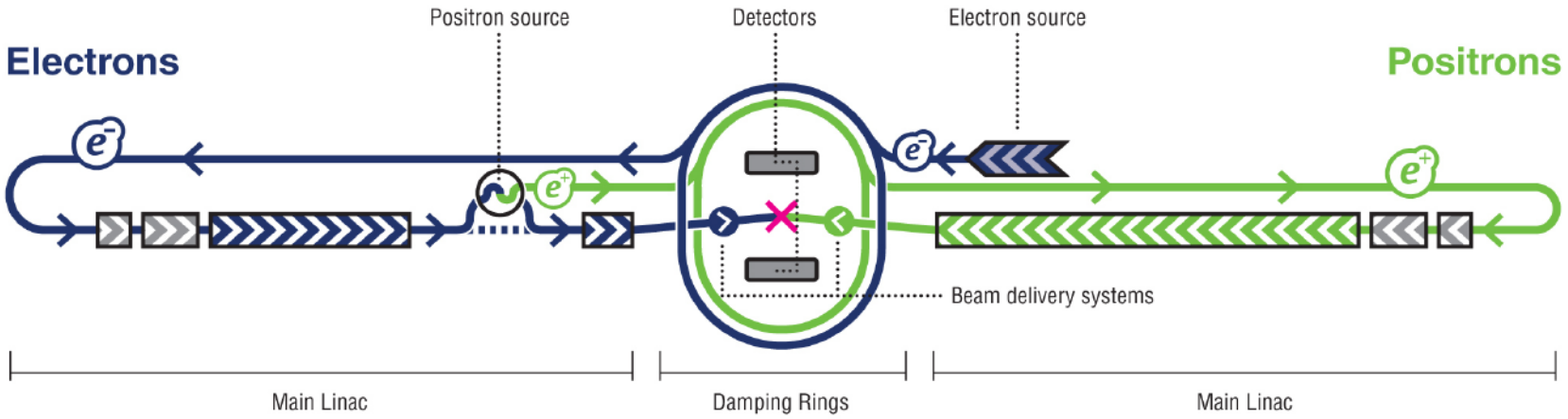
Recent development in FE electronics - PUC

Angel Abusleme
Pontificia Universidad Catolica de Chile

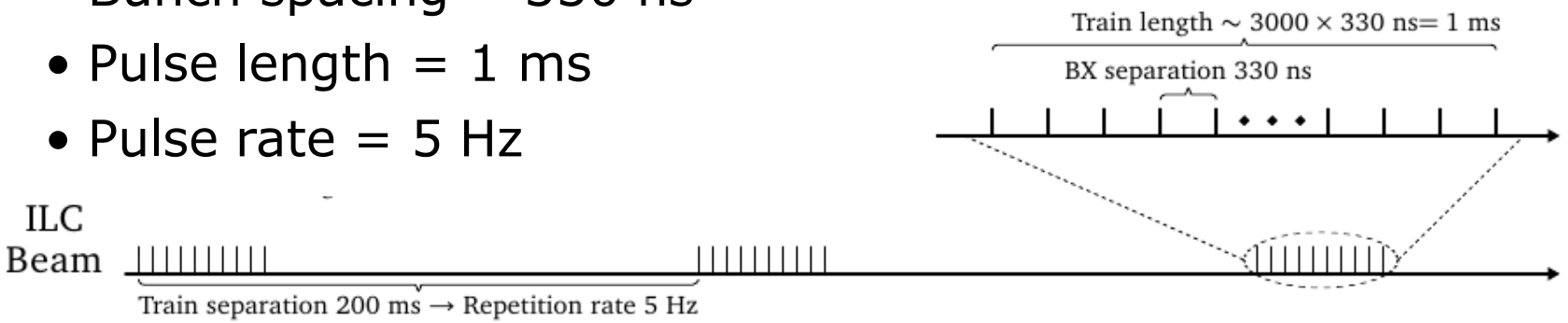
25th FCAL Meeting

October 12-13, Belgrade, Serbia

The ILC: Layout and beam structure



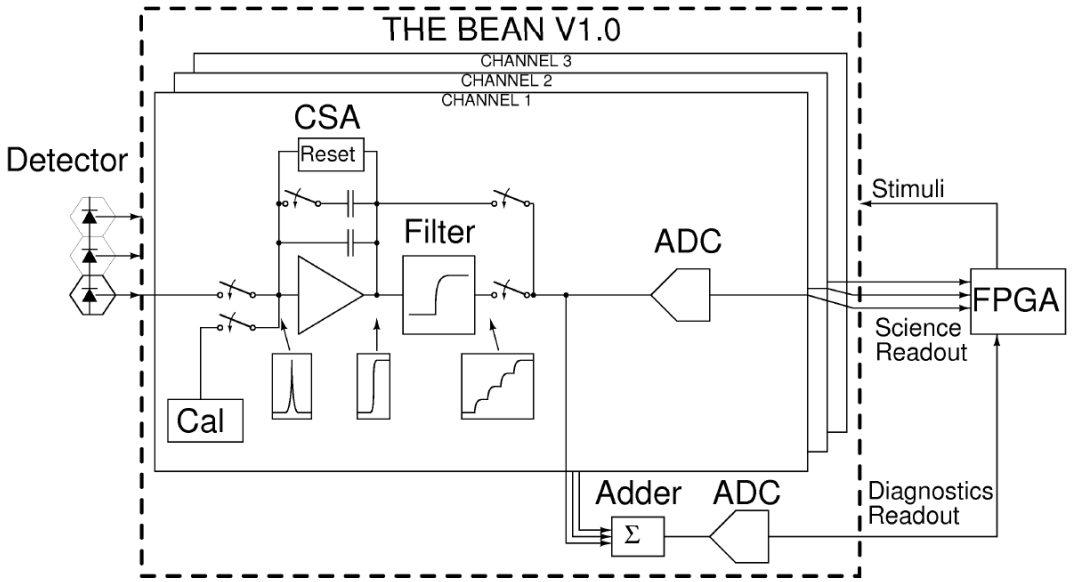
- Center-of-mass energy = 500 GeV
- Peak luminosity = 2 x 10^{34} $cm^{-2}s^{-1}$, particles per bunch = 2 x 10^{10}
- Bunch spacing = 330 ns
- Pulse length = 1 ms
- Pulse rate = 5 Hz

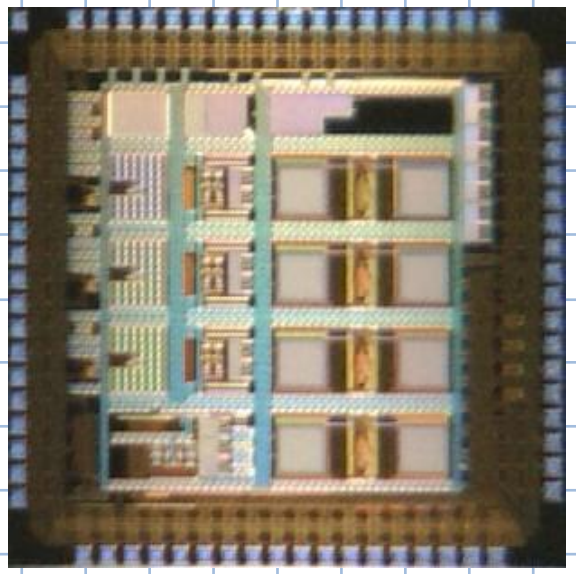


Outline

- The Bean V1.0 (2010)
  - 3-channel Readout chain in 180nm (2010), tested
- ADC linearity compensation (2012 – 2013)
  - Intentionally nonlinear ADC to correct CSA linearity
- Arbitrary weighting function synthesis (2013 – 2014)
- Intentionally nonlinear ADC (ongoing work)

The Bean V1.0: 3-channel readout chain in 180nm (2010)

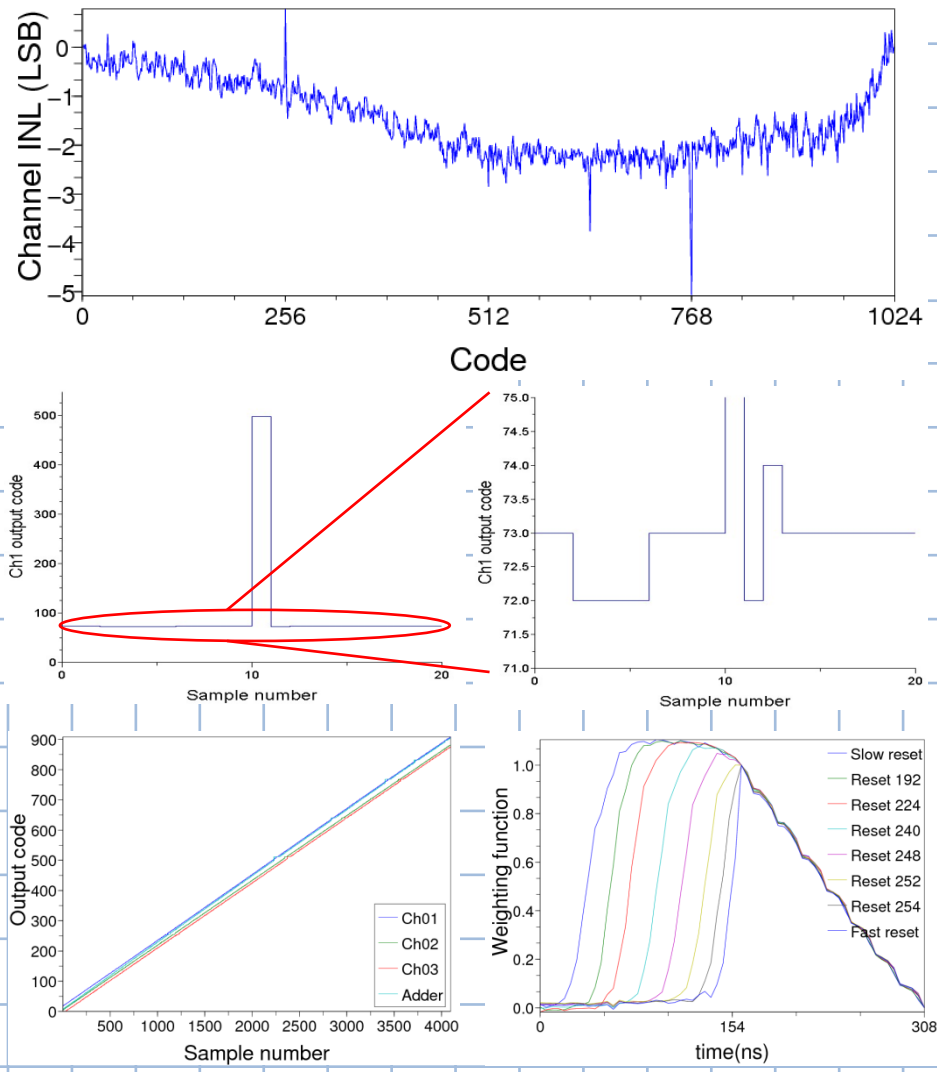




- 72 pads, 2.4mm x 2.4mm (including pads)
- 7306 nodes, 35789 circuit elements
- 360μm channel pitch (including power bus)
- 3 charge amplifiers, 4 x 10-bit, fully diff. SAR ADCs, 1 SC adder, 3 SC filters, etc.

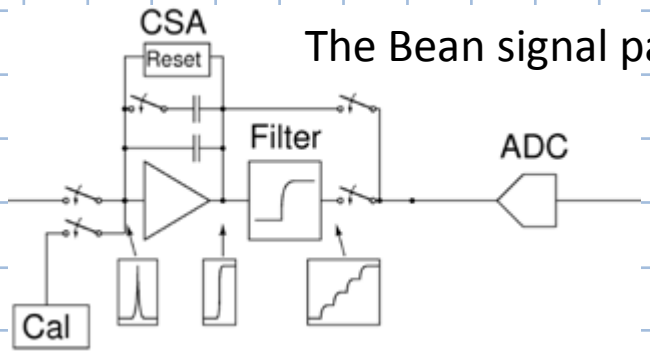
The Bean results summary (2010)

- The chip meets following specs:
  - Functionality
    - Dual gain, physics and calibration modes
    - Fast feedback
  - Input rate
  - Impulse recovery
  - Linearity
  - Noise in Physics mode
- Useful as baseline design

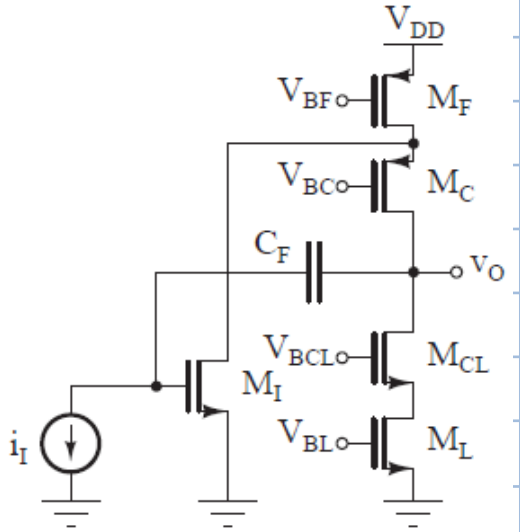


ADC linearity compensation (2012-2013)

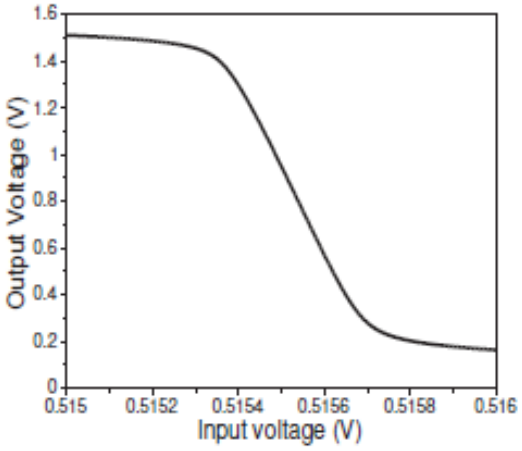
The Bean signal path

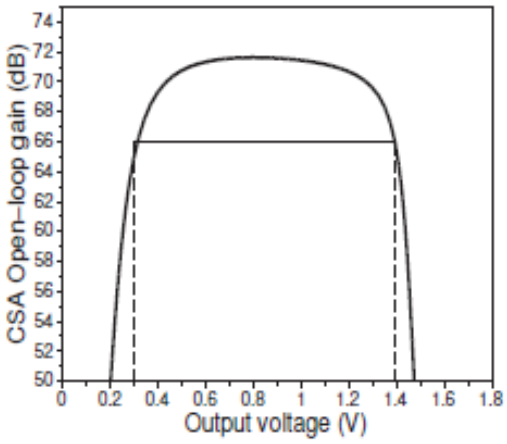


The Bean Simplified CSA schematic



The Bean CSA open loop static transfer characteristic

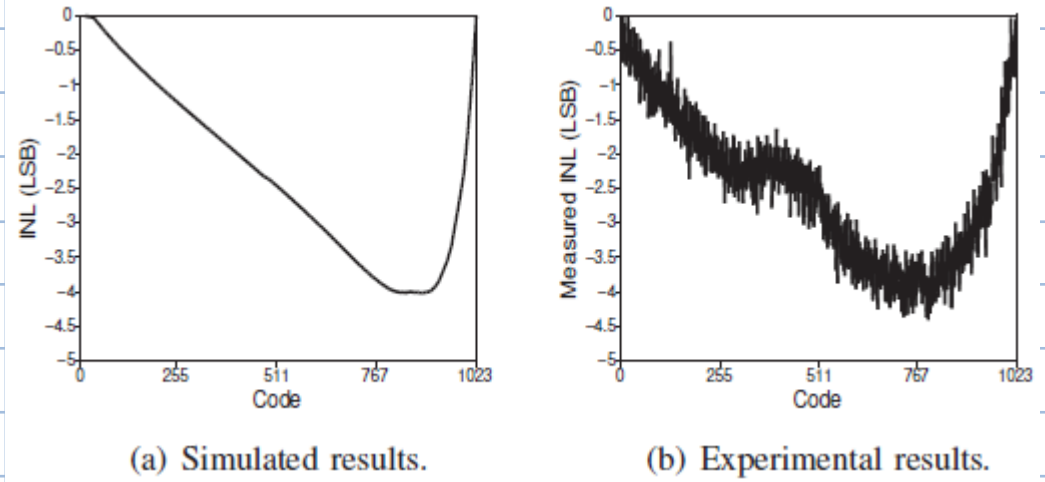




(a) Output voltage vs. input voltage. (b) Open-loop gain vs. output voltage.

Resulting nonlinearity

The Bean CSA closed loop nonlinearity



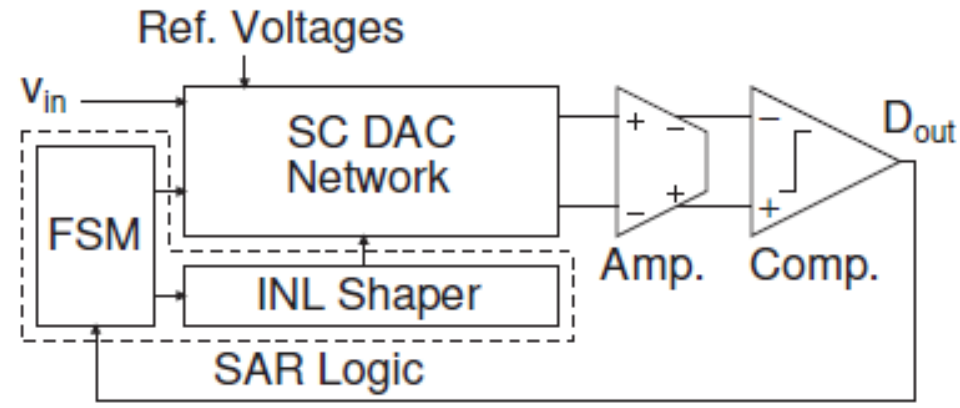
(a) Simulated results. (b) Experimental results.

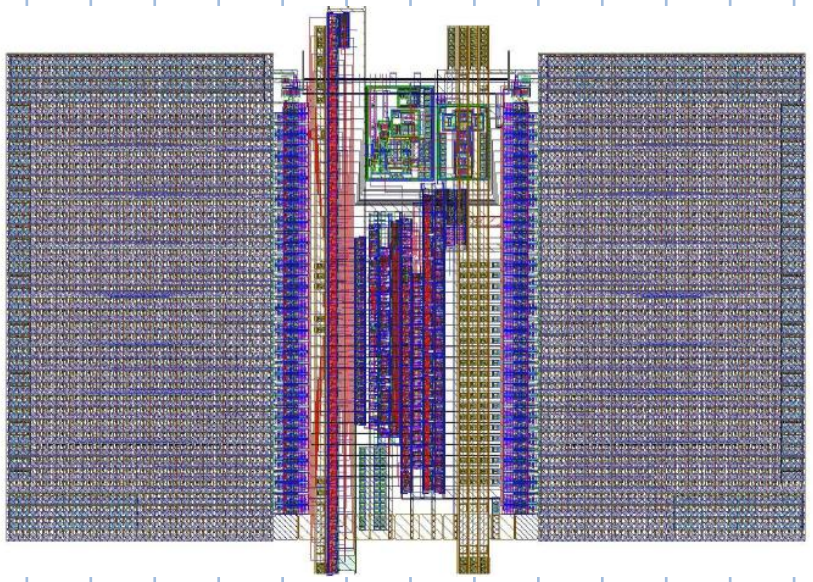
- In order to improve the linearity:
  - output range must be decreased
  - consequently, SNR decreases as well
  - This is compensated through higher power…

Proposed solution

ADC uses systematic process mismatch to correct nonlinearity

Linearity compensation block diagram

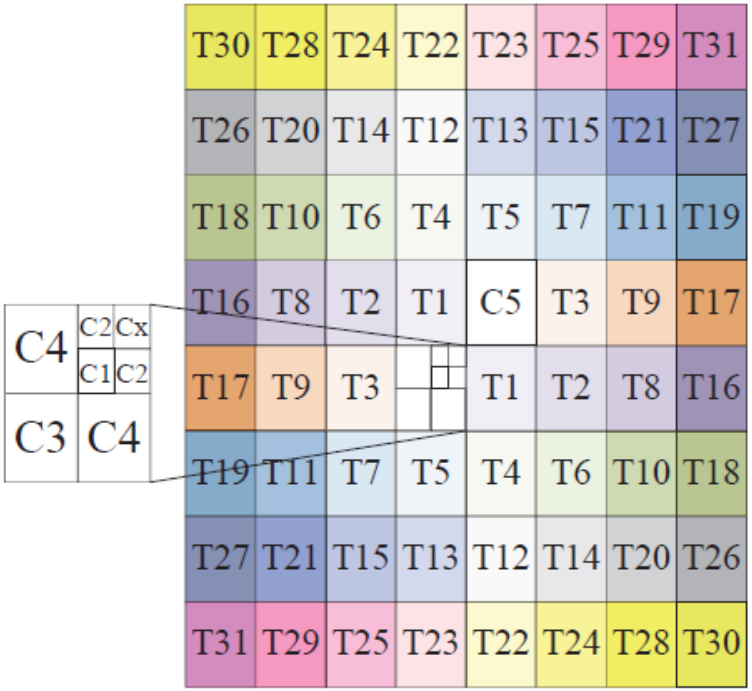


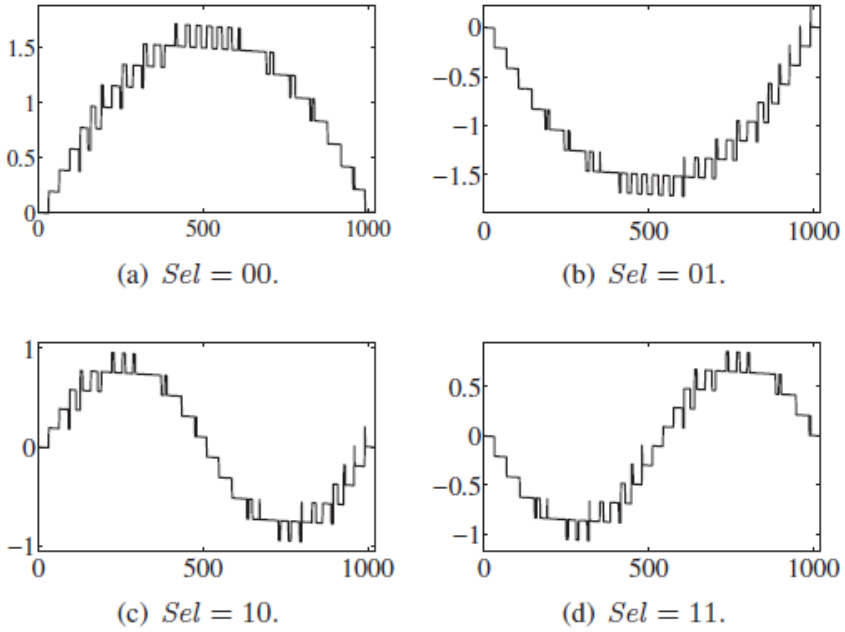


Implementation

Capacitor array is carefully designed to produce four selectable INL shapes

Cap array implementation

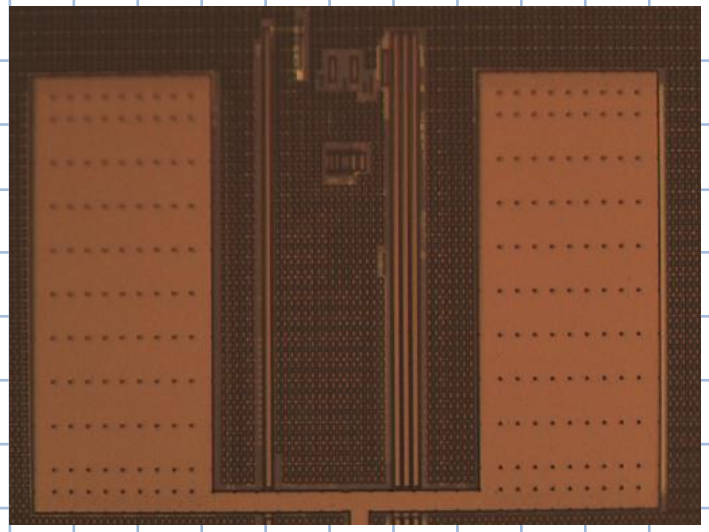




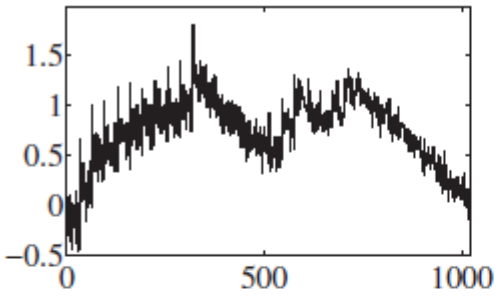
INL simulation results

Test results

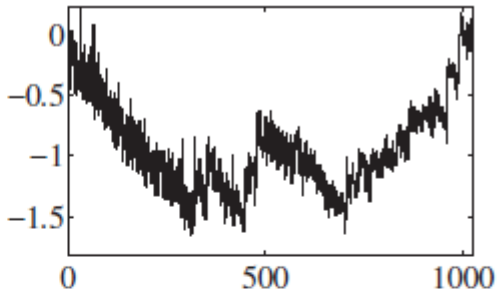
Chip micrography



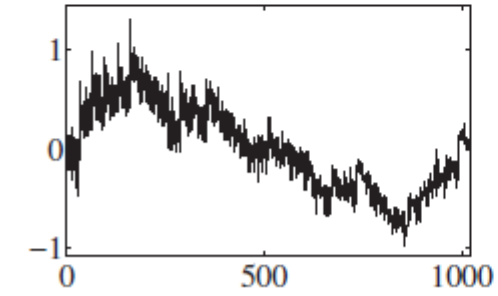
Measured INL profiles



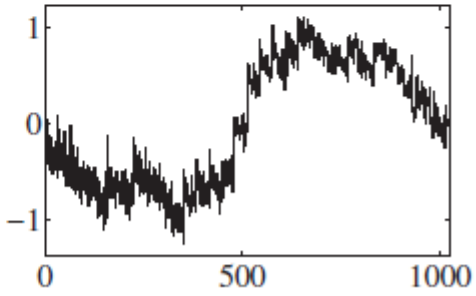
(a) $Sel = 00$.



(b) $Sel = 01$.



(c) $Sel = 10$.

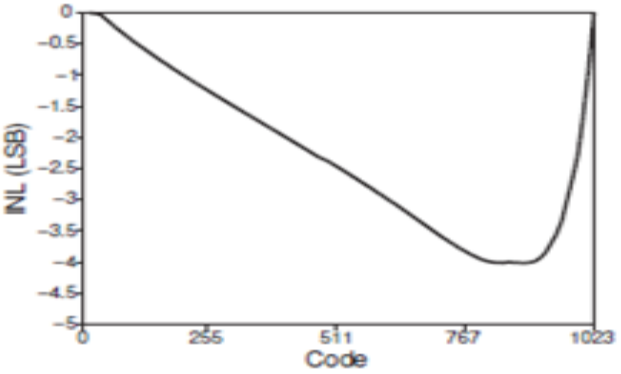


(d) $Sel = 11$.

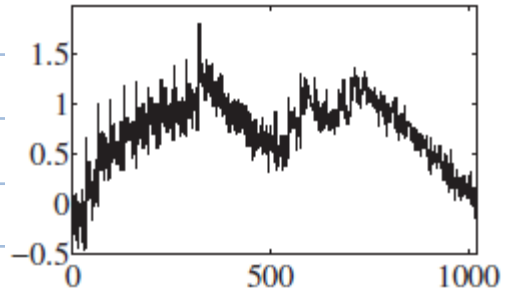
	DNL	INL
$Sel = 00$	$1.10890/-0.43343$	$1.80520/-0.46558$
$Sel = 01$	$0.73167/-0.49624$	$0.20154/-1.66080$
$Sel = 10$	$0.82629/-0.52768$	$1.30450/-0.98749$
$Sel = 11$	$0.79564/-0.49596$	$1.10720/-1.24530$

CSA linearity compensation

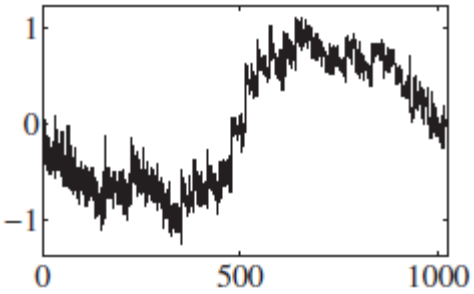
Uncompensated CSA



ADC compensation profiles

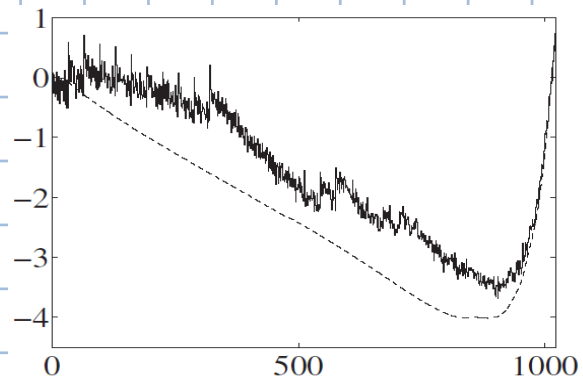


(a) $Sel = 00.$

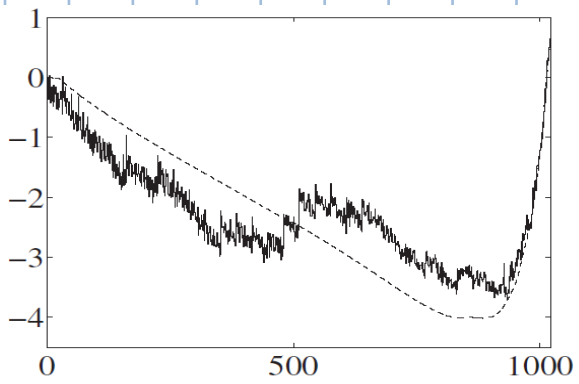


(d) $Sel = 11.$

CSA INL with compensation



(a) Compensated CSA INL using the INL from Fig. 7(a).



(b) Compensated CSA INL using the INL from Fig. 7(d).

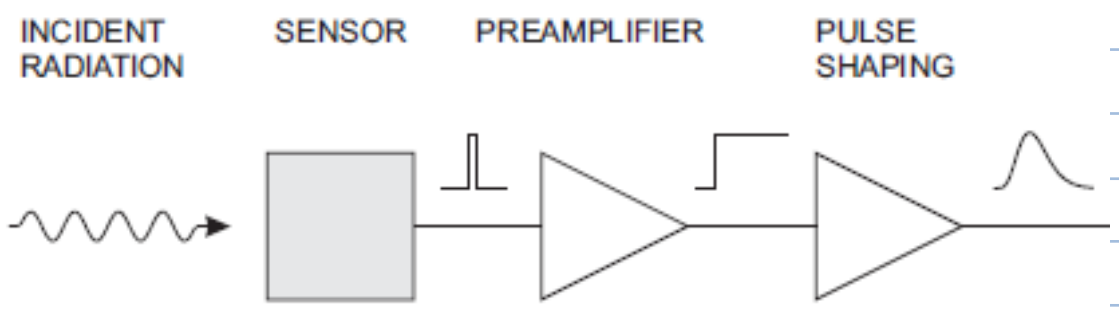
[Alvarez et al, TNS 2014 (submitted)

Conclusion – CSA linearity compensation

- CSA linearity is relevant for FE performance
- CSA nonlinearity can be compensated using ADC
  - Extra cost is zero
  - Compensation uses foreknowledge of fab defects
  - Compensation can be improved by exacerbating fab defects
    - But this requires more Si real state
- Technique has proven to be mildly effective so far
  - But does not hurt
  - Improves efficiency, linearity or SNR
- Technique can be the basis for adaptive resolution

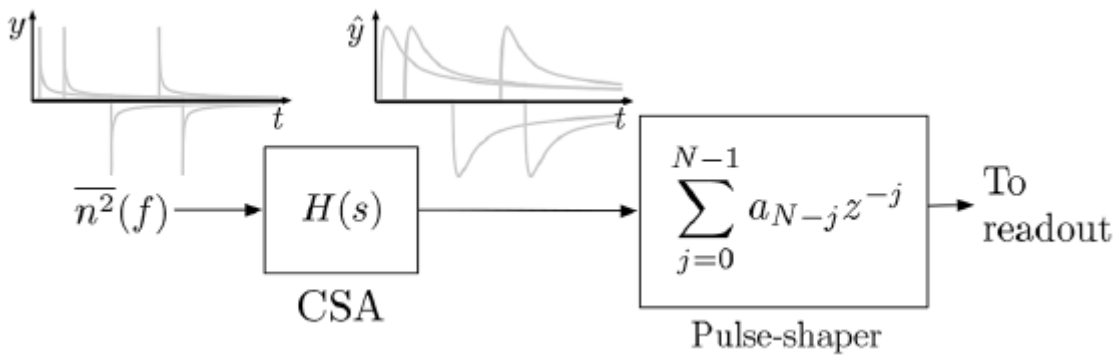
Arbitrary weighting function synthesis (2013 – 2014)

Typical noise processor [Spieler]



- Pulse shaper usually continuous time
- Sometimes with CDS
  - Which makes it a time-varying filter
- Can't sample at peaking time
  - Approximation may lead to error
- Can't synthesize arbitrary weighting functions
  - Usually gets closer to optimal via approximations

Proposed noise processor [Avila TNS 2013]



- Discrete-time processor
  - Compatible with analog SC circuits or DSP
- Holds signal at peak
  - ADC has enough time to sample
- Quasi-optimal weighting function possible
  - Limited by sampling rate
  - CDS is a special case of this discrete-time processor

Formal math of a discrete-time processor

Total contribution of noise originated at a sampling interval Pi and measured at time k

$$\sigma_i^2(k) = \nu \int_{(i-1)T_s}^{iT_s} \hat{y}^2(kT_s - t_a)\,\mathrm{d}t_a$$

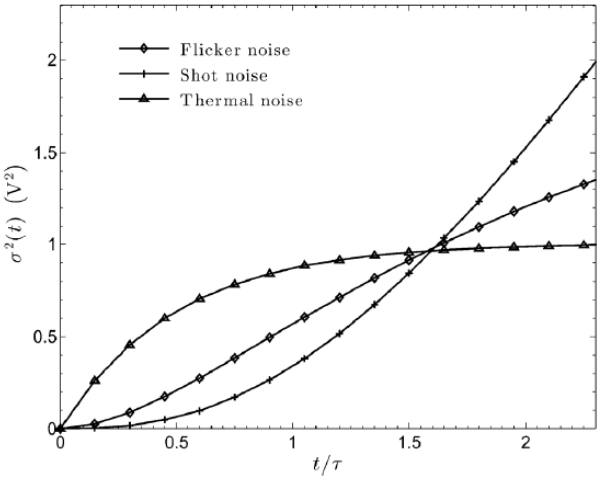


Fig. 4. $\sigma^2(t)$ for thermal, shot and flicker noise with normalized time t/τ and an arbitrary amplitude.

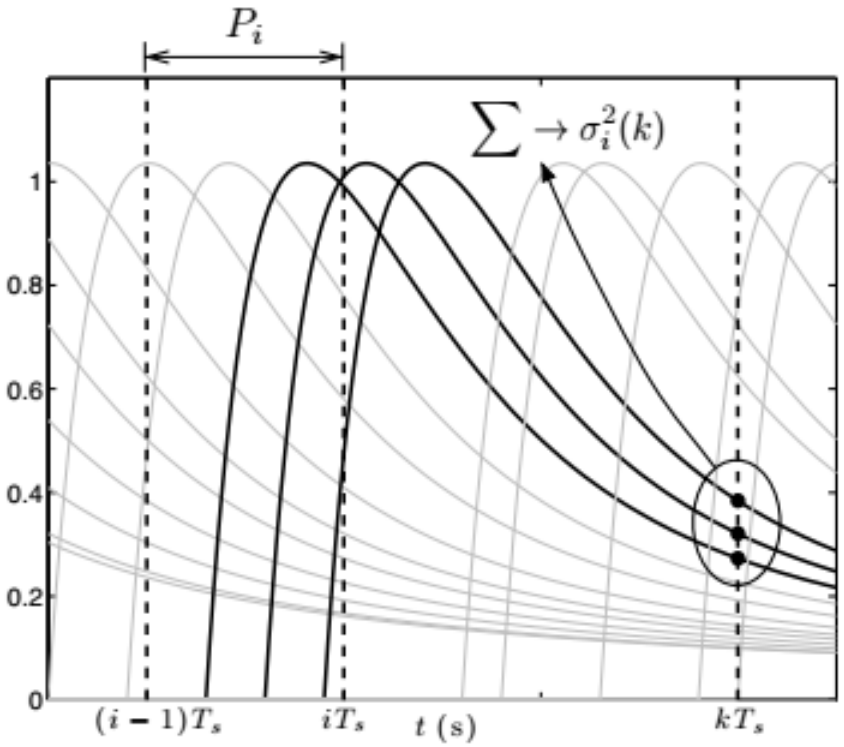


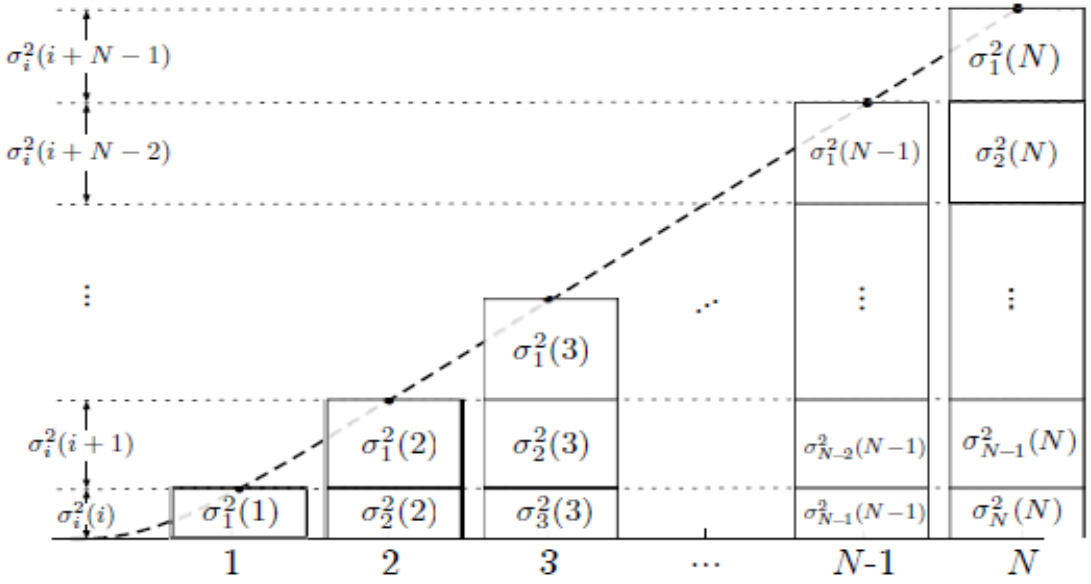
FIGURE 3.2. Noise contribution of the pulses generated within P_i and measured at an arbitrary sample k (i.e., $t = kT_s$), using an arbitrary filtered noise core function $\hat{y}(t)$. The independent contribution of each pulse is pointed out with black dots.

Noise processed as non-correlated contributions for each time interval

Noise at filter input in interval Pi can be simplified to:

$$\sigma_i^2(k) = \begin{cases} \sigma^2((k-i+1)T_s) - \sigma^2((k-i)T_s), & k \geq i \\ 0, & k < i \end{cases}$$

Noise at filter INPUT



Contribution of noise in sampling interval Pi on filter output

$$\hat{\sigma}_i(k) = \sqrt{\sigma_i^2(k)} * \mathcal{Z}^{-1}\{F(z)\}(k) = \sum_{j=0}^{k-i} a_{N-j} \sqrt{\sigma_i^2(k-j)}.$$

Closed-form expression for output noise:

$$\hat{\sigma}^2(N) = \sum_{i=1}^{N} \left(\sum_{h=0}^{N-i} a_{i+h} \sqrt{\sigma^2((h+1)T_s) - \sigma^2(hT_s)} \right)^2$$

Application example

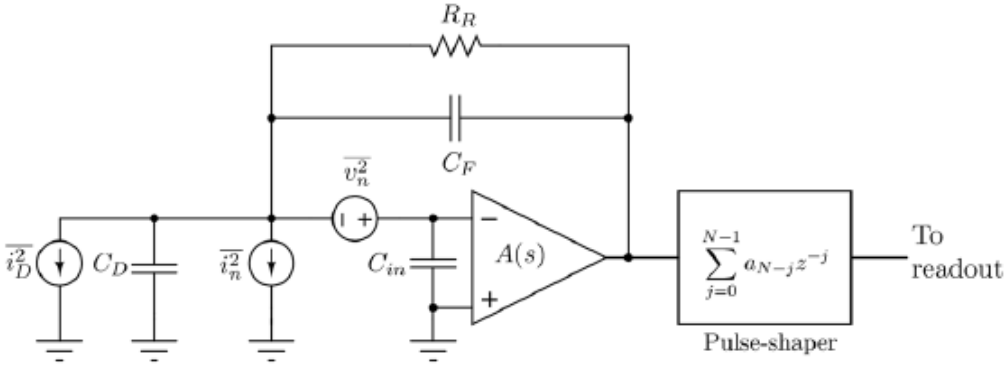
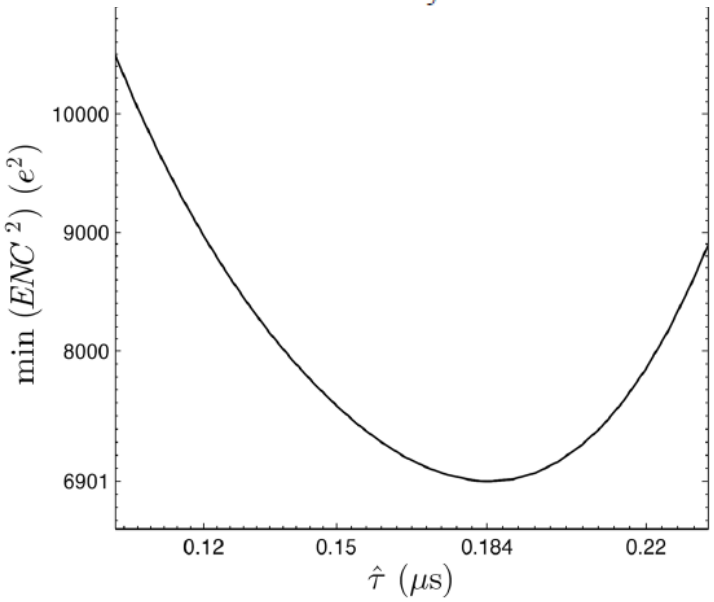
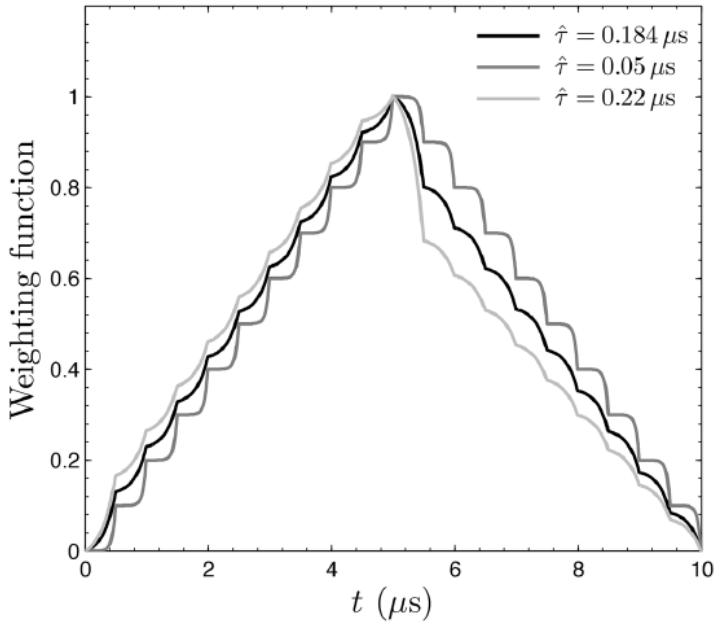
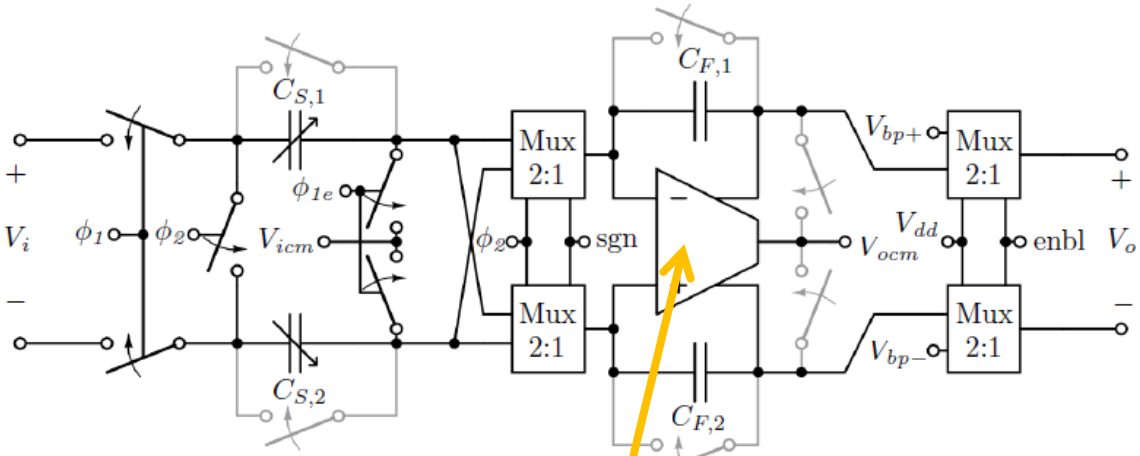


Fig. 5. Front-end circuit used for noise analysis.

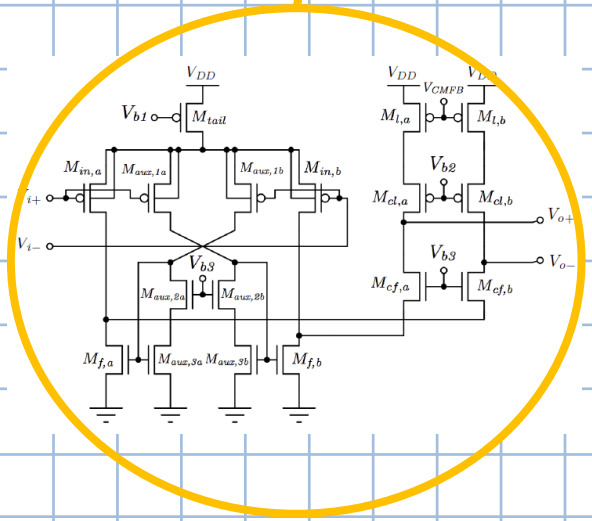


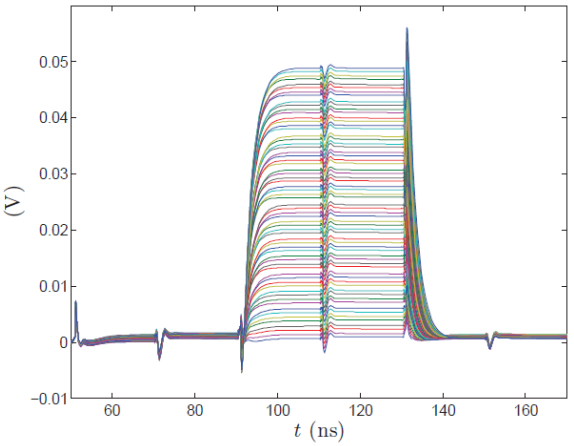


Filter design



Filter schematics





Transient simulations

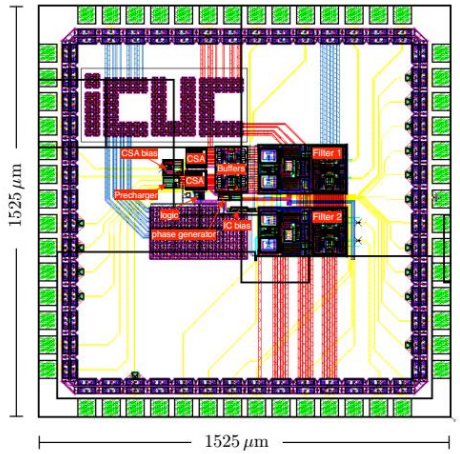
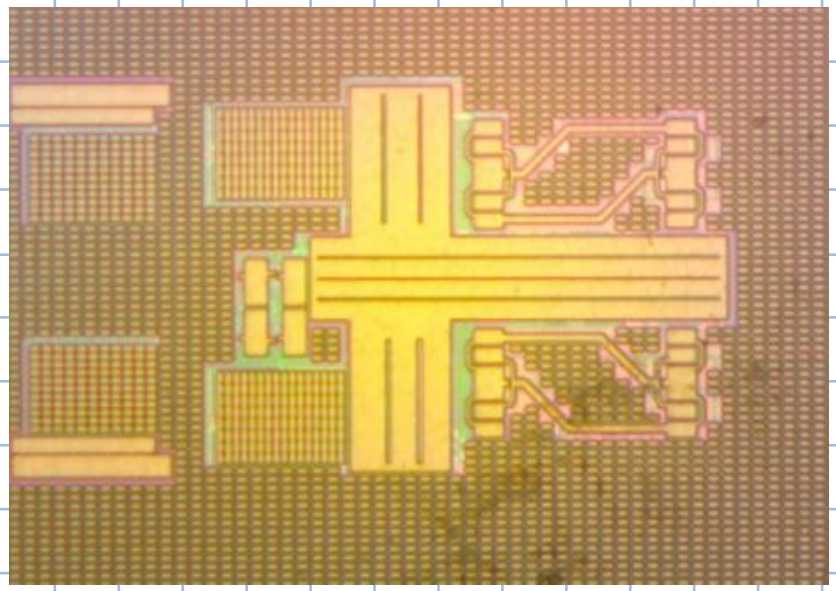


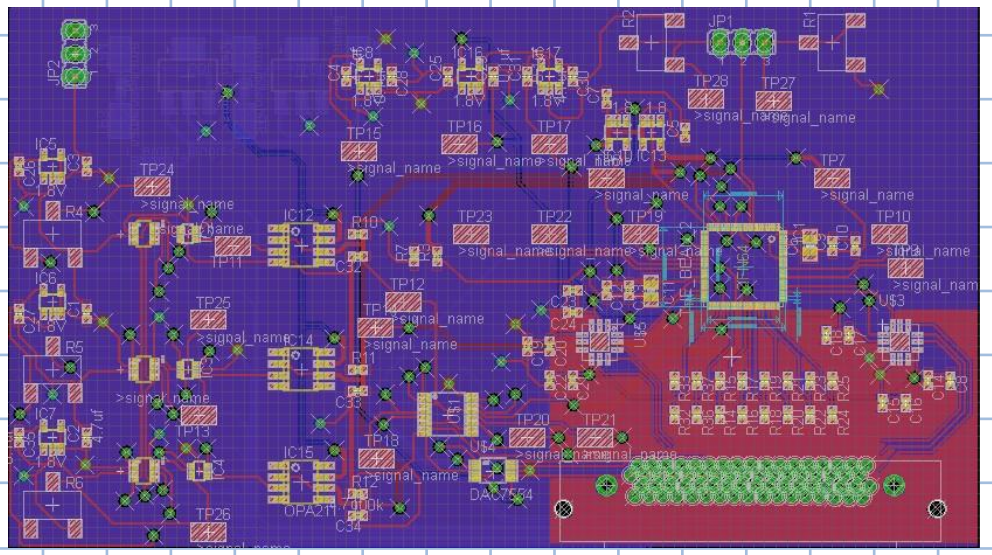
FIGURE 5.1. The Bean V2 prototype layout.

Layout

Filter fabrication and tests (ongoing)



Filter micrography



Board design

Intentionally-nonlinear ADC study

- The energy resolution of a sampling calorimeter can be described as

$$\frac{\delta E}{E} = \frac{A}{\sqrt{E}}$$

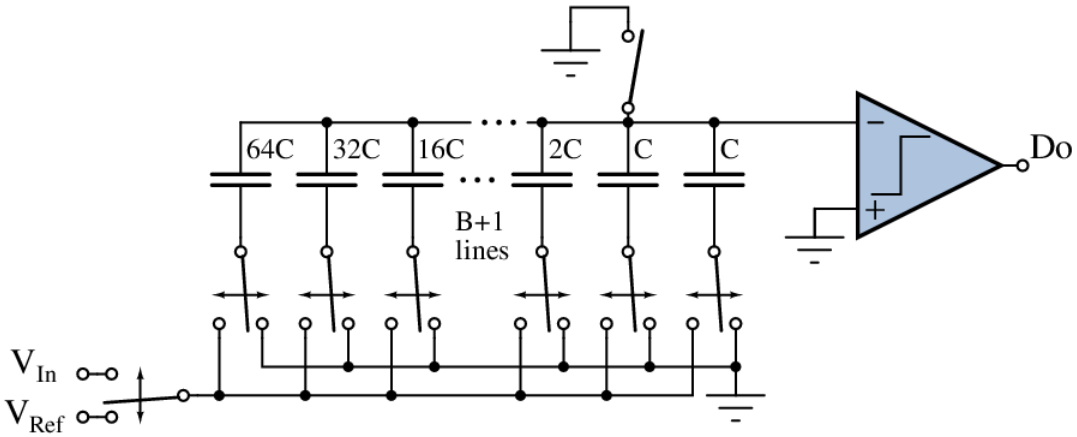
- Required resolution of electronics is a function of the shower energy
  - The bit size changes along the full scale range
  - Idea: to adjust the ADC resolution according to input
    - Otherwise, dynamic range specification is hard to meet

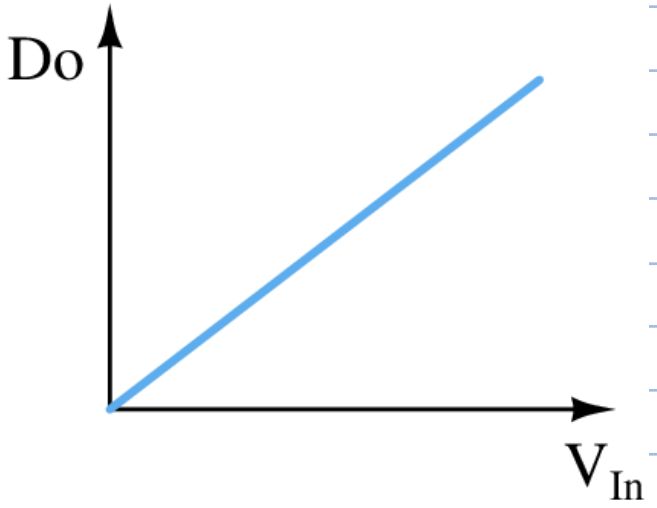
Example: ADC Dynamic range spec

- In BeamCal, the LSB for 1GeV should be 0.2GeV
  - Then, a linear ADC good for up to 1TeV needs 1000/0.2=5000 codes, or **13 bits**
  - However, if the ADC resolution matches the fundamental resolution of a sampling calorimeter, only **8 bits** are required to represent all the information space!
- This does not relax the front-end dynamic range
  - We still want to have a linear CSA
  - This is also required for fast feedback estimations

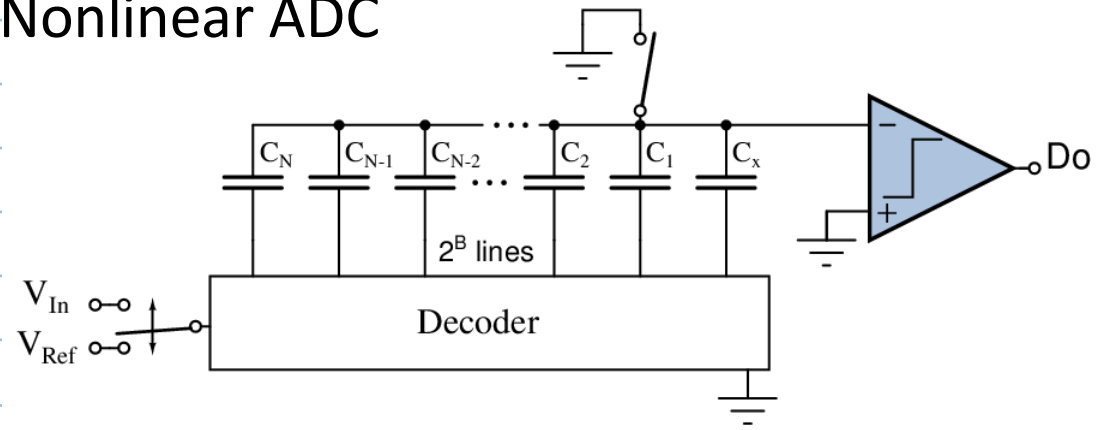
Linear vs. nonlinear ADC design

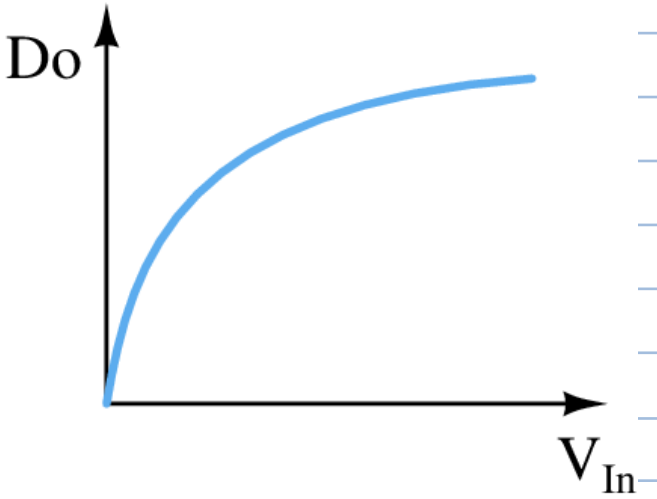
Linear ADC





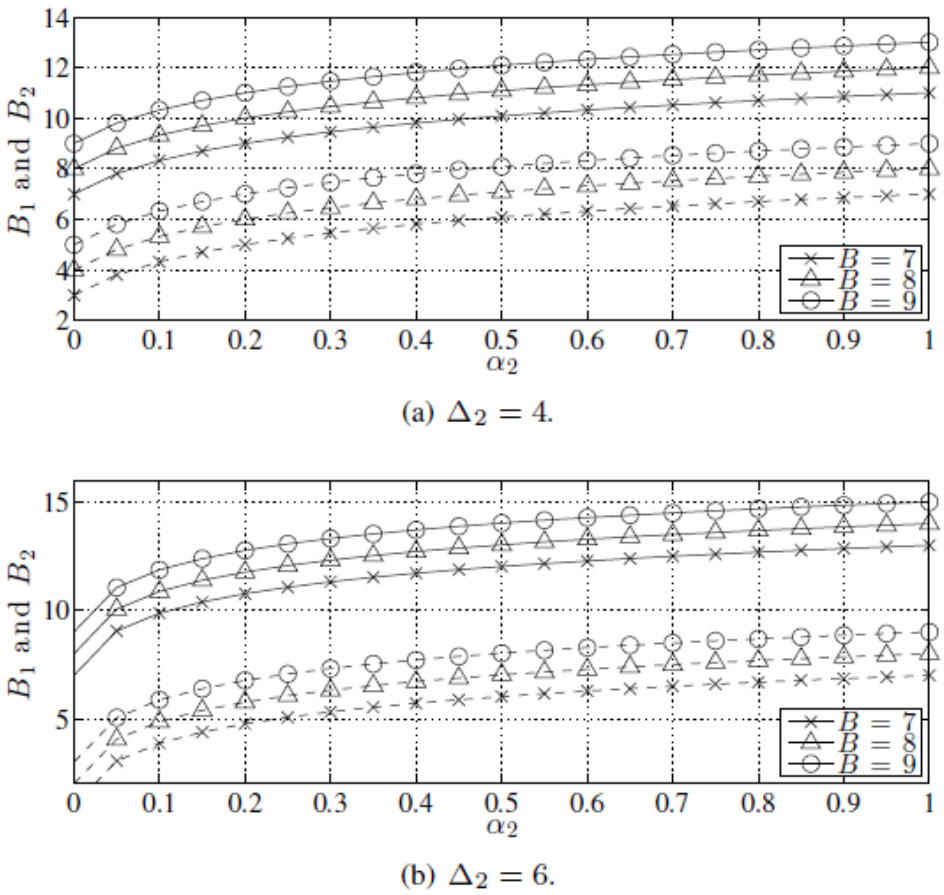
Nonlinear ADC





Example: piecewise-linear ADC

- Two different resolutions
  - Requires only 2 capacitor sizes
  - But capacitors may be quite differen
    - Layout is challenging
  - Many ways to partition resolution in two sections
    - And many tradeoffs



(a) $\Delta_2 = 4$.

(b) $\Delta_2 = 6$.

Fig. 4. B_1 and B_2 as a function of α_2 and B for (a) $\Delta_2 = 4$ and $\Delta_2 = 6$.

To nonlinearize… or not?

SIZE COMPARISON BETWEEN DIFFERENT FULLY-THERMOMETER-CODED SAR ADCS.

	Capacitor Array (C_{tot})	Decoder	Digital Core	Comparator	Amplifier
Standard Linear	$c_u \cdot 2^B$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$
s-section Piecewise	$c_u \cdot 2^B \sum_{i=1}^{s} \alpha_i 2^{\Delta_i}$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$
Fully Nonlinear	$c_u \cdot \sum_{i=1}^{N_{nl}} k_i$	$\propto 2^B L_{min}$	$\propto B \cdot L_{min}$	$\propto L_{min}$	$\propto L_{min}$

- Tradeoff between capacitor array size and decoder size
- But 8 bits instead of 13 bits of resolution!
- Still working on this…

Electronics for BeamCal: Summary

- 3-channel Readout chain in 180nm (2010), tested
- ADC linearity compensation (2012 – 2013)
  - Will be useful in eventual ADC nonlinear design
- Arbitrary weighting function synthesis (2013 – 2014)
  - Intention to extend to asynchronous processing
- Intentionally nonlinear ADC (ongoing work)

Electronics for FCAL: Future plans

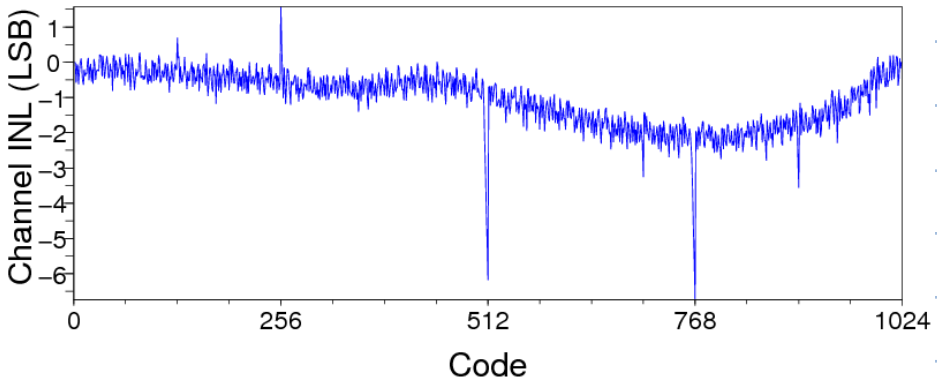
- 2015: Design and test a multichannel FE and ADC IC for BeamCal
  - Synchronous and asynchronous readout
  - Possibly nonlinear ADC
- Joint collaboration with AGH:
  - Eventually converge to the same technology and process
  - Share IP/fabrication runs
  - Student/researcher visits
  - Possible funding applications

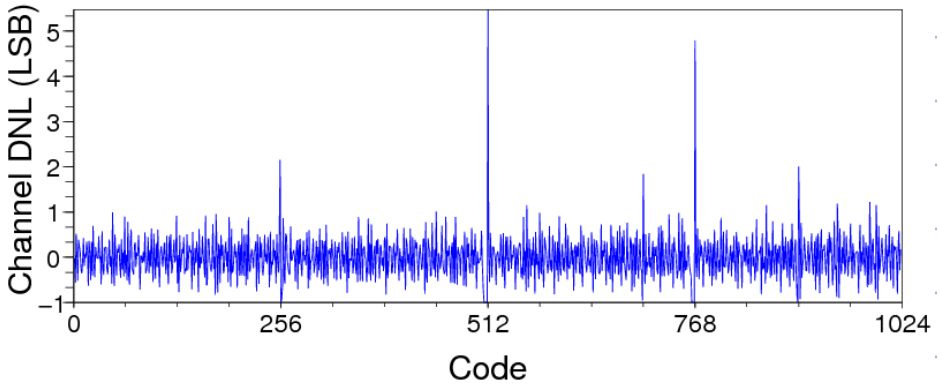
Хвала!

BACKUP MATERIAL

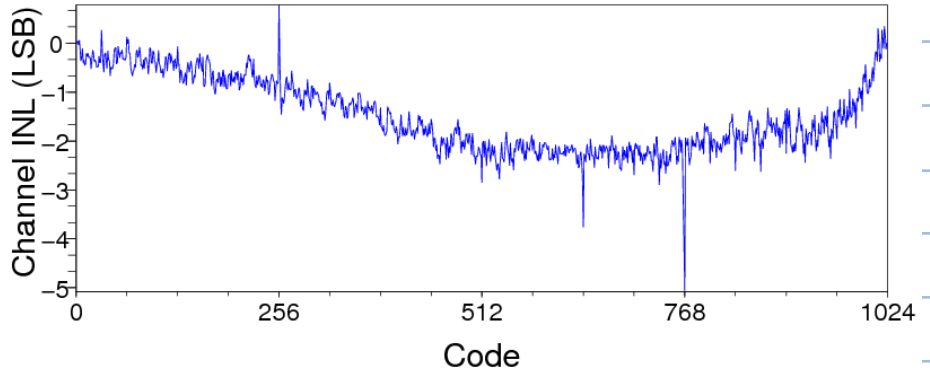
The Bean Linearity Test Results

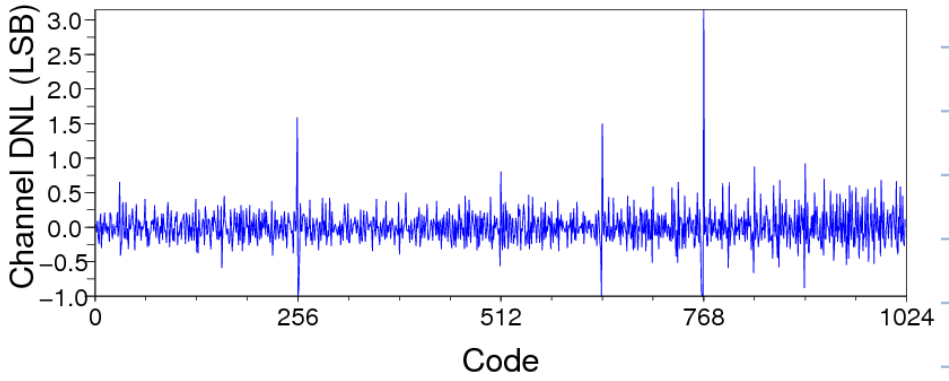
37 pC input (SDT)





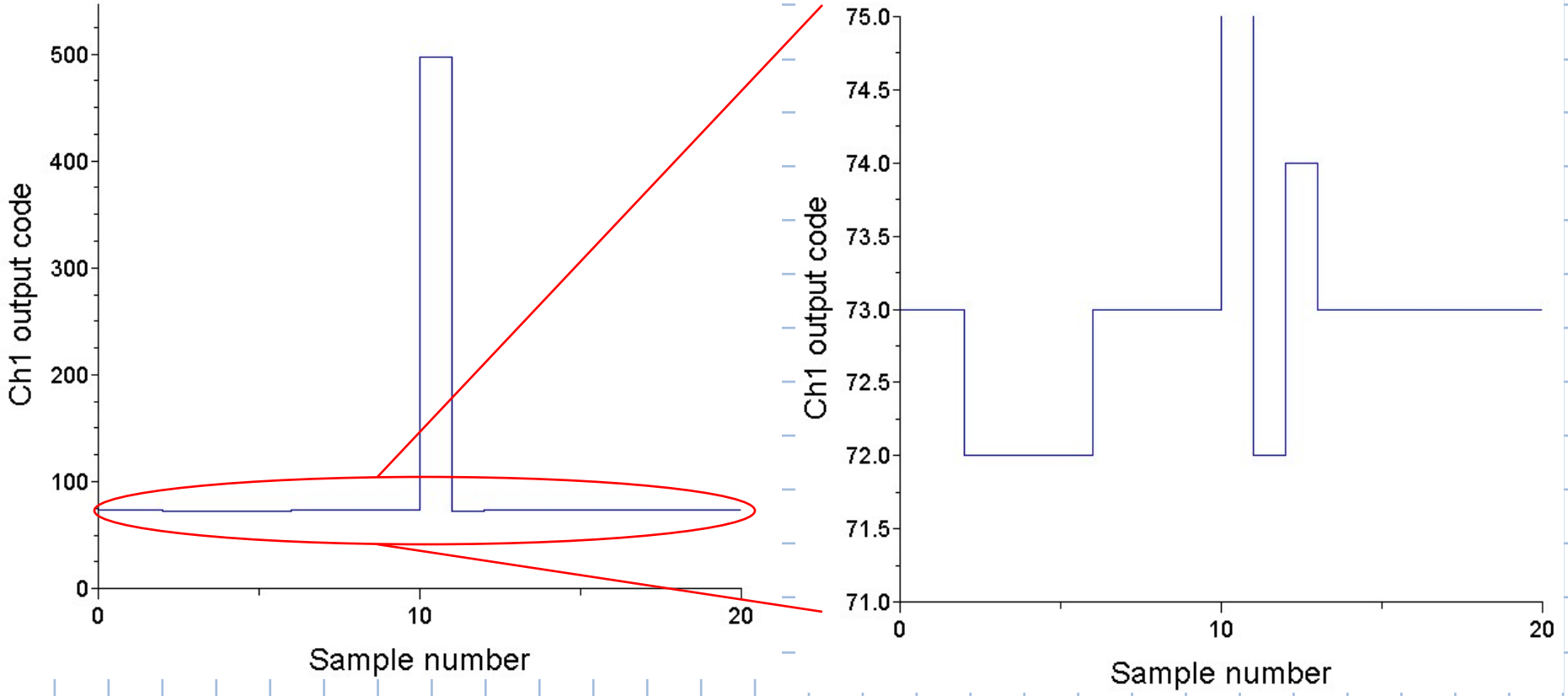
0.74 pC input (DCal)





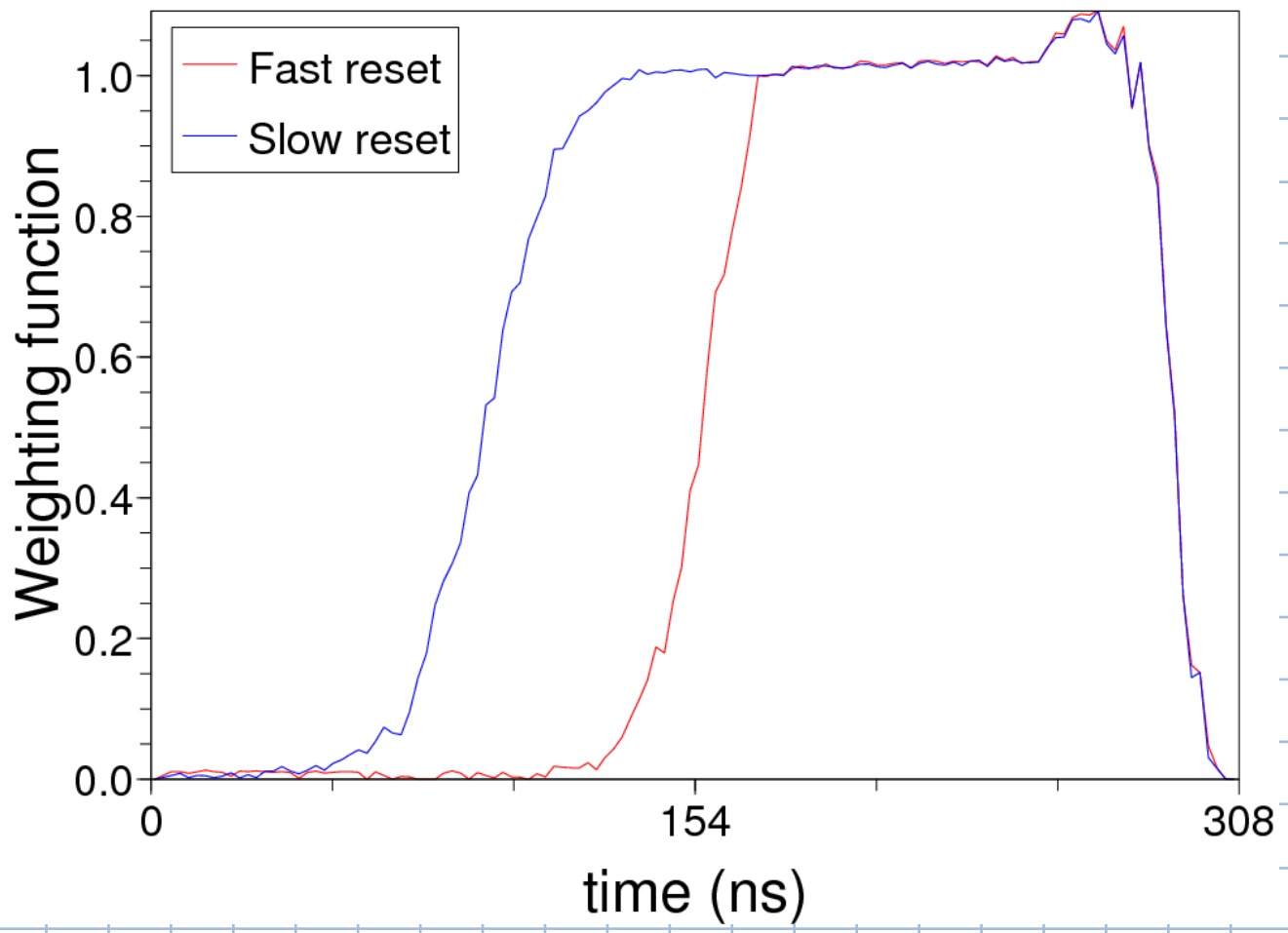
The Bean Bandwidth test results

- Input injected on 10th cycle only
- Digital output recorded, nominal speed



The Bean
Weighting function measurement, SDT

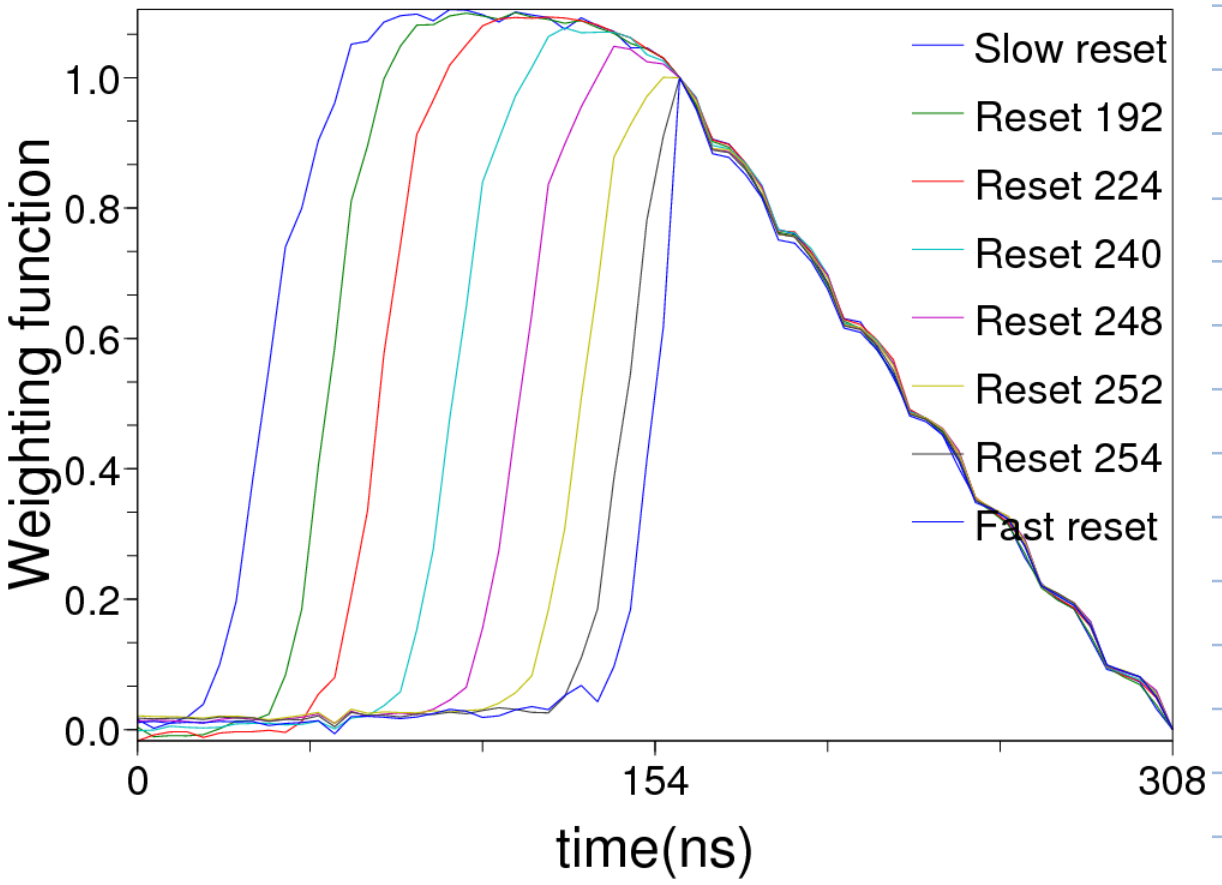
Time resolution: 4.8 ns



The Bean
Weighting function measurement, DCal

Time resolution: 4.8 ns

Series noise coefficient ranges from $37.6\times10^6\ s^{-1}$ to $59.3\times10^6\ s^{-1}$



The Bean
Fast feedback adder measurement

- Adder proved full functionality at nominal speed of operation
- Gains from individual channels to Adder range from 0.329 to 0.345