

HVStripV1

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Presentation Outline

- 1 Introduction
- 2 Testbeam
- 3 Illumination with Fe-55
- 4 Linearity of Response
- 5 Summary

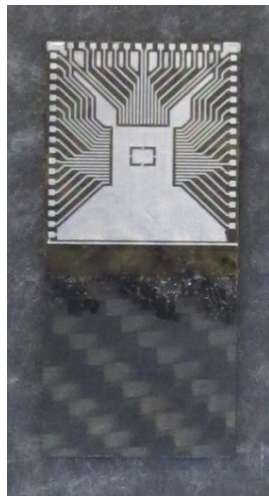
HVStripV1



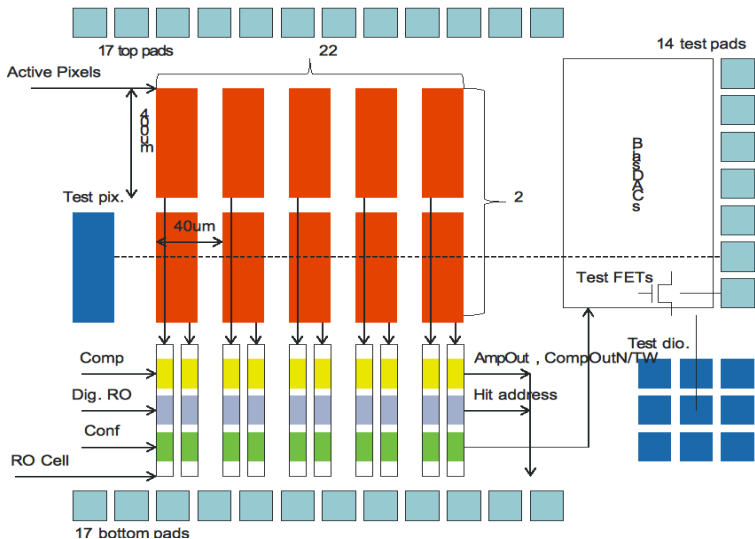
- HVStripV1 is the CMOS testchip (HV-CMOS process) designed by Ivan Peric
- The CMOS technology is being evaluated for potential use in particle physics experiments
- The HVStripV1 test chip allows one to investigate reliability of the technology
- Participating institutions: DESY, Glasgow, KIT, Oxford, RAL, UCSC

HVStripV1 Chip (1)

- Among several test devices also contains strip-like active pixel matrix consisting of 44 pixels
- Pixels are divided into 2 rows and 22 columns with each pixel having dimensions of $40\mu m \times 400\mu m$
- Every pixel contains a charge sensitive amplifier with a source follower

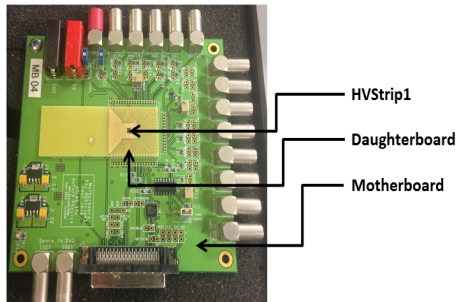


HVStripV1 Chip (2)



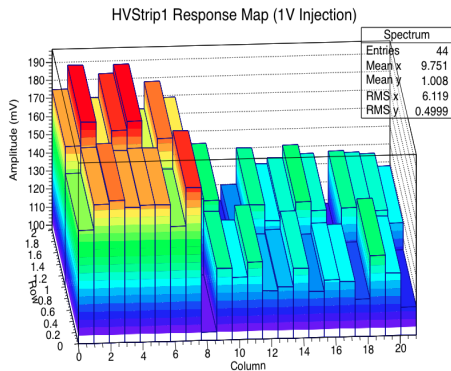
HVStripV1 Chip (3)

- Mounted on daughterboard and subsequently on motherboard
- The arrangement is programmed and controlled via Atlys FPGA board
- First power up less than a week before the testbeam



Initial Tests (2)

- Analogue output pulse heights were mapped for all pixels of several HVStripV1 chips
- 1V injection pulses were used for $\approx 0.5\text{fF}$ input capacitance (equivalent to $\approx 3100e^-$)
- Amplitude drop was observed for all chips after column 7 due to different types of feedback transistors used for pixels
- In particular pixel (8,0) has especially low gain



Presentation Outline

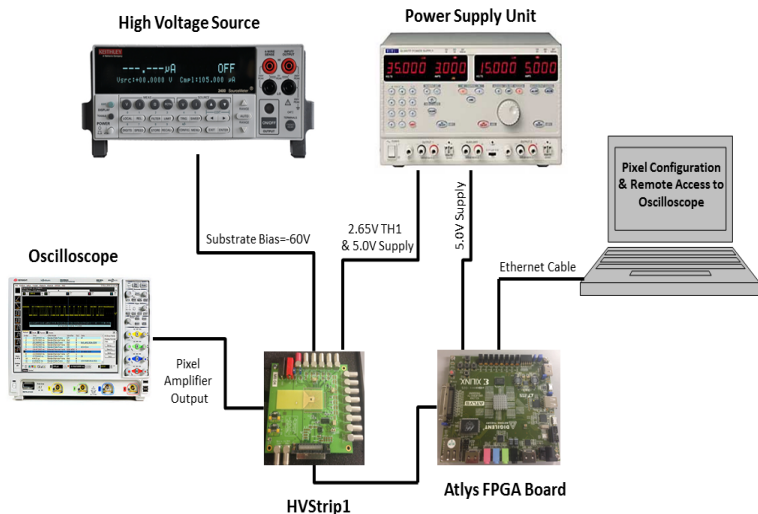
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Overview

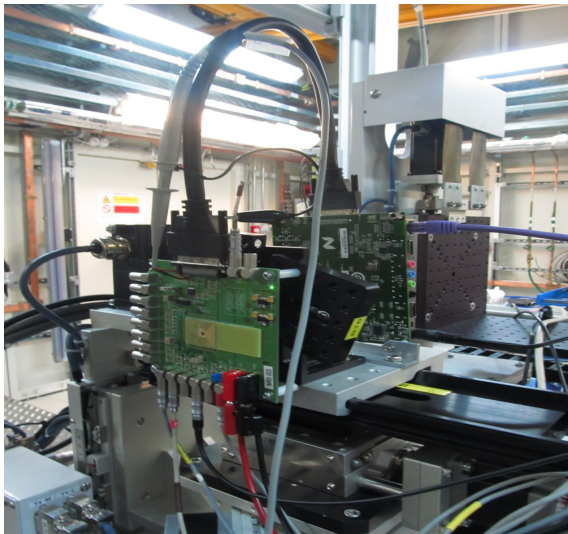
- Testbeam took place at Diamond Light Source in October
- Beam of 15keV X-rays of few μm width (when microfocused) was available
- Correspond to $\approx 4100e^-$
- Considerable limitations for testing the chip were due to absence of proper DAQ system



Experimental Setup (1)

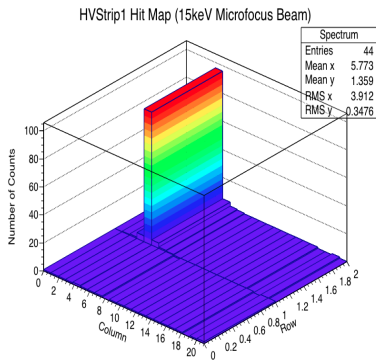


Experimental Setup (2)



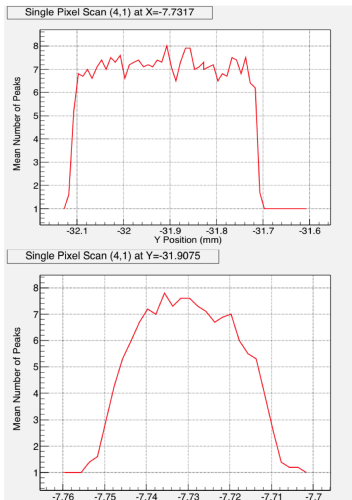
Results (1)

- Bias of -60V applied to the substrate
- The beam position was identified after many attempts of trial and error
- Scans across all pixel matrix had to be performed to accomplish the previous
- The beam was then microfocused and 3mm of Al was placed to reduce intensity



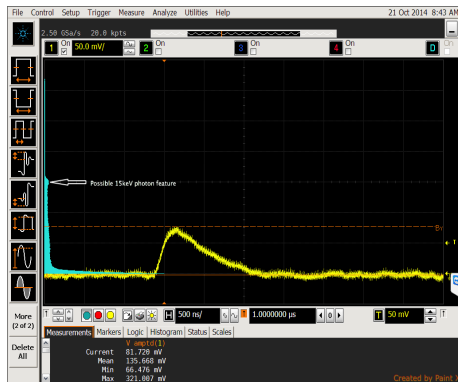
Results (2)

- Scan was performed on one pixel in both dimensions
- Data consists of position of the chip and number of hits above 100mV threshold in 1ms
- Consistent with dimensions of the pixel given in documentation



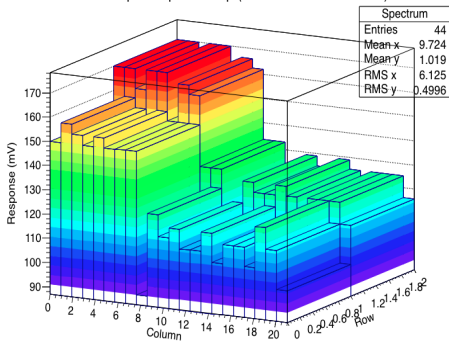
Results (3)

- Another scan performed was across all pixel centres
- Response amplitude was sampled to produce a histogram
- The 15keV feature was identified in most pixels and similarly to charge injection tests the response map was produced
- Response pulse heights vary from 91mV to 170mV (due to different types of transistors used for pixels)

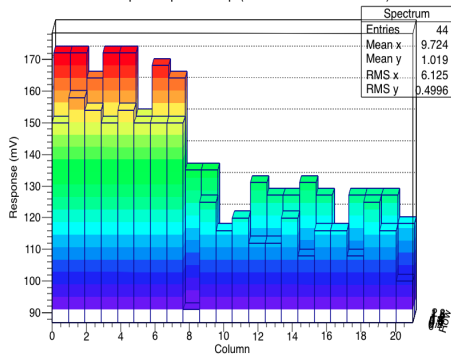


Results (4)

HVStrip1 Response Map (15keV Microfocus Beam)



HVStrip1 Response Map (15keV Microfocus Beam)

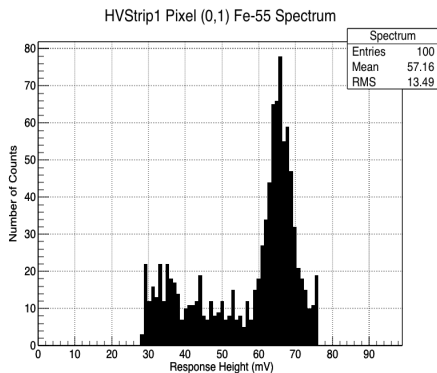


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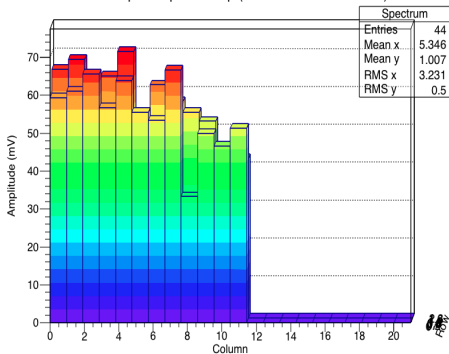
Fe-55

- After the testbeam the chip was illuminated with Fe-55 X-ray source
- The characteristic line corresponds to 5.9keV (correspond to $\approx 1600e^-$)
- Scan was done across half of the pixel matrix
- Results vary from 33mV to 70mV and seem to be consistent with those from the testbeam

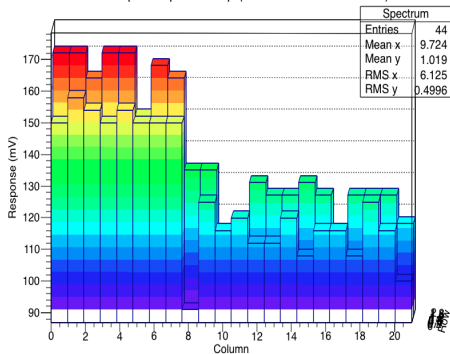


Result Comparison

HVStrip1 Response Map (Fe-55 Irradiation 5.9keV)



HVStrip1 Response Map (15keV Microfocus Beam)

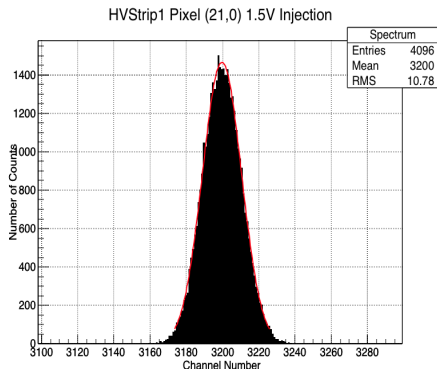


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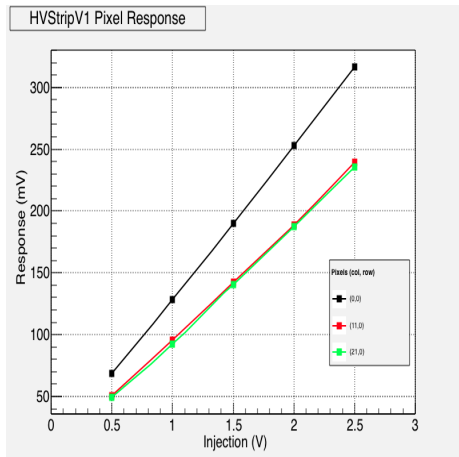
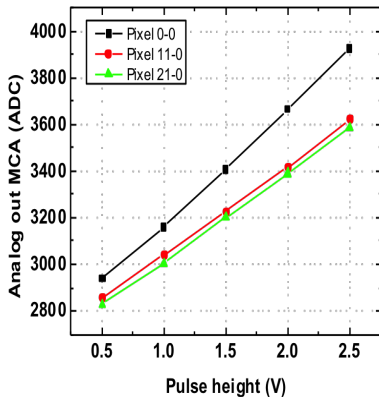
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Linearity (1)

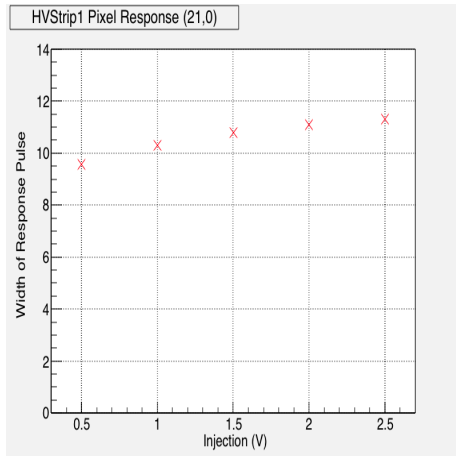
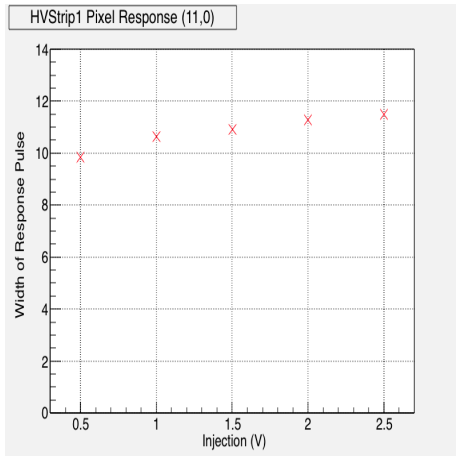
- Linearity of response investigation was done on several pixels
- The setup is almost the same as for analogue injection tests
- In addition MCA was employed for more detailed analysis
- So far all the pixels tested produce linear response



Linearity (2)



Linearity (3)



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Summary

- First results of HV-CMOS strip prototype sensor seem to be consistent with each other
- Still much to be done in understanding analogue response as injection capacitance may not be well defined
- Radiation hardness and suitability for particle physics experiments (like the ATLAS upgrades) is still to be evaluated

Thank you for your attention!