ScCAL Data Acquisition System

Timing

- Common running timing
- Fast commands timing
- Clock Synchronization timing
- AHCAL DAQ readout cycle timing and sequence
- Plans

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Calorimeter for ILC

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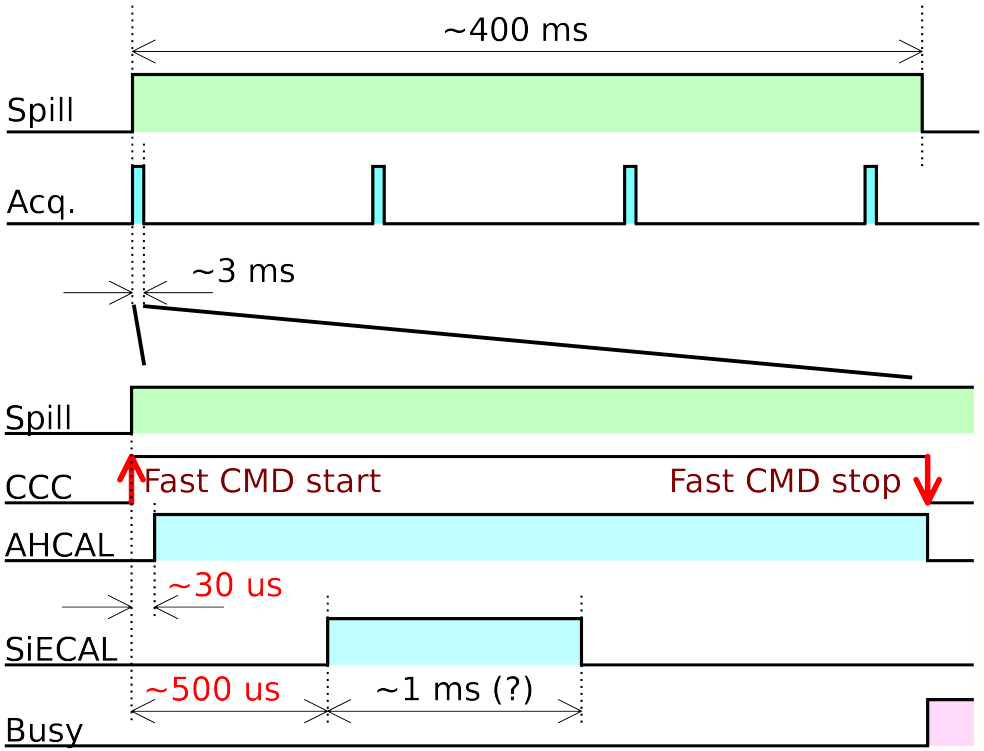
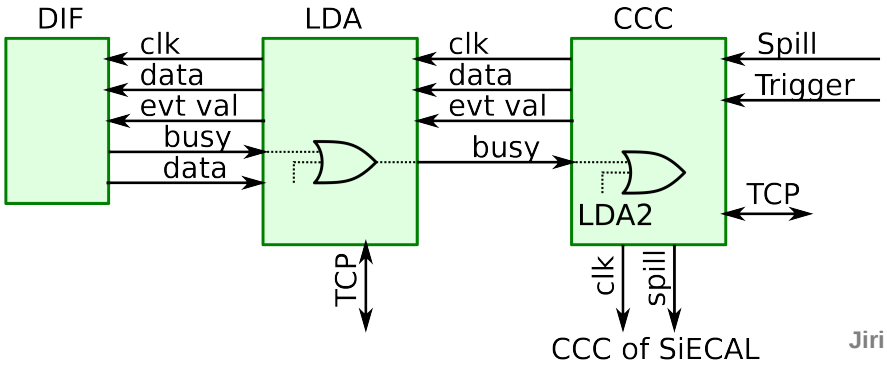
DESY

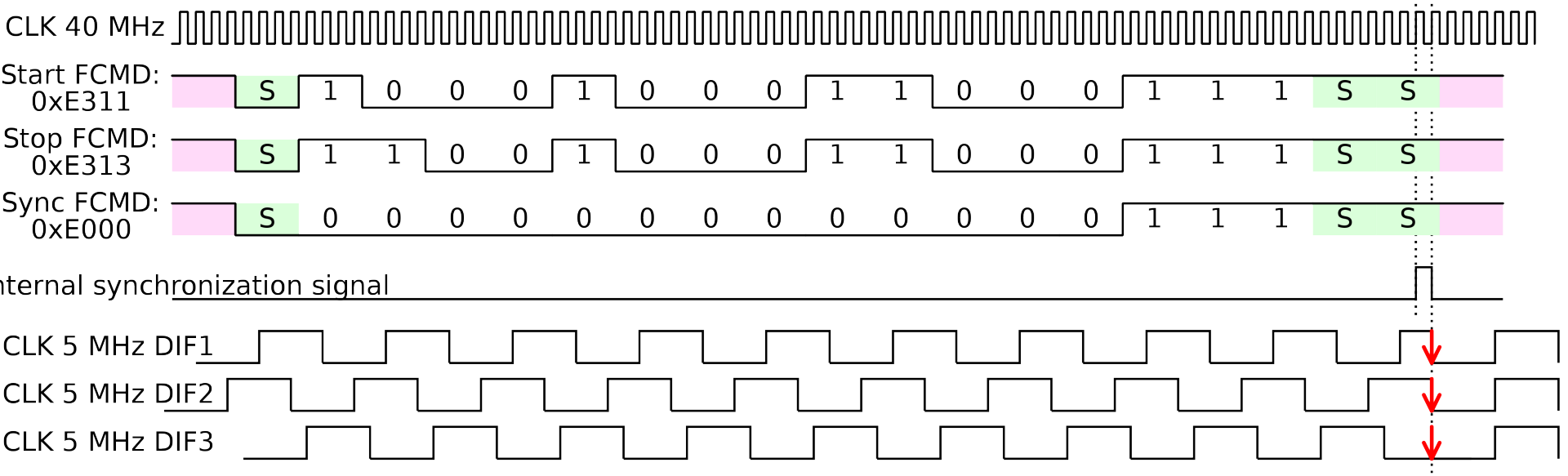
Common running timing @CERN PS

- 40 + 50 MHz clock from ScDAQ CCC
- 5MHz derived clock synchronized for ScDAQ at the beginning of each run
- Fast commands only for ScDAQ
- Busy evaluated only from ScDAQ
- Diagrams: tentative values only (rough estimates)
- RO cycle number in the data packets added by LDA



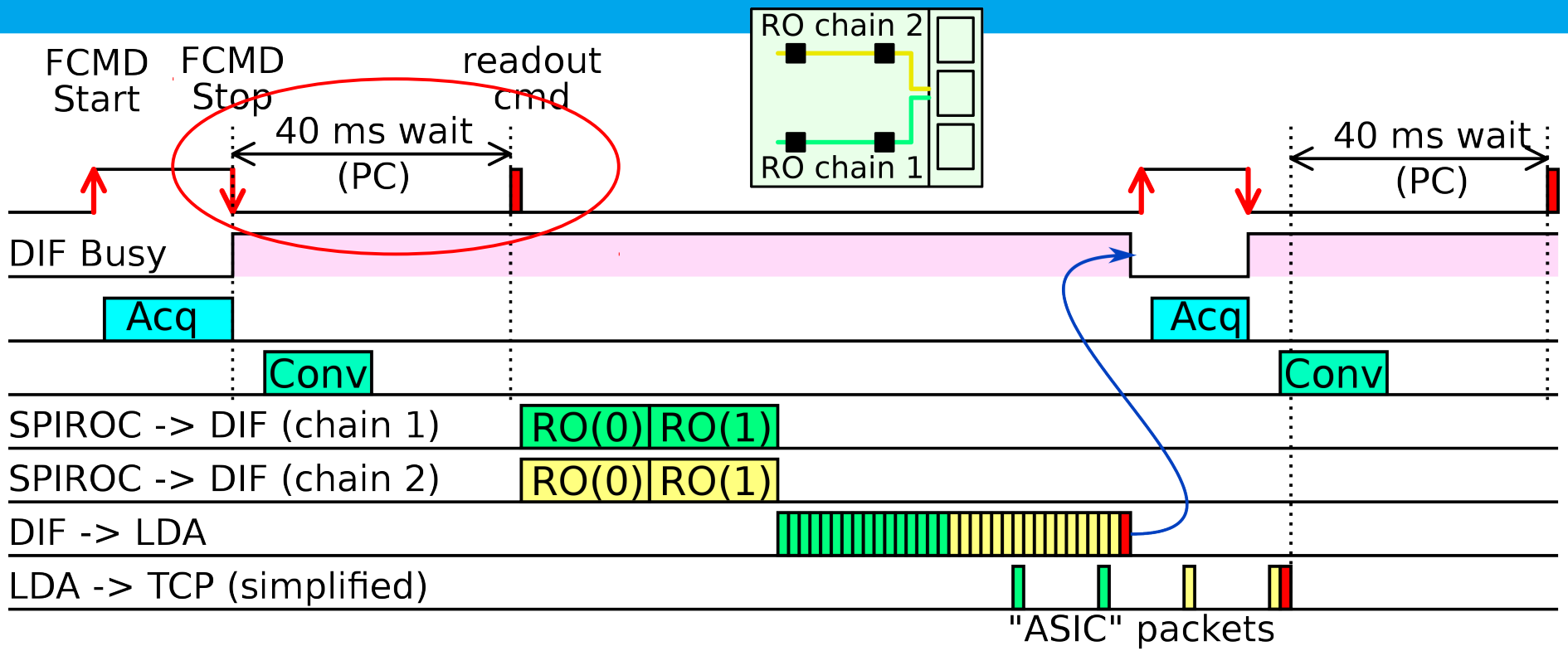


Fast commands and 5MHz clock synchronization



- Fast command format:
  - Waveforms in scale, synchronization registers omitted
  - Bit rate 10 MHz (generated and sampled by 40 MHz)
  - 1 start bit, 16 bit of data (LSB first), 2 stop bits
- Synchronization command is sent before each run by dedicated fast command (0xE000)

Current DAQ timing and sequence

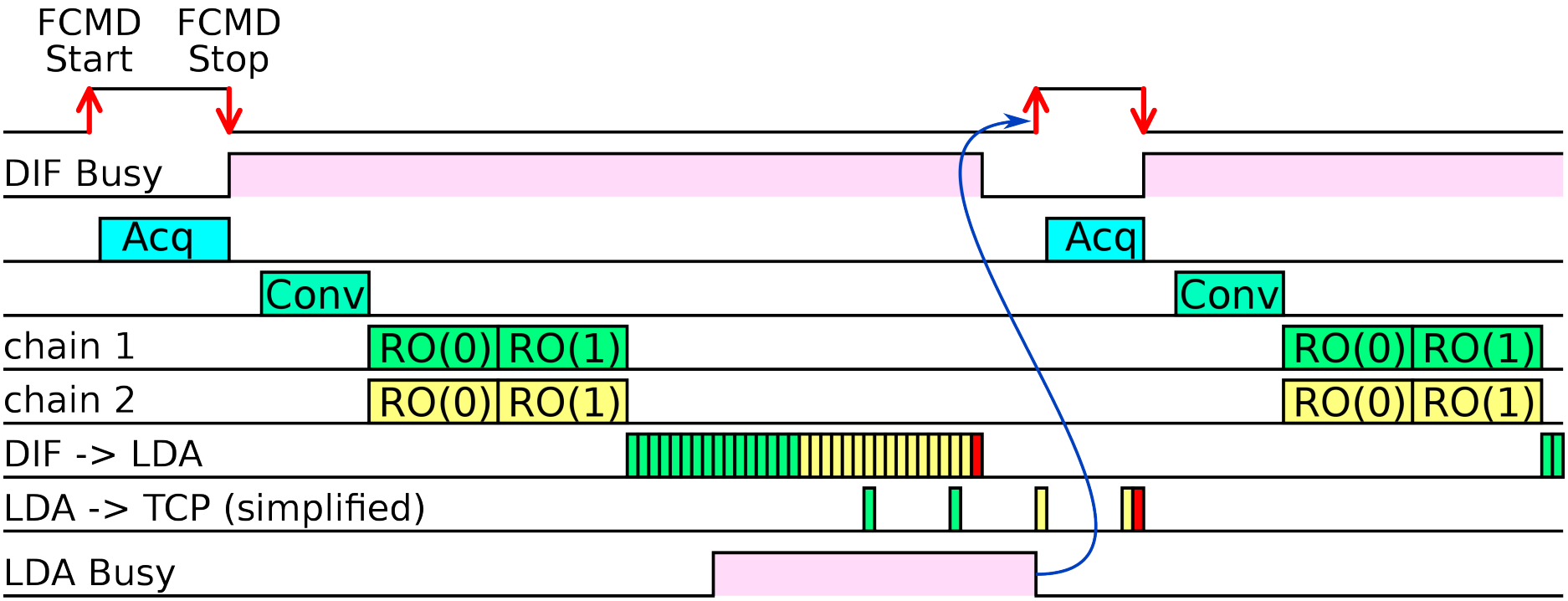


- Acquisition is started when all data are sent from the DIF, however:
- 40ms wait is counted from the last packet received from TCP by Labview. After the timeout a readout command is sent to DIFs
- Speedup is planned (more scenarios)

This year's AHCAL DAQ plans

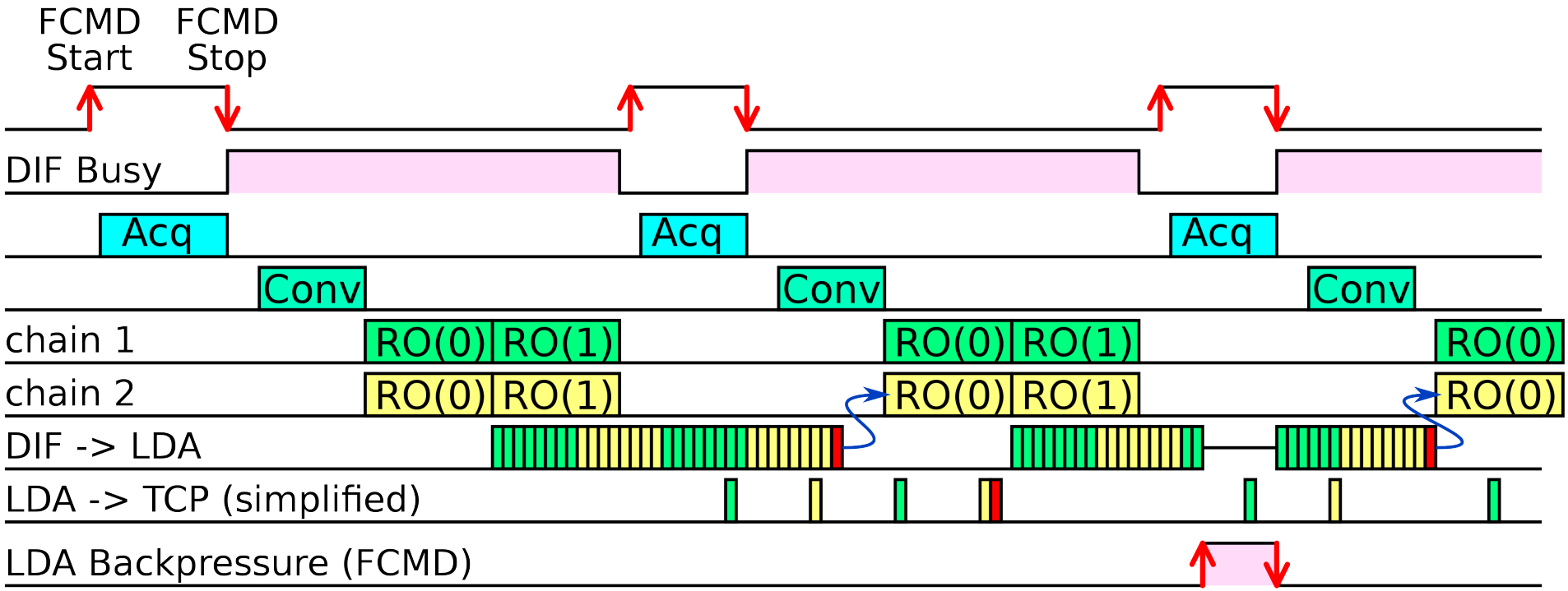
- Wing-LDA
- LDA + DIF speedup (command-less readout, backpressure implementation)
- Modification towards compatibility

Short-term speedup plan



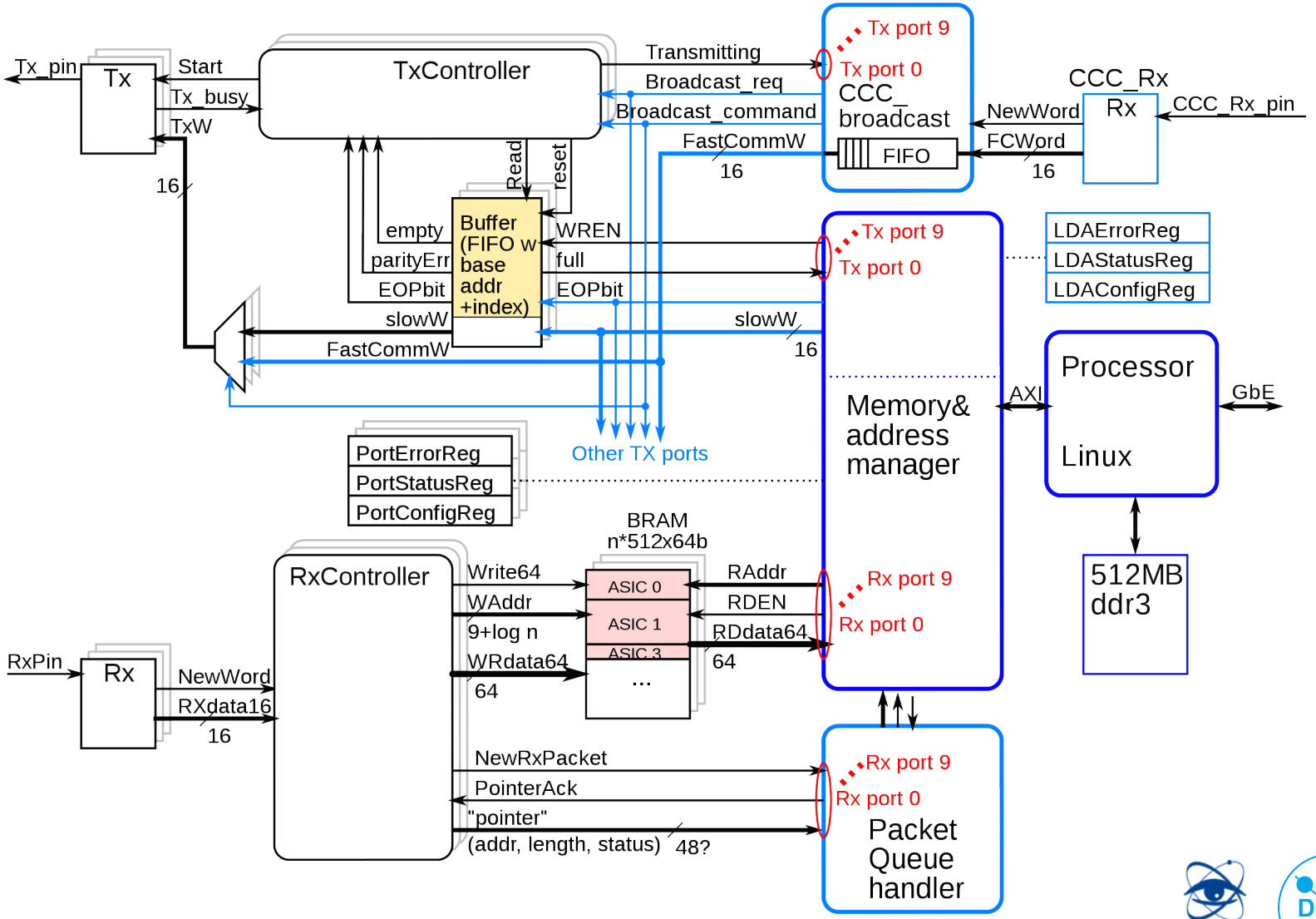
- Readout of SPIROC can start as soon as the conversion is done
- Sending of the data from the DIF to LDA can be started automatically when the LDA is ready to handle the full readout. Easy fix: LDA contributes to the busy signal
- RO cycle number has to be used in the SW, otherwise packets can get misordered

Long-term speedup plan

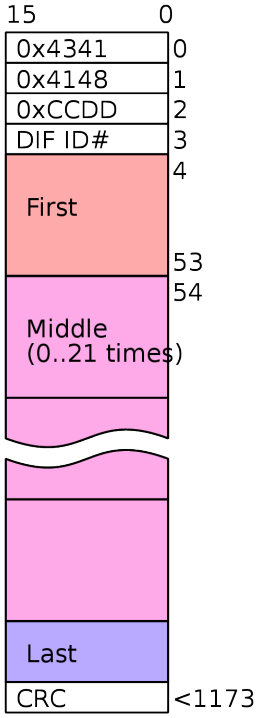


- We can (the DIF is capable of) start new acquisition as soon as all SPIROCs are fully read out
- DIF → LDA transfer will run in parallel (on the background)
- LDA backpressure mechanism needs to be implement
- Danger of EMC noise during acquisition: needs to be explored
- RO cycle number has to be provided by DIFs (not LDA)

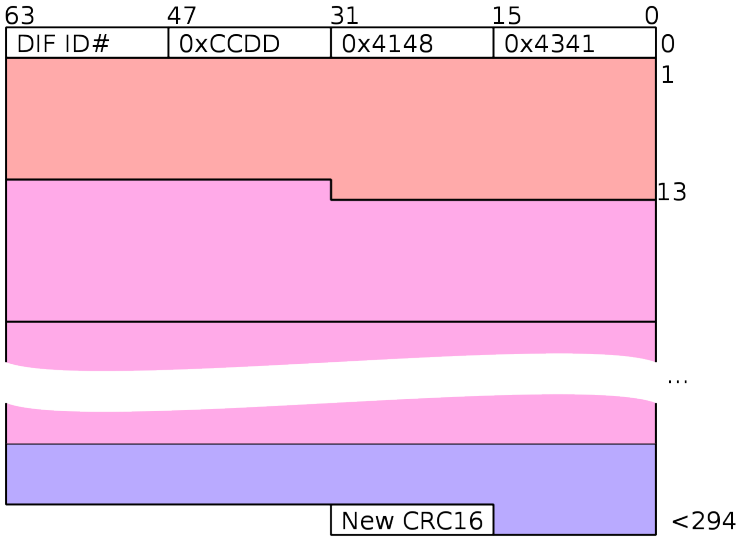
LDA concept 2014-06-24



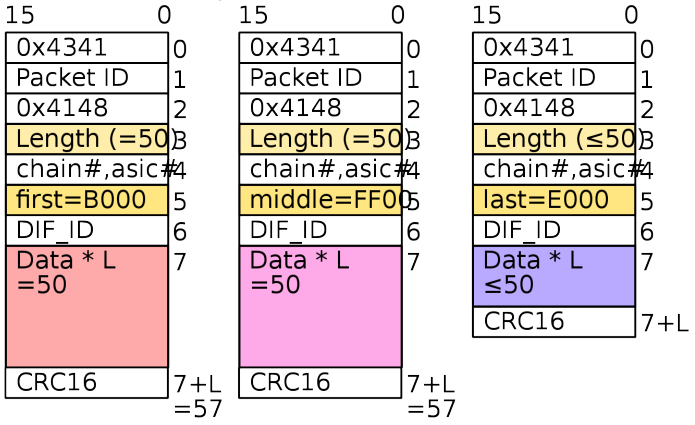
Packet merging



Merget READOUT packet: (16-bit/64bit addressing)



READOUT packets: first, middle and last



Block transfer command,ack