AHCAL DAQ.

Status and Outlook

AHCAL DAQ people

Combined DAQ meeting

DESY Hamburg, Jan. 19th, 2015

HELMHOLTZ GEMEINSCHAFT

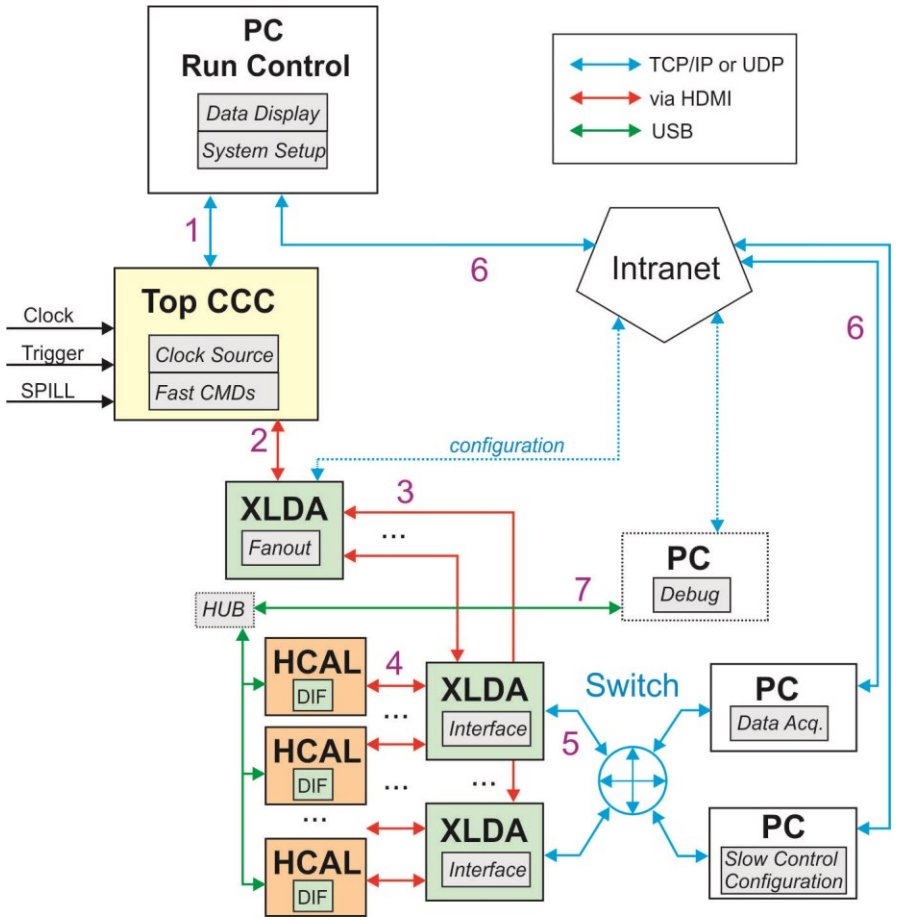
CALICE Calorimeter for ILC

AIDA

DESY

AHCAL DAQ - Structure

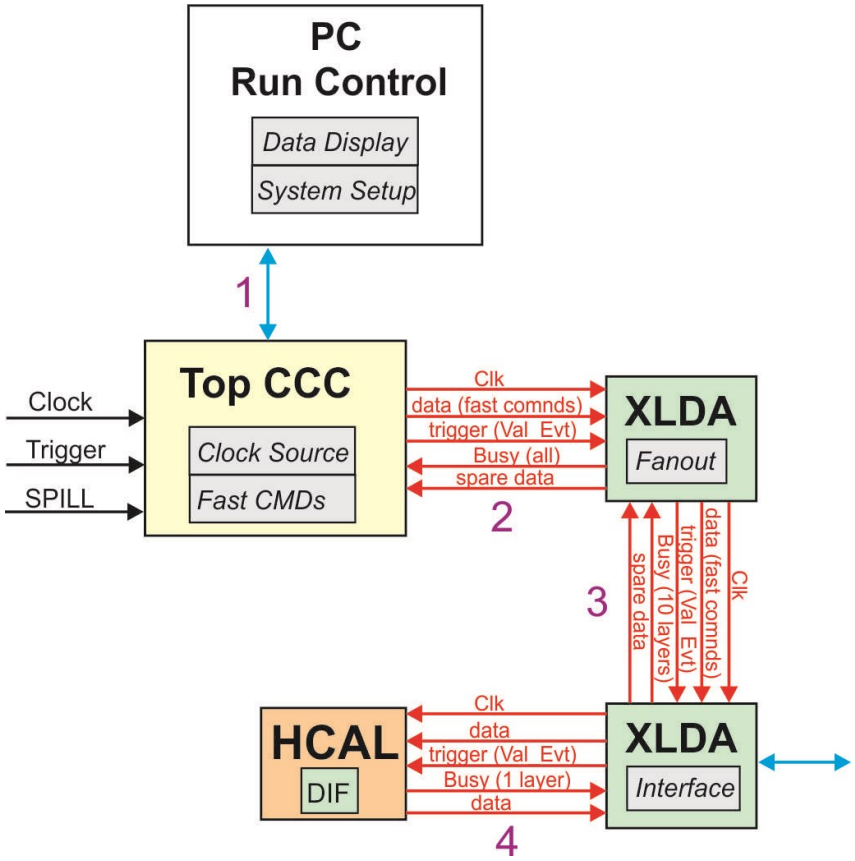
- Run Control PC: Detector Init, Start/Stop Data Taking
- Top CCC: Distribute global signals (Clock, SPILL, Trigger), collect status (BUSY)
- Sub-PCs (each detector): save data, online display, debugging, define configuration data.
- LDA: Zedboard (10 DIFs), to be replaced by Wing-LDA (96 DIFs)
- CCC: Zedboard
- Easily extendable by other detectors.



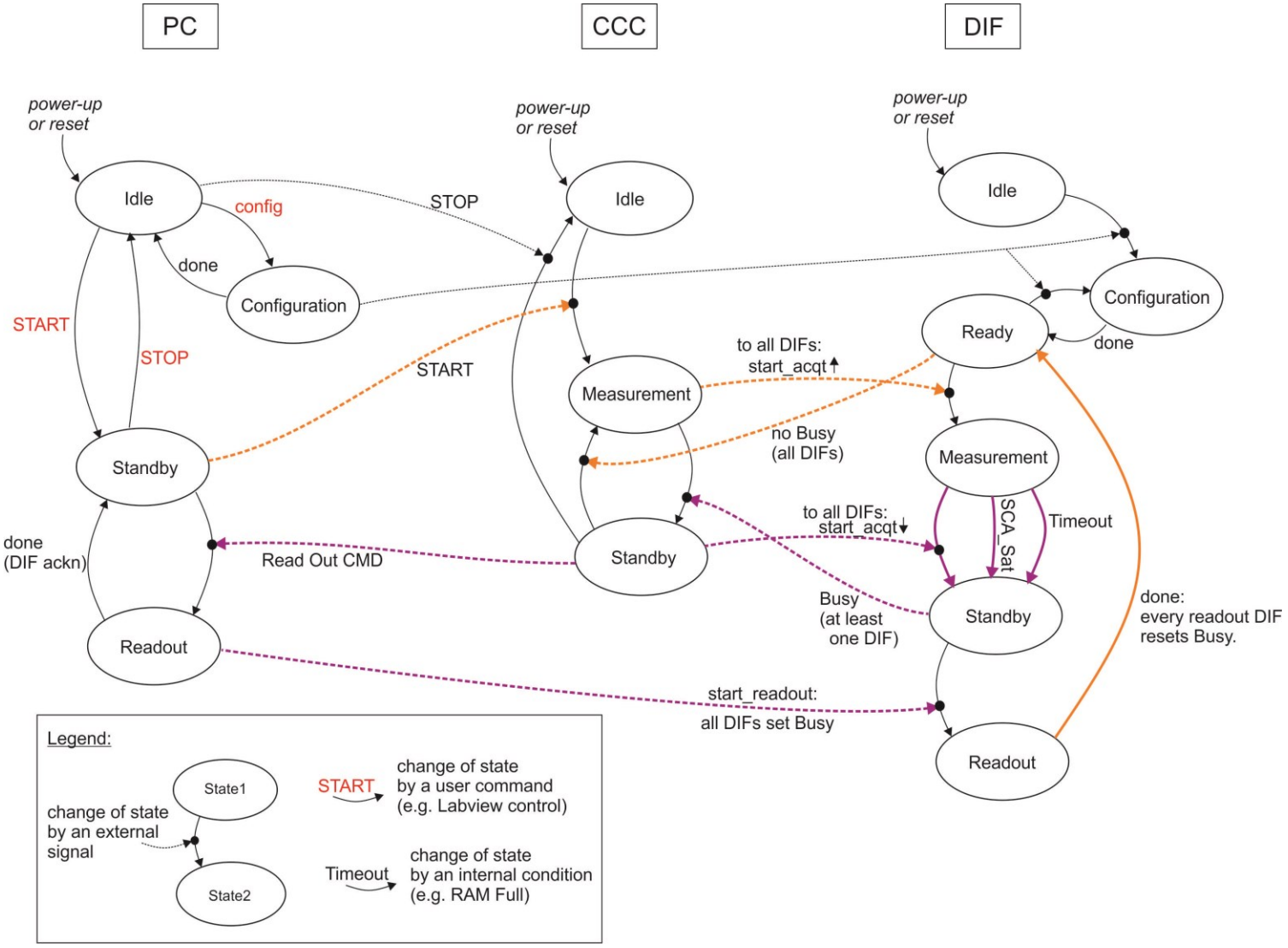
AHCAL DAQ – Interface signals (HDMI)

- Clock: 40MHz
- SPILL as “gate” for data taking
- Trigger for event validation

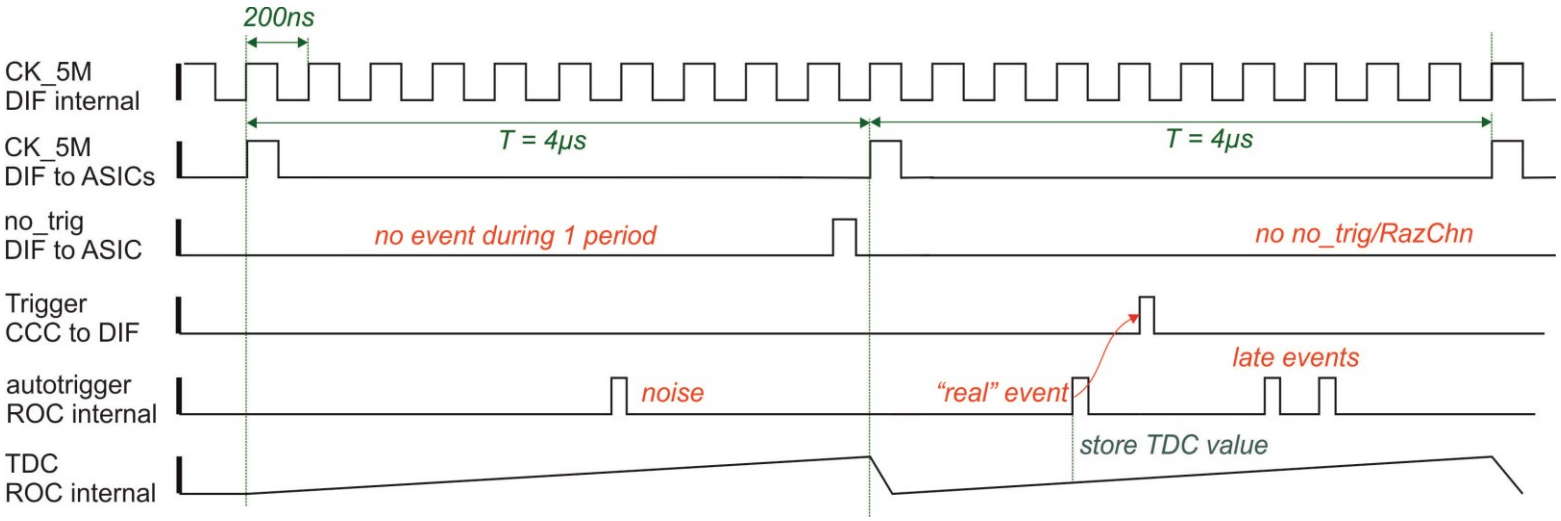
- Fast Commands (Top-CCC to all DIFs): 16-bit (mainly START/STOP)
- Block Transfer Commands (PC to one or more DIFs): n*16-bit, following the original specification from DIF task force
- BUSY (DIF to CCC) for run-control
- Data LDA ⇔ DIF : UART coded



Flow Control (how to use the BUSY)



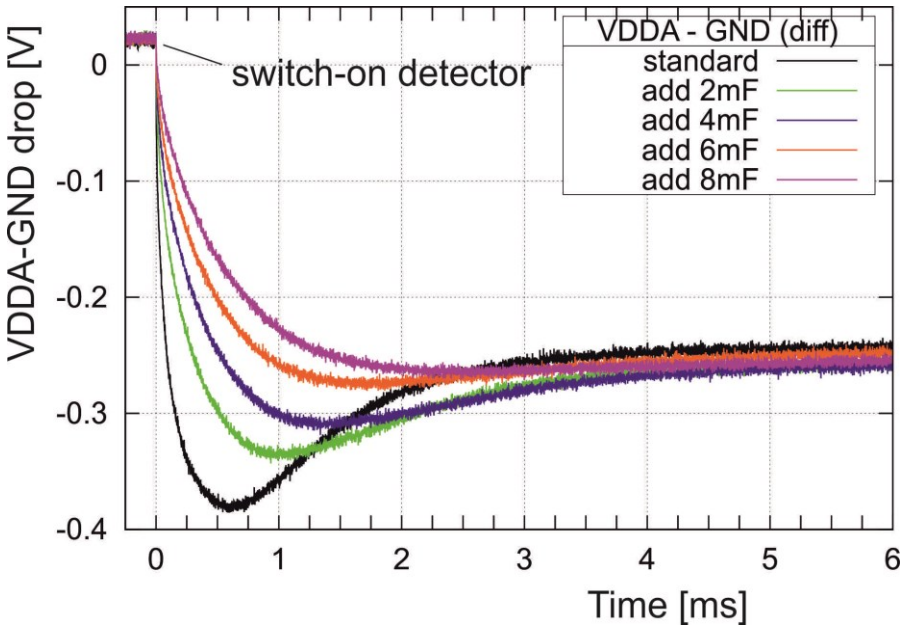
Data Taking

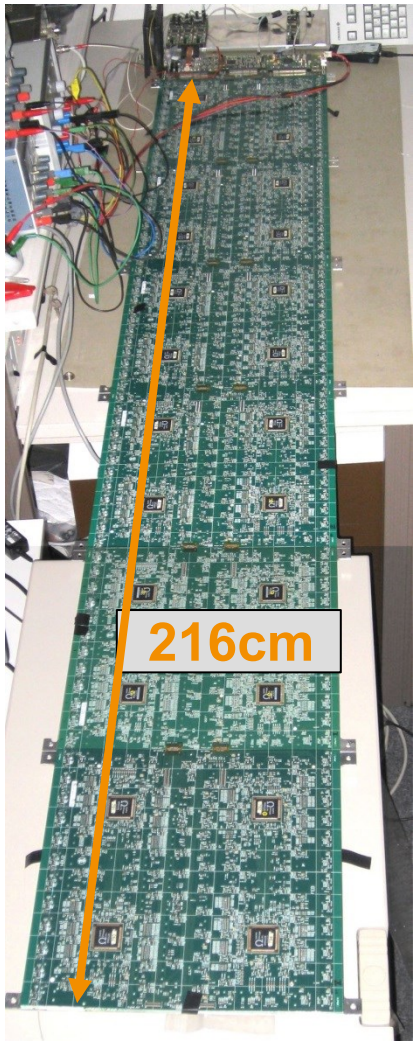


- AHCAL needs event validation (no_trig control) and therefore slow data taking clock (4µs clock period) for SiPM noise cancellation (testbeam mode).
- AHCAL can run with 3-5MHz clock (ILC-mode, tested) technically.
- Three stop conditions defined: memory full, timeout, "stop" from CCC.
- Timing information in readout data: Measmt. Counter, Bunch-X-ID, TDC.
- A full front-end can be read out with 2-4Hz.

Power Pulsing

- Power Pulsing tested with USB DAQ.
- Rather long timing constants when switched on:

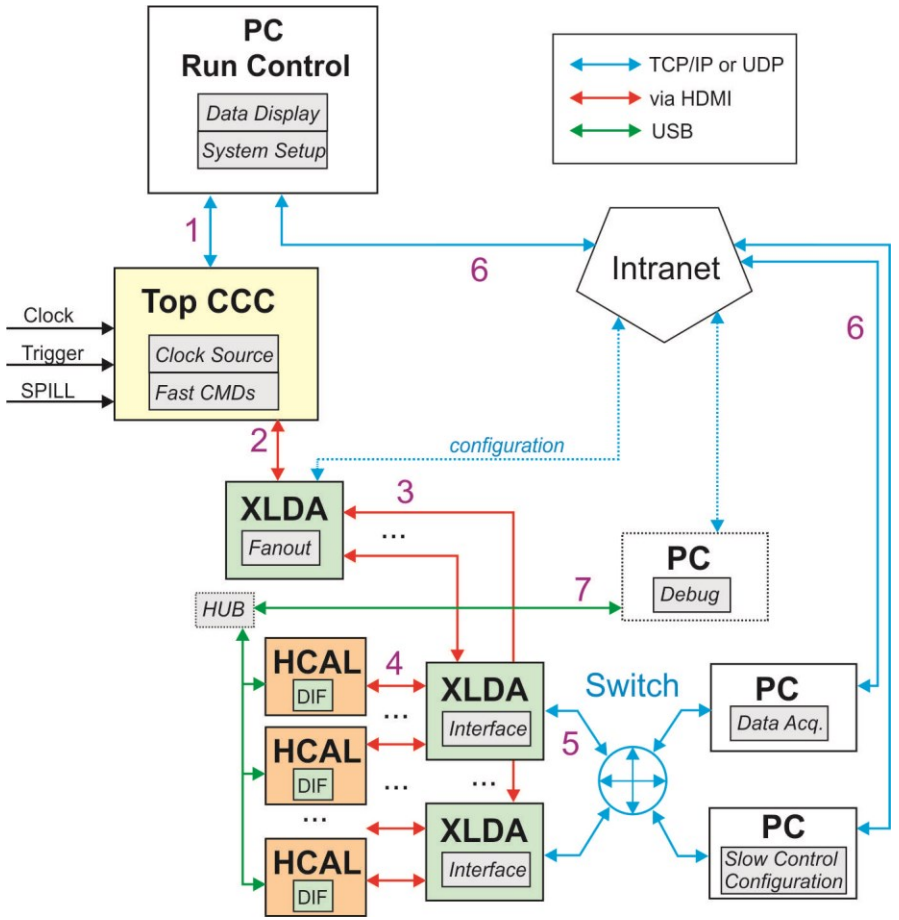




- Needs further testing and integration into new DAQ.
- We cannot operate a full layer without power-pulsing!

Software

- Labview for configuration, global run control and data display. MS-Win on Run Control PC.
  We would like to keep Labview for raw data display.
- Linux and C for data readout (LDA controller, Data Acq. PC). Online display (root based).
- Labview for USB debugging.
- Labview for operation of Wiener MPOD power supply.



Conclusions and Next Steps

- AHCAL DAQ running, can be synchronized best via BUSY to other detectors.
- Next: Power Pulsing with new DAQ and new (available) HBU3.
- This year: Redesign of DAQ Interface Boards (DIF, CALIB, POWER). DIF needs new FPGA (old one outdated): Xilinx ZYNQ
- Soon: Integration of Wing-LDA

- For command structure and further details see: http://adweb.desy.de/~reinecke/DAQ_docu.pdf