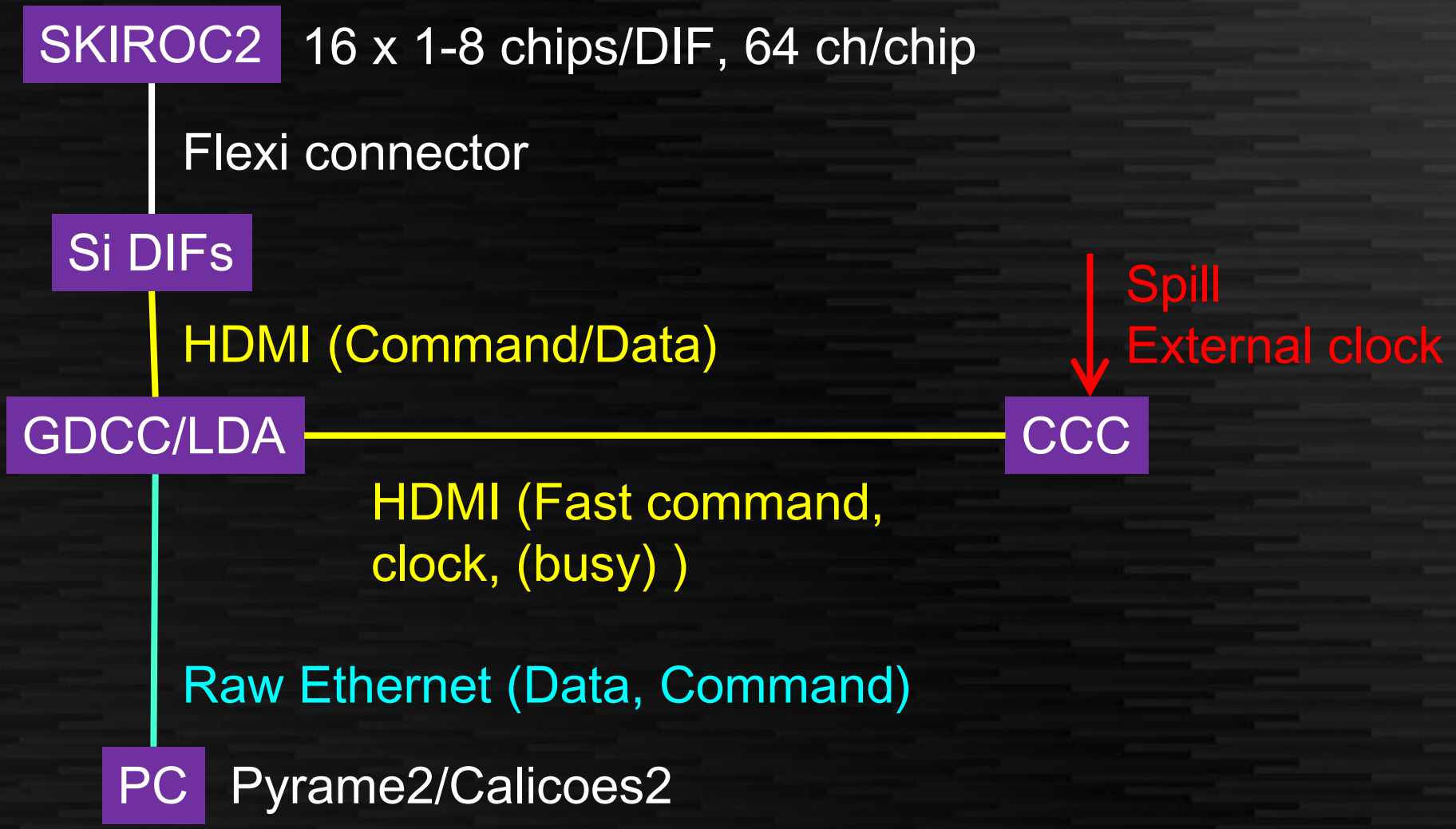
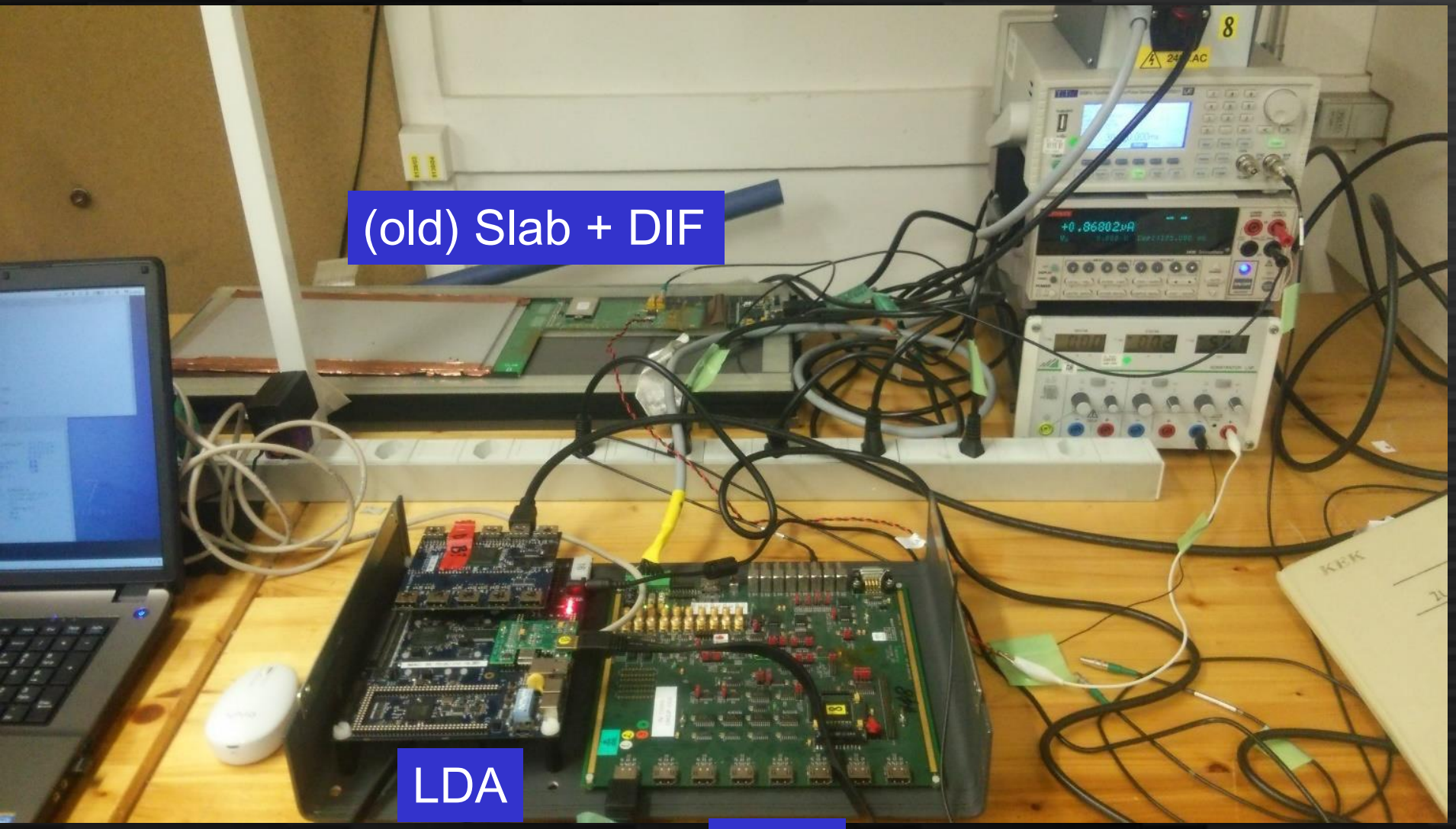
SiECAL DAQ

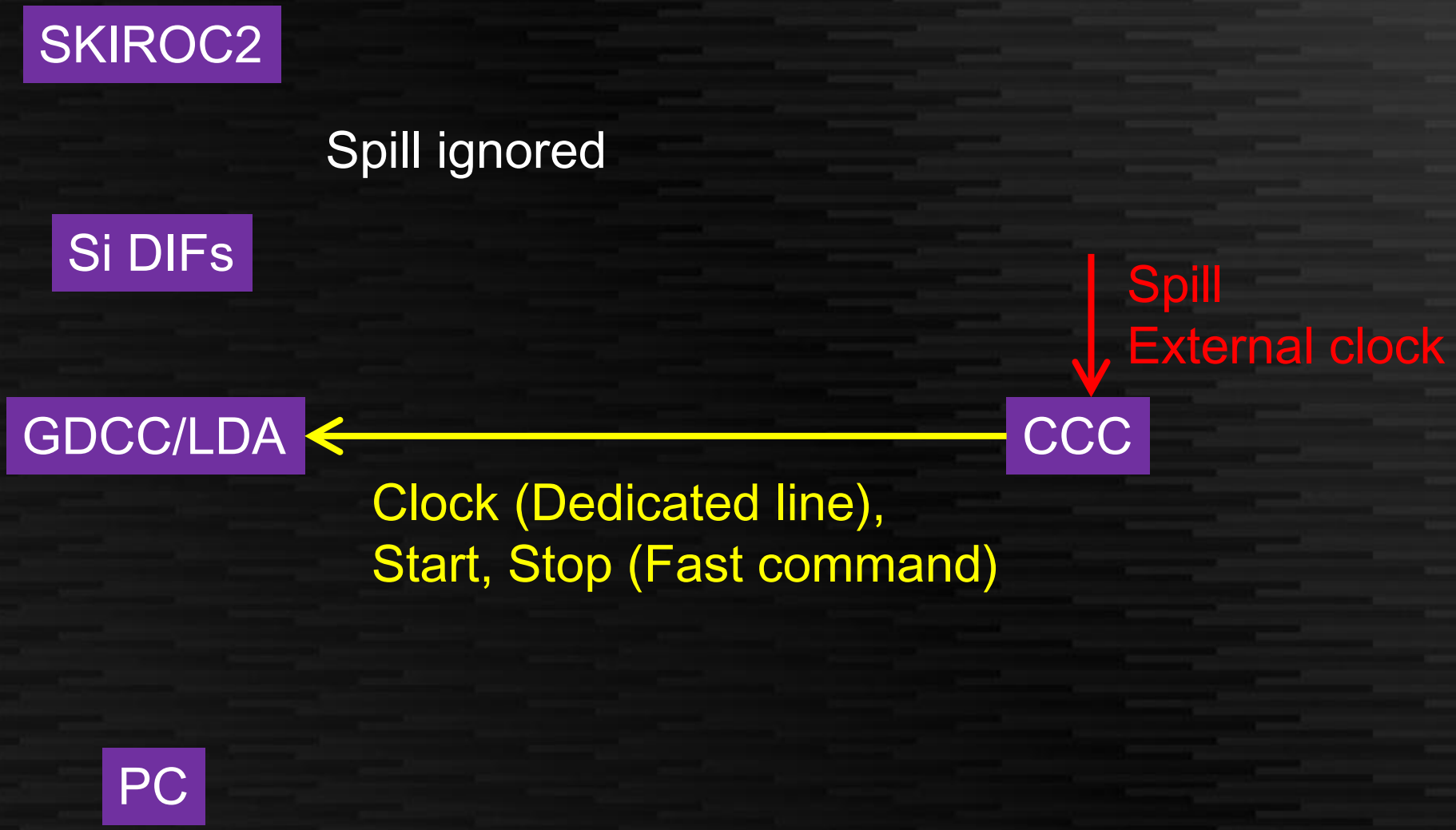
Taikan Suehara
(Kyushu University, Japan)

SiECAL Block diagram

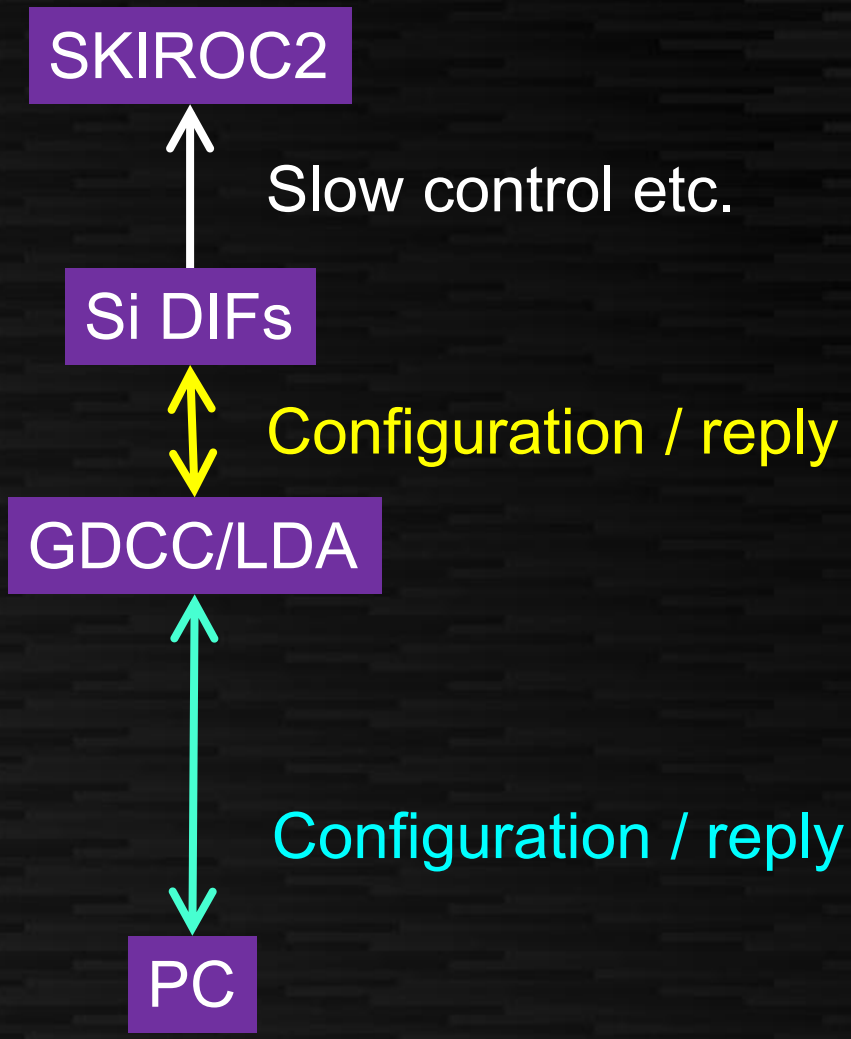



(old) Slab + DIF
LDA
CCC

Before configuration



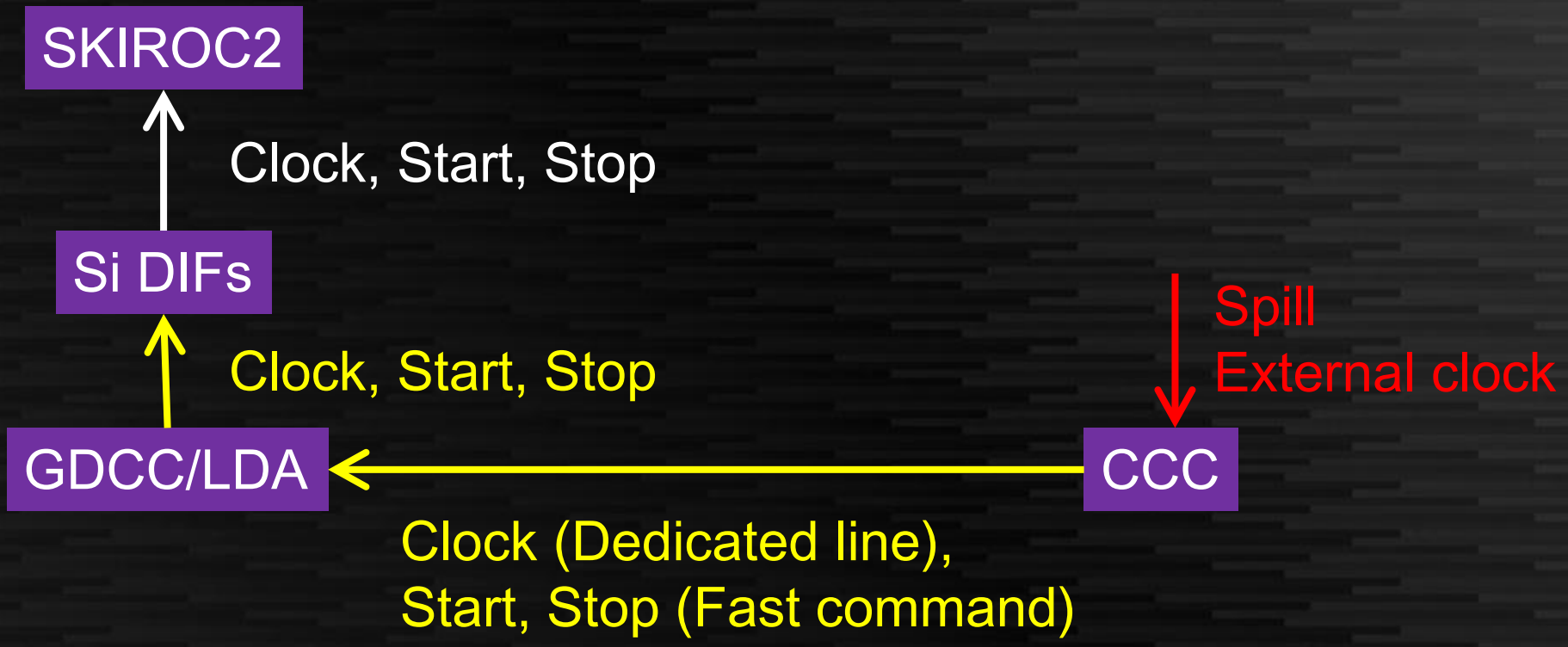
Configuration



CCC

No configuration

After configuration: command flow

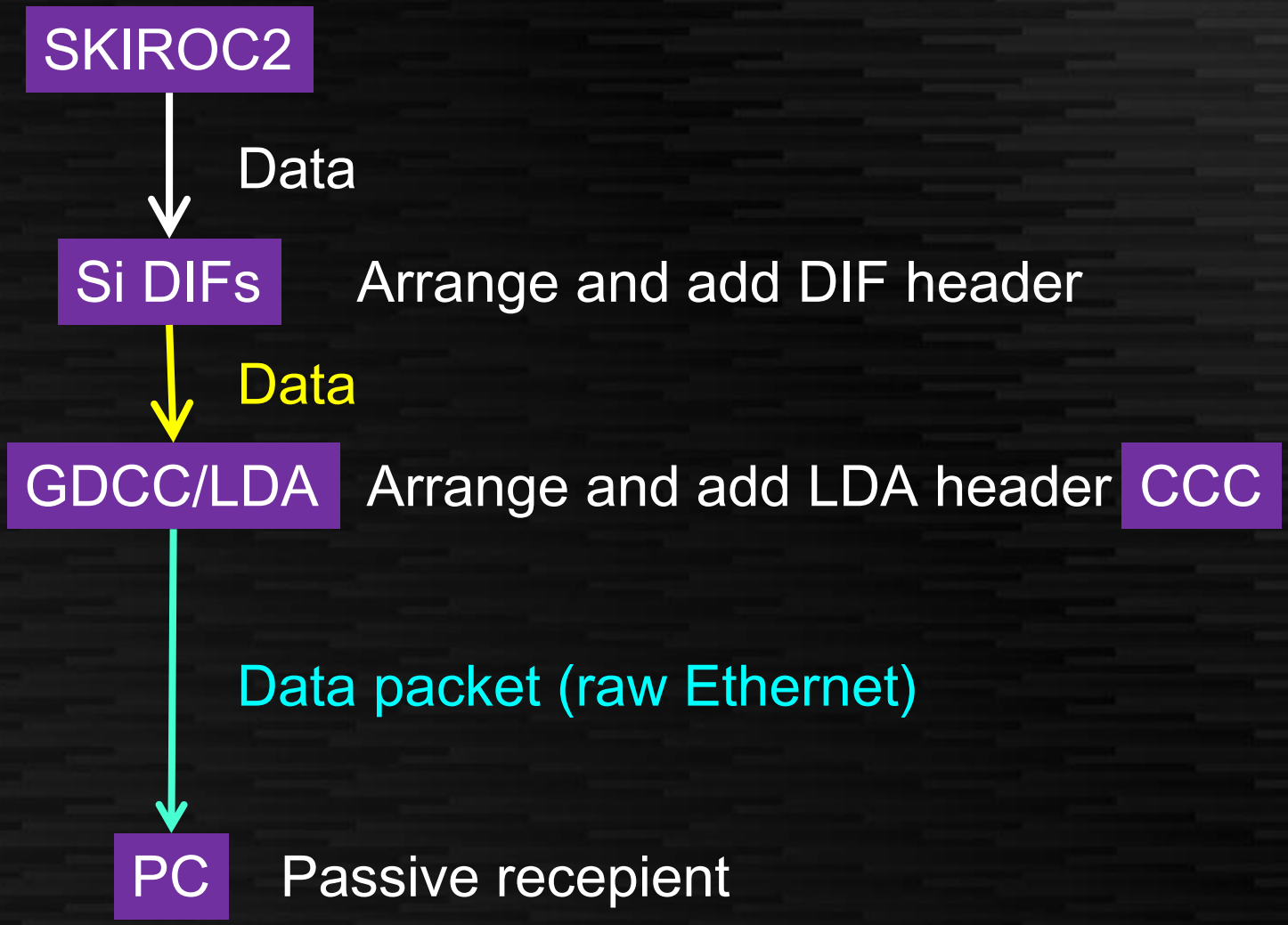


Rising and Falling edge of spill converted to fast commands in CCC

PC

No command related to start/stop

After configuration: data flow

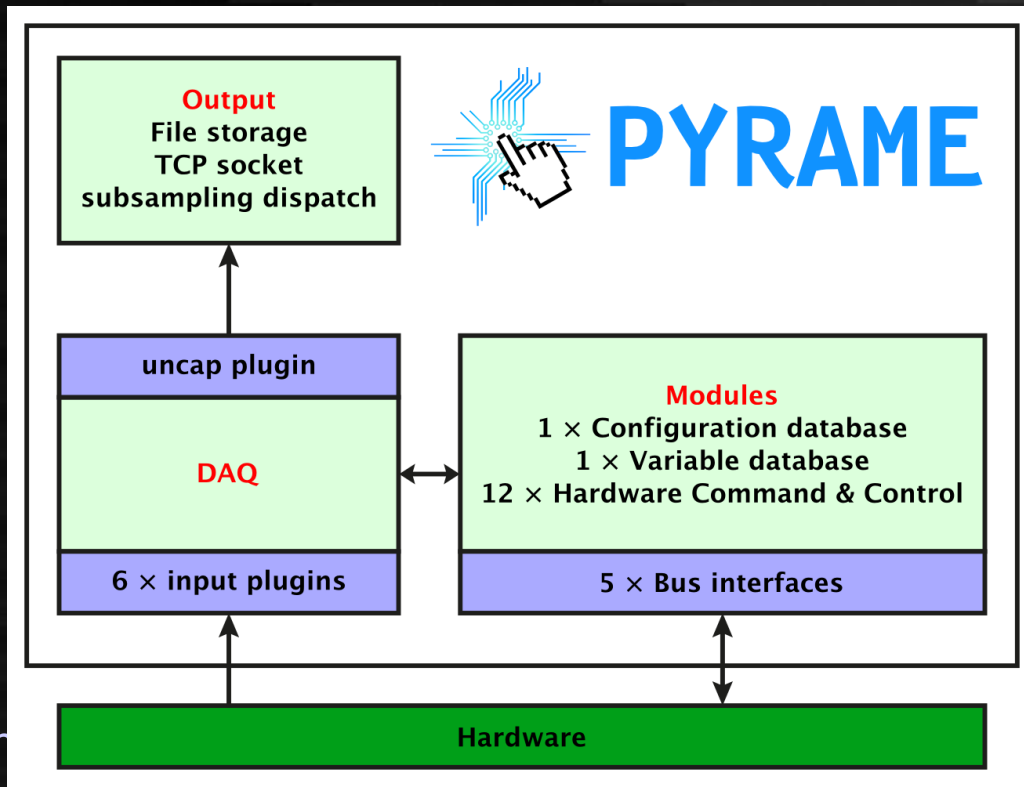


Technology overview: hardware

- CCC: UK origin
- LDA: UK origin, raw ethernet
  - being replaced to GDCC in LLR
  - “compatible” design but fewer packet drop
- DIF: Communicate with compatible commands to UK DAQ
  - 8b/10b encoding, oscillating BUSY

Technology overview: software

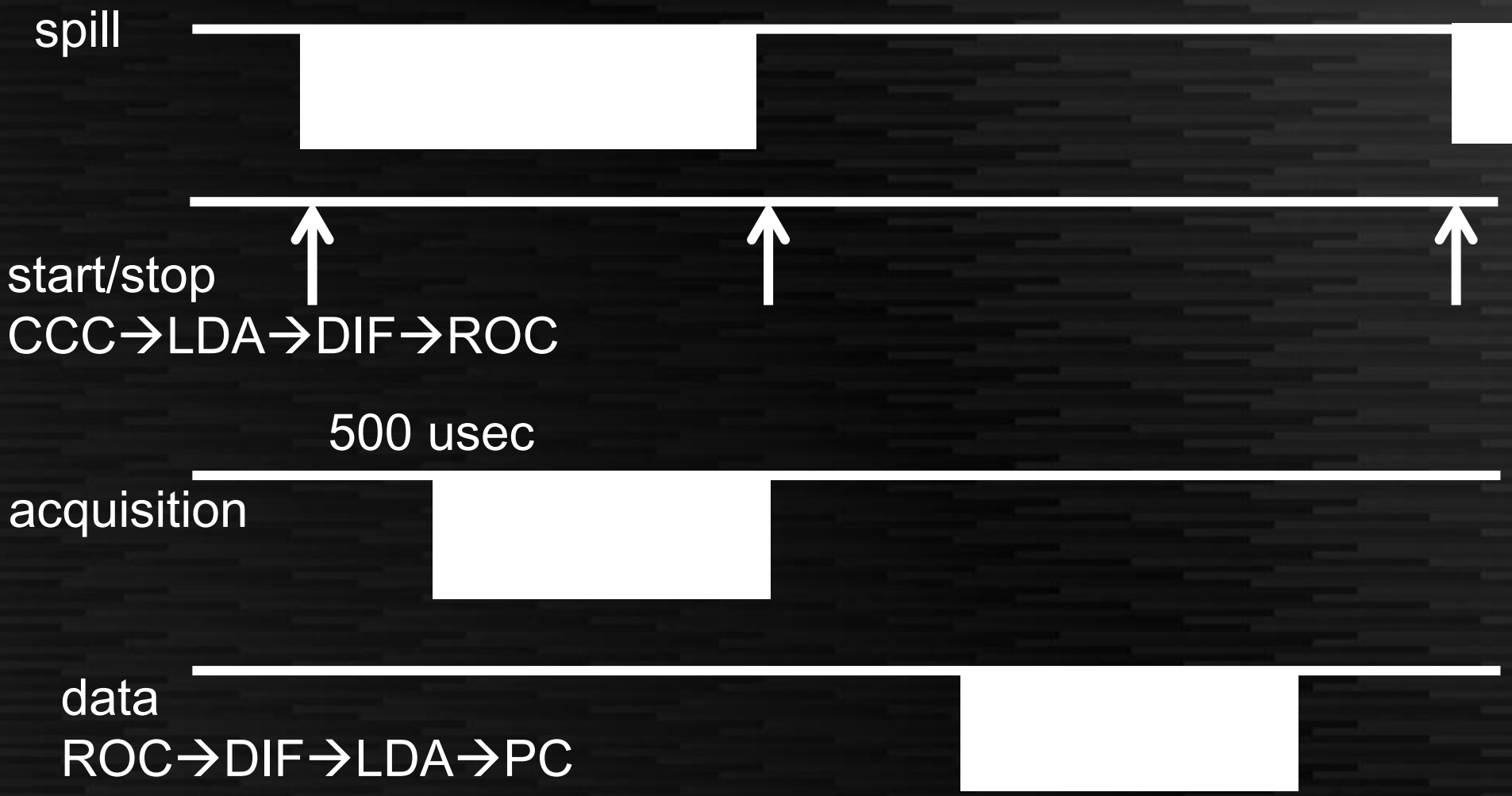
- Pyrame: a modular framework for testbench based on python
  - New version released, well documented
  - http://llr.in2p3.fr/sites/pyrame/
- SiECAL module is coded on CALICOES on pyrame



CALICOES (old) and EUDAQ in CERN TB last year

- CALICOES (pyrame) has a socket output
  - I attached a EUDAQ module via this for CERN TB
- Configuration can be done in the framework
  - Send a message to configure may be possible but not done in CERN TB
- pyrame has event-building feature, but currently not used for combined DAQ
  - Since we built events inside EUDAQ

Timing chart



Things to discuss (shown in kickoff)

- Common master clock frequency
  - To assure simultaneous BX counting
- Common BX clock frequency
- BUSY treatment
- → Common CCC? or just clock synchronization?
- High level DAQ software (EUDAQ?)
  - Run control, event building, run number, monitoring,…
- Common data format (LCIO class)

- Partial or optional sharing of firmware and software
- etc.