Notes from the SiD Workshop

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Optimization Targets

- ECAL with 25 layers only
  - Continue studies from last summer
- HCAL
  - Cell size optimization for a AHCAL
  - RPC vs. Scintillator
- Tracking
  - Layout question
  - Resolution requirements

On RPC's

- Currently have a GIGO problem
- Need to fix this before we can do any sensible comparison
- Jose and Burak promised code & support
- Goal
  - Have a more sensible RPC DHCAL simulation by April

On Tracking

- We have the “usual” questions
  - Layout, aspect ratio, layers
- And a new set because of pixel tracker ideas
  - In HV CMOS (SLAC idea), basically no charge sharing
  - Gives you 50 micron/sqrt(12)~ 14 micron
  - Is this ok, do we need 5.5 micron ?

CLIC all-silicon Tracking

- Rosa offered this to us during the workshop
- My statement
  - Currently no resources to help developing it
  - But definitely interested in testing, using, bug reporting
- Waiting for a first version ...

Other items

- State of the documentation
  - Lots of info → scattered around
  - Very difficult for new people to make a start
- Suggestion
  - News space on Confluence
  - Move stuff in as need
  - Norman and Jan volunteered