ScCAL Data Acquisition System

Timing

- News
- Clock and synchronization
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Calorimeter for ILC

HELMHOLTZ ASSOCIATION

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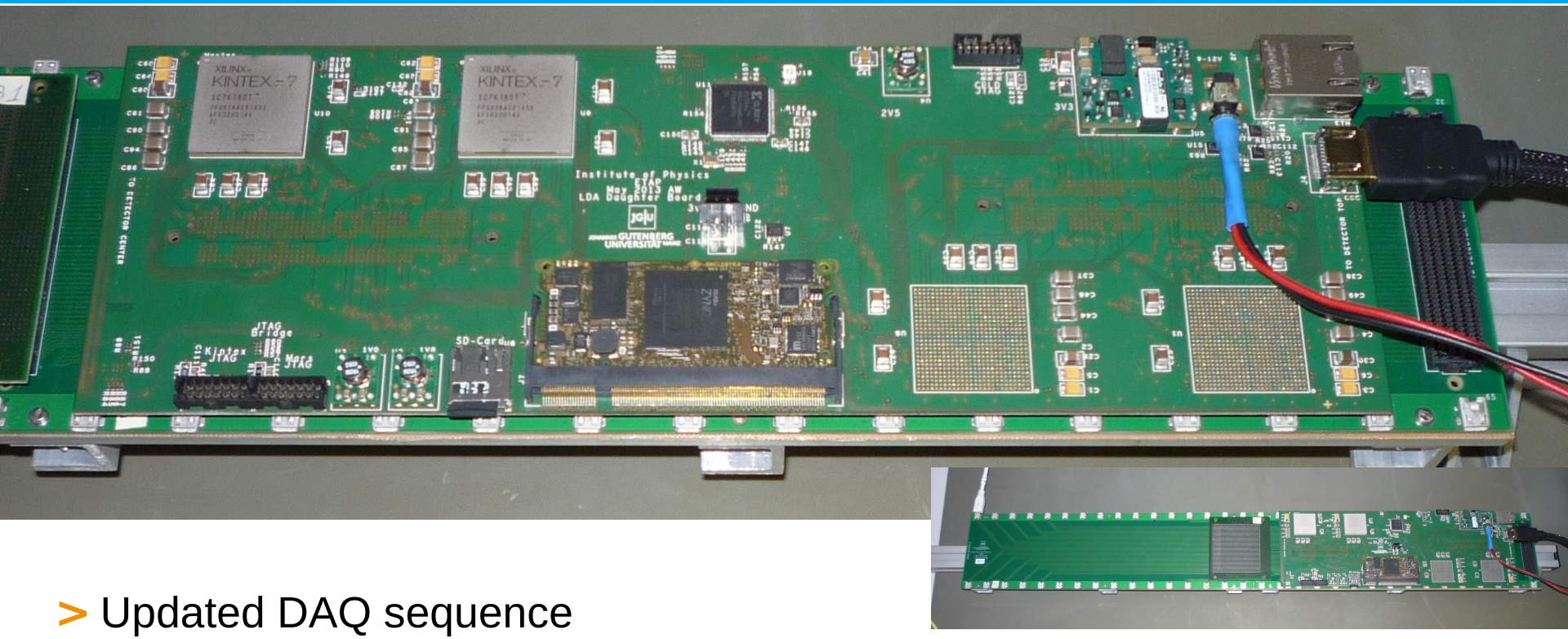
Akademie věd ČR, v. v. i.

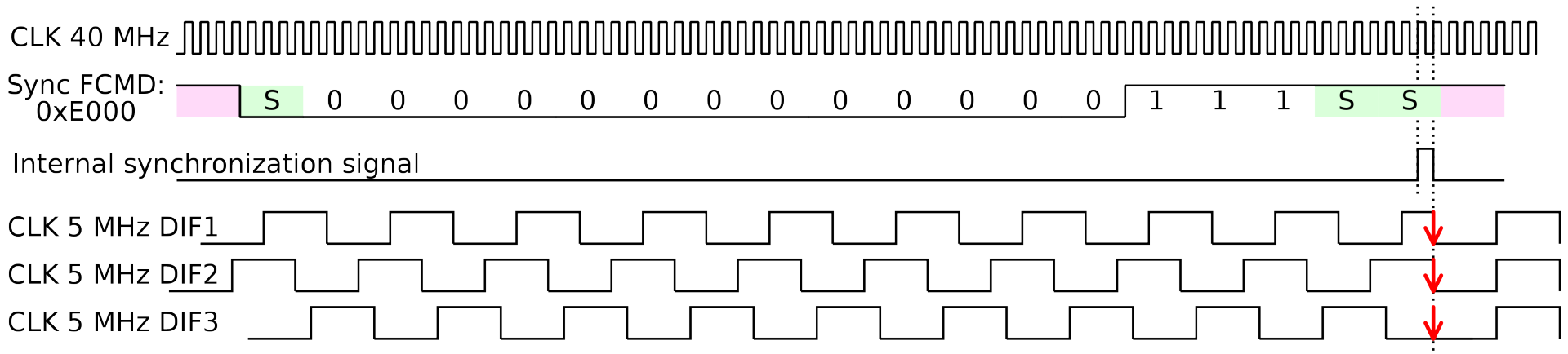
DESY

News



- Updated DAQ sequence
  - No readout command anymore, data sent immediately after the conversion is done
  - Acquisition controlled only by the CCC fast commands (with DIF busy signals)
- Current work in progress: Wing-LDA
- Hardware designed by uni Mainz
  - 2 (out of 4) Kintexes XC7K160, each connects to 24 DIF ports
  - “Mars module” by Enclustra: Zynq 7020 (FPGA +ARM) running Linux, 1G Eth
- Firmware being developed

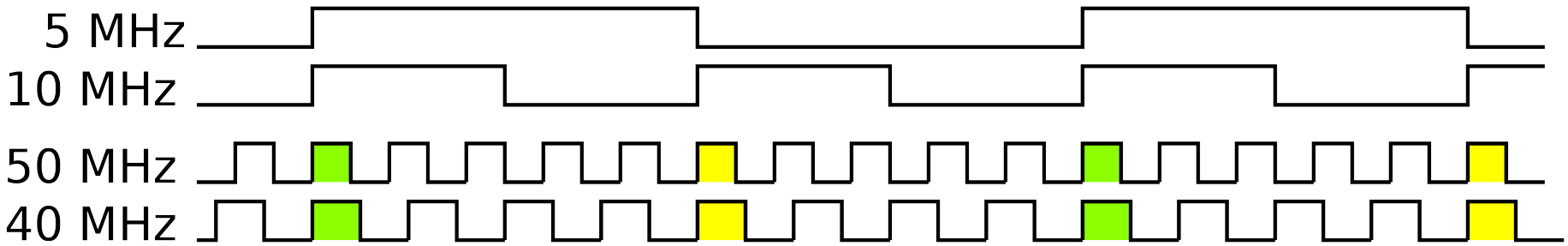
Clocks and synchronization



- Clocks:
  - **40 MHz** from CCC & LDA
  - **5 MHz** internal DIF clock (phase aligned with 40 MHz clock)
  - **250 kHz** BxID counter in TB mode (phase-aligned with 5 MHz), started by START ACQ fast command
- CCC and LDA send fast commands anytime (synchronized only with 40 MHz clock, no slower clock synchronization)
- DIF 5 MHz clock is synchronized by a Sync command: 0xE000 (LSB first!)
  - Sent before each run
  - Any Fast command take effect only after first 5 MHz tic
  - After reception of the sync command all DIFs share the same slow clock
- Readout cycle
  - Incremented by 1 by “stop acq” command in the LDA
  - Cleared by a special command to the LDA

Possible solution for common synchronization

- DIF clock 40 MHz to 50MHz?
  - 40 MHz is fundamental for DIF at the moment
  - Change to 50 MHz would require whole DIF retiming
  - For the next DIF version?
- Switch the CCC ↔ ScCAL LDA link to 50 MHz?
  - Not generally impossible, since 40 MHz and 50 MHz are both multiples of 5MHz
  - I need to know exact synchronization of other detectors to explore this possibility
- Restrict the CCC to send data only at selected clock edges according to the slower clock sync?
  - Easy to ScCCC, we have VHDL source code access.
  - Possible for others?
- Should we unify the CCC?

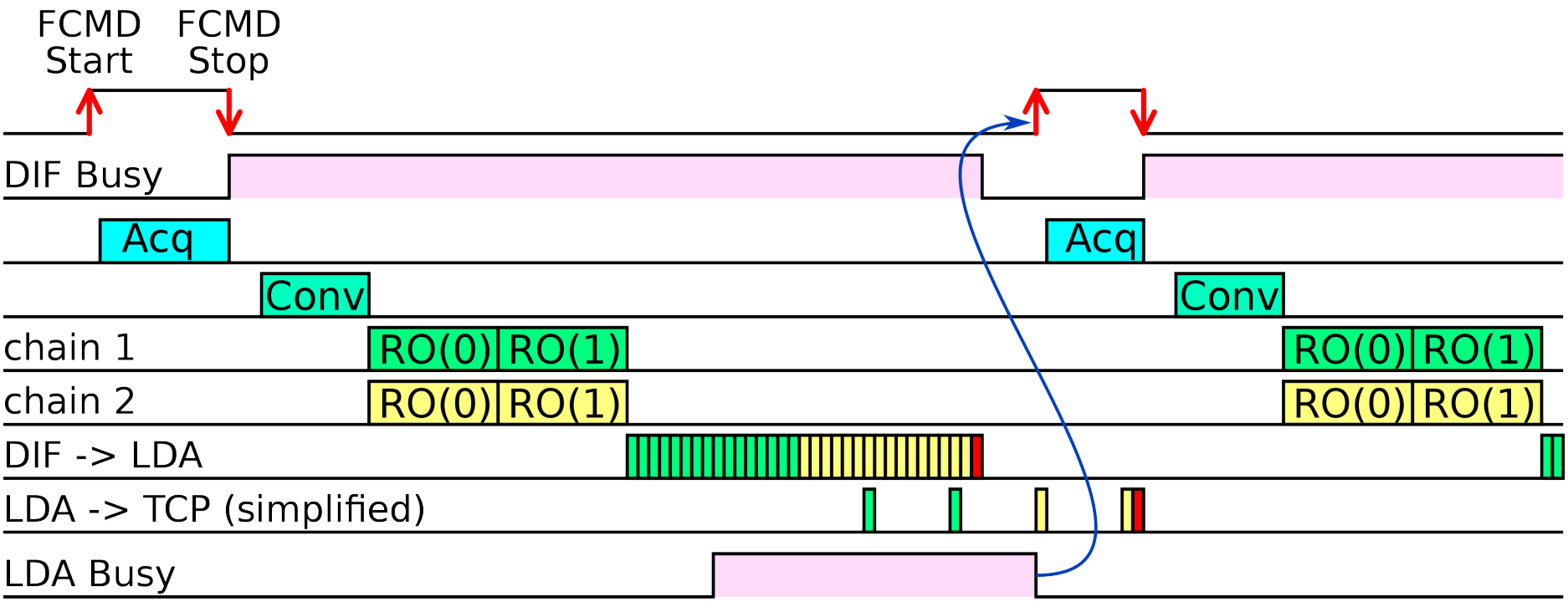


Backup

Questions to the discussion

- How precisely do we need to synchronize?
  - Precisely?
  - <20 ns?
- Do we want to use a single CCC for all detectors? If so:
  - What is the electrical specification? LVDS, but coupling?
  - What is the protocol specification
- What will be the fist common running that we should prepare for?

Short-term speedup plan (done)



- Readout of SPIROC can start as soon as the conversion is done
- Sending of the data from the DIF to LDA can be started automatically when the LDA is ready to handle the full readout. Easy fix: LDA contributes to the busy signal
- RO cycle number has to be used in the SW, otherwise packets can get misordered