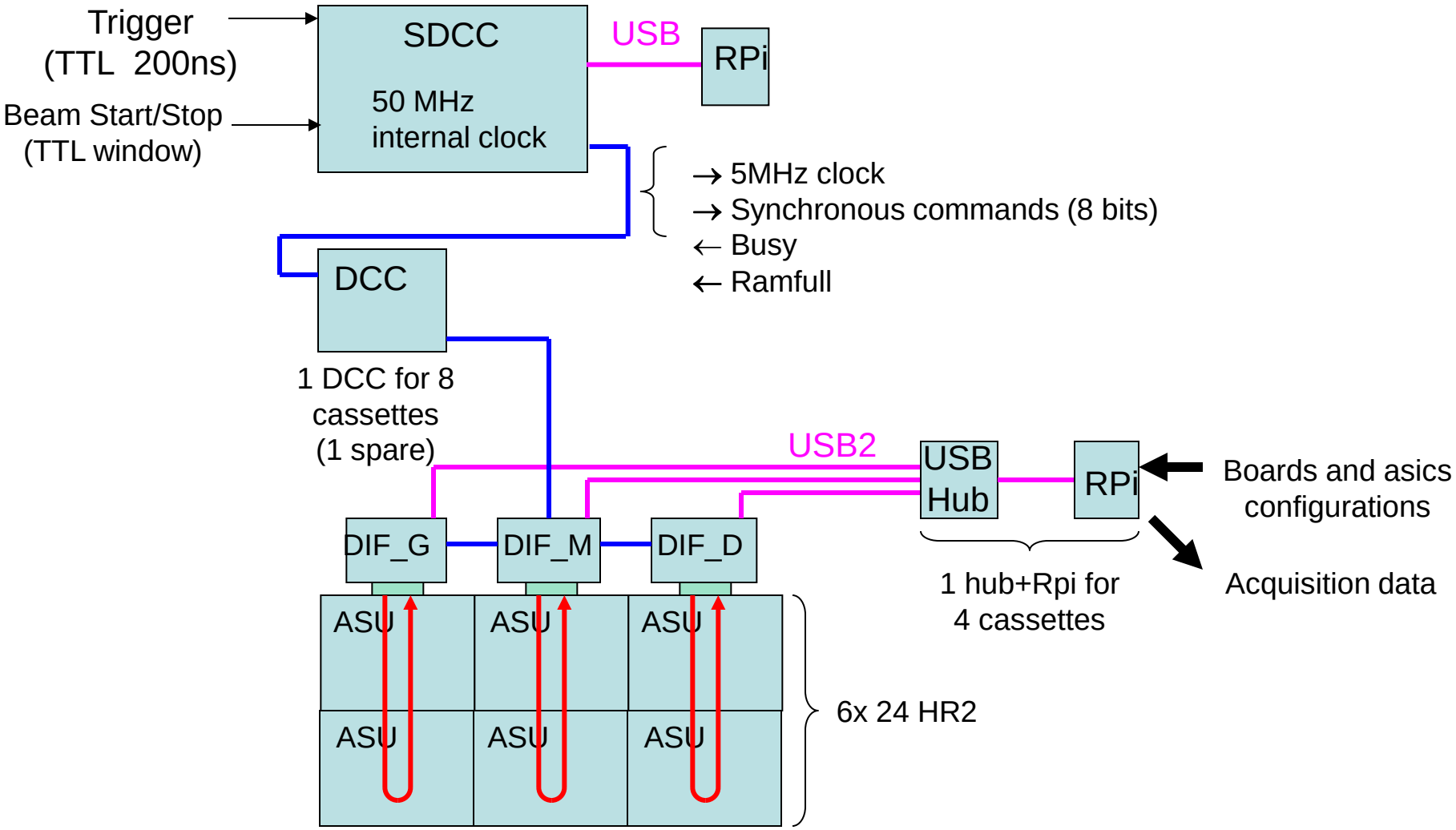
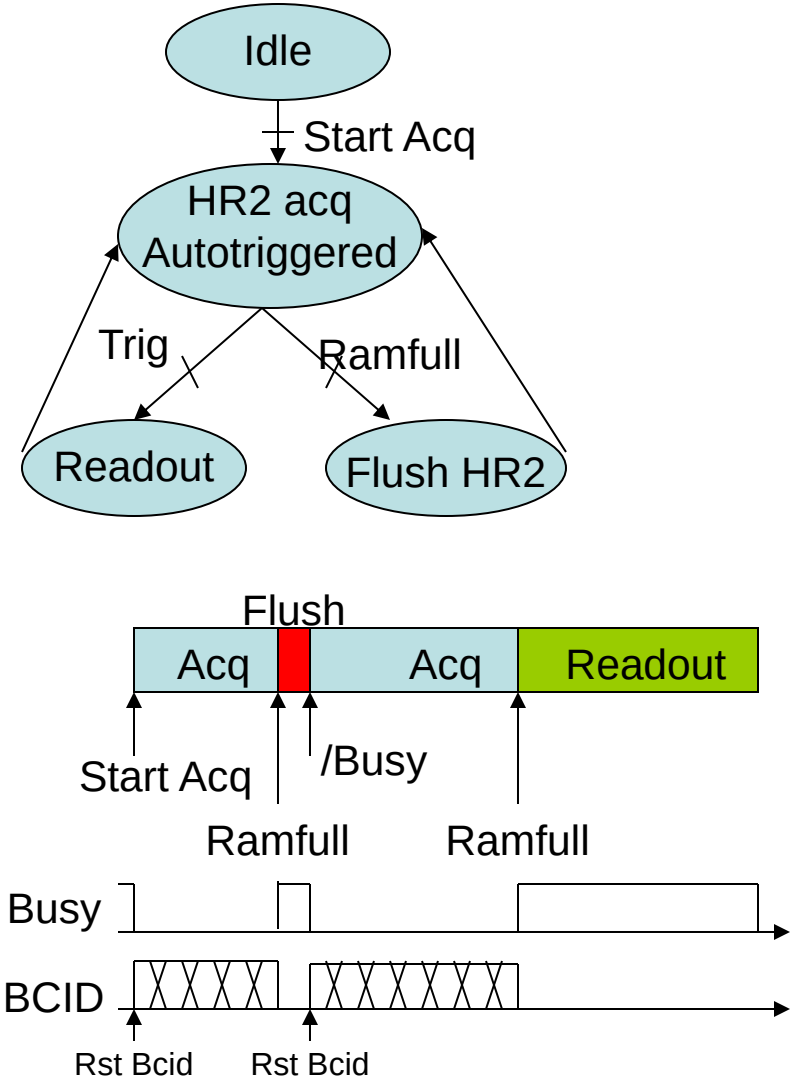
Hardware General View of SDHCAL

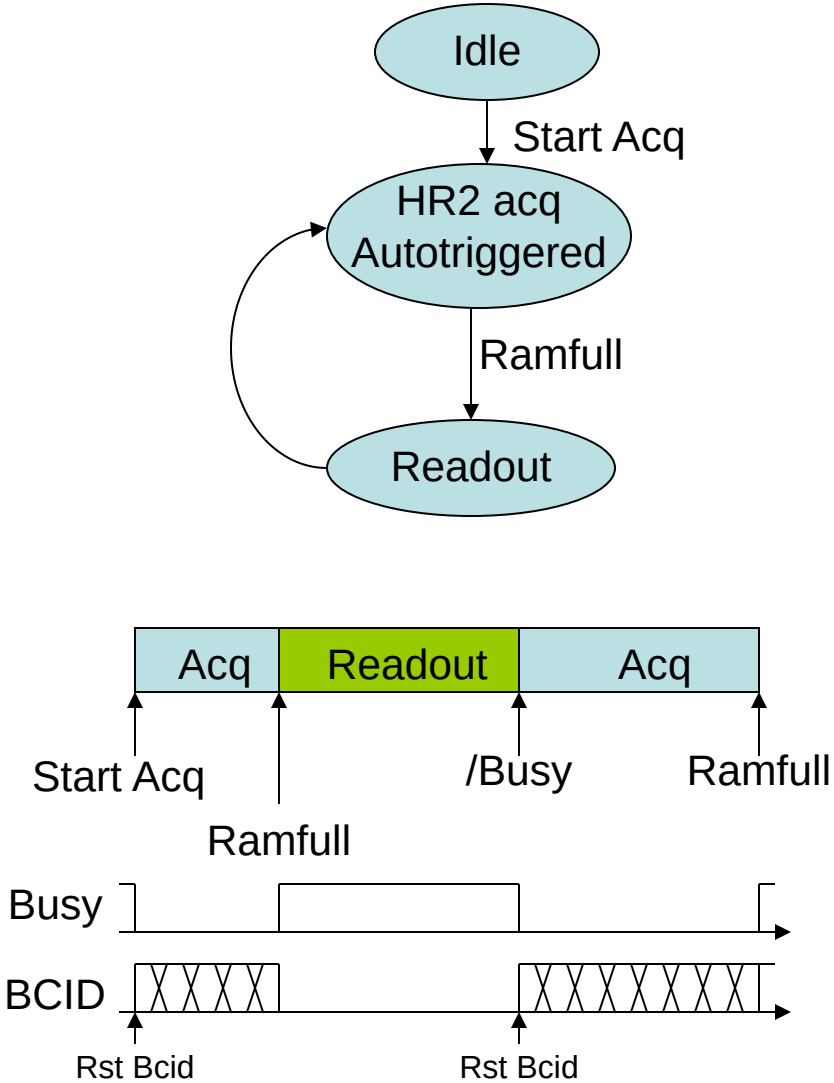


SDCC modes

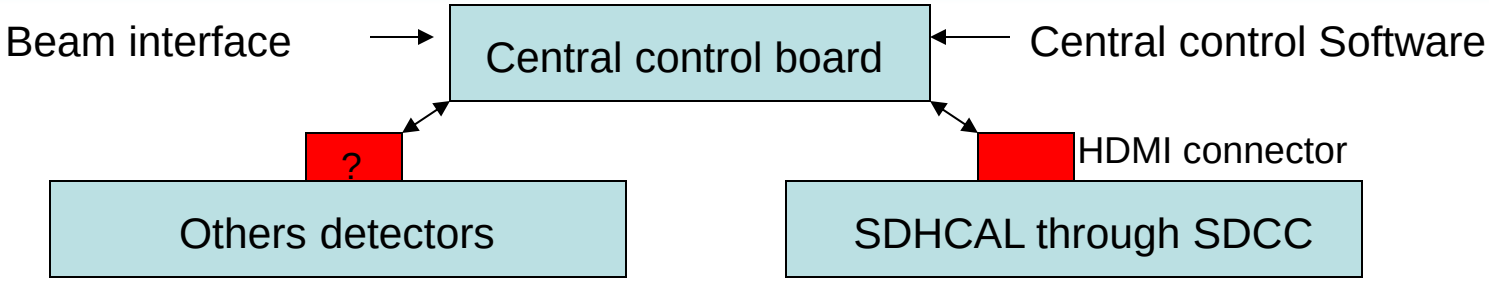
« Beamtest Mode »



« ILC Mode »



Central control



SDHCAl link to the central control board, AT LEAST :

- Centralized clock with frequency complient with all detectors (for us, 5MHz)
- Synchronous reset
- Start acquisition
- Trigger if working with external triggers
- Busy from SDHCAL

```
clk_lda_dcc_p              : in std_logic;  -- pin 1, AC coupled
clk_lda_dcc_n              : in std_logic;  -- pin 3, AC coupled
cntl_lda_dcc_p             : in std_logic;  -- pin 4, AC coupled
cntl_lda_dcc_n             : in std_logic;  -- pin 6, AC coupled
data_dcc_lda_p             : out std_logic; -- pin 7, DC coupled
data_dcc_lda_n             : out std_logic;
-- pin 9, DC coupled
sp2_dcc_lda_p              : out std_logic;
-- pin 10, DC coupled
sp2_dcc_lda_n              : out std_logic;
-- pin 12, DC coupled
trigger_from_lda_p         : in std_logic;
```

Future?

Who will be in beam test?
Assume SiECAL, AHCAL/ScECAL and SDHCAL?

When will the common beam test take place?

Who will design the central control board?

Who will design the software central?

When will we put all that together?
Assume it will take place at CERN?