

# Construction of the modules and impressions of the Pixel-TPC testbeam

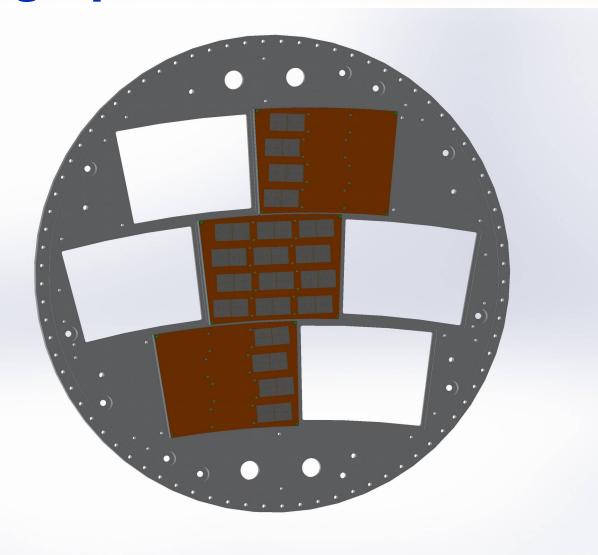
Michael Lupberger

University of Bonn PIXELS

LCTPC WP Meeting 02.04.2015



## **Design phase**





Endplate from inside:

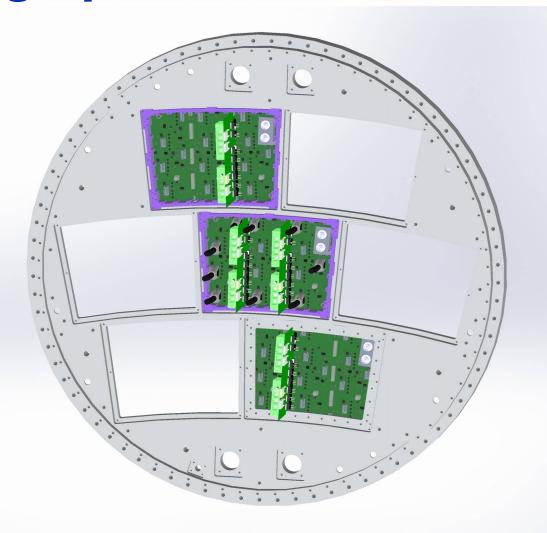
3 Modules

- 1x 96 InGrids
- 2x 24 InGrids

Guard on Insensitive area Grids slightly below



## **Design phase**





Endplate from outside:

3 Modules
Data readout
by HDMI cables

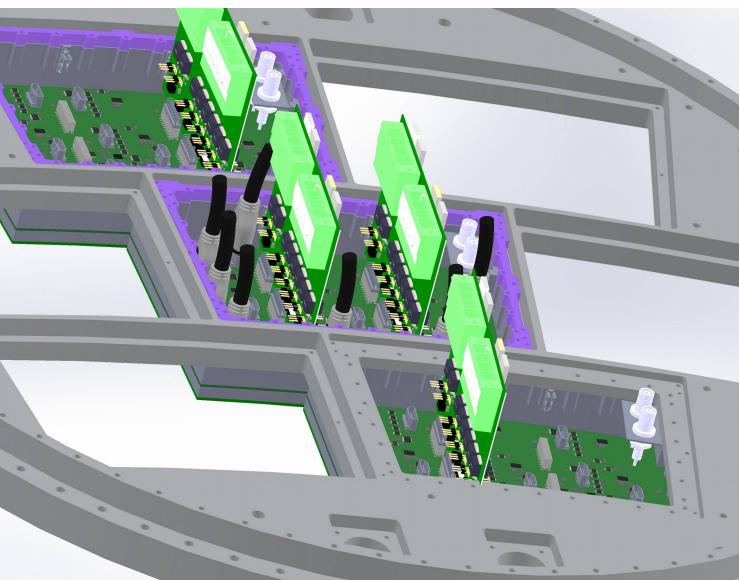
Water cooling inside module

Low voltage power boards

Grid, anode HV



## **Design phase**





Endplate from outside:

3 Modules
Data readout
by HDMI cables

Water cooling inside module

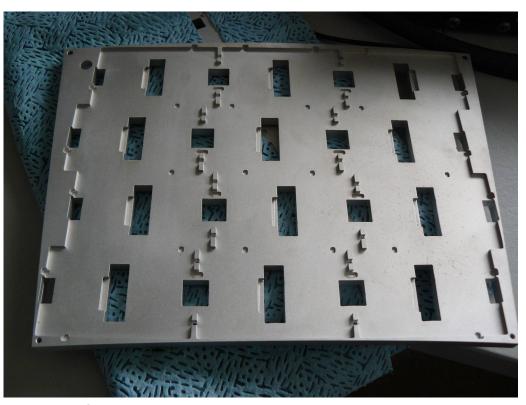
Low voltage power boards

Grid, anode HV



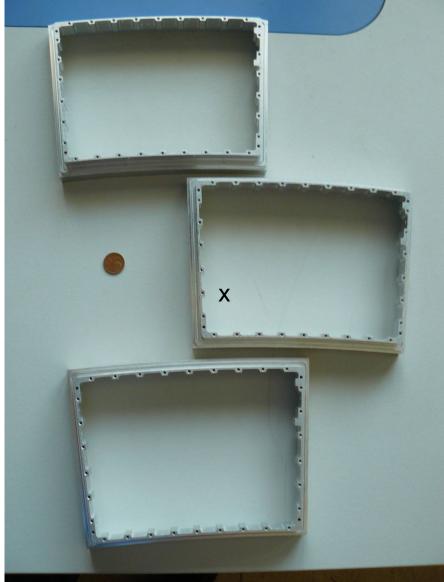




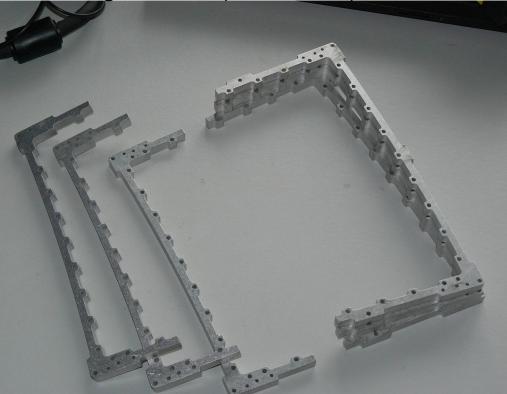


Carrier mechanics including cooling





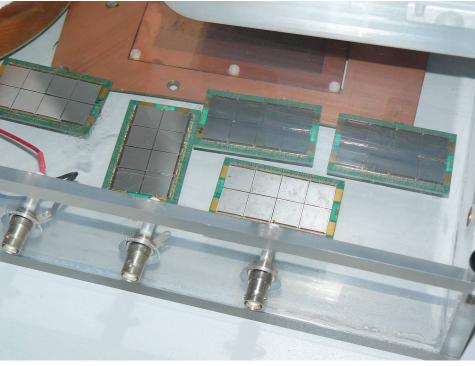








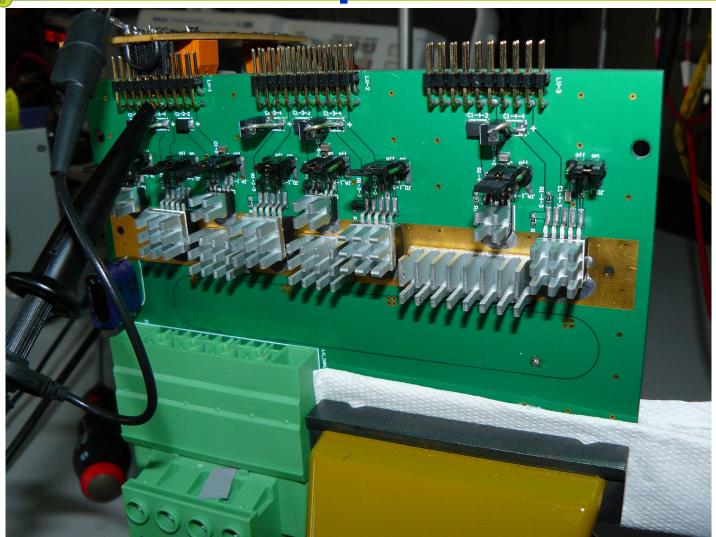




Octoboars in clean room

Octoboars waiting for assembley





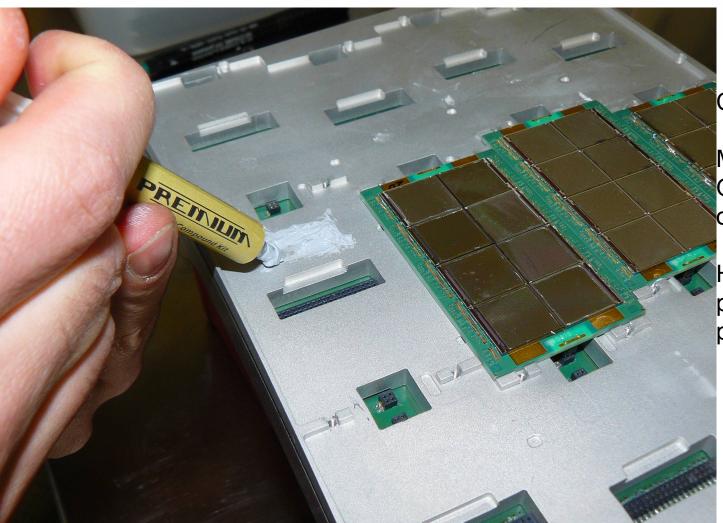


Low voltage power boards for Timepix chips:

- connector to
   Intermediate board
- capacitors
- LDOs
- connector to thick cables





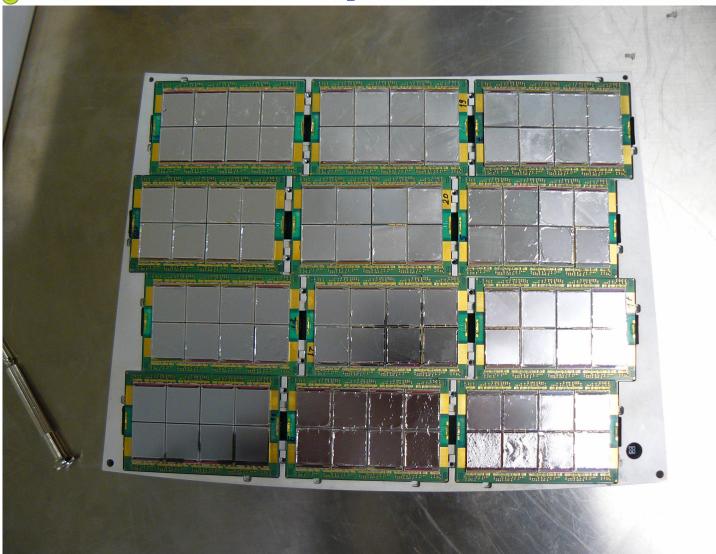


Clean room work:

Mounting of Octoboards on central module

Heat-conductive paste to cooling plate



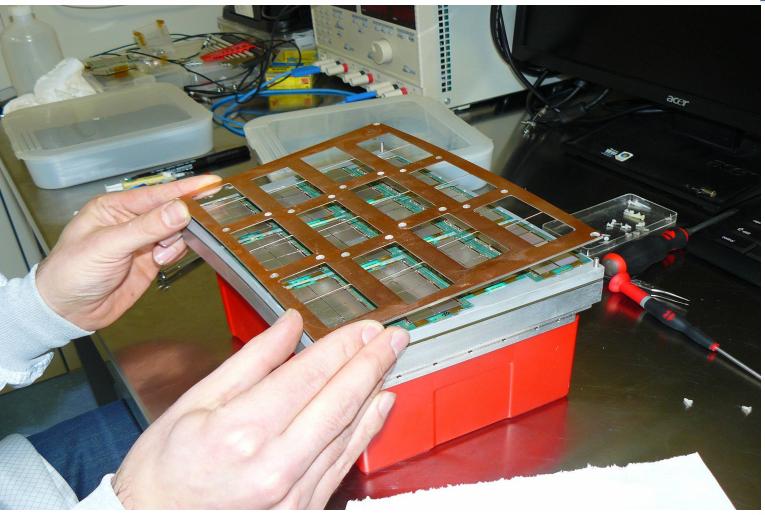




Clean room work:

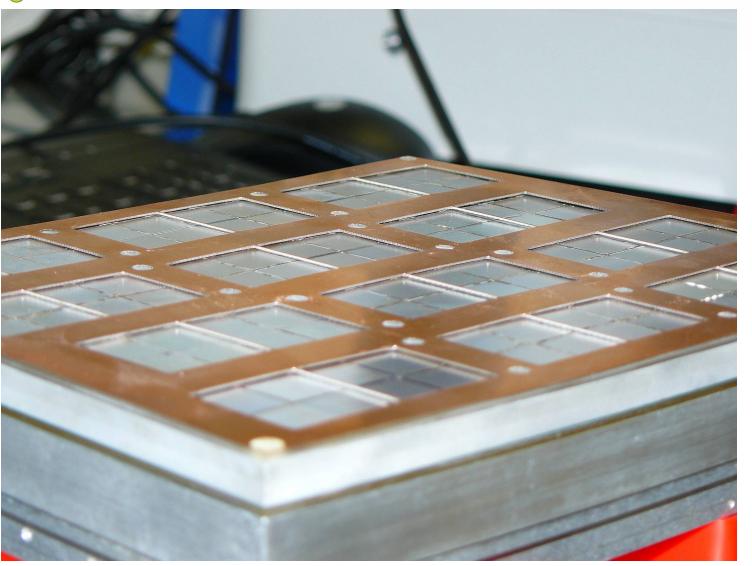
Mounting of Central module with all ocotboards







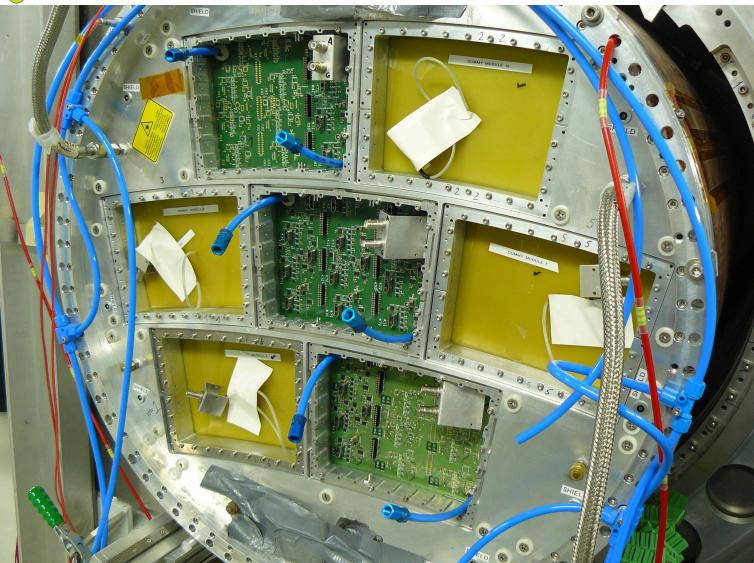






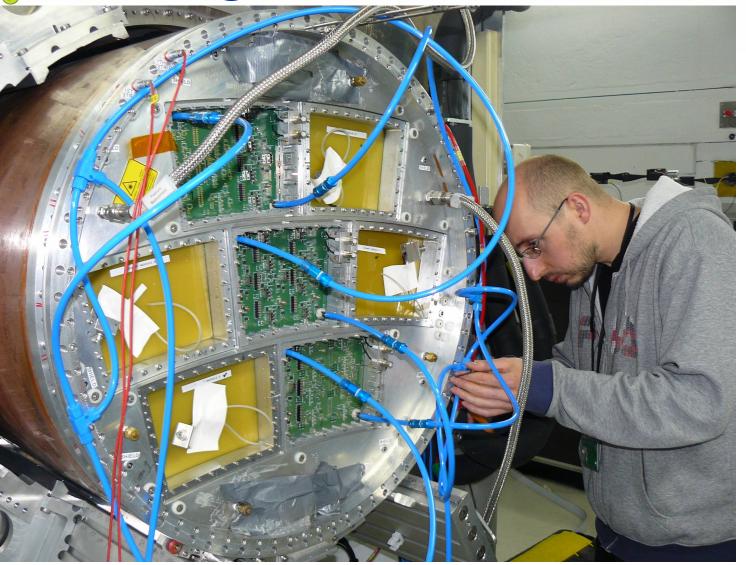




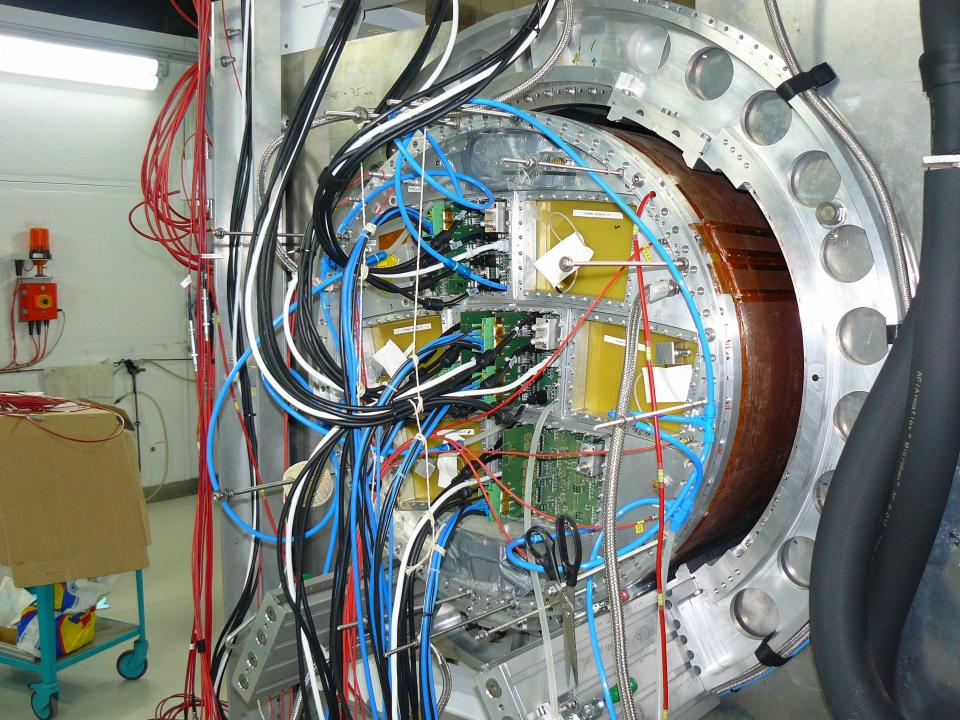












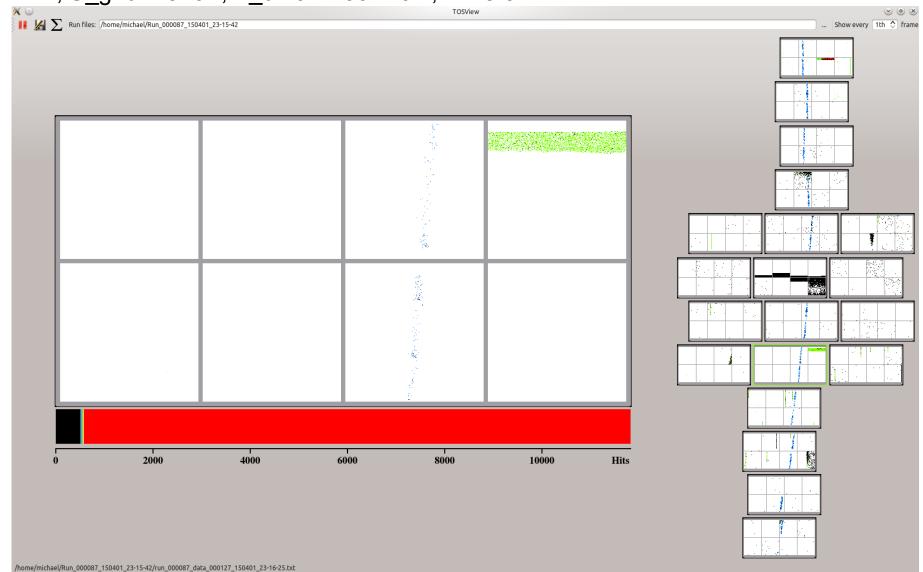






Event display image (not aligned) from a run with: B= 1T, U\_grid = 340V, E\_drift = 230 V/cm,  $z \approx 5$  cm





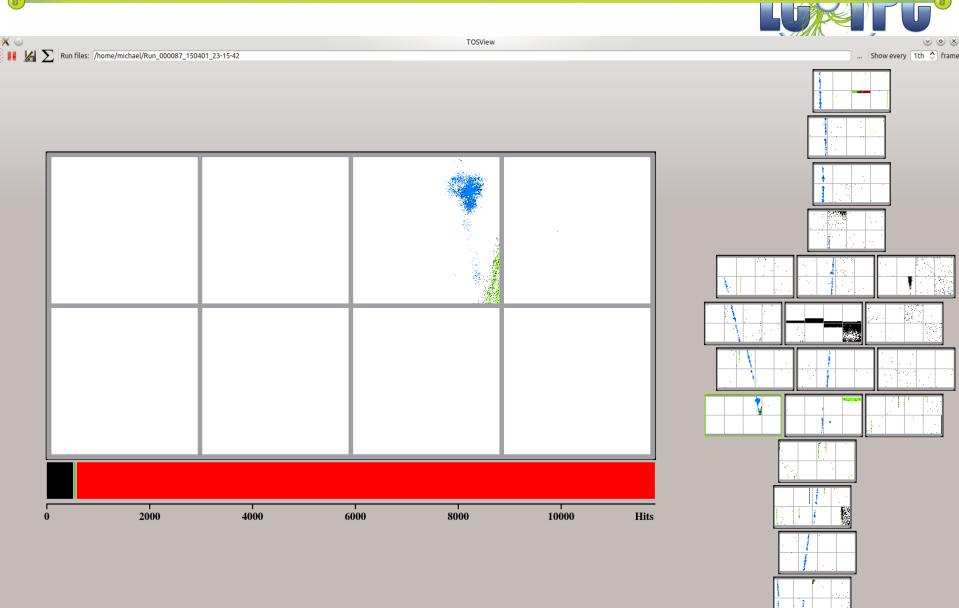


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