Asian Module R&D
Status & Plan

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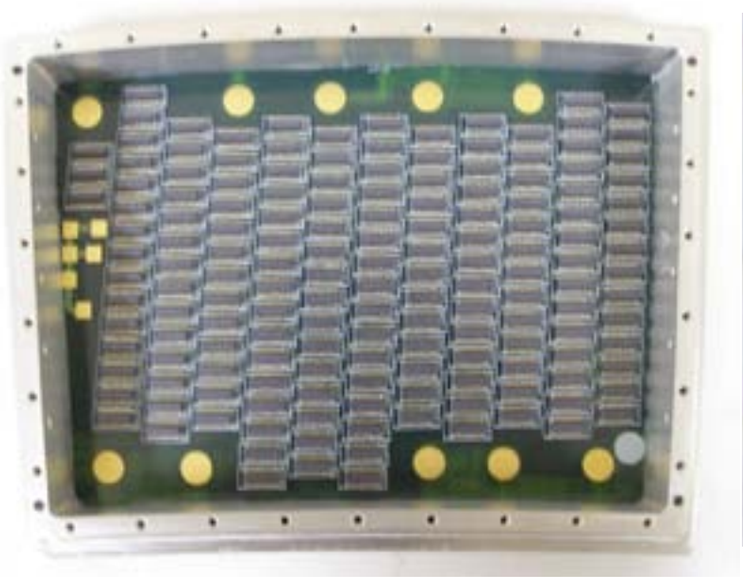
on behalf of LCTPC-Asia/Japan

Conceptual design of our module

Minimize insensitive regions(module boundary, GEM frame)

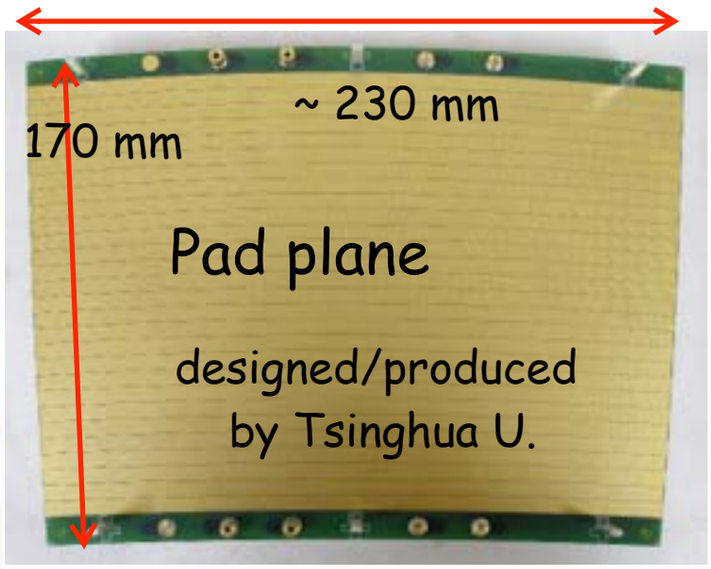
pointing IP

no side frame



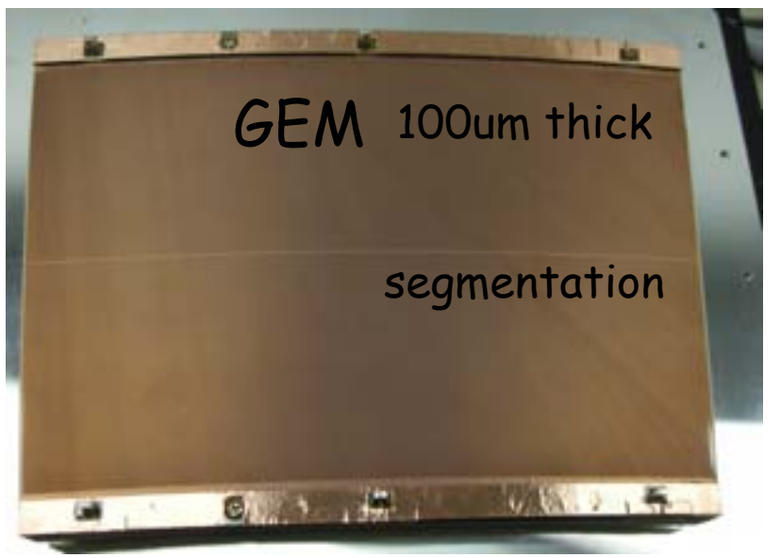
Bunch of tiny connectors
(40 pins) 161 connectors

all other space for HV supply
+ Back Frame



28 pad raws (176/192 pads/raw)
~1.2(w) x 5.4(h) mm^2
staggered every each layer

Total 5,152 ch/module



Double GEM (100um thick)
for simpler structure

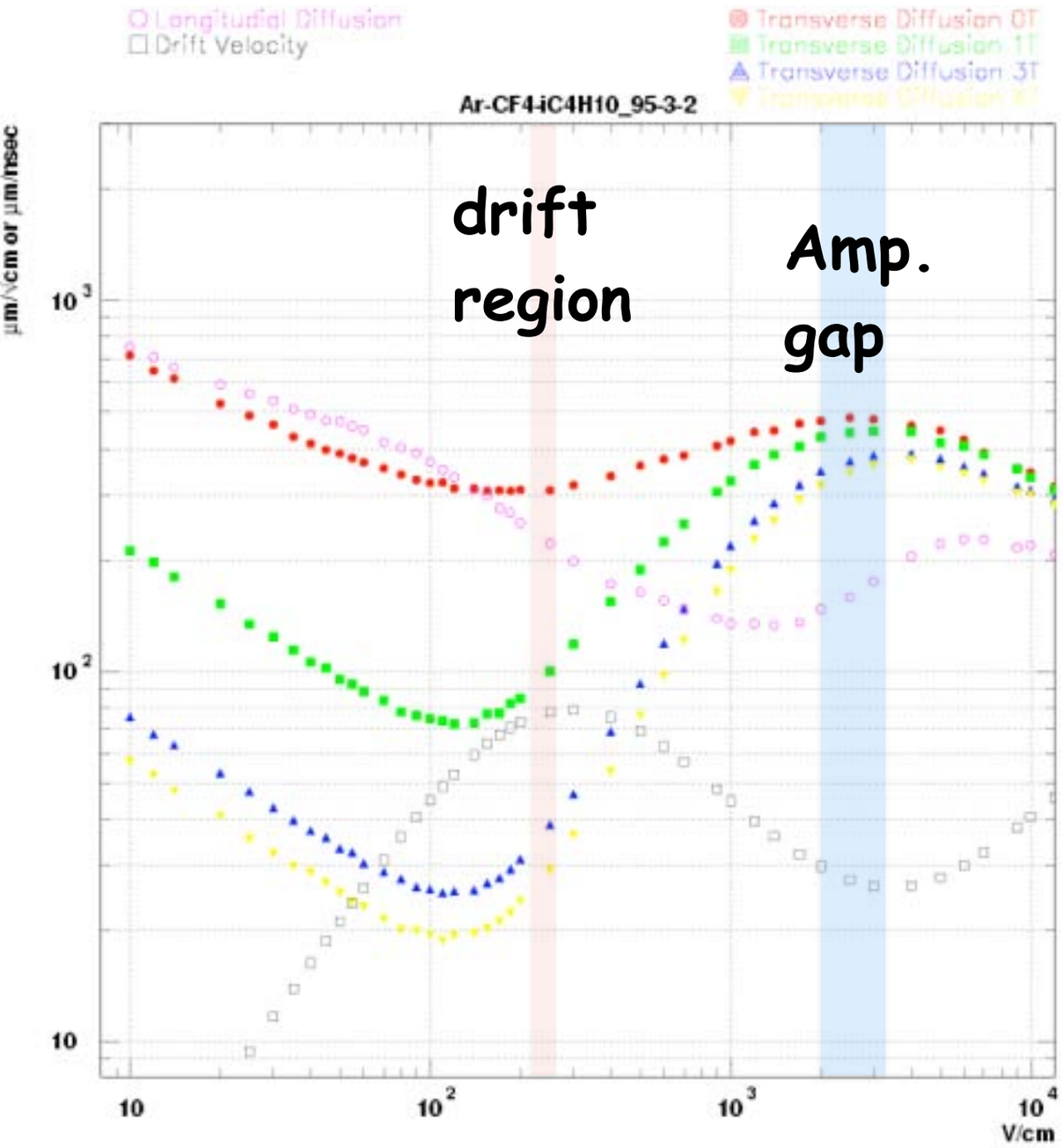
GEM electrode is divided in the middle of R

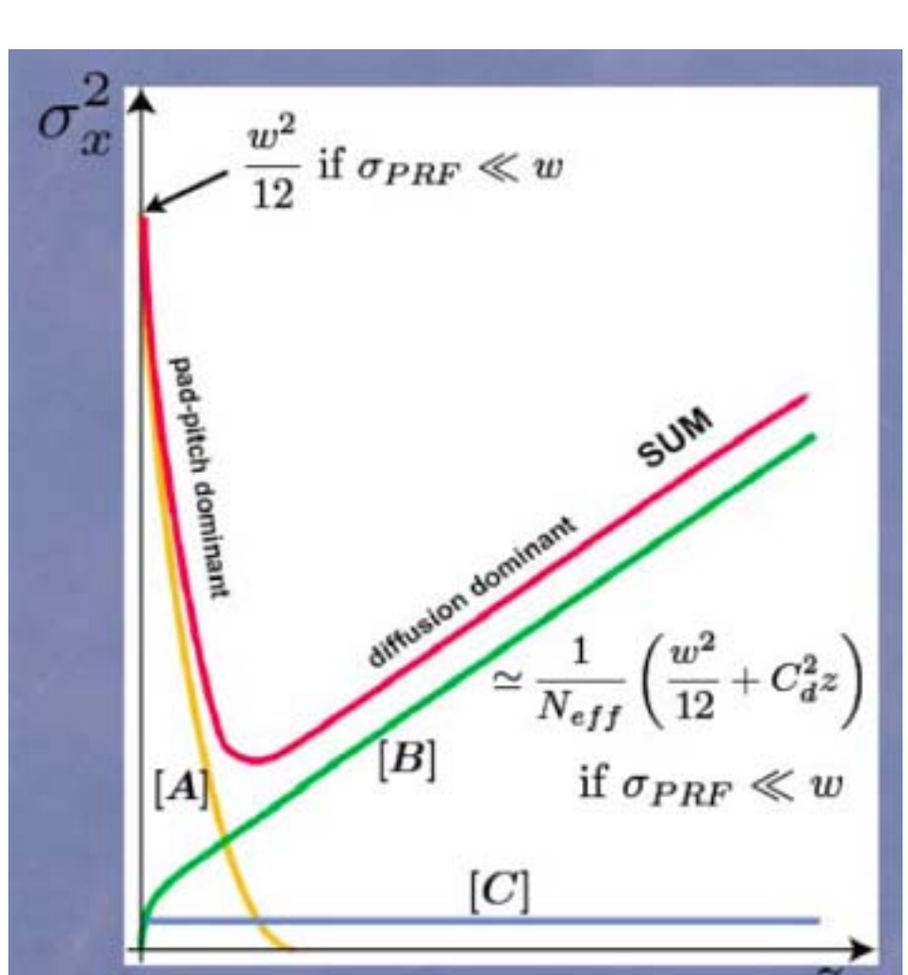
Gate GEM is assumed above GEM structure

Pad size

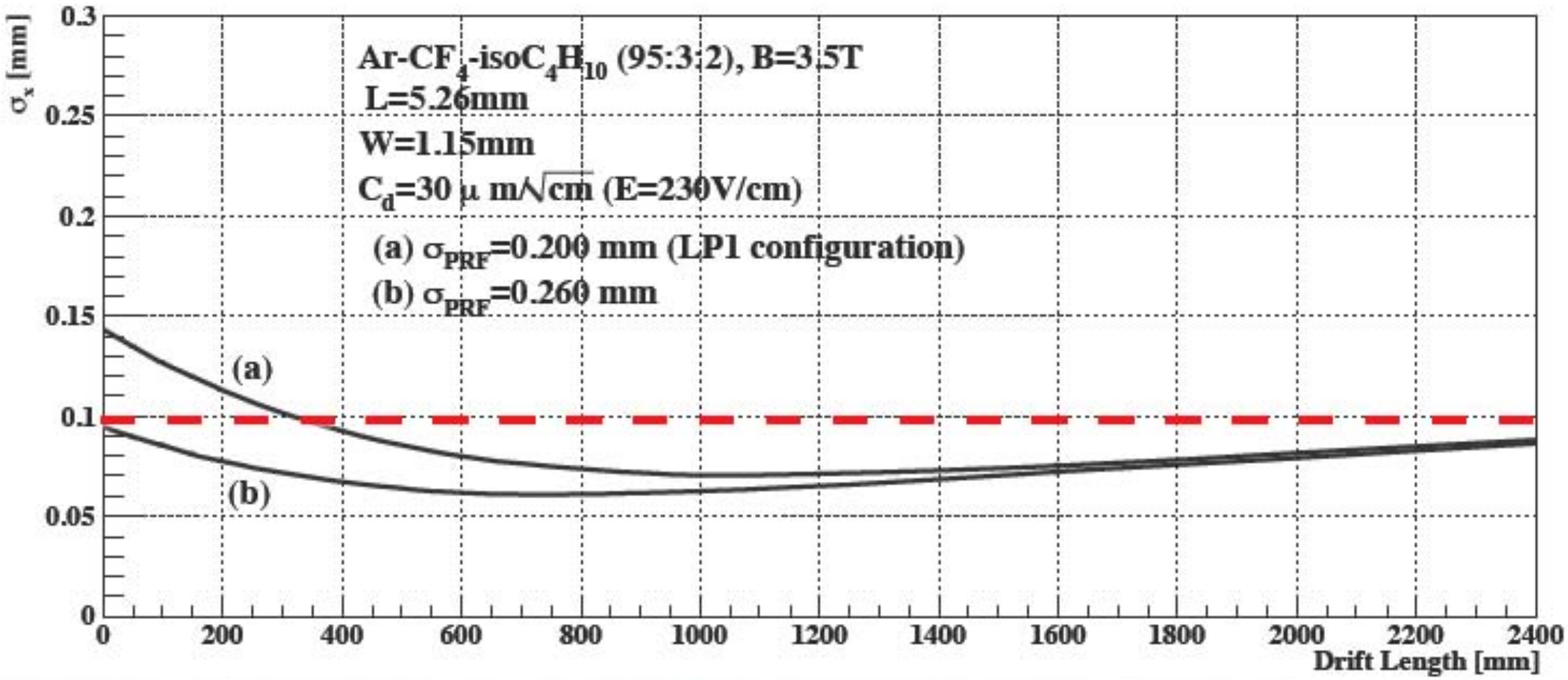
We have a reason to choose 1mm pad width for GEM

Optimum pad width is 3~4 times of diffusion @ amp. region(PRF)
in order to avoid hode scope effect





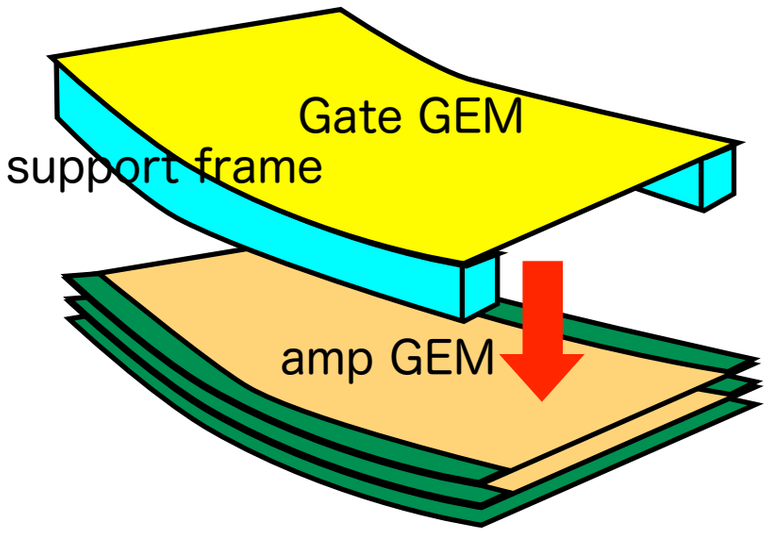
Extrapolation to the ILD-TPC

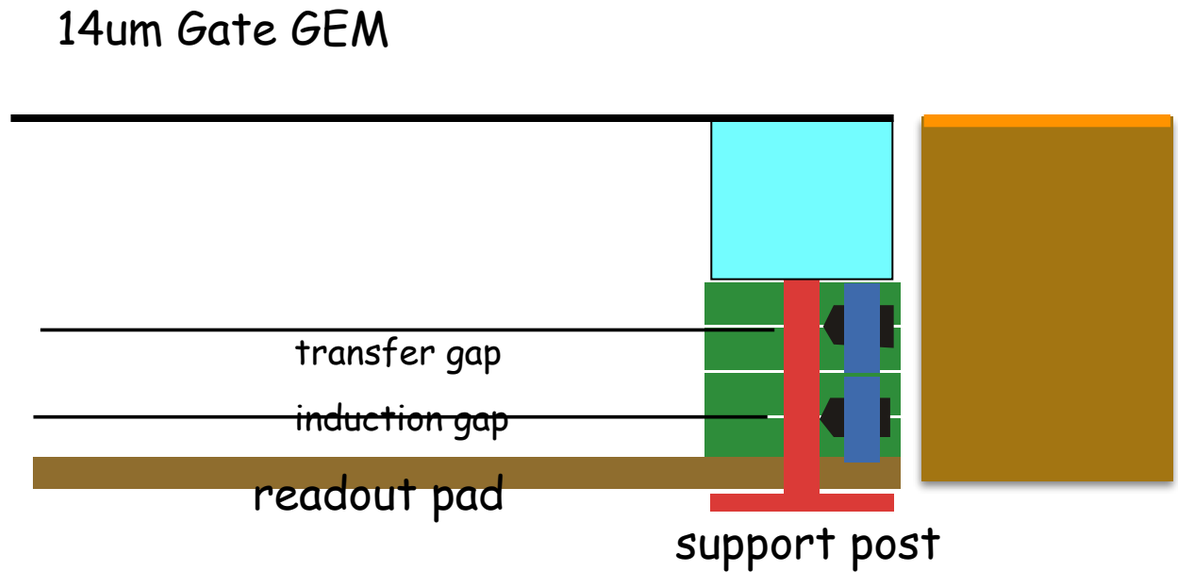


The expect perfo
satisfied with th

In order to achieve 100um res. all over the drift volume,
we have to have more diff.@amp region or narrower pad

GEM stretching method





tension of GEM is applied against post

post metal

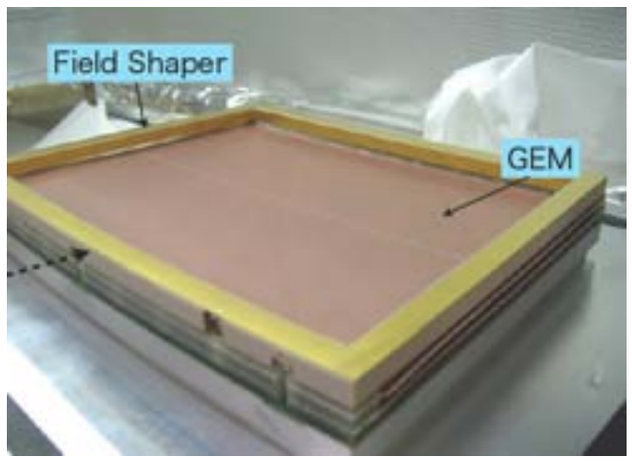
too much room for adjustment

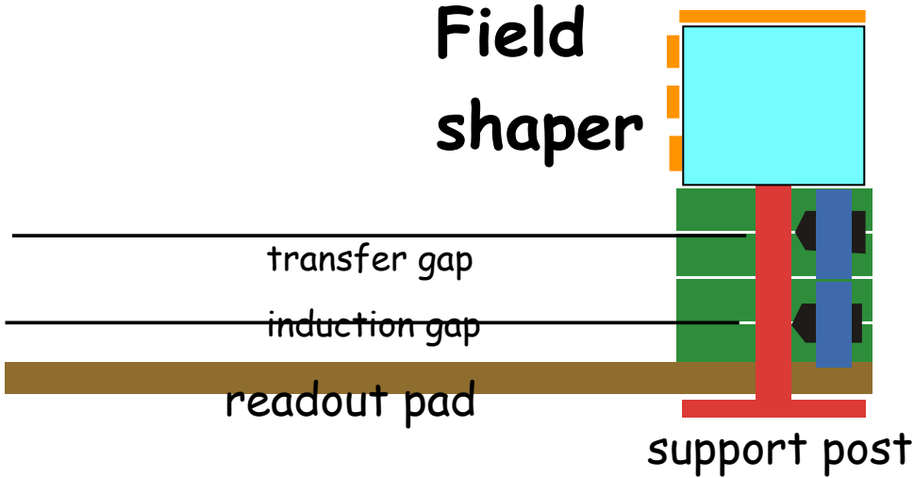
difficult to align GEM on the place

Gate GEM was not ready at the beginning

ugly structure(metal post, frame) distort E field

with side frame





GEM sheet

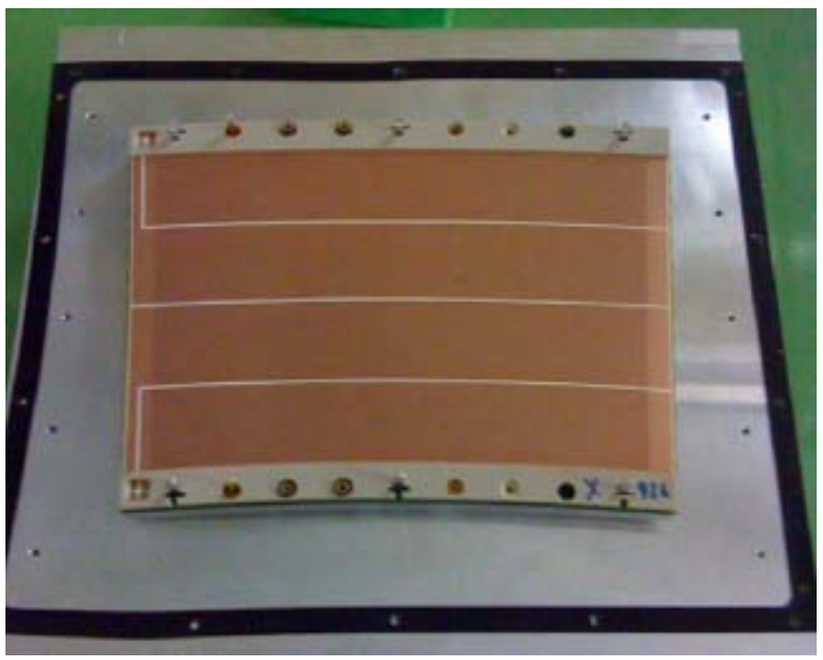
segmentation 2

-> observe frequent trip

gap 300um

-> gap was too short

one segment trip -> discharge@gap



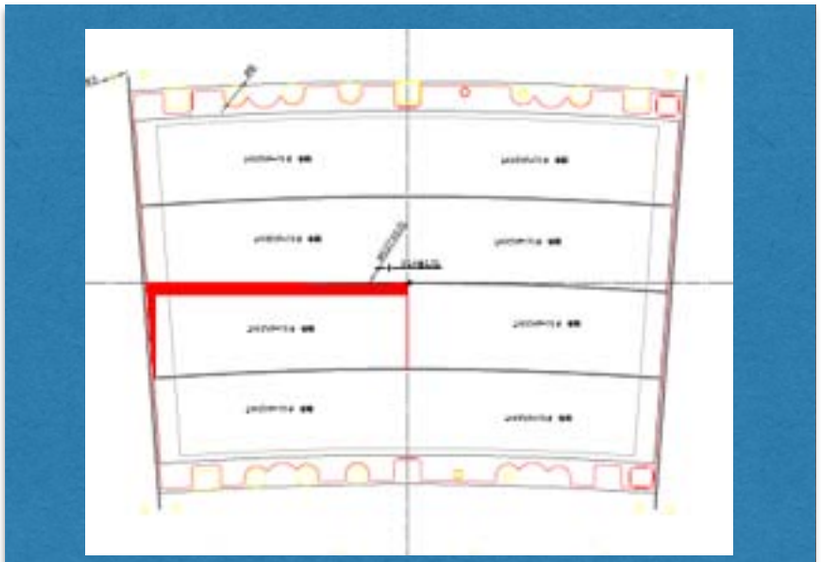
segmentation 4

-> improve? but many discharge

gap 1mm

-> HV OK but

-> this gap provide another distortion



no segmentation@front/ 4 segments@back

-> distortion became smaller

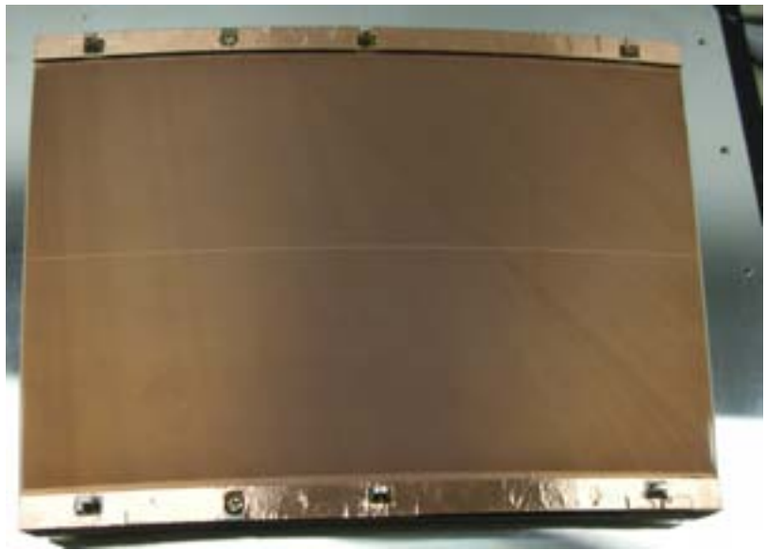
gap 500um

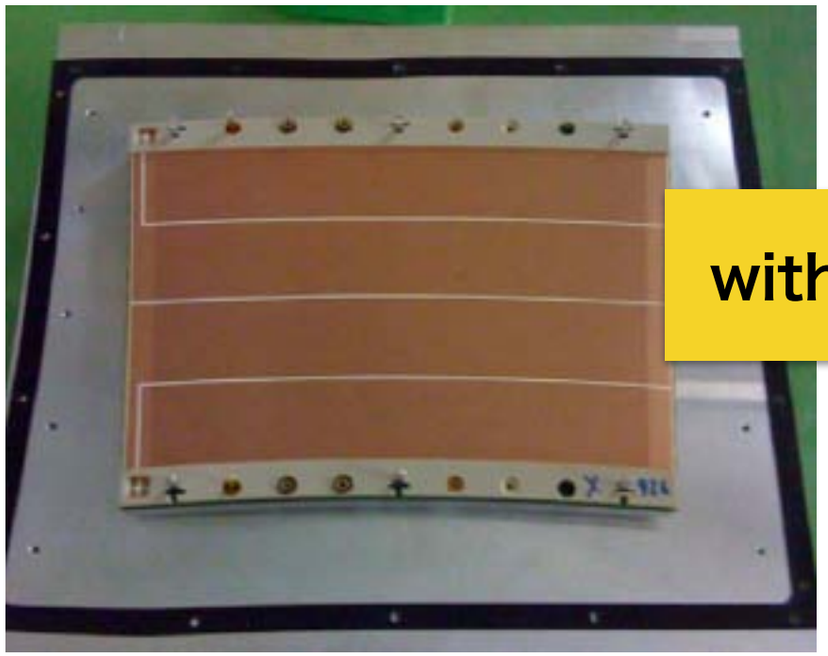
GEM sheet

se

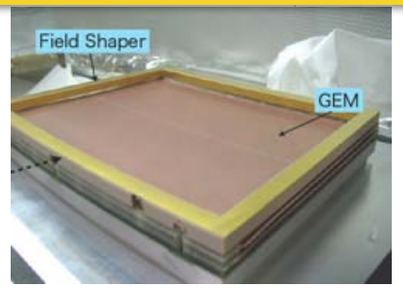
gc

seg





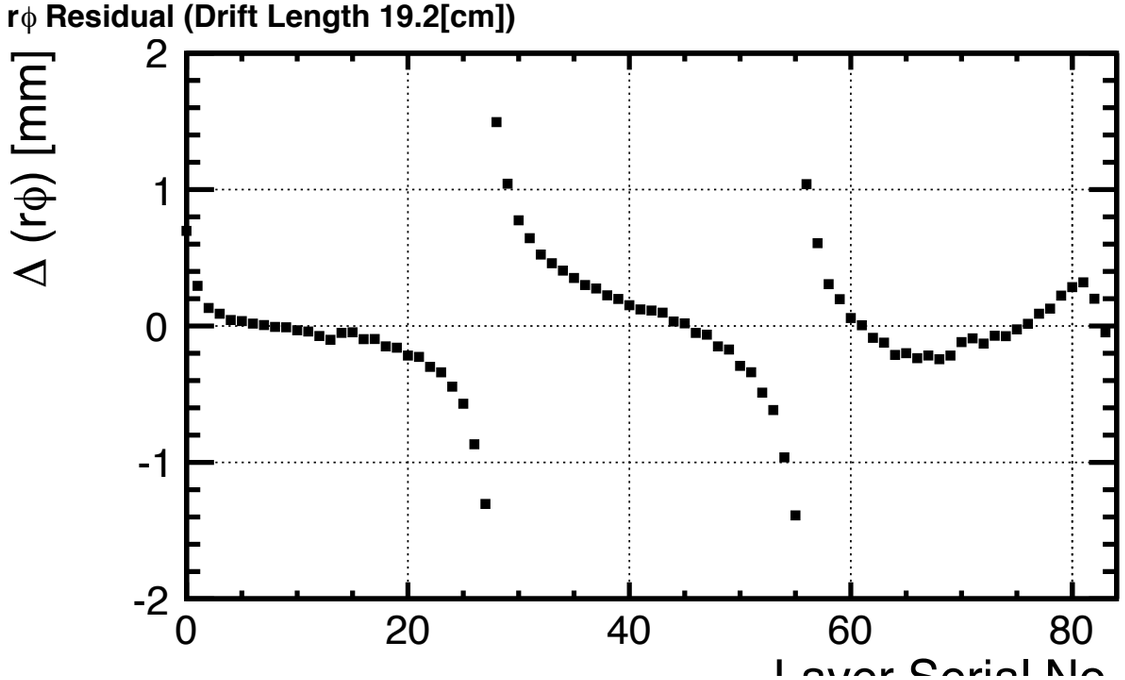
with field shaper

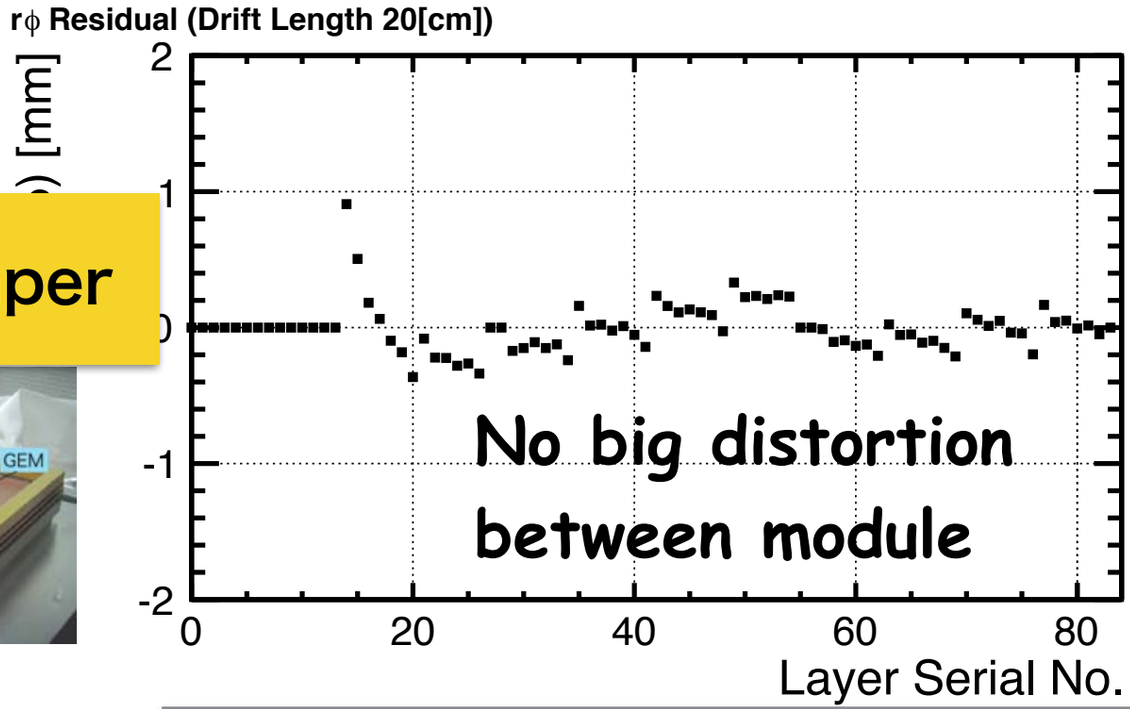


no segmen

-> dist

gap 500um





No Beam test

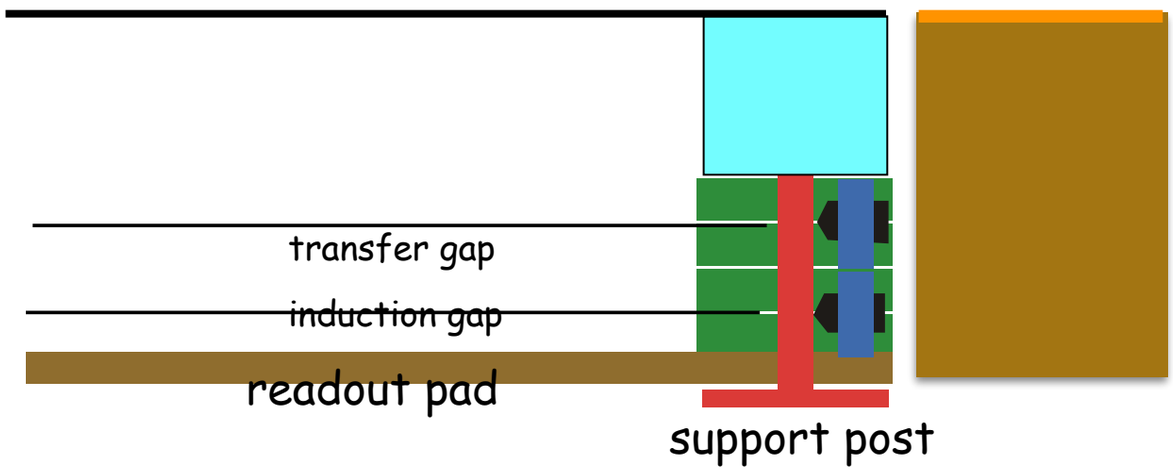
GEM discharge study

Micro discharge is counted during long term GEM operation
for 50um(CERN,Raytech, Scienergy) and 100um(Scienergy) GEM
Result will be reported by Kato

no clear difference

Gate will be ready until Fall 2015

We can test the original configuration
Gate effect with beam track
transmission, distortion
distortion in module
distortion between modules



this module will be studied using Laser beam this year
No clear plan for DESY test beam (budget,,,)

NEXT module

Upper structure

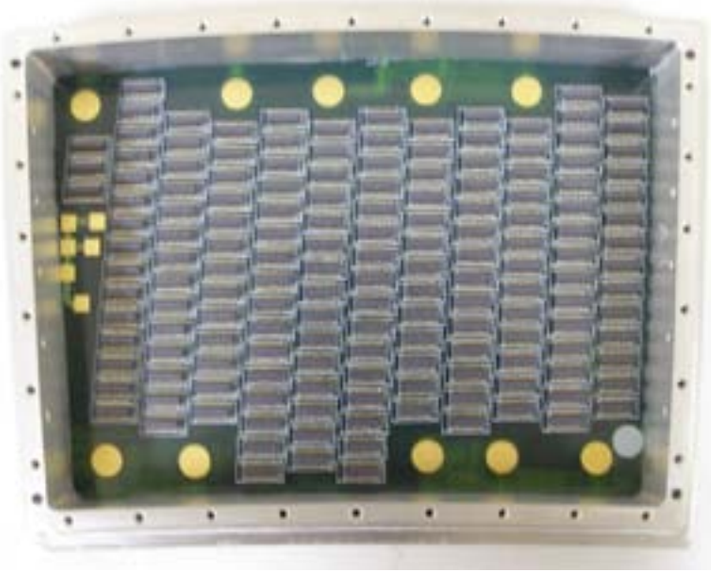
Gate GEM
GEM Amplification

how do we mount ?

PCB

Readable channel is 60% of LP1

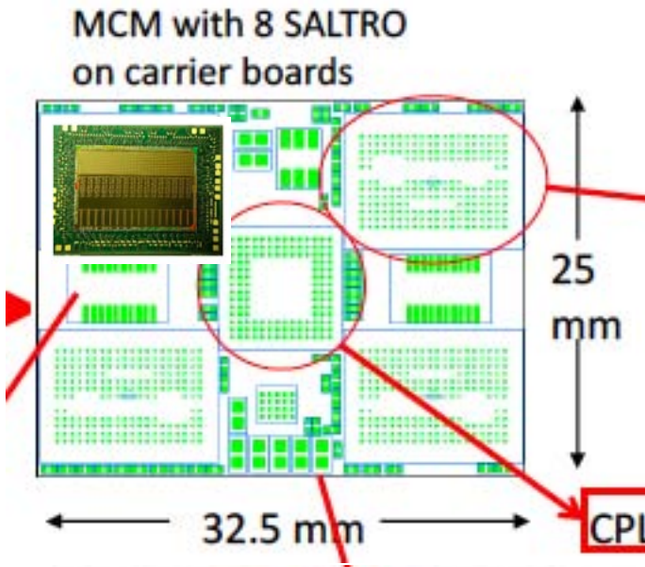
how do we read ?

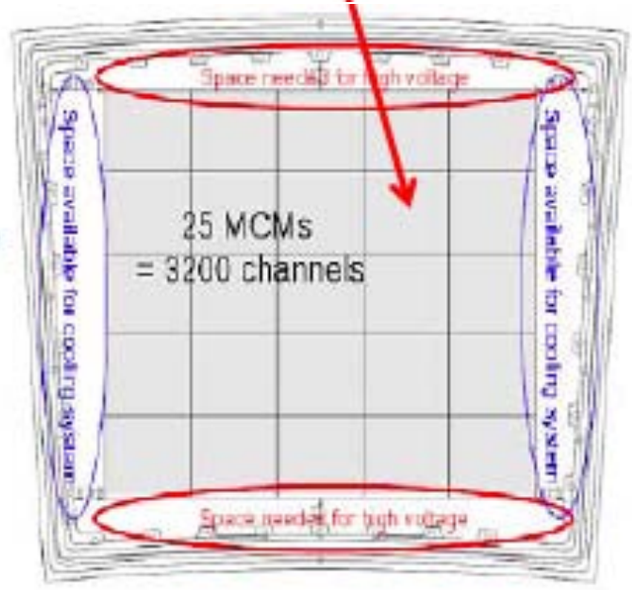


Lower structure

RO electronics/cooling/HV

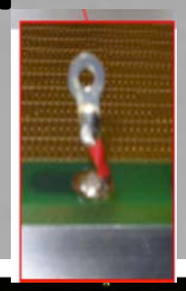
how do we cool ?

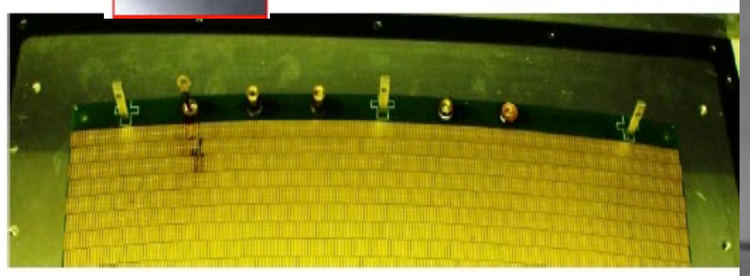




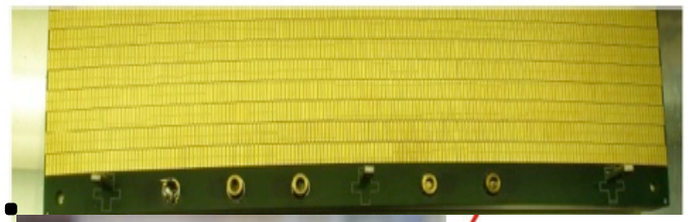
Upper structure

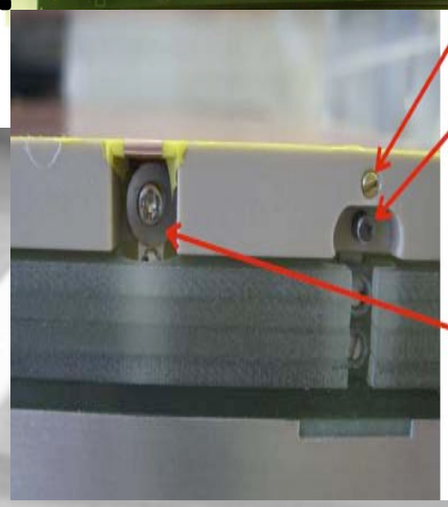
Different scheme is tested





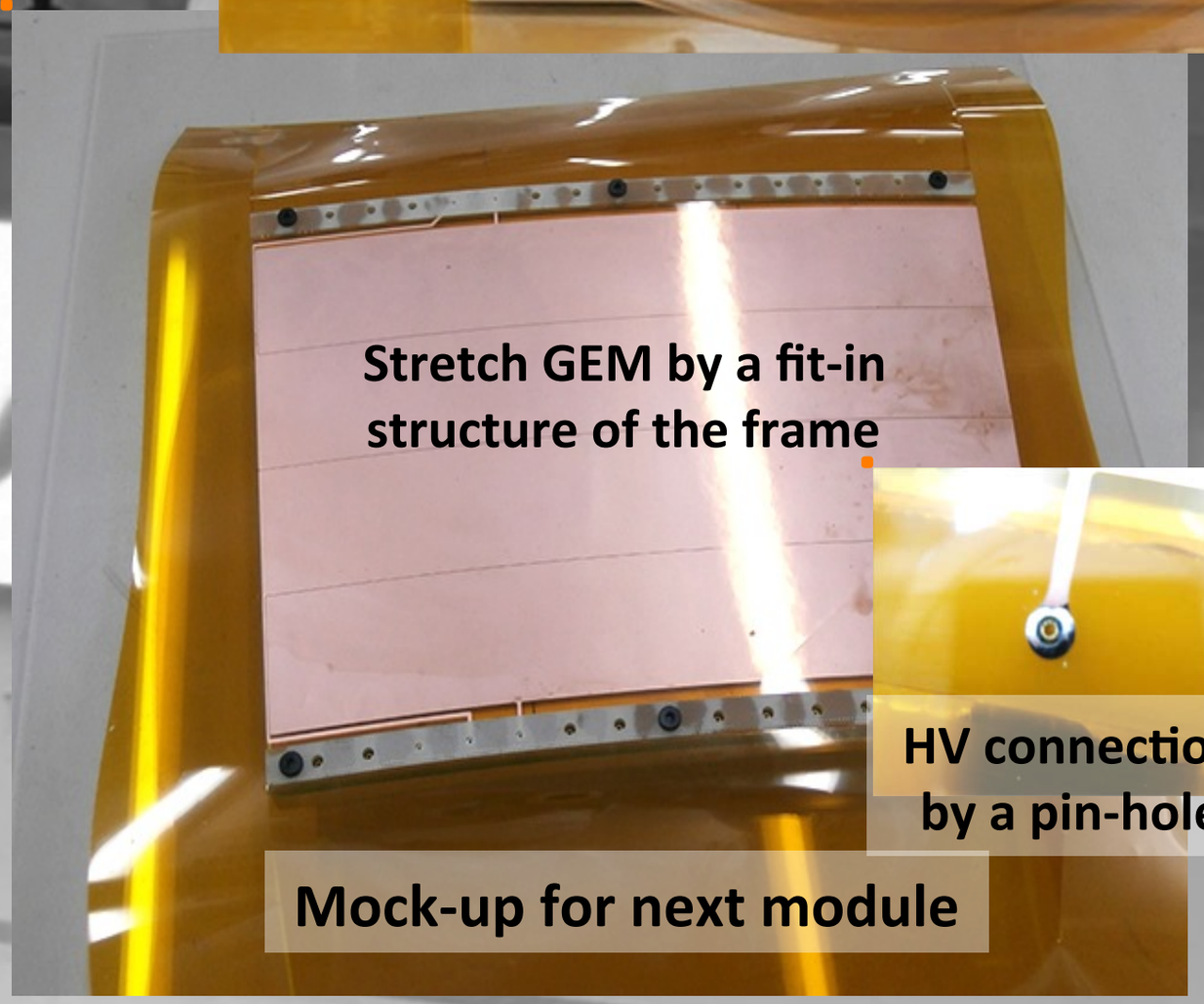
The top side of the pad plane





Current module

Gem flatness ≤ 100 microns (measured)



Stretch GEM by a fit-in structure of the frame

HV connection by a pin-hole

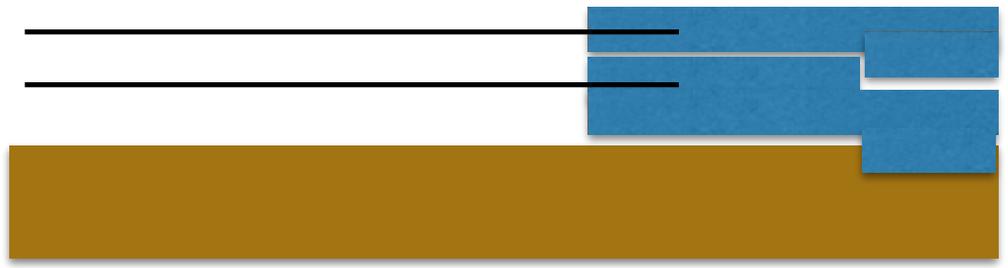
Mock-up for next module

Upper structure

Fit-in structure

no room for adjustment

elasticity of GEM sheet



HV connection

pin and receptacle

Mockup is just delivered

We will check fabrication process / stability / replacability

HV connection stability….

amp. GEM structure 2 GEM or 3 GEM

we couldn't establish advantage of 2 GEM (simpler ?)

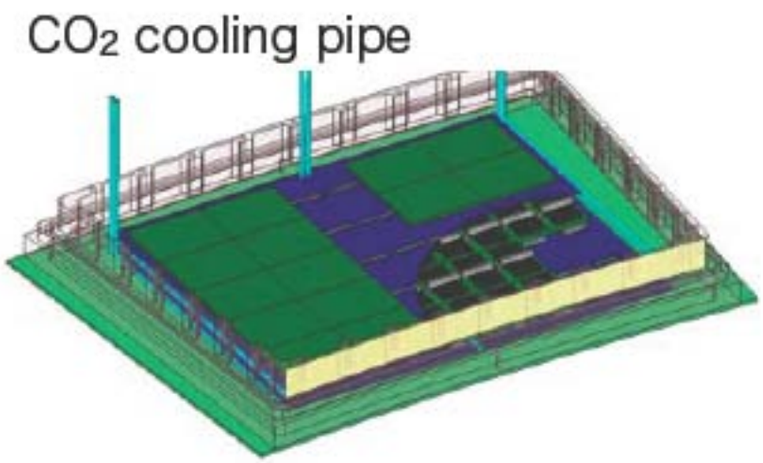
How do we get more diffusion ? if we choose 1mm pad pitch

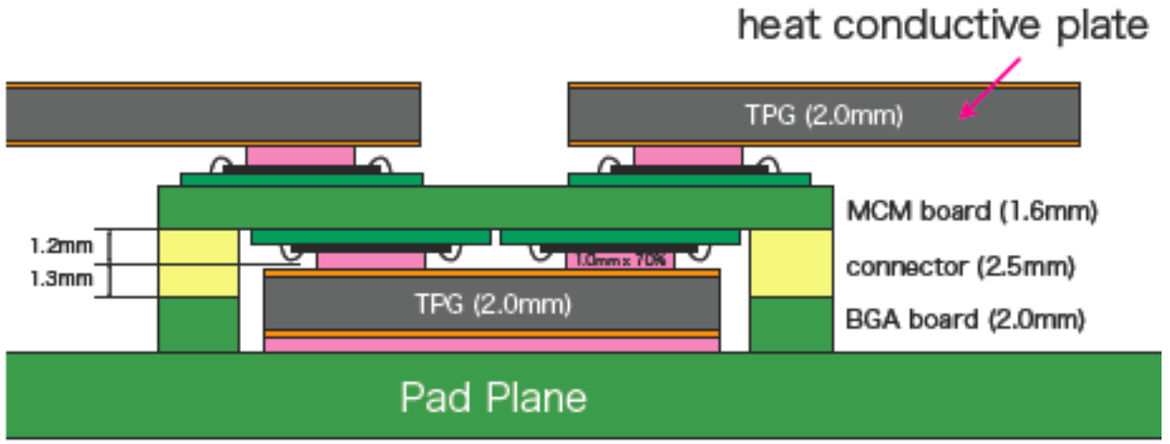
1cm Amp. region is acceptable ?

-> total 2cm thick structure above PCB ????

Lower structure

Readout electronics (Leif)





Cooling scheme is studied by Takahiro

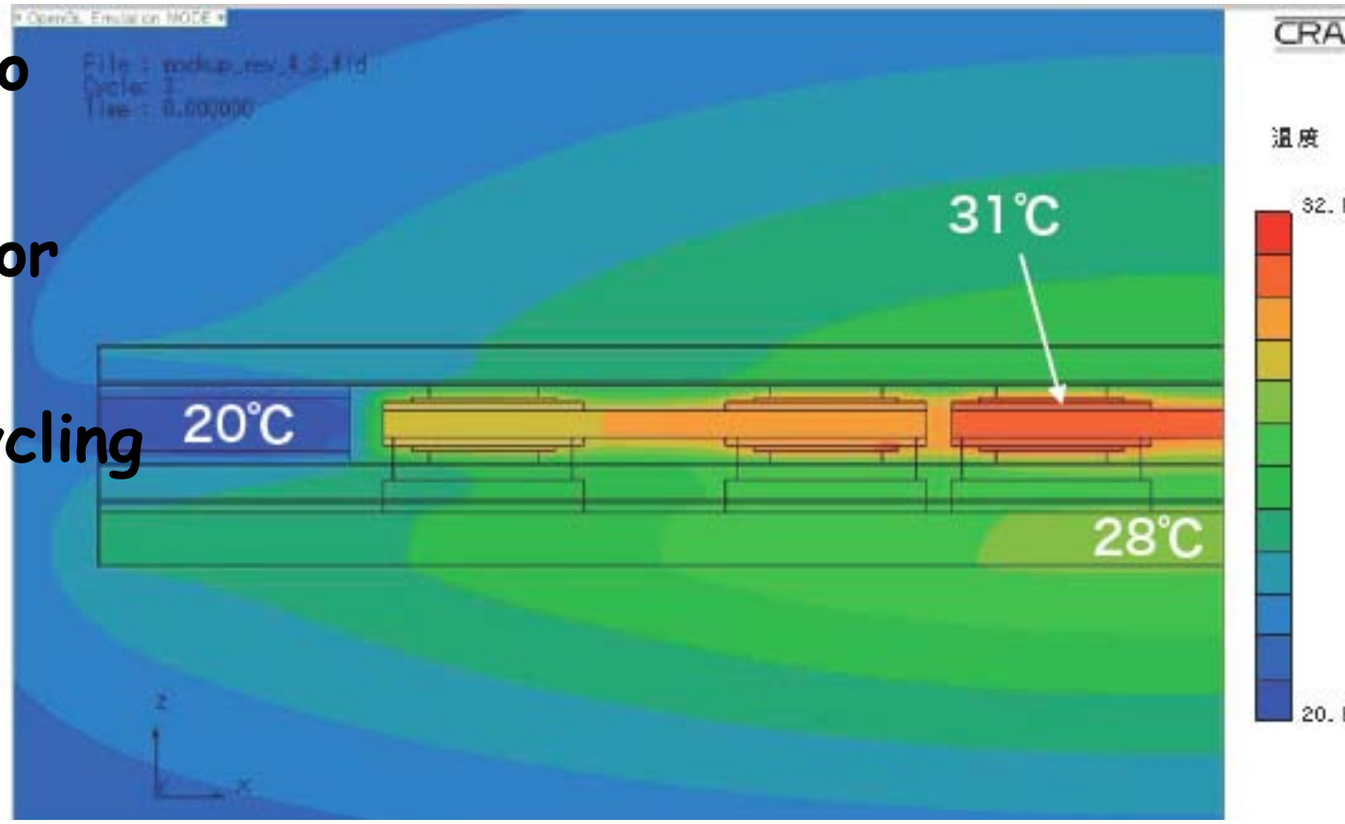
simulation using TPG as heat conductor

non-negligible temp. gradient

w/o power cycling

heat flow through connector

Mockup study will be started



design of PCB toward next module

Not considered yet under 3200ch readout environment

It depends on how we set the goal of Next module

pad size is be kept and sensitive area is reduced

same width but 50% longer height and cover all area

20% larger pad in width&height cover all area

design of PCB is related to upper/lower structure

Upper structure must be considered through mockup study

Cooling scheme is also studied more

We may need at least 1 year to study these.

How do we fit into Common PCB plan ?

Unfortunately our budget of 2015 is very limited

What we can @2015 is

production of realistic GEM gate fit on the current module

test this module with laser facility

mockup study of upper structure

mockup study of cooling system

Summary

We have met real problems of module and learned many things

distortion related local module structure

GEM electrode gap : predictable and correctable

need more study for ExB effect

module gap : list. reduced by proper Field shaper op.

module gap distortion is correctable or not?

We still need to show advantage of our concept

minimize boundary effect

Test of new upper structure is on going.

Cooling is also considered using another mockup

These results will be integrated into next module design