Development of readout electronics for a TPC

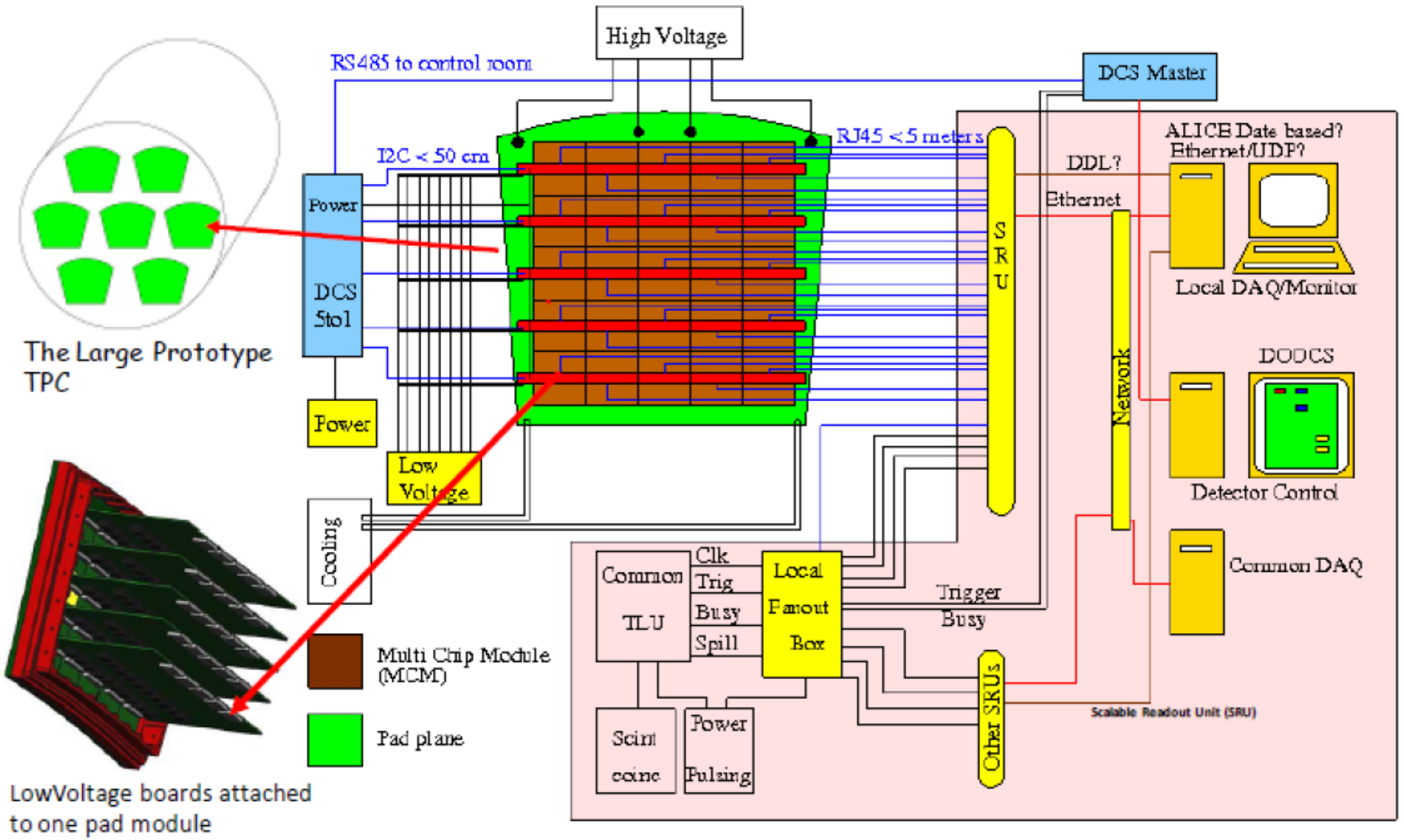
Status 22.4.2015

Organization of the presentation:

Overview of the readout system
The good news:
- Boards for the final system that are ready and works
- Prototype boards for testing that are ready and works
- Boards under development

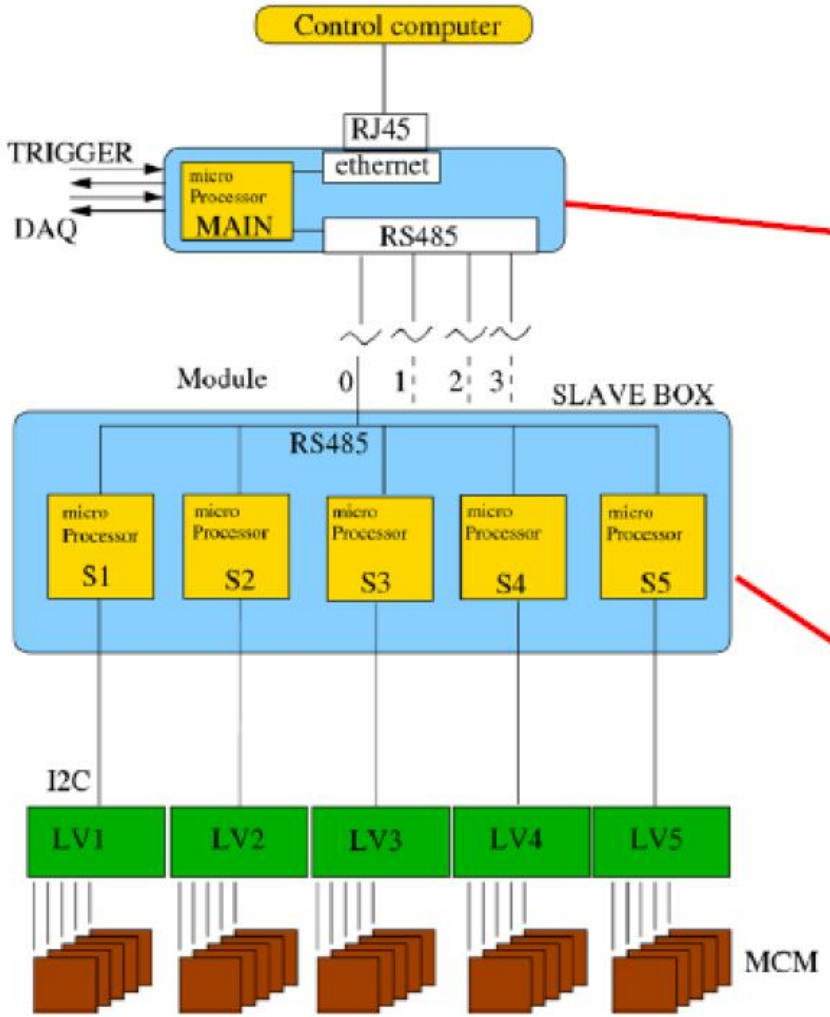
The less good news:
- The Carrier Board
- The finances

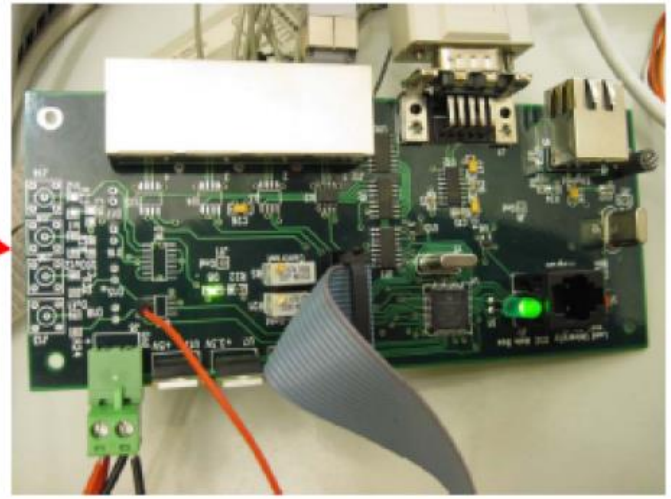
Overview of readout system

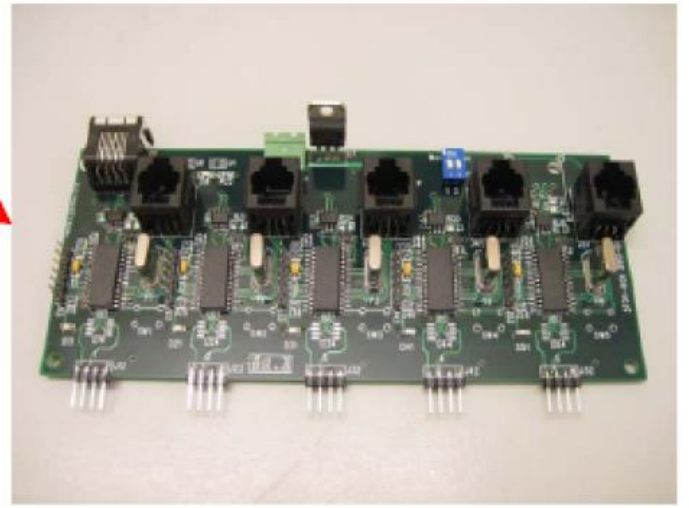


The Detector Control System

- Two types of boards have been constructed
- The master control board
- The slave module (5-1 board)
- Both are ready and succesfully tested
- Some 700 parameters will be monitored using DOOCS (Oliver Schäfer)
- The structure of the DOOCS firmware has been agreed upon







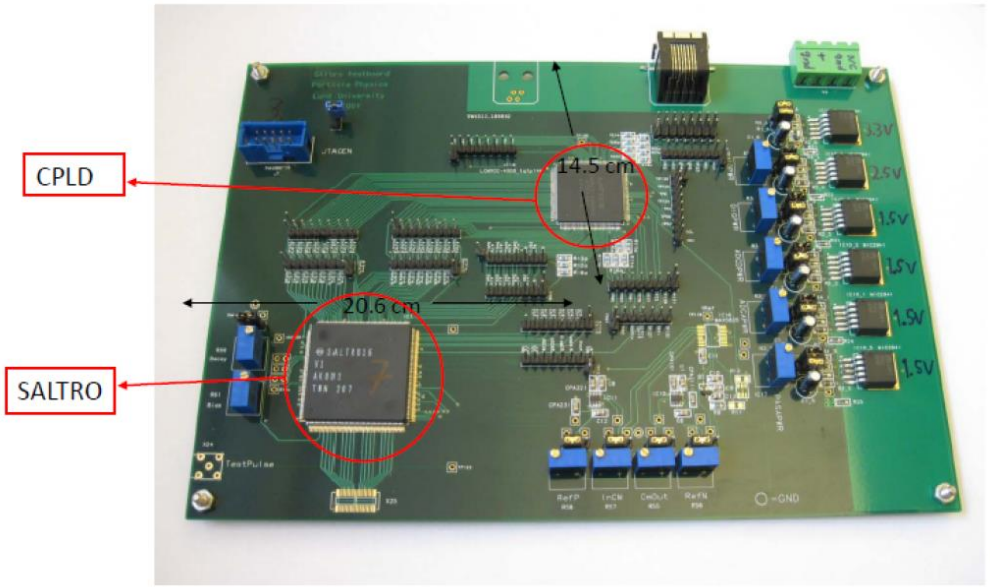
The MCM Development Board

- Stand alone board (size 210x 145 mm2) for one SALTRO in QFP package

- The board is used to develop the firmware of the MCM and the serial readout

- The firmware for the CPLD is being developed by Brussels and Wuhan

- Two possible ways for readout:
  - use ALICE DATE with the DDL optical link
  - direct readout using optical ethernet



- The first tests established the communication between the SALTRO-chip and the CPLD as well as with the SRU using the DDL optical link. The ethernet option will be used to avoid being dependent on the ALICE DDL libraries

- The direct communication between the SRU and the MCM-board requires modification of the FPGA firmware on the SRU. This is done by Wuhan (Fan is back to work after her parental leave).

- 3 boards have been produced for 3 identical readout system placed in Brussels, Wuhan and Lund

The Low Voltage Prototype Board

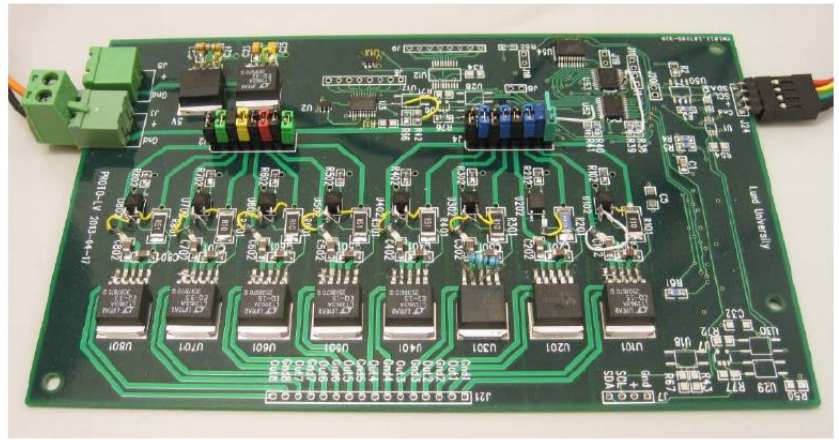
- The Low Voltage Prototype Board provides voltage for one MCM-board

- It is used to debug the desig on the final LV-board

- It provides voltage and some configuration parameters to the Test Set-Up

- The board is ready and has been used to verify the communication with:

    - the Test Socket Board
    - the Detector Control Boards



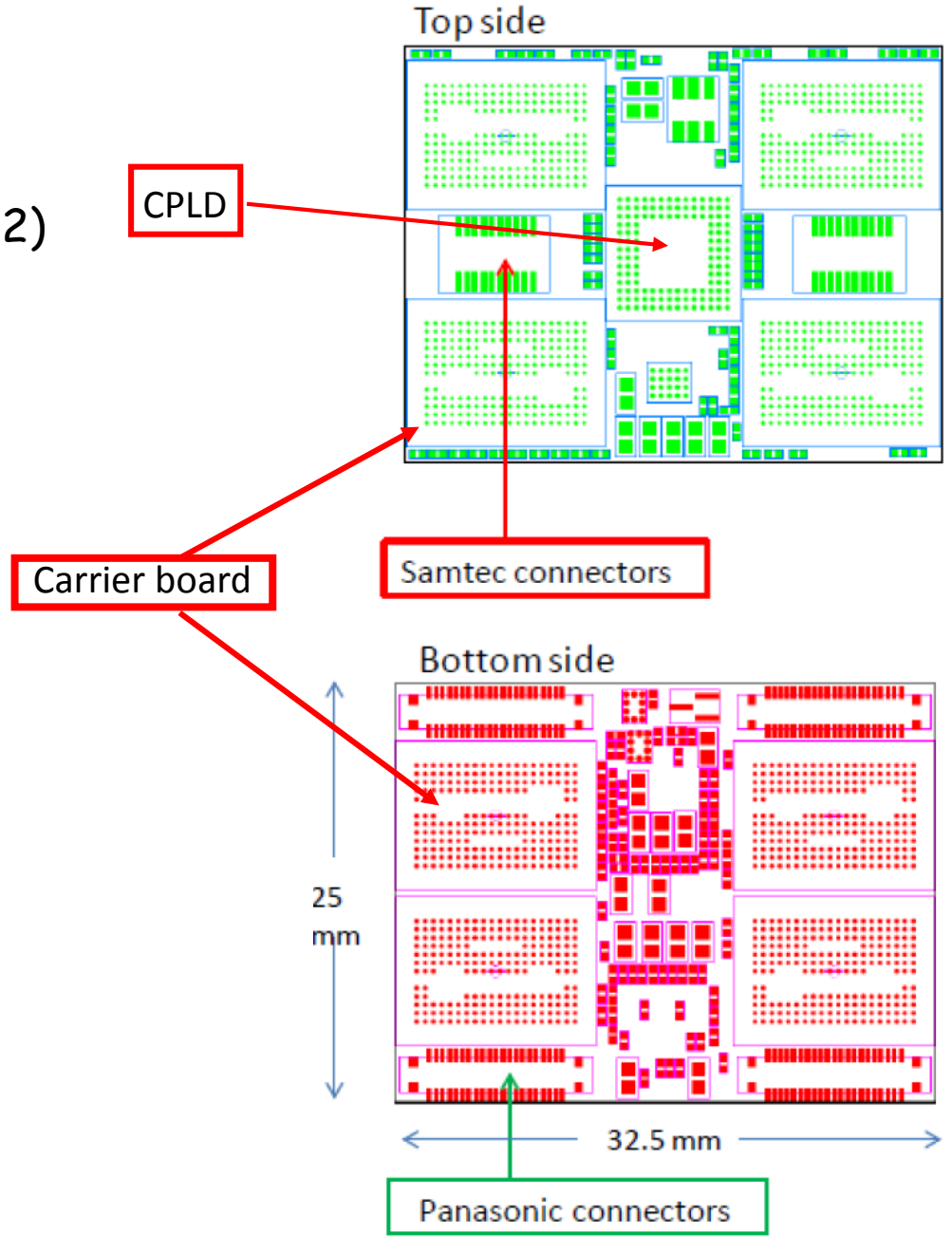
The Multi Chip Module

- 8 carrier board on each MCM-board (size 25x32.5 mm2) (4 on the top side and 4 on the bottom side), mounted by soldering of small tin balls on the back side of the carrier boards

- 1 CPLD (size 8x8 mm2), which provies communication between the DAQ and the individual channels

- 4 micro-connectors on the bottom side, in order to connect to the pad plane

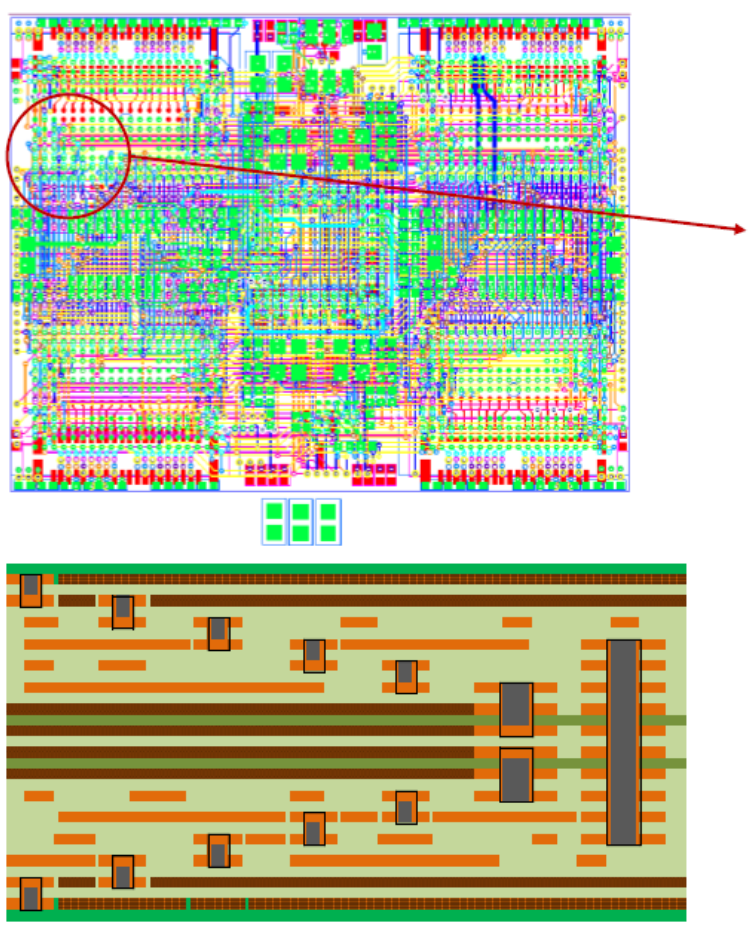
- 2 connectors on the top side for LV-supply and signal transport

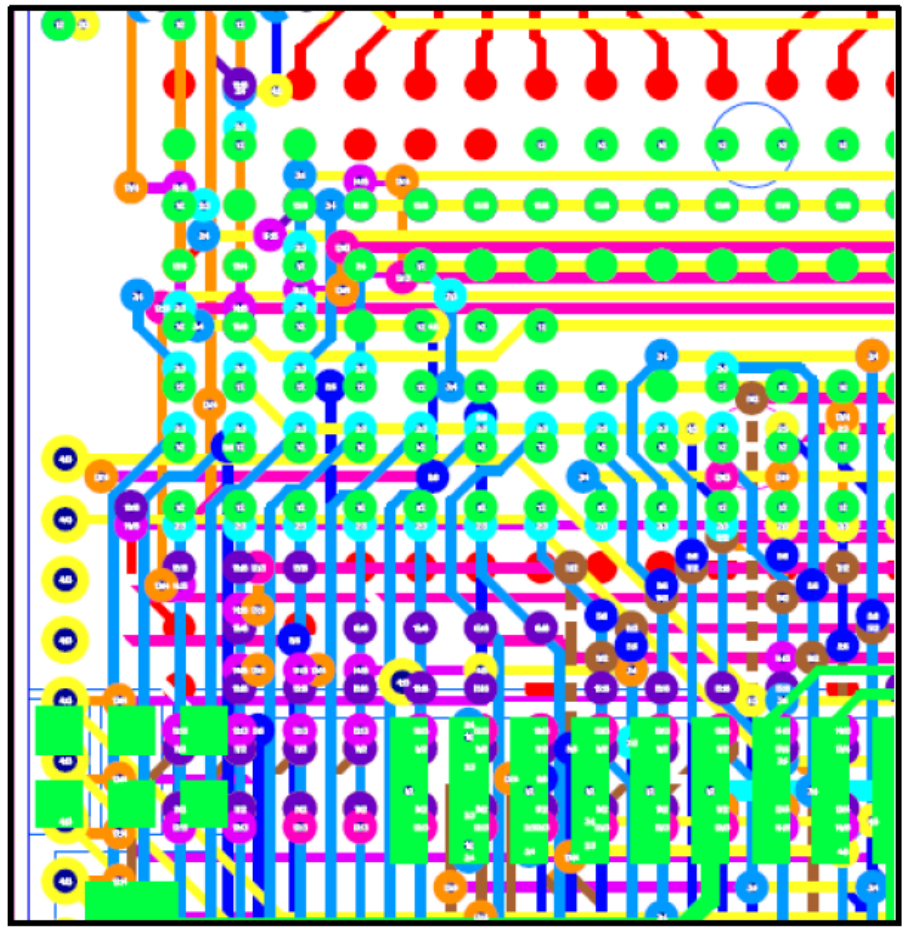


The Multi Chip Module (contd.)

The MCM-board is designed in High Density Interconnect (HDI) technology. This technology allows for higher routing density for both signal lines as for voltage supply

This leads to a reduction of the numer of layers
16 layers compared to > 20 in conventional PCB design





Ideas on cooling of MCM-boards in a module

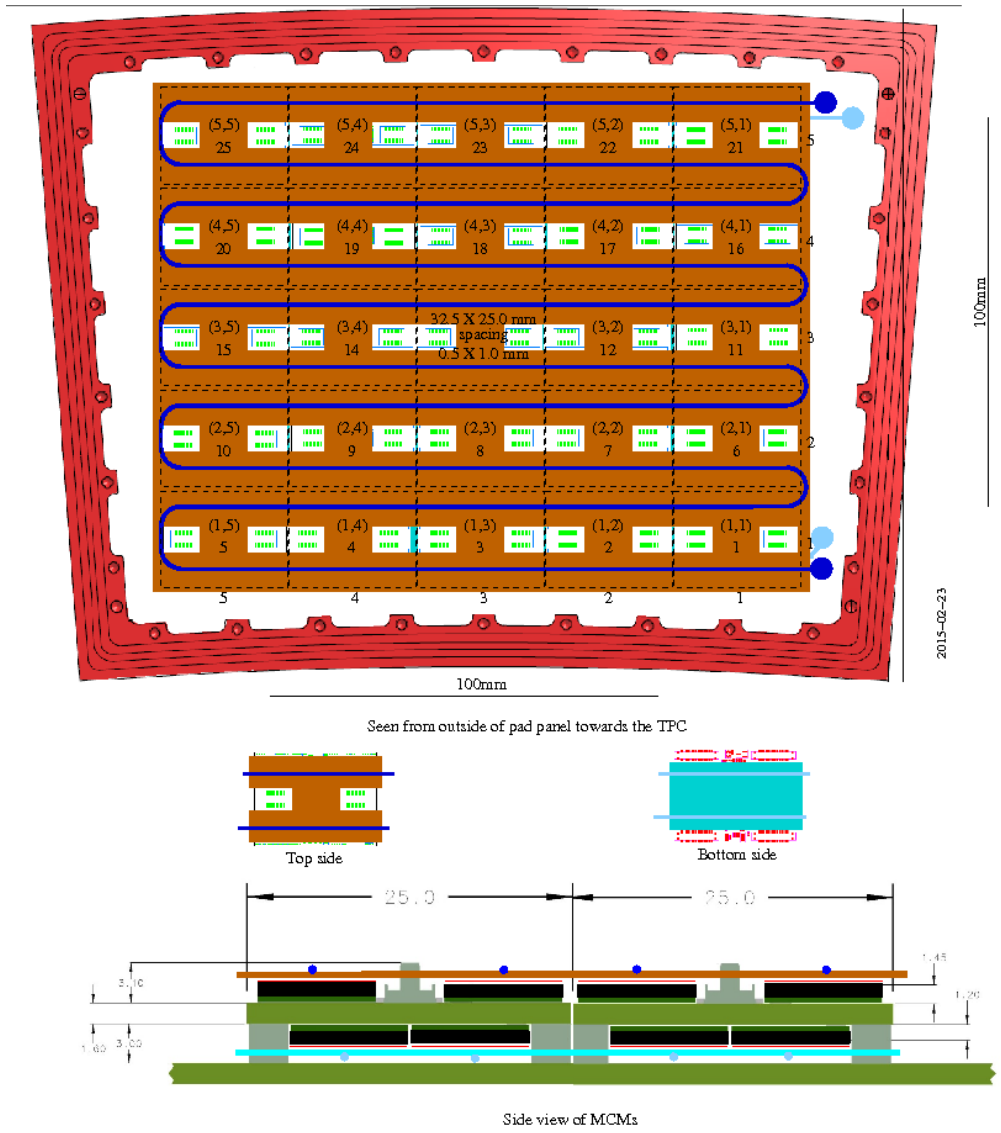
- Two thin plates of good thermal conductivity, with cut outs for the connectors, are placed on top and bottom, respectively, of the 5x5 matrix of MCM-boards.

- Cooling pipes are placed in grooves on the plates according to the picture and glued or soldered onto the plates.

- The thin red lines, in the side view, represent thermo leading material to account for the not completely even epoxy surface of the chips

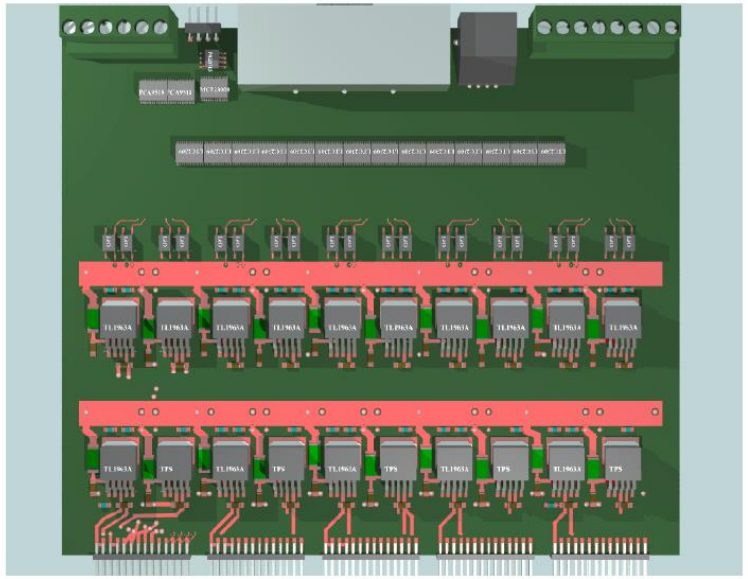
- In case one cooling loop is not sufficient it can be subdivided into max one cooling loop per row.

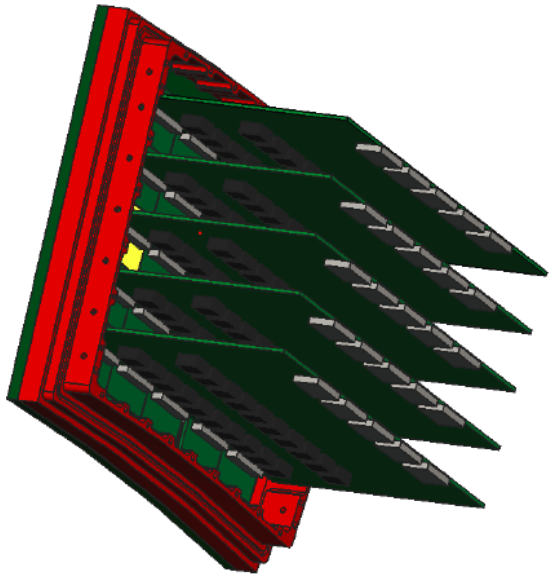
- It should be possible to mount the MCM-boards before the pad modules are installed into the TPC. Thus, the cooling system should be made compatible with this.



The final Low Voltage board

- The LV-board provides low voltage for five MCM-boards
- It contains 40 voltage regulators (8x5)
- The communication with the CPLD on the MCM is transmitted through the LV-board
- There are 5 LV-board per pad module
- The overall layout of the LV-board is ready
- The final dimensions of the board is determined by the size and positioning of the connectors, which is dependent on the layout of the cooling system, but is limited by the transverse dimensions of the pad module
- The LV-boards will be connected directly to the MCM-boards i.e. no cables will be needed



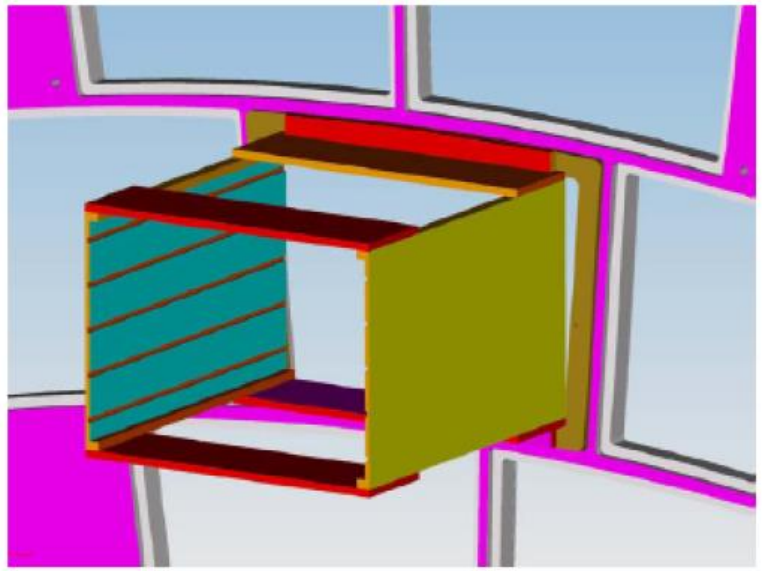


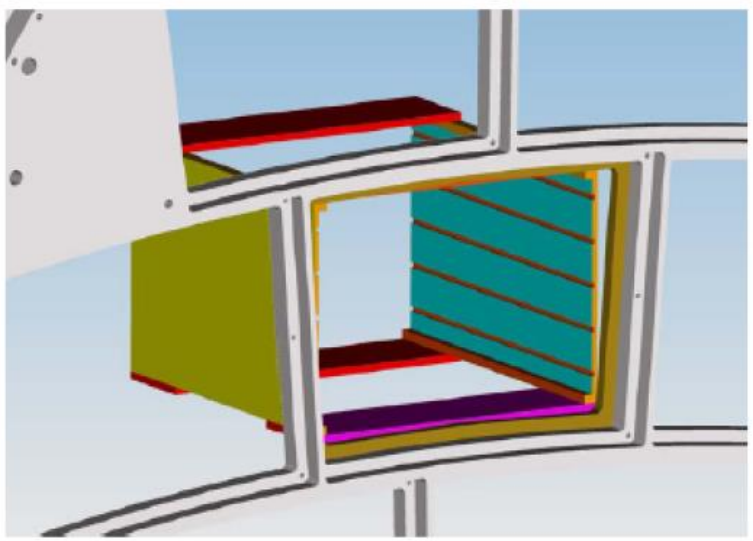
The mechanics

- The mechanics should allow for as simple as possible mounting of everything that has to be attached to the pad plane (electronics boards, HV-cables, cooling)

- The figures show the first ideas on the support structure (Bernd Beyer). The groves on the sides are for the LV-boards

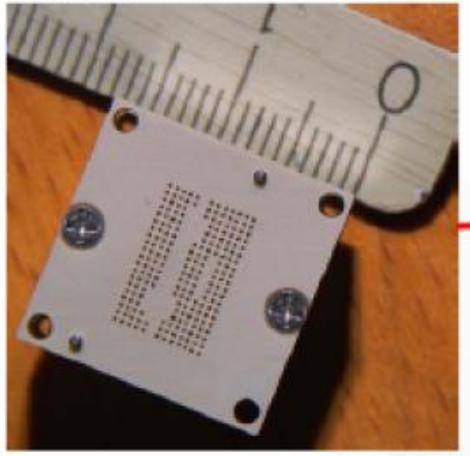
- Possible mounting procedure:
  1) mount the pad module with MCM-boards and cooling pipes
  2) connect cooling pipes to the outer world
  3) connect HV-cables
  4) mount the support box
  5) attach cables and cooling pipes to the support box in a proper way
  6) slide in the LV boards



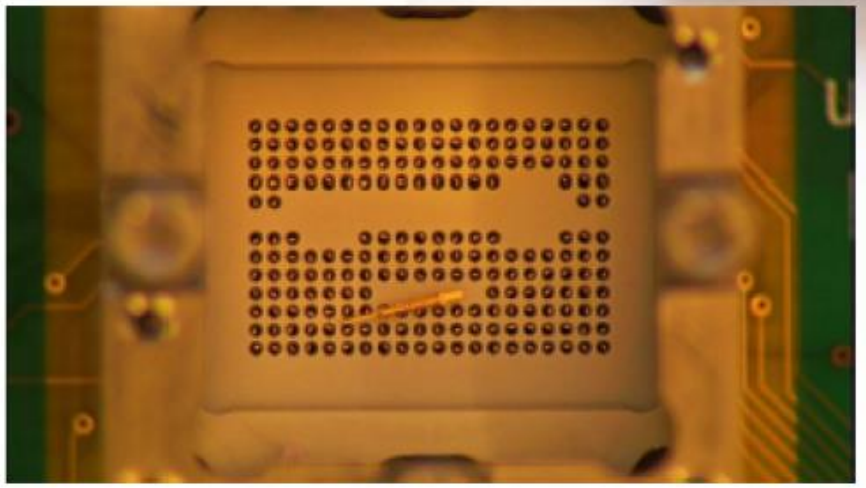


The Test Boards

Test socket



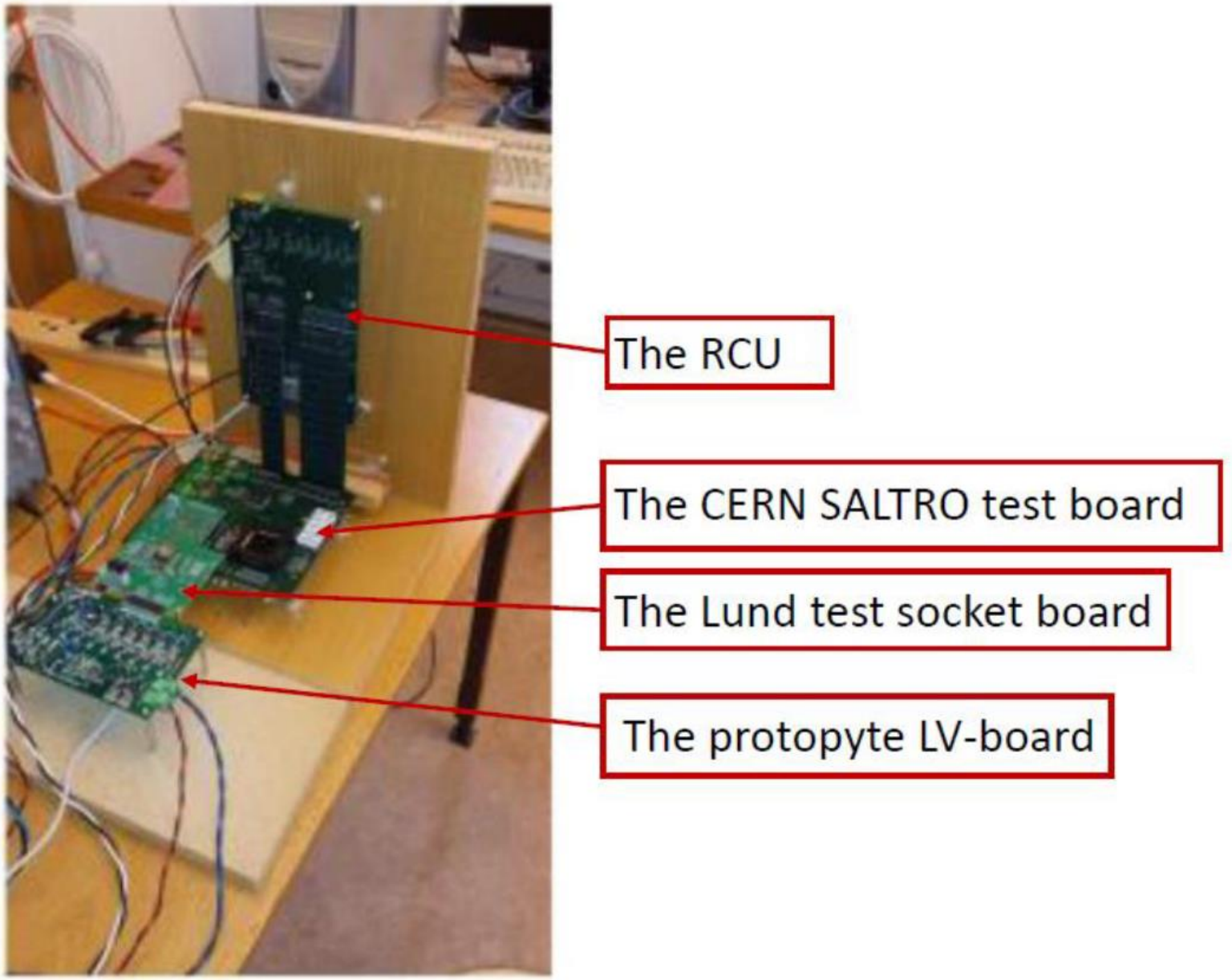
Lund test socket board



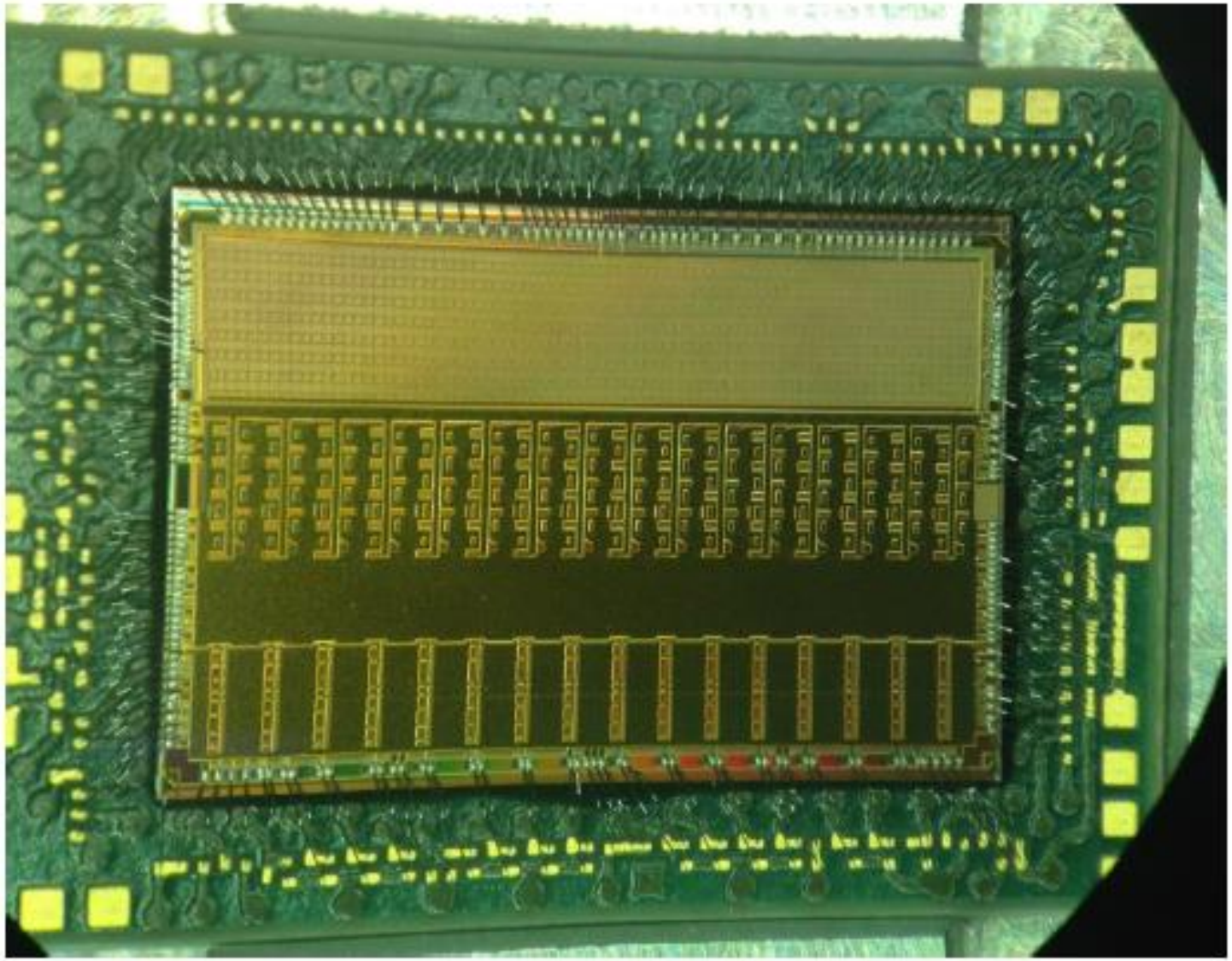
CERN test board

The Test Set-Up

- The software used to read out the data from the test set-up is EUDET TPC DAQ, which is also used for the test beam

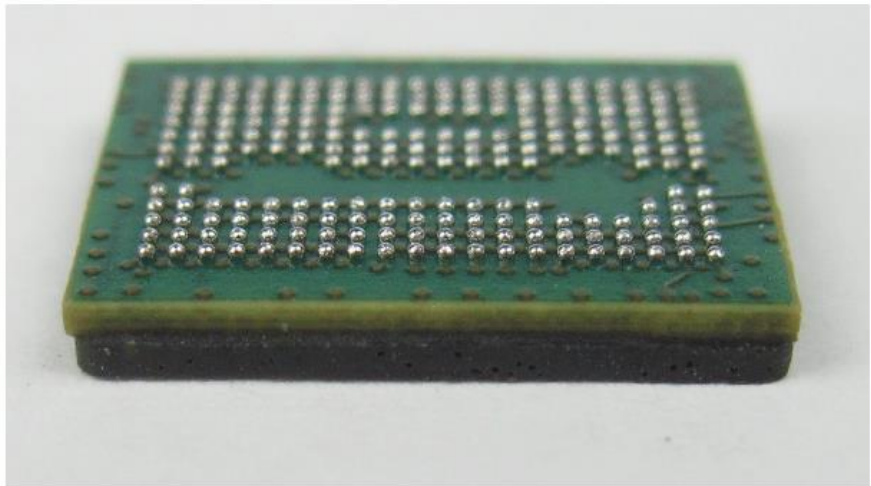


The Carrier Board



- A Carrier Board (size 12x8.9 mm2) with a fully bonded chip. It contains more than 200 bonding wires (left)

- The bottom surface of the Carrier Board with tin balls applied.
On the top surface the epoxy layer can be seen (below)



Test results

- The naked carrier board has been carefully tested for bugs but none were found

- Documentation by photo have been required after each step in the mounting procedure:
  - after bonding to check that there are no shorts between bonding wires
  - after mounting of the passive components to see that the right components are mounted

- The digital communication with the chip has been established

- It is possiblle to write into the registers and the information written is not getting lost.

- Values written in the registers can be read back

- However, the chip behaves unstable (write and read failures)

- We suspect problems with the sampling clock on the carrier board. The fault rate depends on the activity on the data bus to the chip

- Progress is very slow due to lack of money

Finances

- After 9 years of continous funding the Swedish Research Council decided not to give further support to the electronics development. The project was rated high by the referees. Compared to previous years there were very many application that were not approved.

- A new application has been submitted to the Research Council with a somewhat different focus. Mainly the salaries of the engineers are requested.

- For the ESS in Lund a project to search for n-nbar oscillations is discussed and a Letter of Interest has just been submitted. High resolution tracking is required and can be provided by a TPC where our electronics is useful. Estimated total cost for the project is 100 MEuro ± 50%. Time schedule foresees a Technical Design Report in 2017 and that contruction starts 2019.

- An application to the Faculty with the title: 'General purpose readout system for micro pattern detectors for ionizing radiation' has been submitted. We request 1.415 kSEK (~ 140 kEuro) over 4 years to partly cover the salaries of our engineers.

- There are several Swedish groups interested in the ESS experiment and a common application to the Research Council for infrastructure funds is in preparation and will be submitted until May 5th.

Summary

- Several electronics boards are ready and have been tested / are in operation
- The boards which are not ready yet are dependent on test results
- Development of the firmware is continuing
- The presently bad financial situation makes progress slow
- Several applications for support has been sent in / are in preparation