



# AIDA/ AIDA-2020 (mini) Trigger/Timing Logic Unit (mini TLU)

Synchronization for combined beam tests

Making life easier (?)

Request for Comments



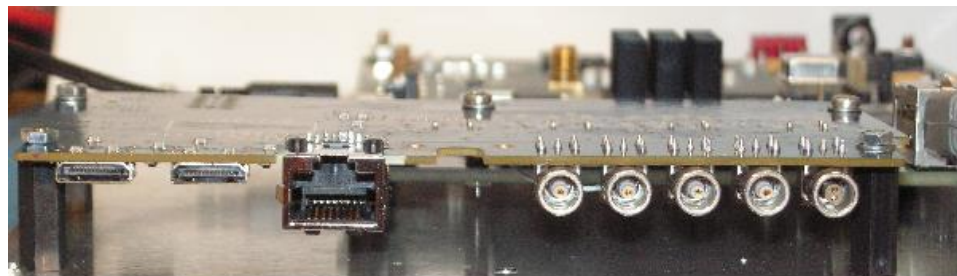
# Introduction

- **PROVIDE SIMPLE TIMING/SYNCHRONISATION INTERFACE**
  - DEVELOPED FOR AIDA
  - WILL BE DEVELOPED AND SUPPORTED IN AIDA-2020
- **TWO MODES**
  - SYNCHRONOUS MODE ( COMMON CLOCK )  
SYNC/TRIGGER/BUSY SIGNALS
  - ASYNCHRONOUS MODE ( EUDET MODE )
  - MODES CAN BE MIXED ON DIFFERENT INTERFACES
- **LVDS SIGNALS ON HDMI CABLES. COMPATIBLE WITH CALICE CCC AND DIF → LDA LINKS.**

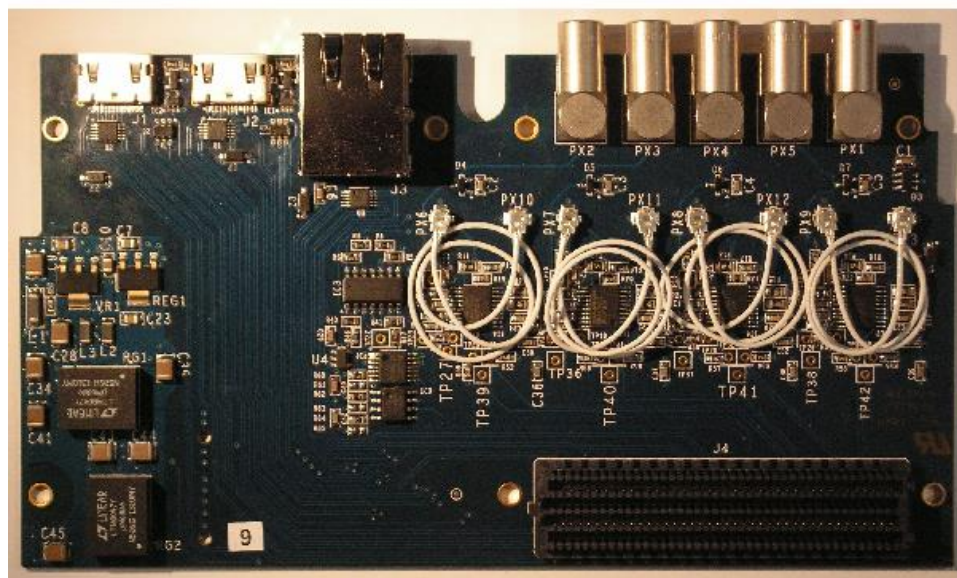


# Hardware

- Implemented as FPGA Mezzanine Card (FMC).
- Plugs into off-the-shelf FPGA carrier
- Four trigger inputs
  - Software adjustable threshold
  - Threshold and CFD
- Three Device Under Test interfaces
  - Can be fanned out to up to 30 DUT interfaces in synchronous mode with external fanout.
- Open Hardware, Open Firmware:  
<http://www.ohwr.org/projects/fmc-mtlu/wiki>



DUT0 (HDMI) DUT1 (HDMI) DUT2 (RJ45) Trigger Inputs Clock I/O





# Hardware

- Currently only as boards bolted to plate
- Design for box in progress





# TLU Uses

- Like a NIM crate
  - Smaller
  - Trigger/busy logic
- Synchronize multiple DAQ systems
  - Mix triggered and “no trigger” ( self triggering, continuously active )
  - Multiple ways of synchronizing data – count triggers, correlate timestamps.



# What do *you* want?

- TLU intended to be of general use
  - AIDA-2020 aimed as building capability
- Direction of development steered by users
  - Can only be steered by users if you tell me what you want...