# SPT Power Dissipation

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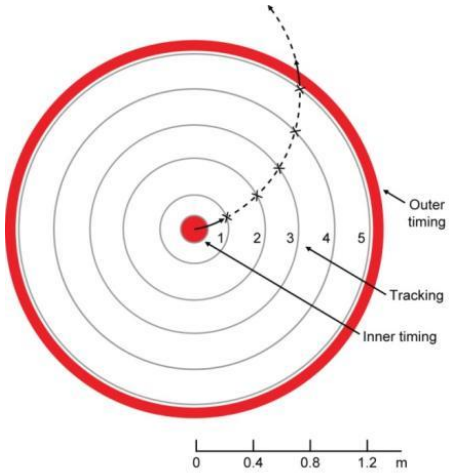
This document calculates the approximate power dissipation in a silicon pixel tracker (SPT) for ILC.




## Tracking layers

Following the proposed beam structure at the ILC, the tracking layers integrate all events during the entire 1ms-long bunch train and are read out in the 200 ms long inter-beam intervals.

The sensors are biased but may not consume any power during the bunch train. Powering off the SPT is not going to deliver significant savings due to the very small duty cycle of the beam, but may create unwanted power supply transients. In the following calculation the sensor is considered continuously powered.

### Number of sensors:

The total area of the SPT is 70 $m^2$. If each sensor is 80 mm square, the SPT will consist of approximately 11,000 sensors.

The pixel size is taken as 50 µm square, and each sensor will contain 1600×1600 pixels.

### Readout scheme:

Each sensor is read out independently during the 200ms beam-off time. “Read out” means that each pixel is powered and queried for signal.

Row-by-row readout is considered here for its simplicity. After the bunch train, each row is powered up in sequence, and the signal in each pixel is compared to a threshold. Two variants of that are possible:

a) Threshold comparison per pixel. Each pixel contains a CDS circuit, a comparator and a digital buffer, and outputs either logic high or low when interrogated.

b) Threshold comparison per row. The signal of each row is read out in parallel to a row CDS circuit, positioned at the bottom of the sensor. The CDS circuit contains the comparator as well. The digital signals are then multiplexed and read out from one buffer per chip, e.g. a LVDS driver. In the pixel there are only 3 transistors – reset transistor, a source follower and a column switch.

It is not obvious whether (a) or (b) will be more power efficient. In (a) the signal remains local and will suffer less from load capacitances, which would be beneficial if the supply currents of the CDS and comparator circuits can be made very small. However, (a) will have 3 orders of magnitude higher number of transistors per sensor than (b), and much larger part of the pixel will be occupied by electronics instead of charge collecting elements.

## Readout timing:

The time available for readout of each row is 200ms/1600 = 125 µs. This is very slow by any standards, and allows either sub-µA in-pixel circuitry or row readout from one end of the chip with source follower currents of the order of 1 µA.

## Power calculation:

A realistic number for the current draw in the in-pixel source follower (present in both (a) and (b)) is 1 µA. This is assuming 180nm CMOS process.

When addressed, a row will dissipate 1600*1µA*1.8V = 2.88mW. Since one row per sensor is always powered, the total power dissipation of the SPT from pixel power alone is 11000*2.88mW = 31.68W.

The power consumption for the CDS and comparator circuits is taken as 1600*5µA*1.8V = 14.4mW. These can be either in pixel or common for the whole sensor. In-pixel circuitry is likely to have lower power consumption at the expense of increased overall sensor complexity.

The power for driving the LVDS output is 5mA*1.8V = 9mW. The absolute minimum LVDS supply current is determined by the need to develop 340mV across 100Ω load, or 3.4mA. Not all of this power will be dissipated in the volume of the SPT, but here it is assumed so as a worst case scenario.

The total power dissipation is then Ptot = 11000*(2.88mW + 14.4mW + 9mW) = 289W.

A simplistic power consumption formula could look like this:

$$Power = V_{CC}\left[\left(\frac{D}{P}\right)I_{SF} + \left(\frac{D}{P}\right)I_{CDSCMP} + I_{LVDS}\right]\left(\frac{A}{D^2}\right)$$

where:

$V_{CC}$ is the supply voltage (1.8V)

$D$is the sensor chip size, assumed square (8 cm)

$P$ is the pixel pitch (50 µm)

$I_{SF}$ is the in-pixel source follower current (1 µA)

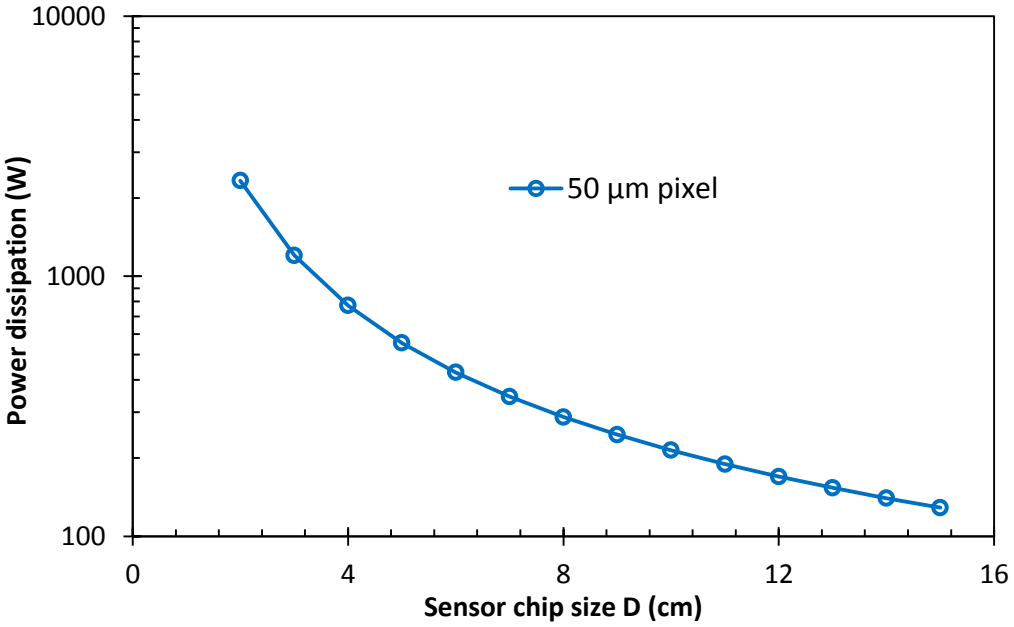
$I_{CDSCMP}$ is the current consumption of the CDS and comparator circuits (5 µA)

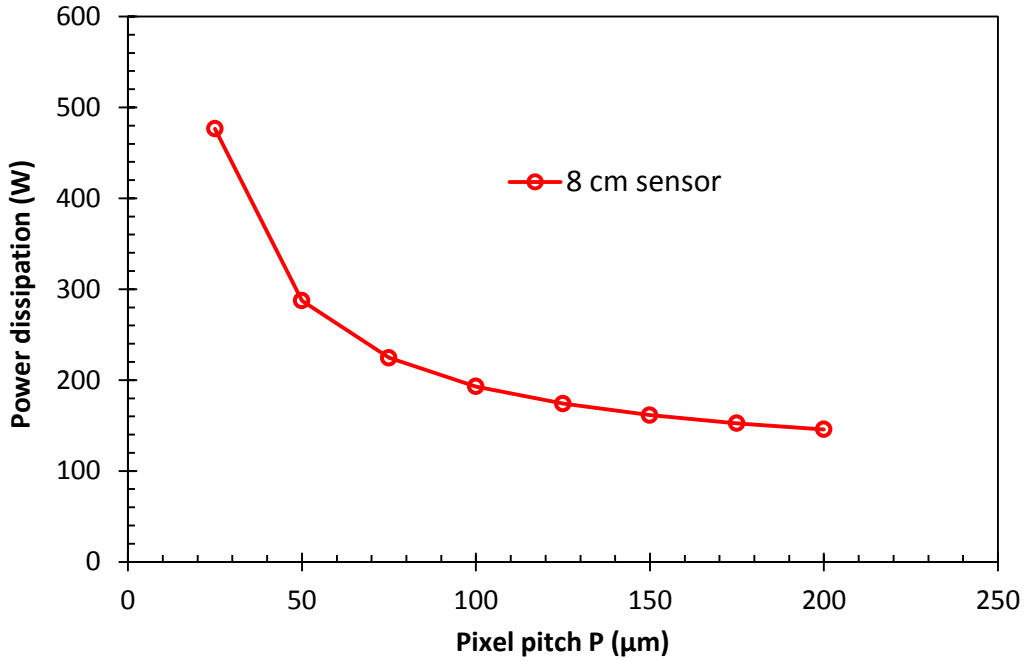
$I_{LVDS}$ is the current consumption of the LVDS output circuitry (5 mA)

$A$ is the SPT area (70 m$^2$)

The power dissipation follows nearly 1/x type dependence on the pixel pitch and sensor chip size. Two cases are shown in the following figures – one for fixed pixel pitch and varying sensor chip size, and vice versa.

In practice the pixel current consumption is expected to decrease as the sensor size decreases (by driving smaller capacitance), and the overall power consumption will be a less steep function of the pixel pitch and sensor chip sizes.



## Timing layers

Time stamping ensures that hit information is stored for each bunch crossing. This requires that each pixel is active during the bunch train and records the collected charge with in-pixel CDS and comparator circuitry. The hit density is supposed to be very small and it is very unlikely that a row will be hit twice, so the logic could be simple "wired OR" type.

There are 3 timing layers with total area of 119 $m^2$, or 14700 sensors with size 90mm × 90mm each and pixel size of 150µm (600×600 pixels).

Sensor readout is done during the beam off time, when the pixel array can be powered off. The response time of the in-pixel amplifier and comparator should be around 150ns. This is significantly faster than the integrating tracker, and whether similarly low pixel supply current can be possible remains to be seen. For now we assume that the supply current per pixel can be the same.

From the considerations for the time integrating tracker the power dissipation per pixel can be taken as 6µA*1.8V = 10.8µW. The total pixel power dissipation during BX is 14700*600*600*6µA*1.8V = 57kW. Adjusted for the beam duty cycle of 1/200, the average power becomes 285W.

To this we have to add the LVDS power per sensor 14700*9mW = 132W, and some power for the digital functionality for collecting and storing hit information – for now this can be the same as the LVDS power.

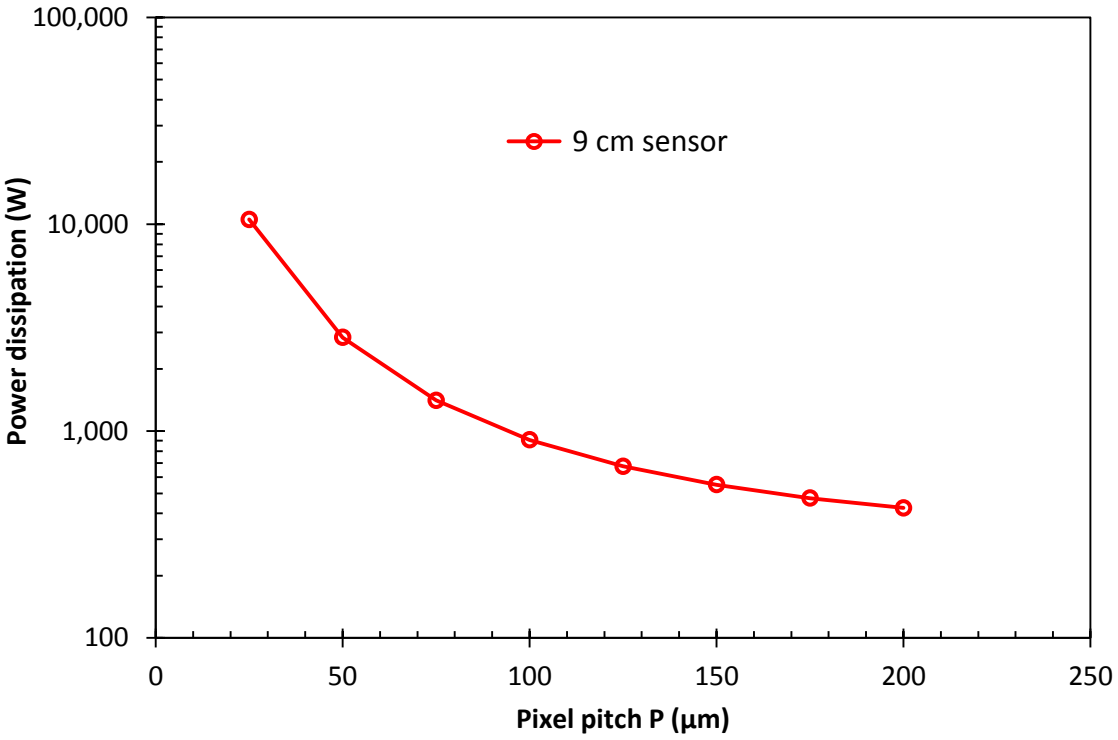
For 150µm pixels the total power for the timing layers becomes 550W, consisting of 264W steady state dissipation and 57kW pulsed power with duty cycle 1/200.

The power dissipation formula is:

$$Power = V_{CC}\left[\delta\left(\frac{D}{P}\right)^2 (I_{SF} + I_{CDSCMP}) + 2I_{LVDS}\right]\left(\frac{A}{D^2}\right)$$

where $\delta$ is the beam duty cycle (=1/200).

The power dissipation is a very strong function of the pixel pitch, as shown in the figure below, and this could be an important parameter for optimisation. The high peak power is also an area of concern because it is likely to involve local power storage or appropriately sized power supply cabling, and this can increase the material budget.


100,000
10,000
1,000
100
Power dissipation (W)
9 cm sensor
0
50
100
150
200
250
Pixel pitch P (µm)