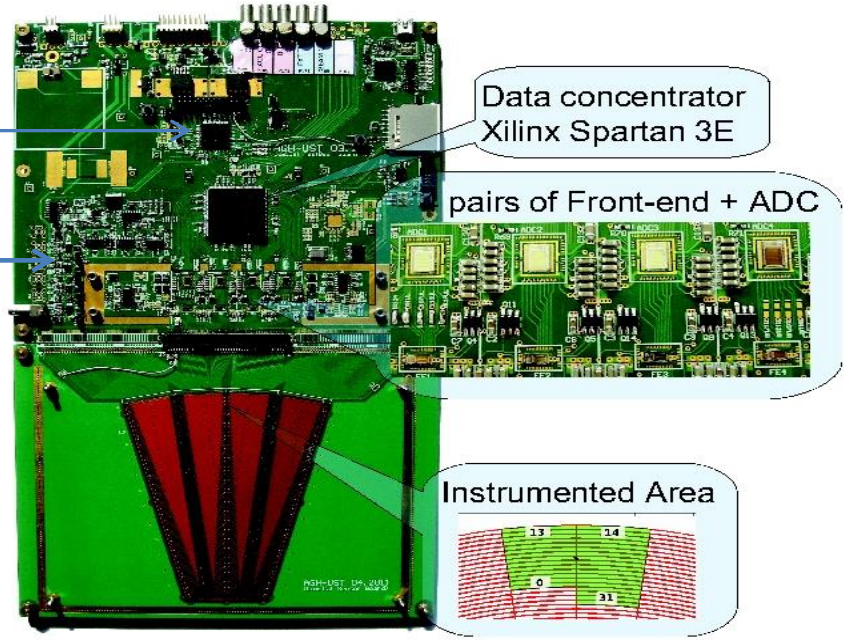
New readout board –

Start discussion on the PCB design, prototyping, potential of contributions from partners involved

L. Zawiejski, IFJ PAN

12th FCAL Hardware WG Meeting, July 7, 2015

” Old” readout and sensor boards

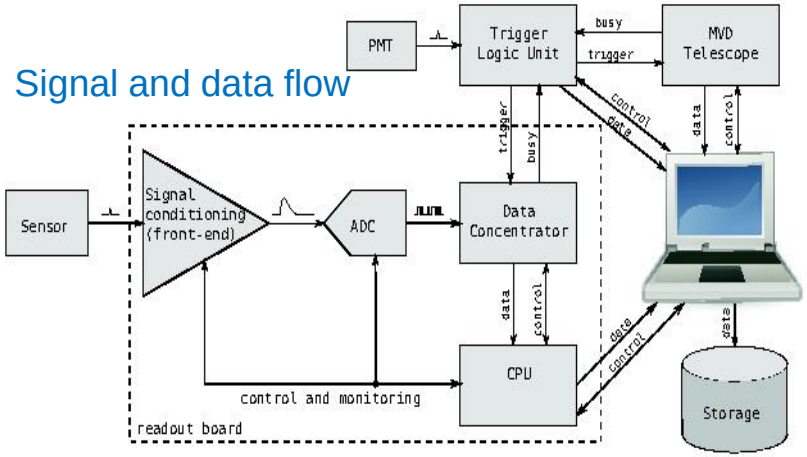


Sensor board with glued sensors and kapton fan-out wire bounded

- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam) ILC mode

FCAL DAQ system

Signal and data flow



Acquisition software used in test beams (based on EUDAQ) allow to

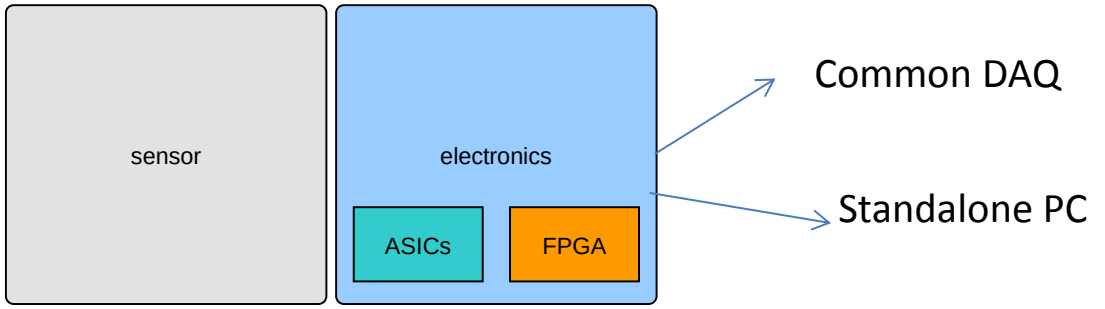
- Sending configuration
- Collecting data (events, monitoring)

ROOT monitor allows on-line monitoring

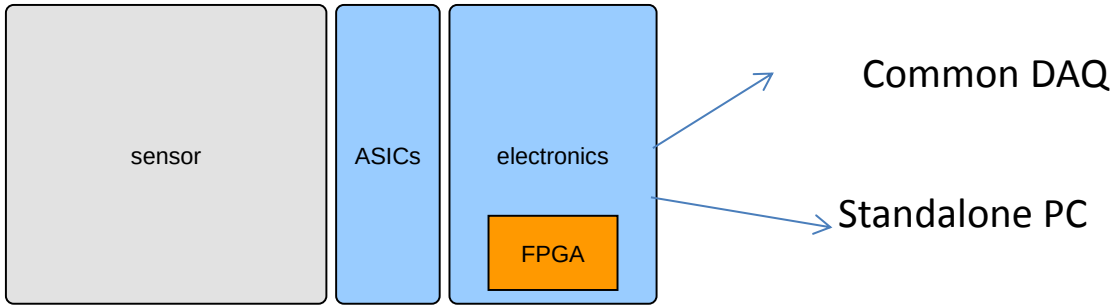
New PCB - should keep this style?

Possible solution for electronic board

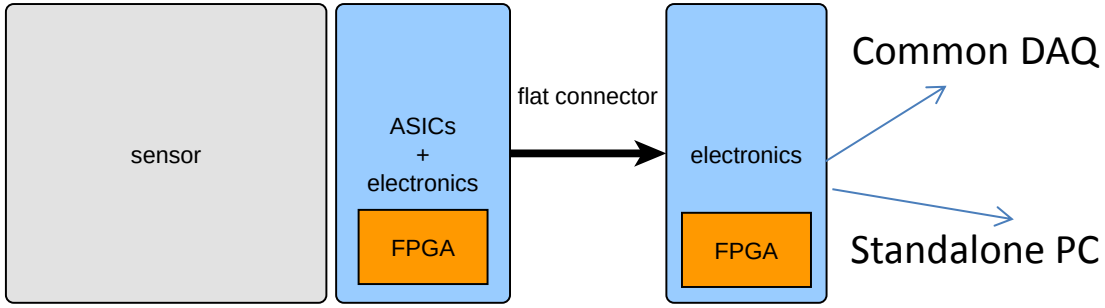
The current version



Option with the separated
ASIC and digital part (with FPGA)



Minimalisation?



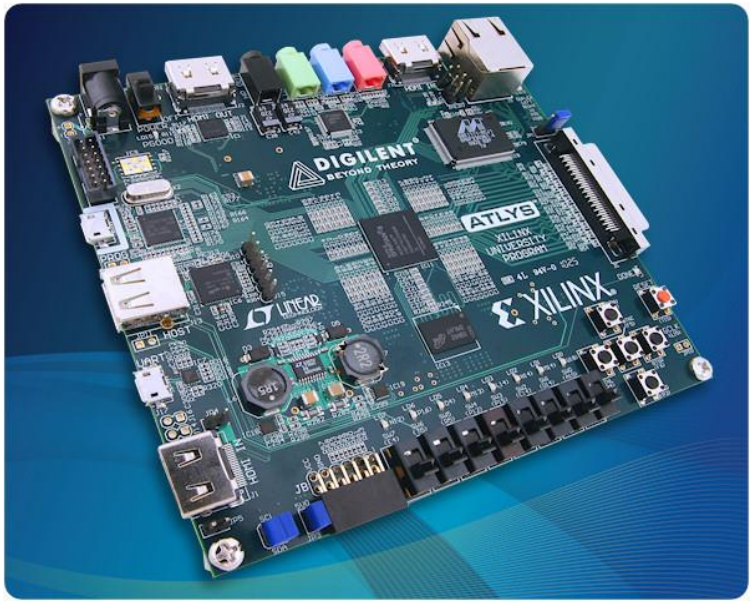
Possible contribution from IFJ PAN -

(What at present day lies in our manpower and financial capabilities)

We want to create a full-valuable test stand for FPGA

We start learning with:

FPGA – Digilent Atlys Xilinx Spartan-6 LX45



It can be communicated by
Ethernet, USB, HDMI interfaces