Status of HV-CMOS submission in AMS350

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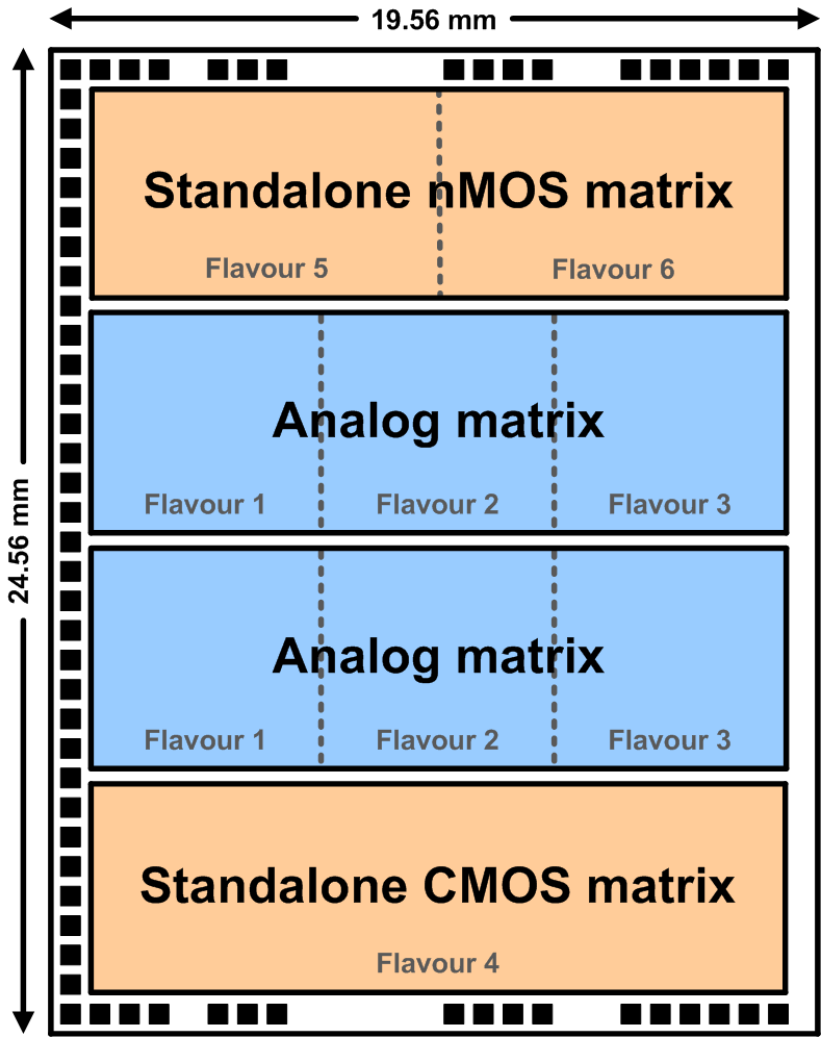
Outline

1. Architecture and floorplan
2. Pixel schematics and layouts
3. Simulations

Pixel demonstrator - Floorplan



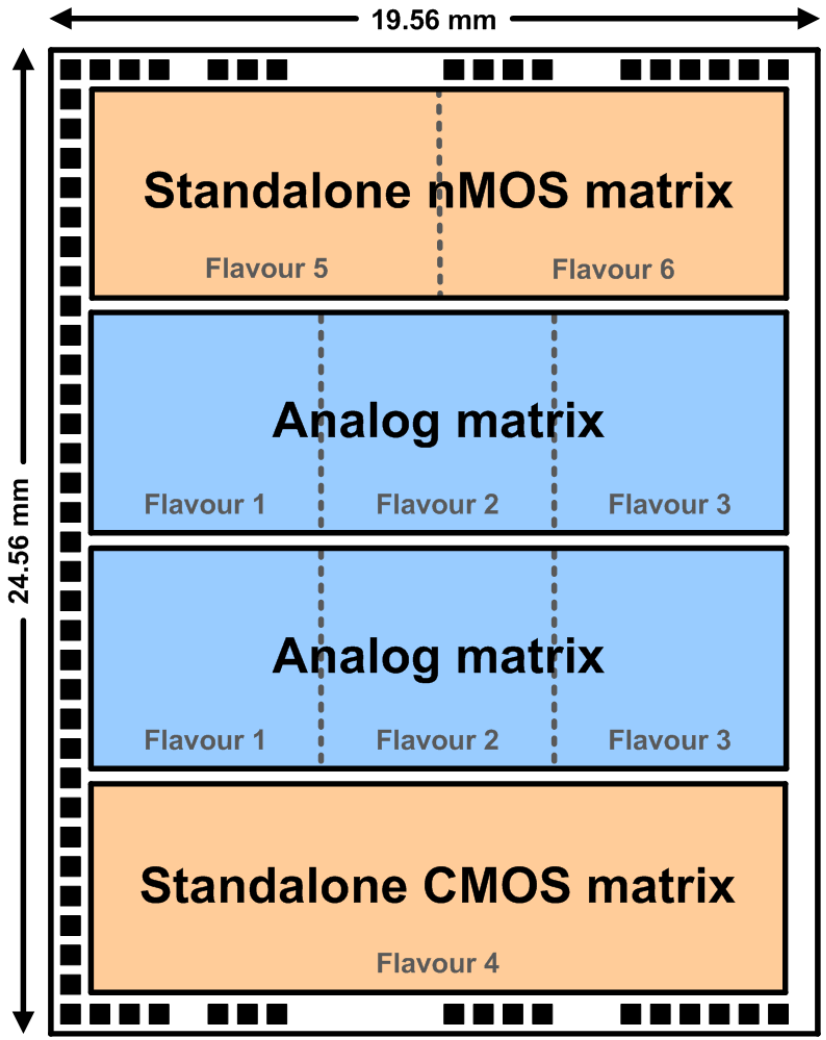
Areas (from top to bottom):

- digital pixels with standalone readout
  - in-pixel nMOS comparator
- analog matrix
  - different flavours in terms of gain and speed
- analog pixels with standalone readout
  - CMOS comparator in the periphery

Main features:

- ams 0.35 µm High-Voltage CMOS (H35)
- submission through an engineering run
  - submission in September 2015
- different substrate resistivities
  - 20 Ω·cm (standard value), 200 Ω·cm, 1k Ω·cm

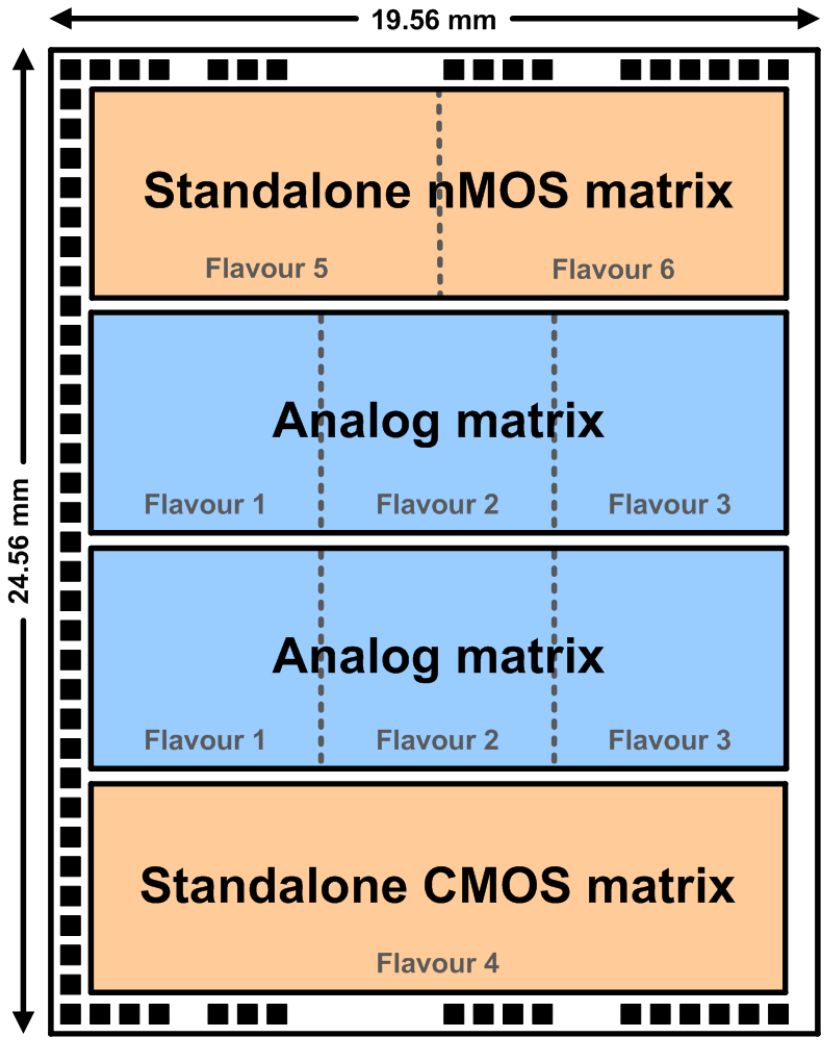
Pixel demonstrator - Floorplan



Digital pixels with standalone readout:

- 16 rows x 300 columns standalone pixels
- in-pixel amplifier and nMOS comparator
- 2 flavours (150 columns each):
  - nMOS comparator
  - nMOS comparator with TW compensation
- readout with FEI4 (bump/capacitive coupling) or with digital block in the periphery of the matrix
- 1-to-1 connection of each pixel to its digital cell in the periphery
- Digital block with same functionality as in FEI3
  - time-stamp storage
  - pixel address generation

Pixel demonstrator - Floorplan

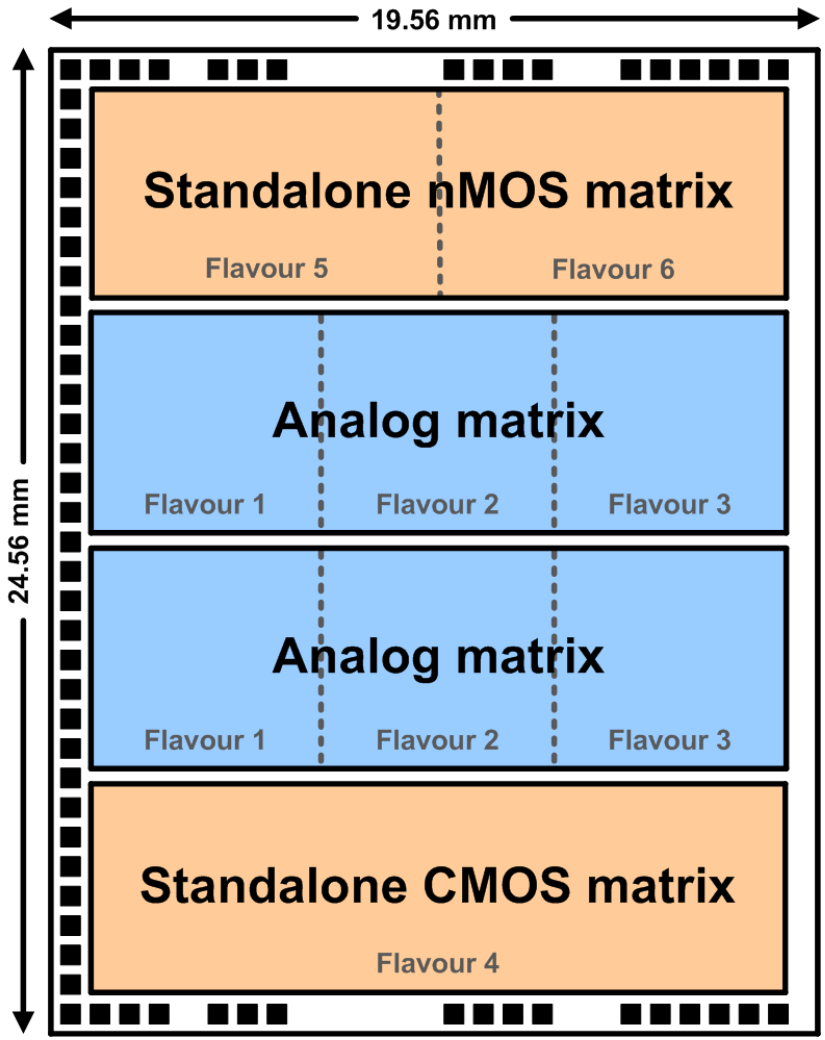


Analog matrix:

- 23 rows x 300 columns analog pixels
- in-pixel amplifier
- 3 flavours (100 columns each):
  - gain
  - speed
- readout with FEI4 (bump/capacitive coupling)

- 2 analog matrices, same idea, mirrored

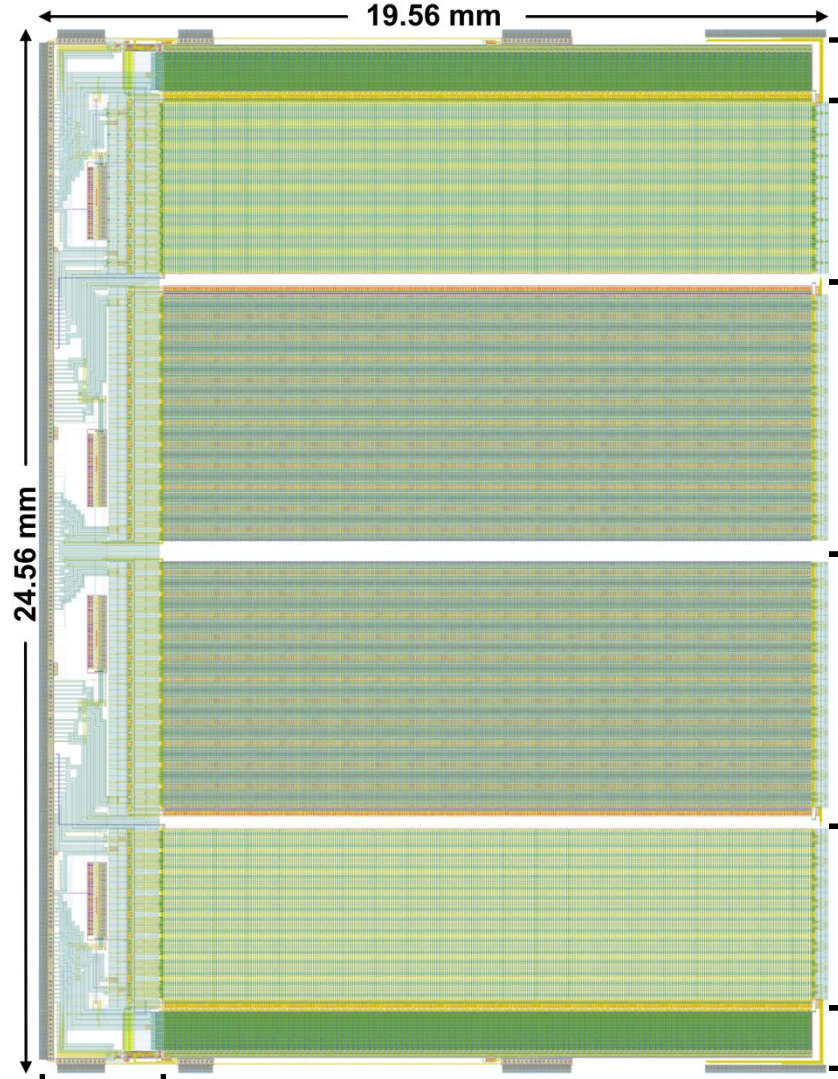
Pixel demonstrator - Floorplan



Analog pixels with standalone readout:

- 16 rows x 300 columns standalone pixels
- in-pixel amplifier and CMOS comparator in the periphery
- readout with FEI4 (bump/capacitive coupling) or with digital block in the periphery of the matrix
- 1-to-1 connection of each pixel to its digital cell in the periphery
- Digital block with same functionality as in FEI3
    - time-stamp storage
    - pixel address generation

Pixel demonstrator - Layout



← Digital and control circuits (15 mm x 1.45 mm)

← 16 rows x 300 cols **standalone nMOS matrix** (15 mm x 4mm)

← 500 µm gap

← 23 rows x 300 cols **analog matrix** (15 mm x 5.9mm)

← 500 µm gap

← 23 rows x 300 cols **analog matrix** (15 mm x 5.9mm)

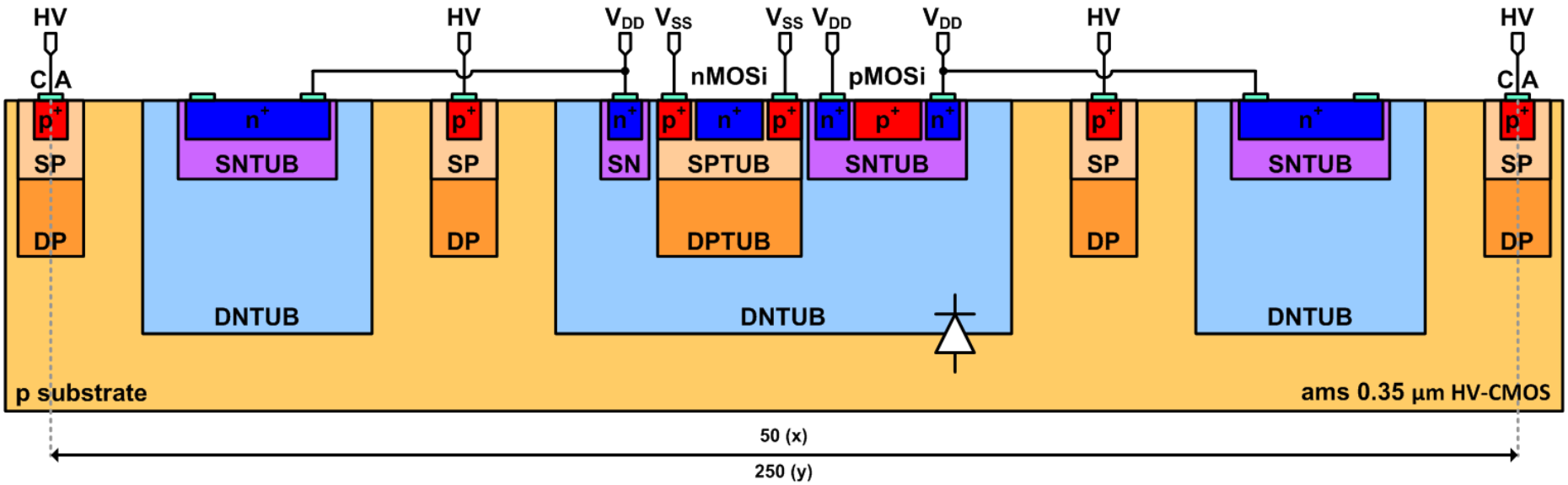
← 500 µm gap

← 16 rows x 300 cols **standalone CMOS matrix** (15 mm x 4mm)

← Digital and control circuits (15 mm x 1.45 mm)

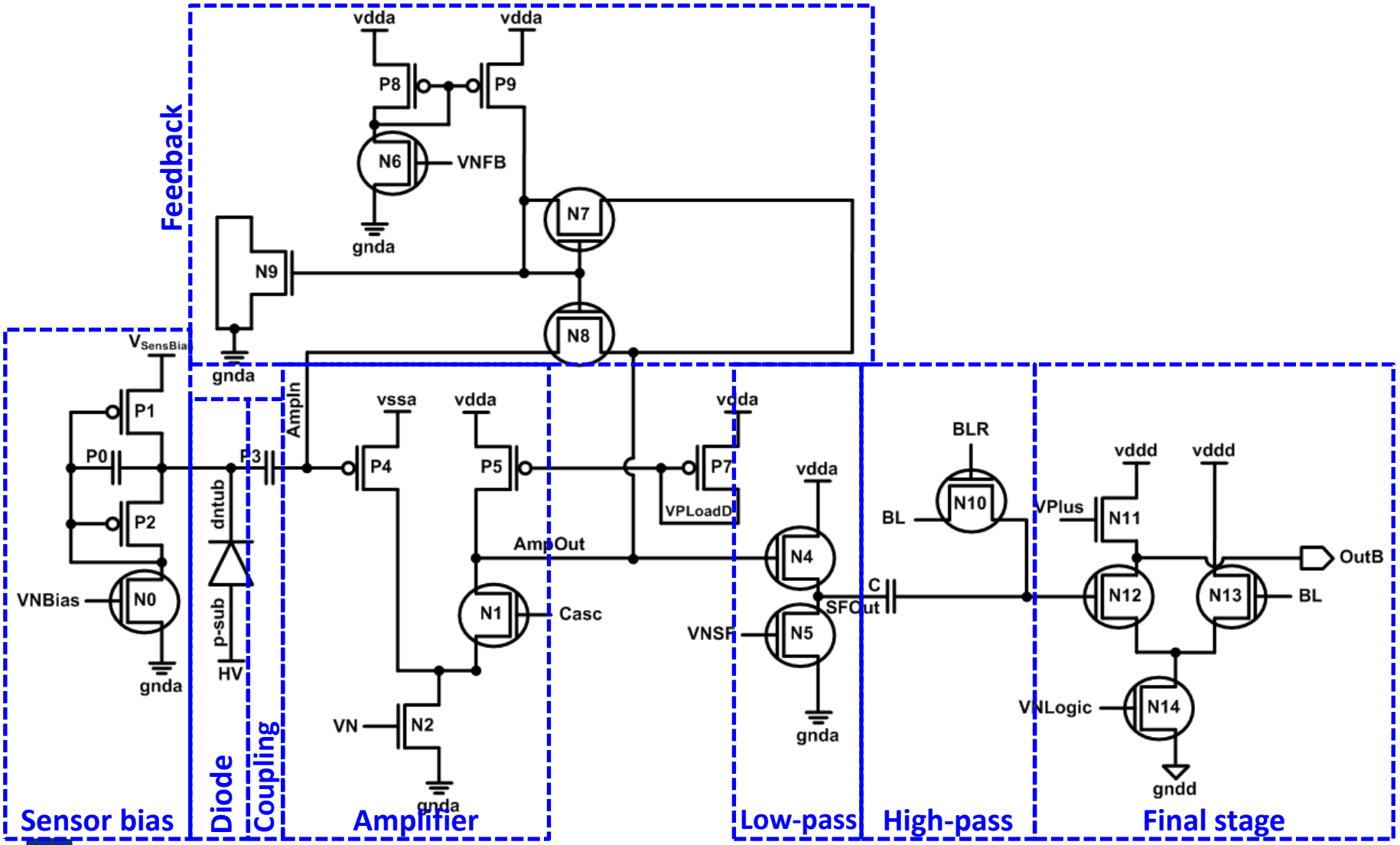
← Pads, bias circuits and power lines (2.97 mm x 24.56 mm)

Pixel demonstrator - Sensor cross-section

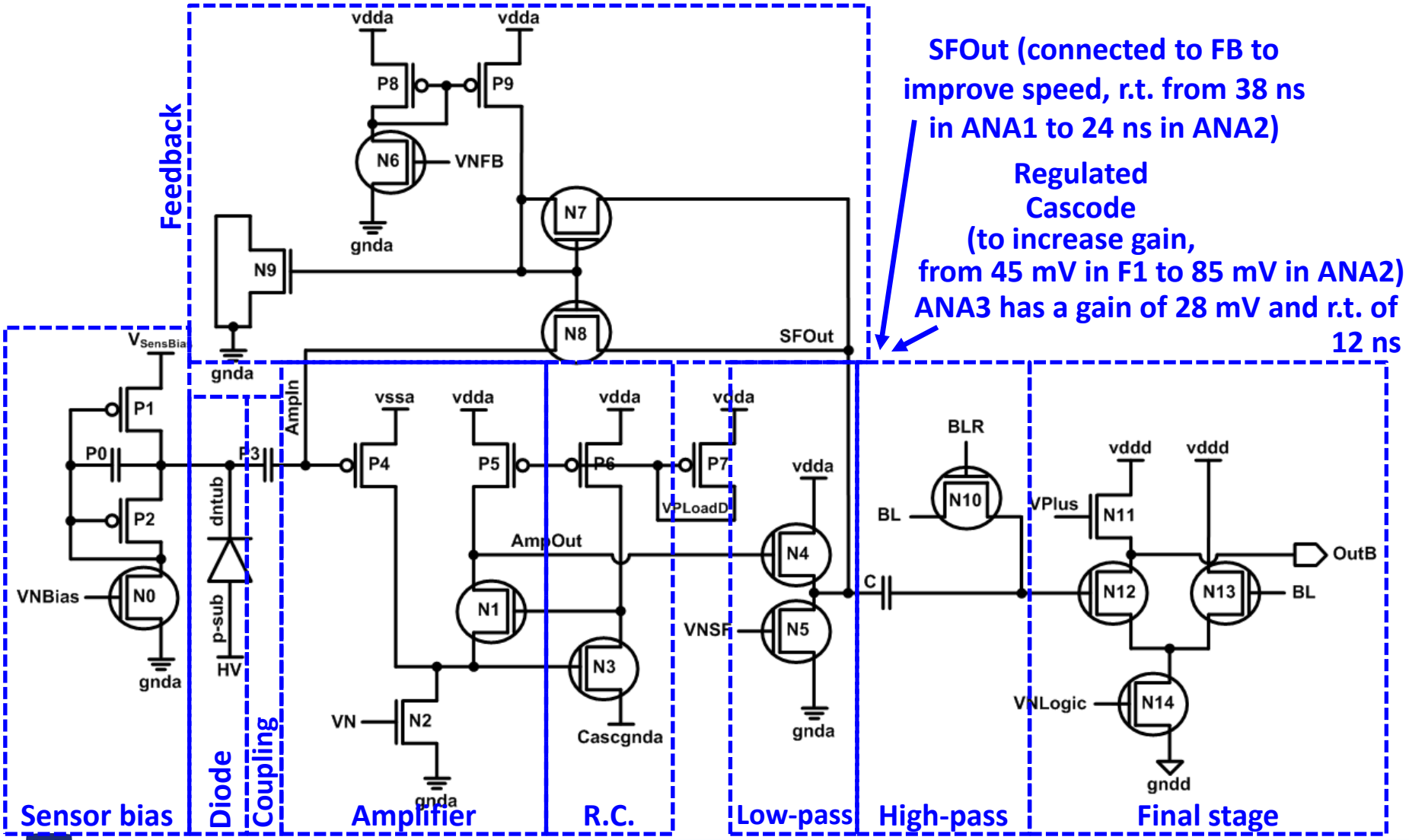


- **Pixel pitch is 50 µm x 250 µm**
- Discontinuous DNTUBs (where possible)
- DPTUB guard rings (HV) of 2 neighbouring pixels are overlapped
- Sensor with round shaped corners to avoid electric peak fields
- Guard rings are thick and uniform
- Transistor areas are covered with metal for shielding

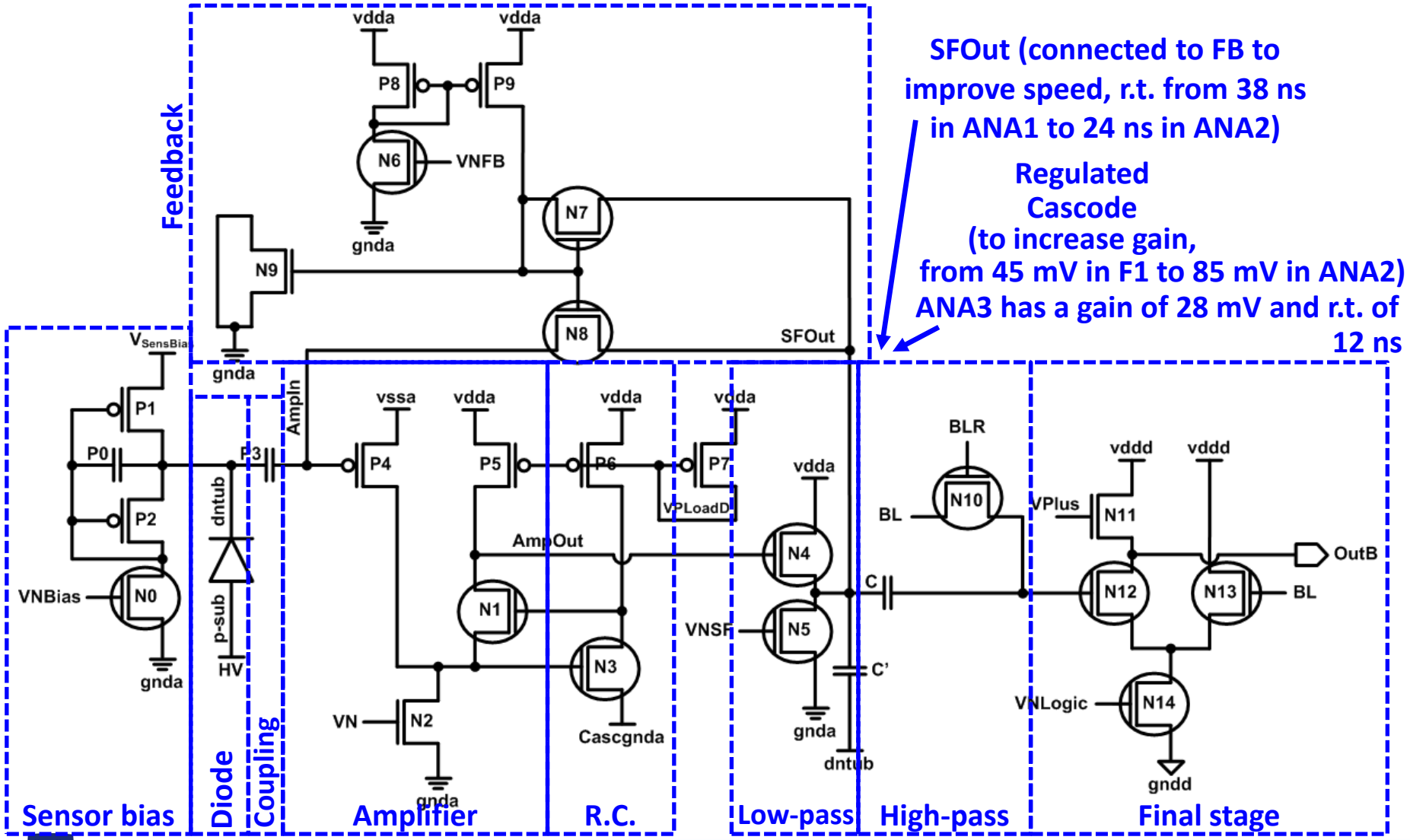
Pixel demonstrator - Pixel schematic (analog 1)



Pixel demonstrator - Pixel schematic (analog 2)



Pixel demonstrator - Pixel schematic (analog 3)



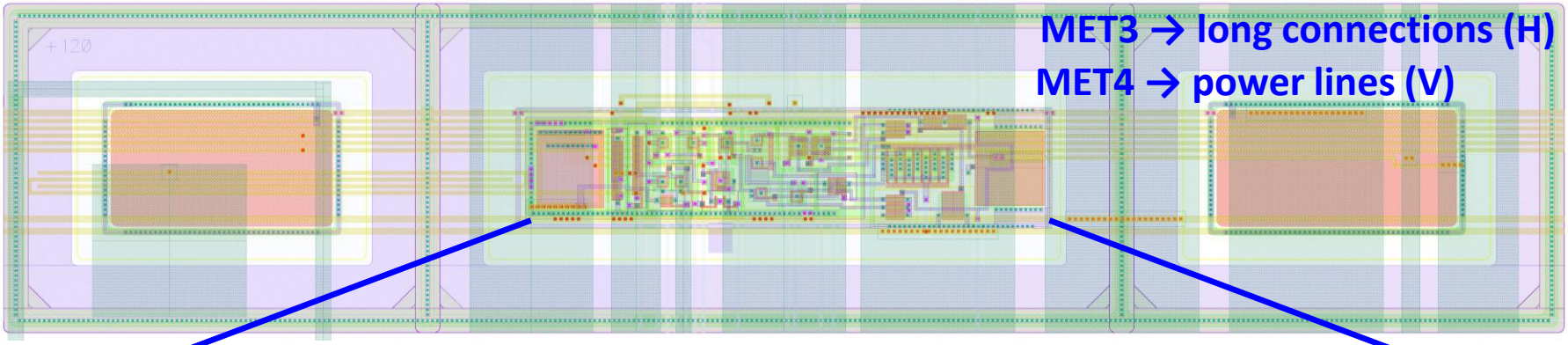
Pixel demonstrator - Pixel layout (analog)

MET1 → in-pixel connections

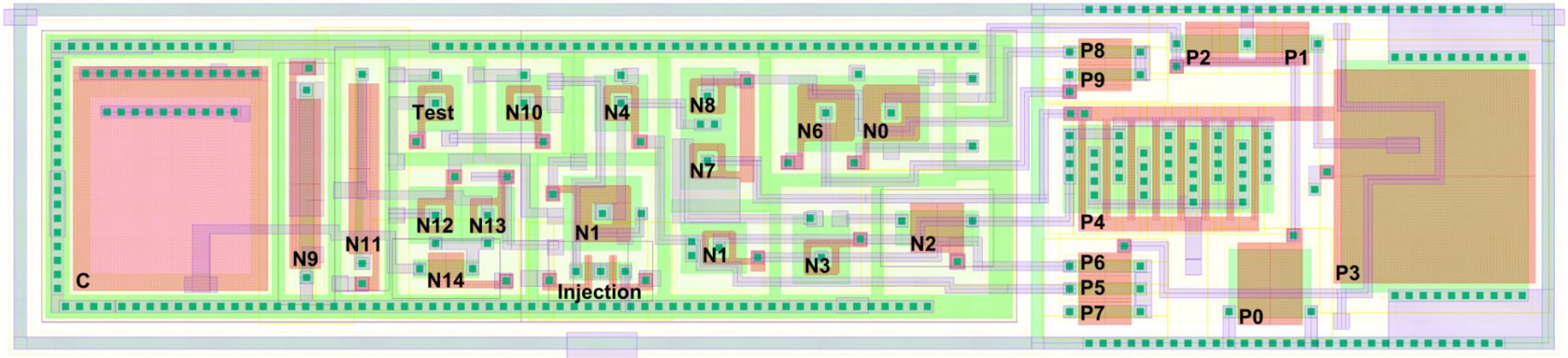
Pixel size is 50 µm x 250 µm MET2 → bias lines (V) + shielding

MET3 → long connections (H)

MET4 → power lines (V)



Transistors area is 20.25 µm x 87.7 µm



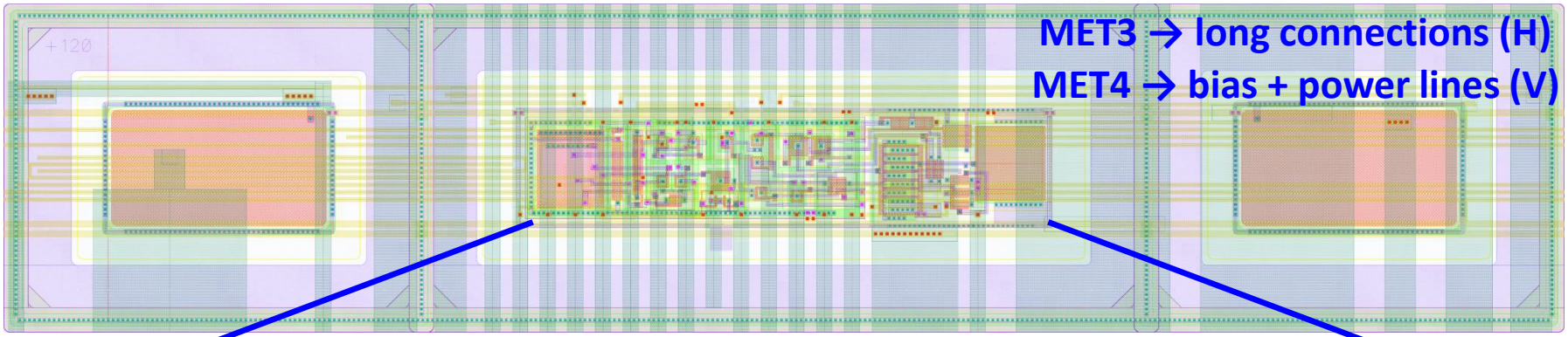
Pixel demonstrator - Pixel layout (stand CMOS)

MET1 → in-pixel connections

Pixel size is 50 µm x 250 µm MET2 → shielding

MET3 → long connections (H)

MET4 → bias + power lines (V)



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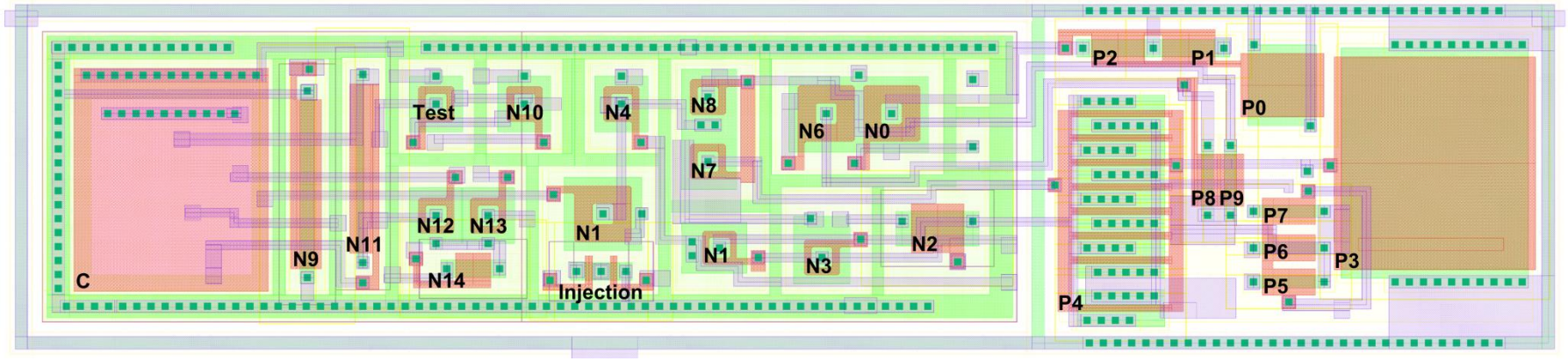
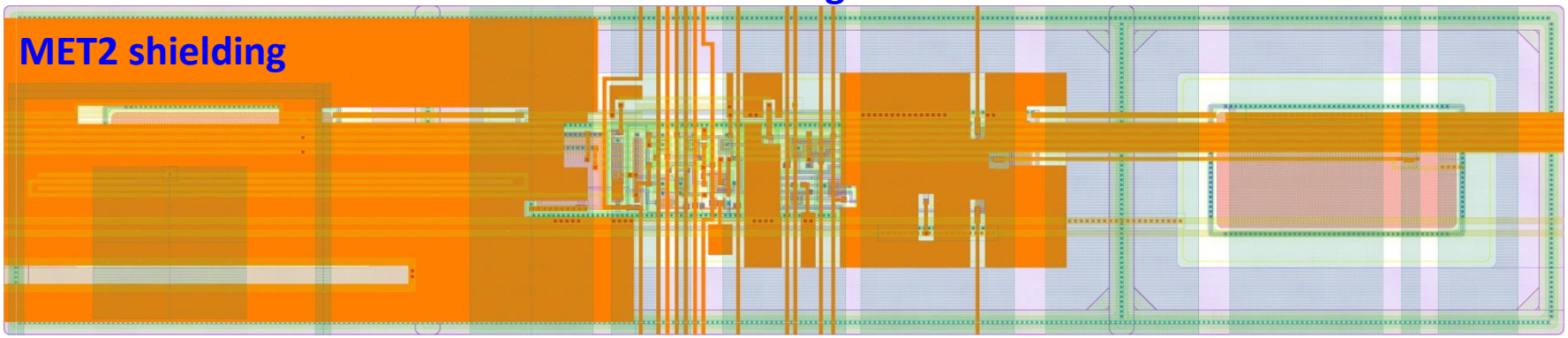


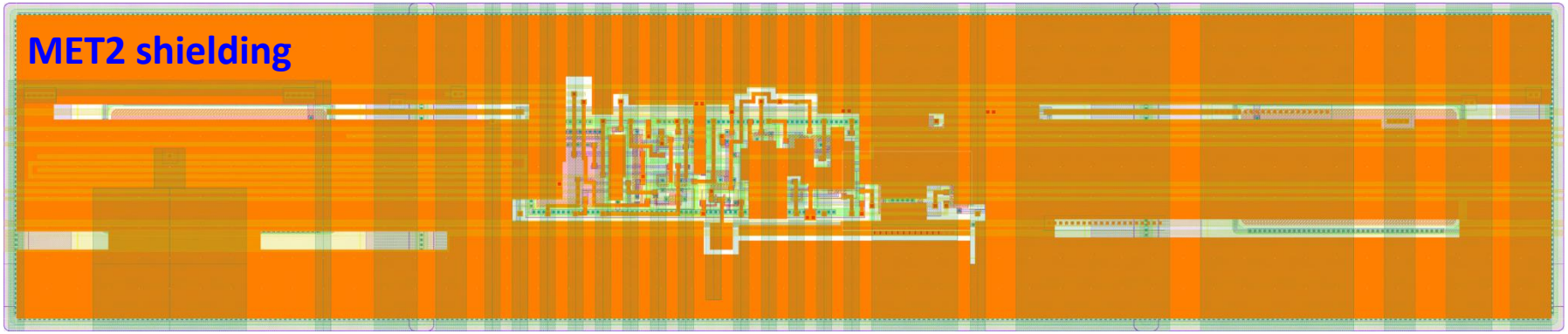
- Pixel area is equal to analog pixels, standard CMOS comparator in the periphery.

Pixel demonstrator - Shielding

Analog

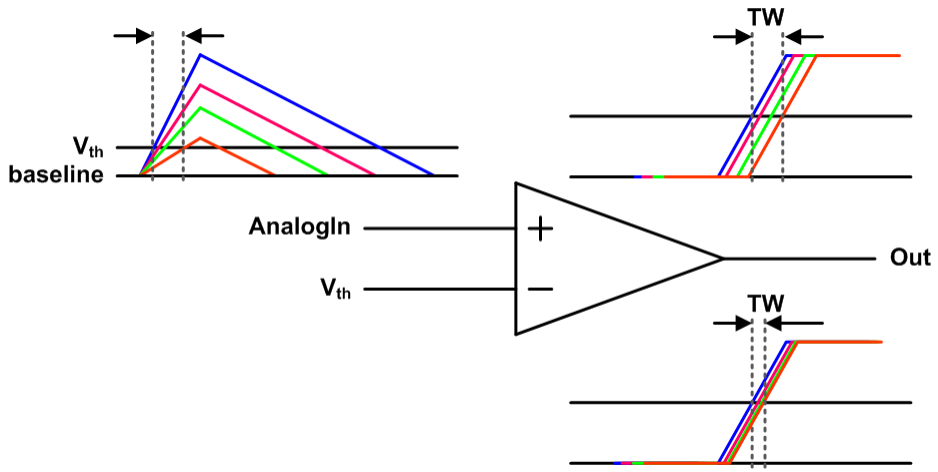


Standalone CMOS



Pixel demonstrator - Time walking compensation

- **Discriminator:**
- nMOS comparators inside the pixel area.
- Low and high energy particles generate signals that cross the threshold voltage at different times (also the response time of the electronics is dependent on the signal strength). This time difference is the time walk.
- Idea of time walk compensation → The propagation time through the comparator is independent of the amplitude of the signal generated by the sensor.

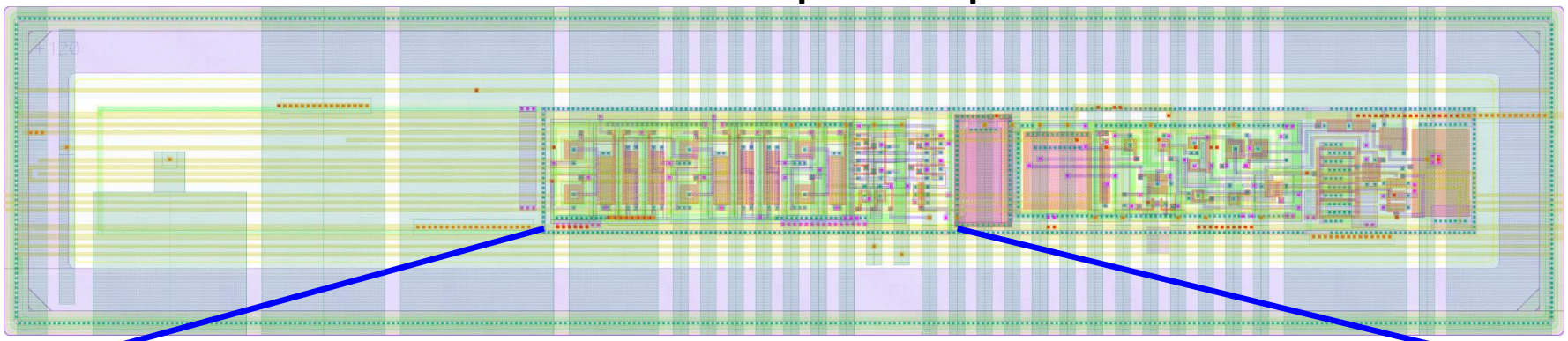


Without compensation
(TW ≈ 25 ns with
standard resistivity)

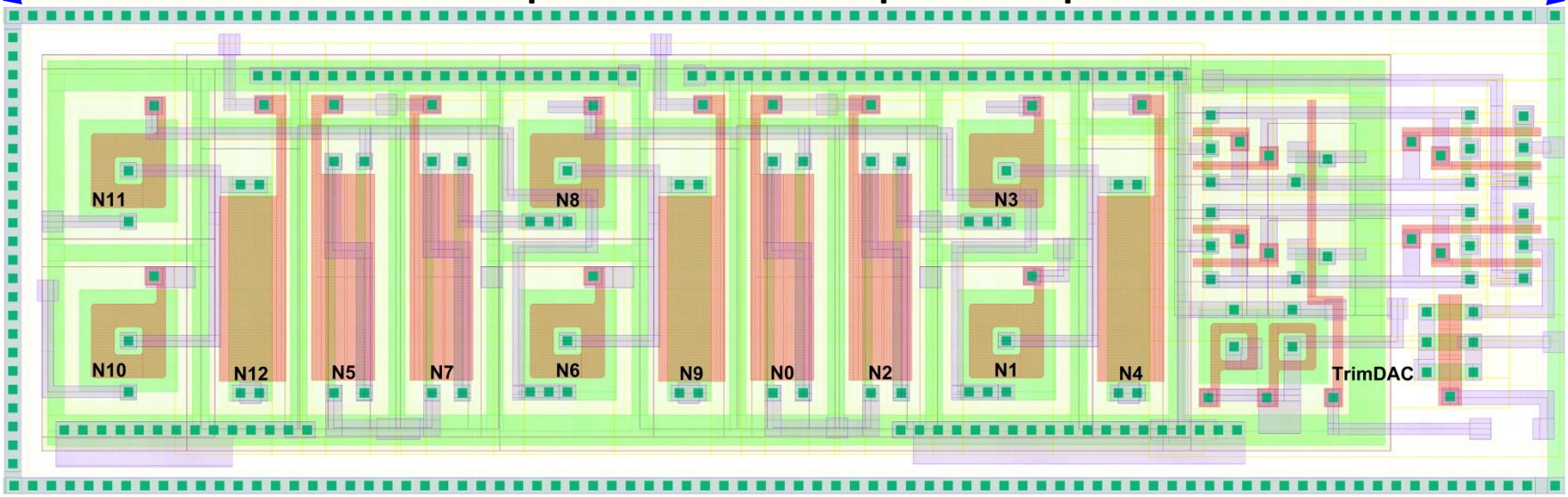
With compensation
(TW ≈ a few ns only)

Pixel demonstrator - Pixel layout (stand nMOS)

Pixel size is 50 µm x 250 µm

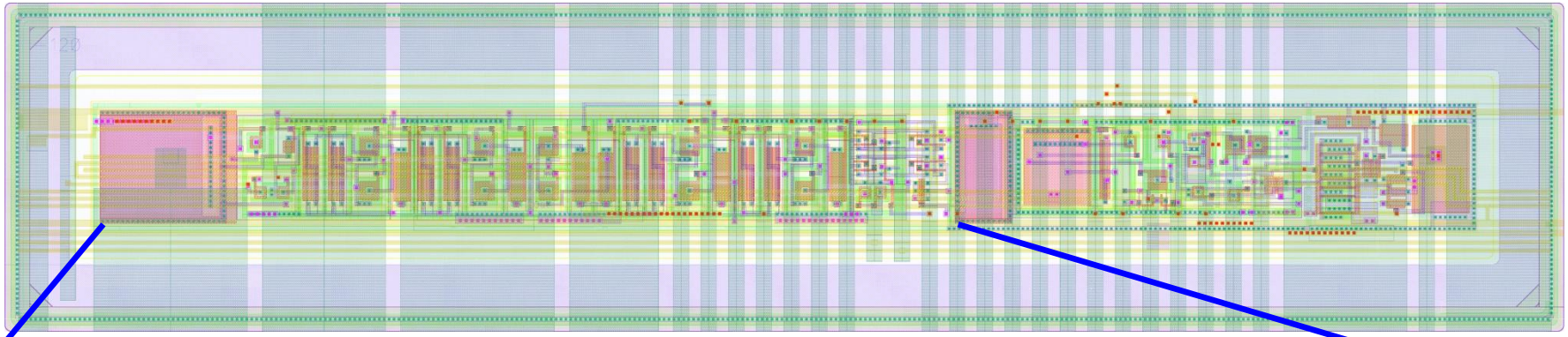


Comparator area is 21.5 µm x 67.3 µm

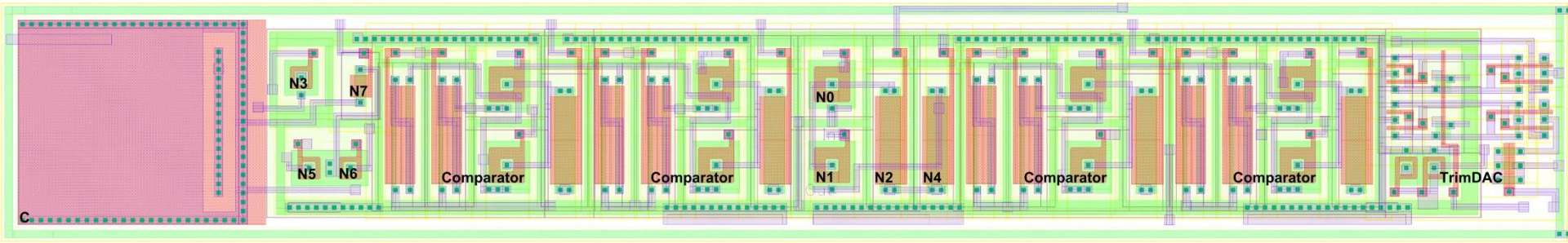


Pixel demo - Pixel schematic (stand nMOS with TW)

Pixel size is 50 µm x 250 µm



Comparator area is 21 µm x 139.97 µm

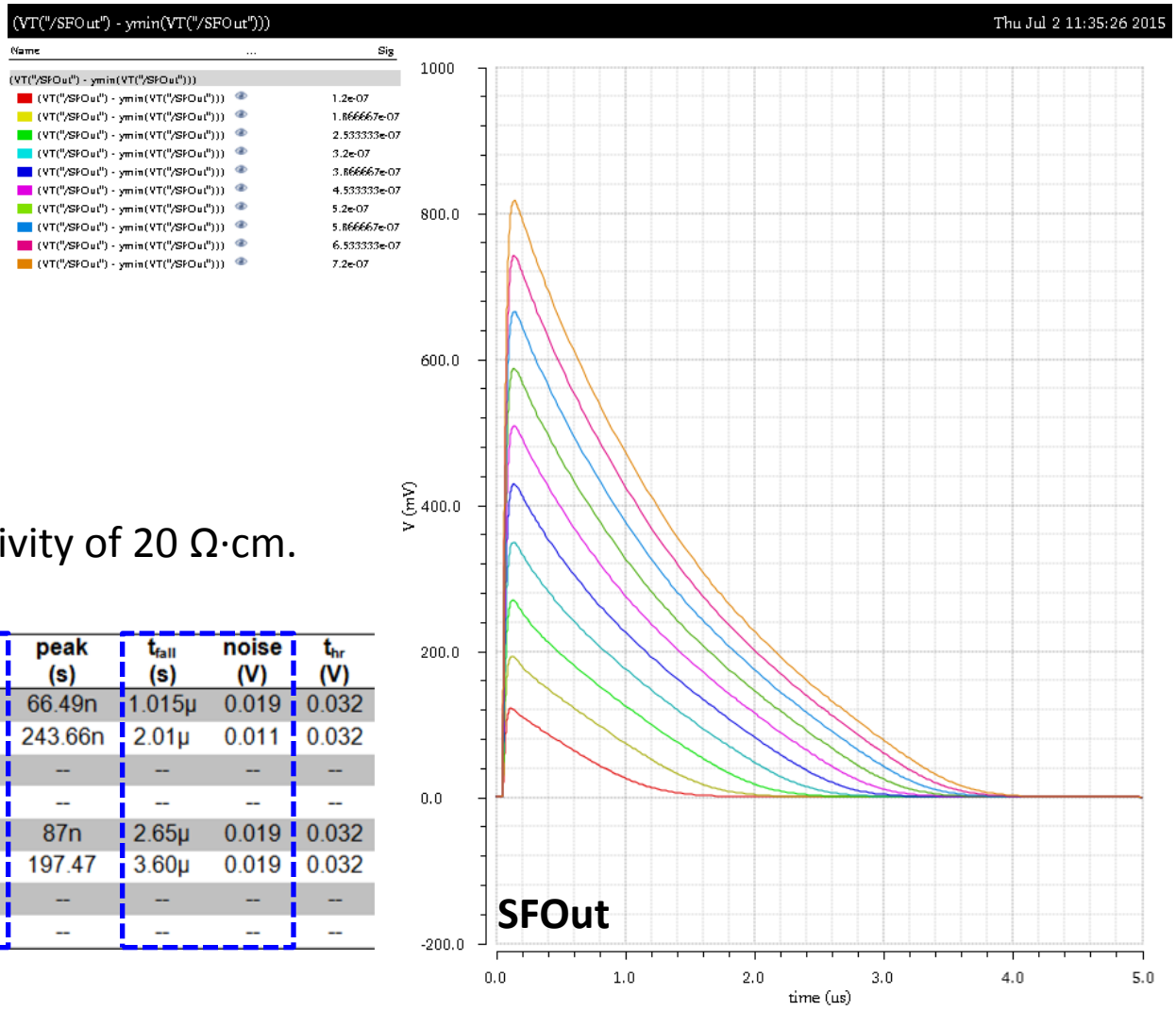


Pixel demonstrator - Simulations (analog)

	Cell	Node	V_{min} (V)	V_{max} (V)	ΔV (V)	t_{rise} (ns)	Noise (V)
Pre-layout →	ANA1	SFOut	1.30378	1.35076	0.046982	38.48	0.00463
Post-layout →	ANA1	SFOut	1.30368	1.33317	0.029492	73.14	--
	ANA1	OutB	1.83829	1.58659	0.251700	44.21	--
	ANA1	OutB	1.83903	1.68523	0.153798	75.78	--
	ANA2	SFOut	0.49654	0.58362	0.087078	24.71	0.01047
	ANA2	SFOut	0.49656	0.55297	0.056410	50.00	--
	ANA2	OutB	1.83830	1.32186	0.516440	24.98	--
	ANA2	OutB	1.83904	1.51890	0.320140	51.12	--
	ANA3	SFOut	0.49654	0.52498	0.028445	12.28	0.00390
	ANA3	SFOut	0.49656	0.51574	0.019178	26.04	--
	ANA3	OutB	1.83829	1.70113	0.137154	14.02	--
	ANA3	OutB	1.83904	1.74662	0.092413	29.66	--

- Simulations with a resistivity of 20 Ω·cm and a signal of 600 e-.

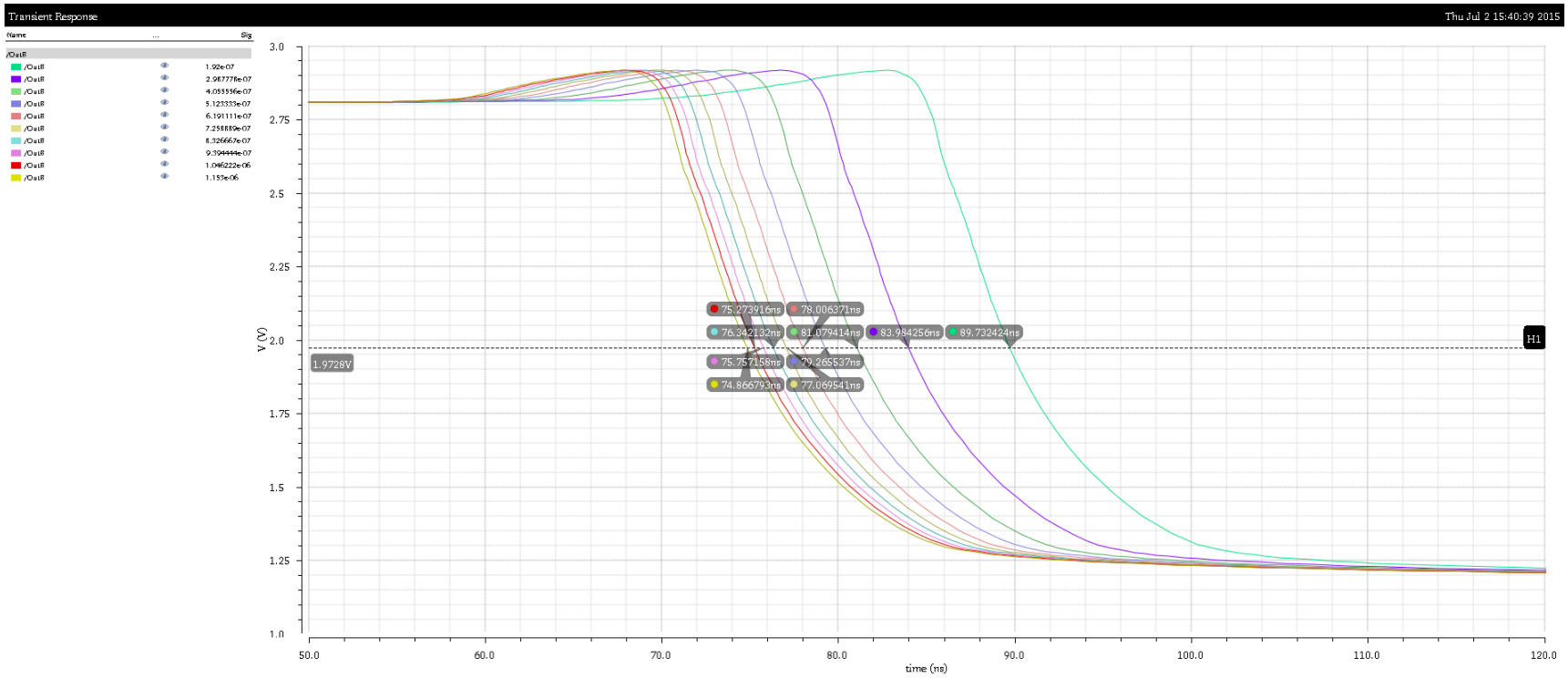
Pixel demonstrator - Simulations (stand nMOS)



- Simulations with a resistivity of 20 Ω·cm.
- Signal of 750 to 4500 e-.

Sig (σ)	Node	V_{min} (V)	V_{max} (V)	ΔV (V)	t_{rise} (s)	peak (s)	t_{fall} (s)	noise (V)	t_{hr} (V)
0.5	SFOut	0.723	0.845	0.121	33.5n	66.49n	1.015µ	0.019	0.032
0.5	SFOut	0.723	0.995	0.271	149.7n	243.66n	2.01µ	0.011	0.032
0.5	OutB	2.808	1.135	1.673	14.52n	--	--	--	--
0.5	OutB	2.809	1.172	1.636	40.21n	--	--	--	--
3	SFOut	0.723	1.540	0.816	40.19n	87n	2.65µ	0.019	0.032
3	SFOut	0.723	1.474	0.751	103.67	197.47	3.60µ	0.019	0.032
3	OutB	2.808	1.135	1.673	13.38n	--	--	--	--
3	OutB	2.808	1.170	1.638	40.82n	--	--	--	--

Pixel demonstrator - Simulations (stand nMOS)



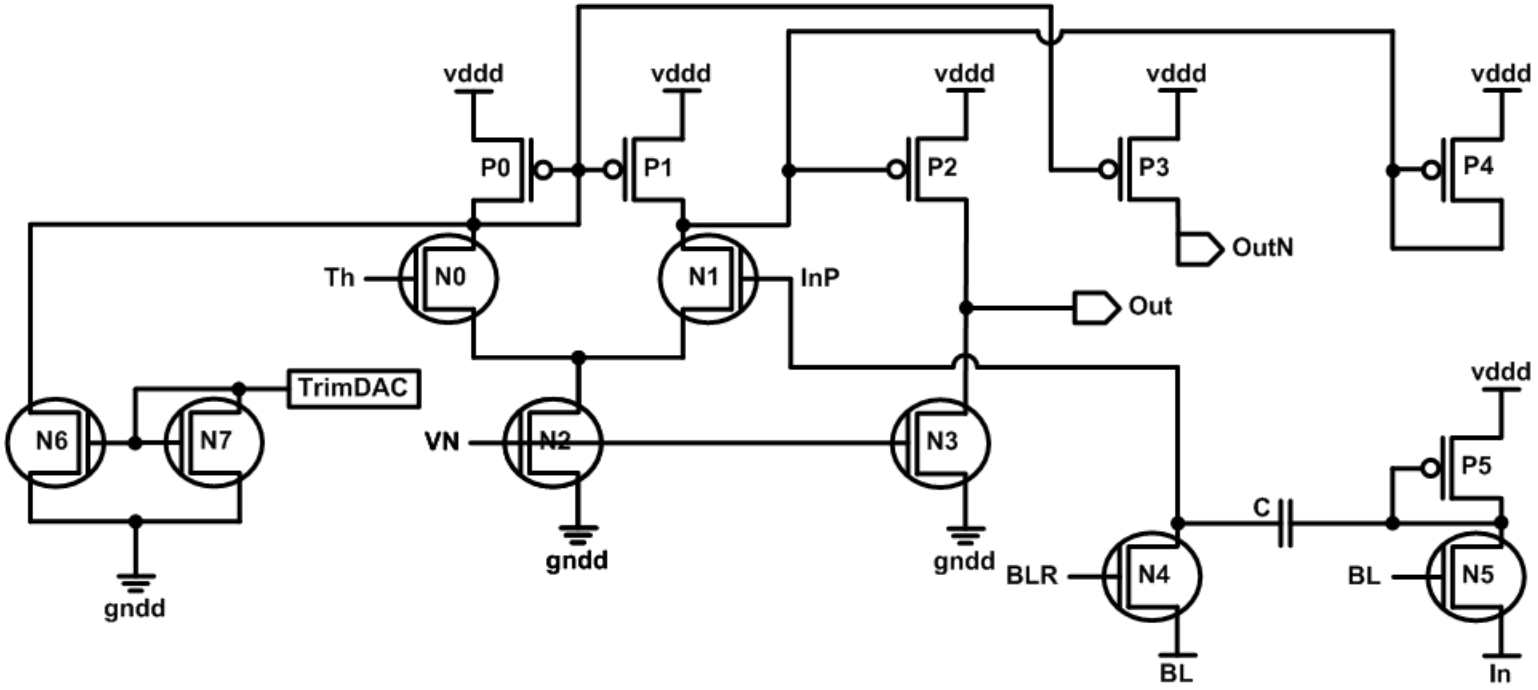
TW = 14.87 ns (Resistivity = 80 Ω·cm)

≈ 25 ns (25 ohm·cm) < TW < ≈ 4 ns (1k ohm·cm)

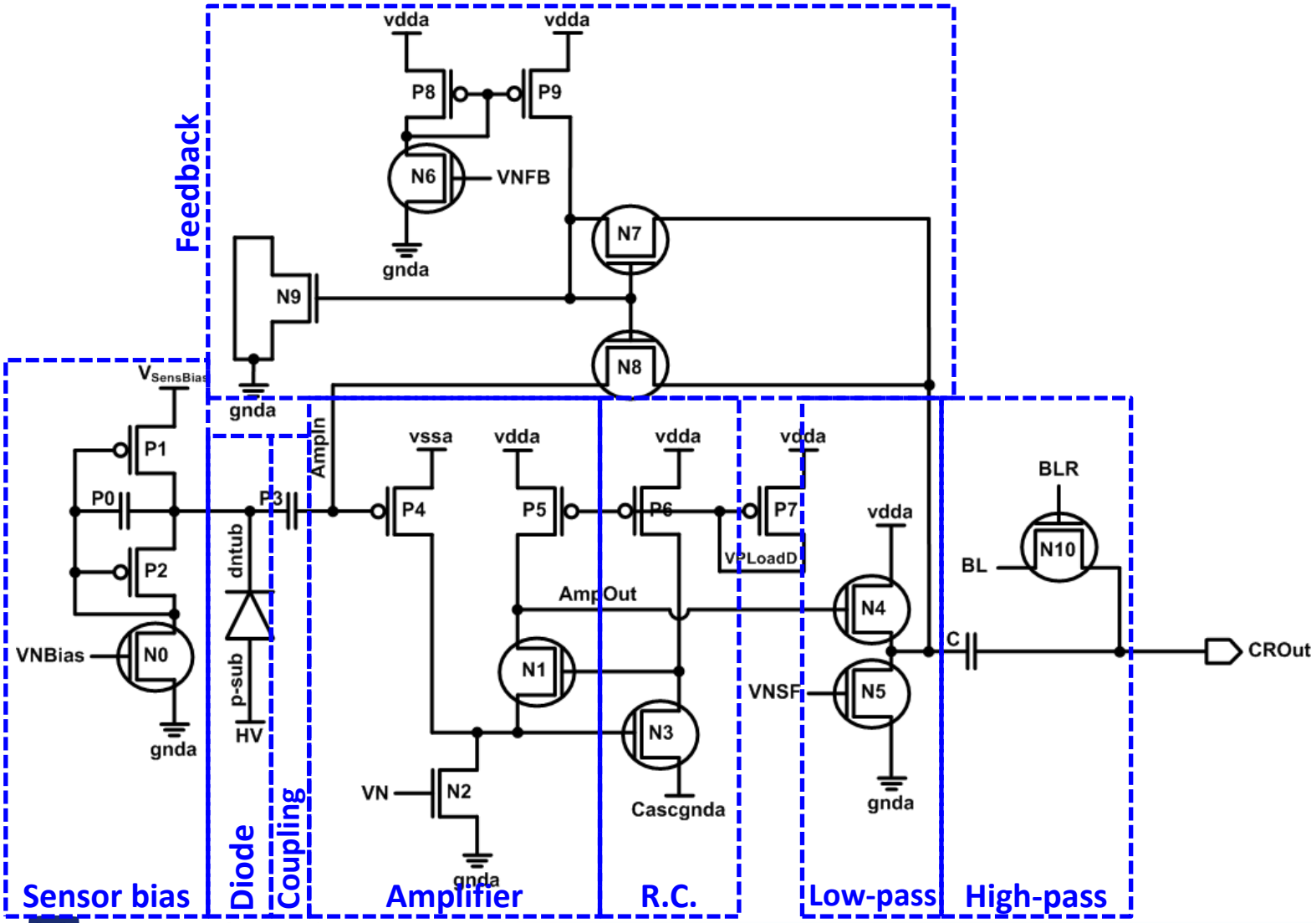
Backup slides

Pixel demonstrator - Pixel schematic (stand CMOS)

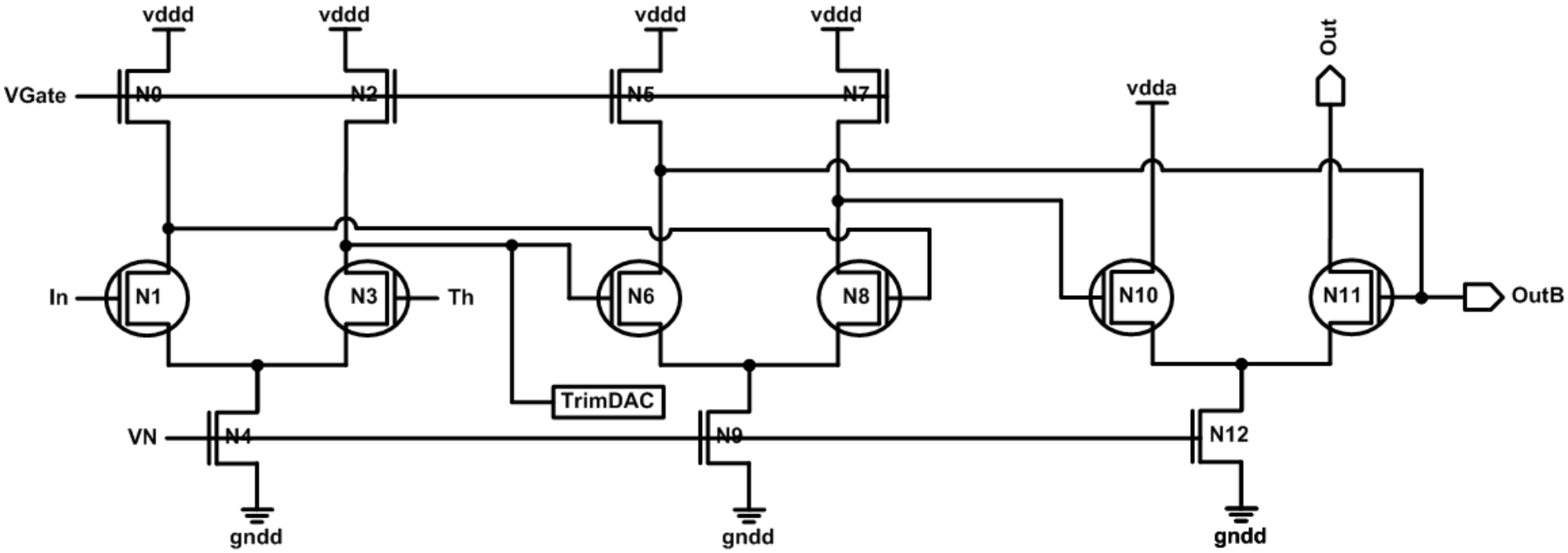
- Pixel area is equal to analog.
- Comparator:



Pixel demonstrator - Pixel schematic (stand nMOS)



Pixel demonstrator - Pixel schematic (stand nMOS)



Pixel demo - Pixel schematic (stand nMOS with TW)