B.Dolgoshein

CALICE meeting, DESY, October 12, 2005

SiPM's production, tests and long term behavior

MEPhI&PULSAR

In framework of CALICE
collaboration and ISTC project 3090

SiPM production status

1	SiPM's transferred to ITEP	~2600	
2	Ceramic plates (3x5 mm^2 ±30μm) for SiPM assemblies are ready to use	~5000	
3	SiPMs on ceramic plates+tiles for 6 cassettes + spares transferred to DESY	~1300	

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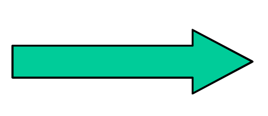
Problems

- Tests performed at DESY for first and second cassettes discovered SiPMs with long discharge (LD)
- There are ~10% SiPMs with LD at ITEP recommended voltages (working point)



SiPMs mass production and transferring to ITEP were stopped

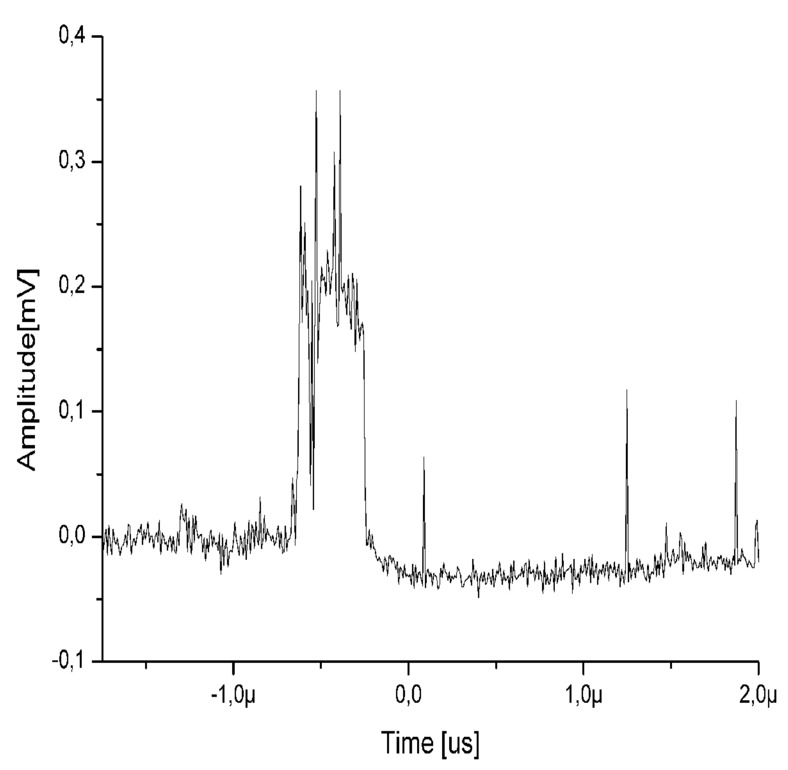
Example of long discharge signal

- Most probable reason is:

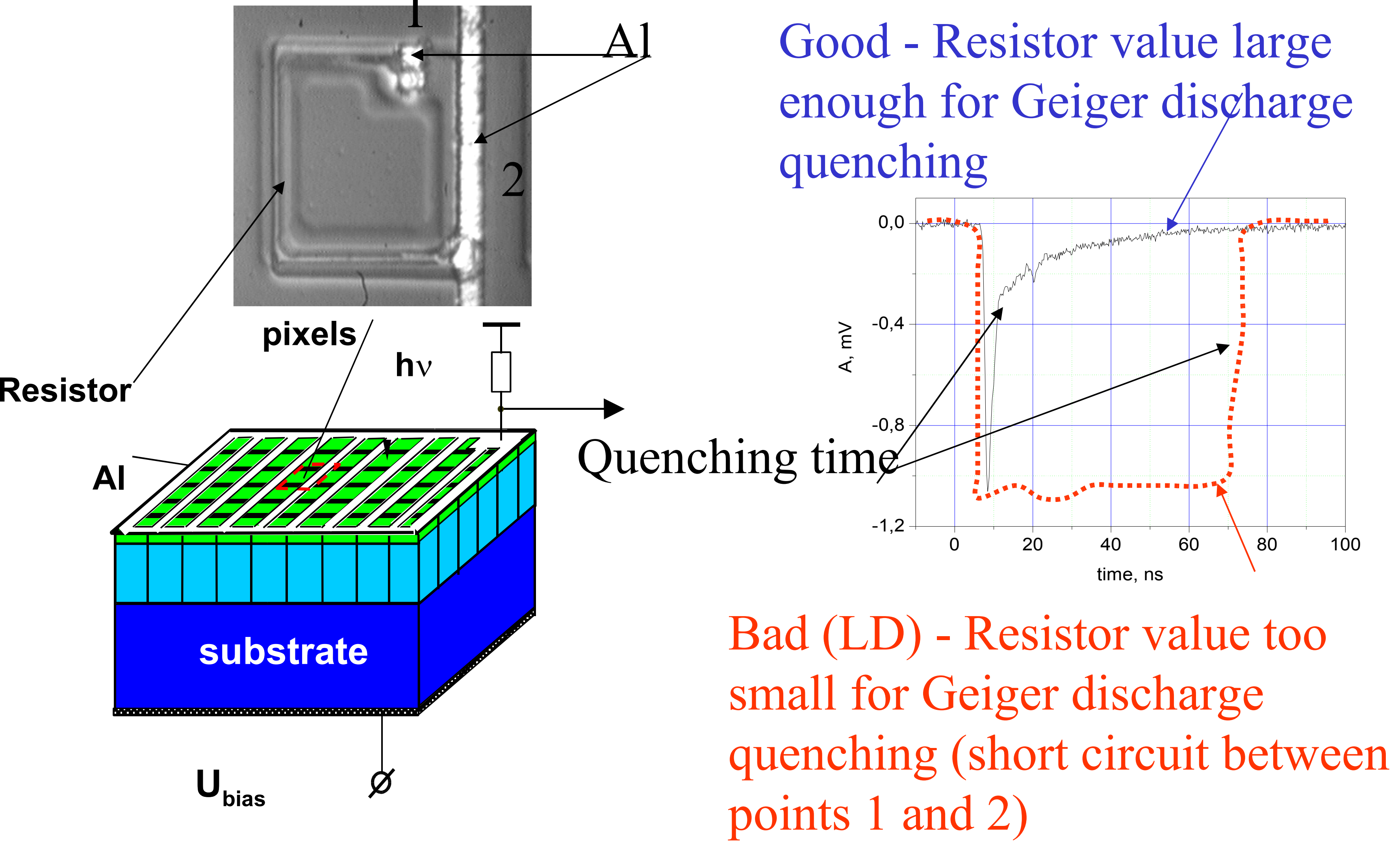
Something happens with a quenching polysilicon resistor (its value is reduced from a fev MOhm down to ≤100 kOhm for some pixel(s)

➡ quenching current rises up to ≥10μA

➡ quenching time rises up to ≥100 ns



Silicon Photomultiplier –multipixel device with common readout



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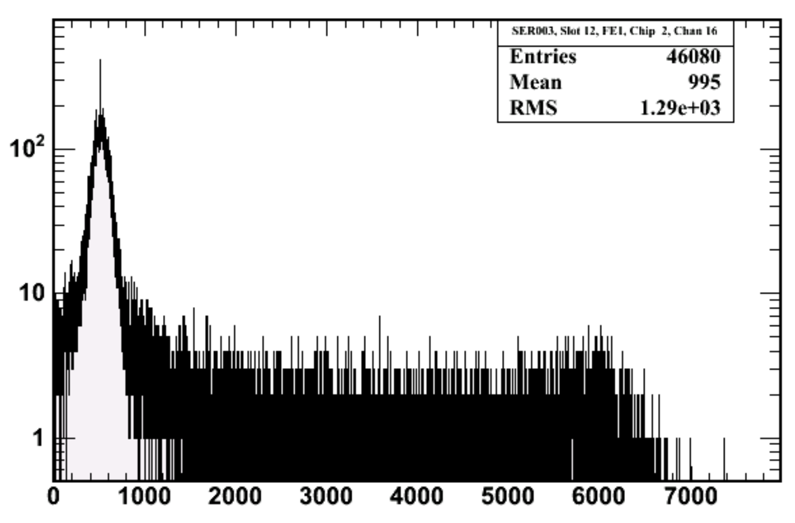
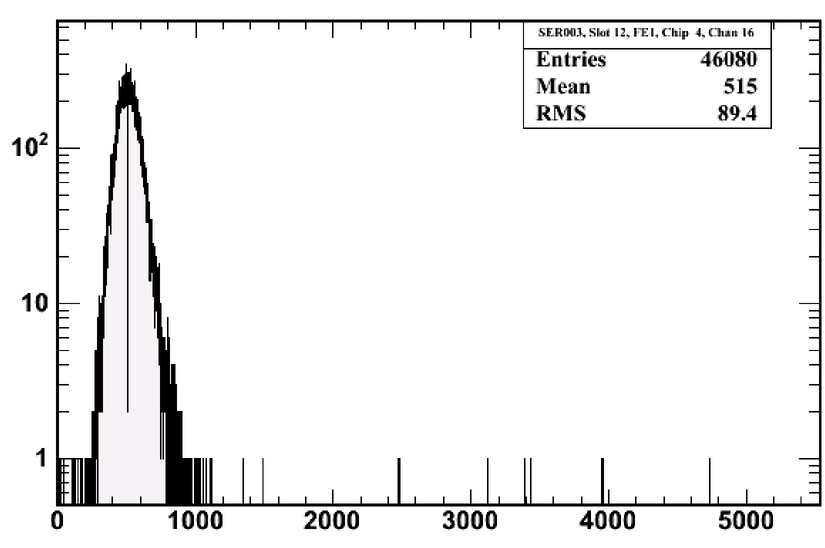
DAQ method

~50000 events collected with longest shaping time and highest gain:



High frequency LD



Good SiPM

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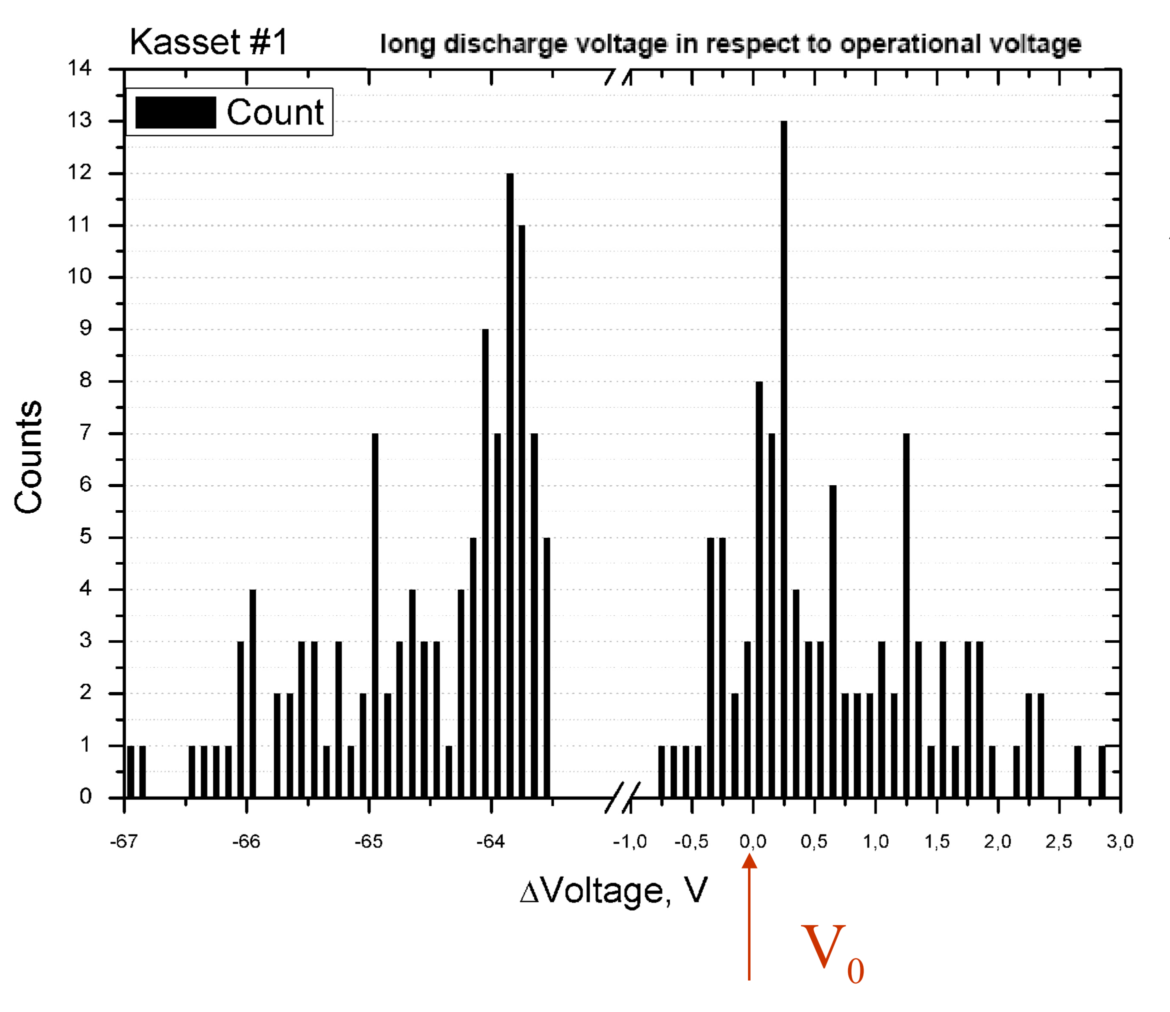
LD behavior observations: module 1

All LD are observed within 2-2.5 V over the ITEP voltage



$\Delta V = V(LD) - V(ITEP)$

Same observed in module 2

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Long discharge history

	Module 1(220 tiles)	Module 2 (220 tiles)
May	5 (scope Elena)	
Jun.	14 (DAQ)	
Jul.	-	6 (DAQ)
Aug.	61 (DAQ)	32 (DAQ)
Sep.	48 (DAQ)	21 (DAQ)

All measurement done @ ITEP voltage (+/-100mV), no temperature correction

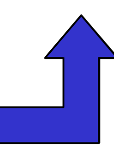
Checked correlations of LD SiPM with:

- SiPM production number
- nominal bias voltage (ITEP value)
- gain
- current at nominal voltage
- position in the cassette
- electrical channel

!Strongly overvoltage dependent!

➔No evidence of correlation found yet for both modules

➔No evidence of long term behavior of LD because of



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LD signature:

High level dark current at V_0+ (3…5)V

current measurements at different voltages

Module 1, V0+5, I μA

Module 1, V0, I μA

200
150
100
50
0

0
0.5
1
1.5
2

All SiPM with LD

All good SiPM

LD:possible origin

- **<u>SiPM production procedure:</u>**

<u>List of main operations</u>

4. SiPM on wafer production
6. Wafer cutting (SiPM 1x1 mm^2)
8. Mounting on precision ceramic plate+bonding+(protective layer)
10. Mounting into the tiles (ITEP)
12. Soldering in the module

- **<u>Tests</u>**

SiPM on wafer testing before cutting (fig) with probe station

MEPhI test

1LD/24SiPM's , V_0+2V, one months

Initial test with LED (ITEP)+Long term stability test (ITEP) (fig):

-10-15% of 230 have a big dark current+or does not work

-2LD/230 SiPM, 3 weeks, V_0+4V

Test at DESY:

10% LD at V_0 ; 50% LD at V_0+2.5V

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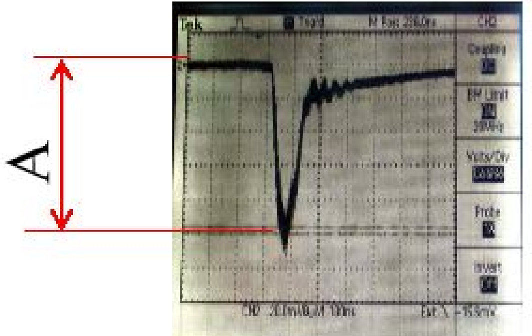
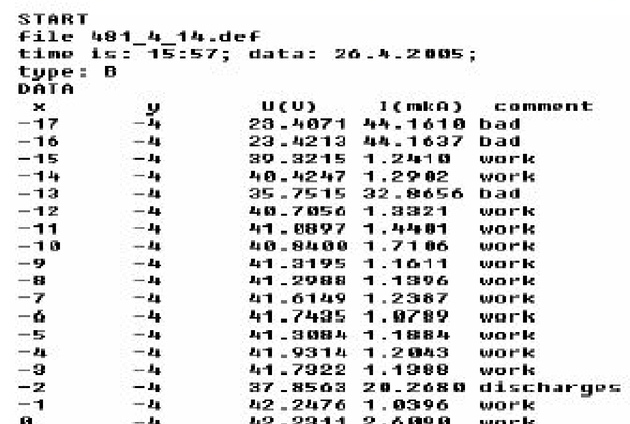
PULSAR semiautomatic probe station for the initial SiPM selection on the uncut wafer

Selection criteria

- Proper Geiger signal to the LED pulse
- For operational voltage when SiPM response has amplitude A SiPM current should be less then certain value

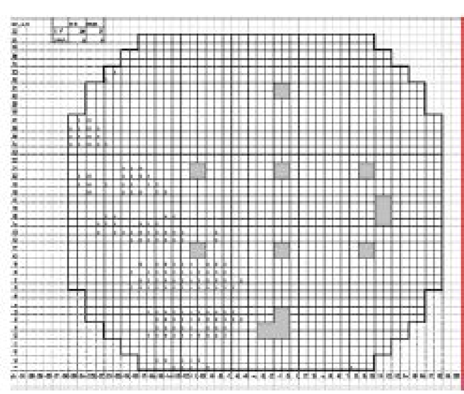




START
file 401_4_14.def
time is: 15:57; data: 26.4.2005;
type: B
DATA

x	y	U(V)	I(mkA)	comment
-17	-4	23.4071	44.1610	bad
-16	-4	23.4213	44.1637	bad
-15	-4	39.3215	1.2410	work
-14	-4	40.4247	1.2902	work
-13	-4	35.7515	32.0656	bad
-12	-4	40.7056	1.3321	work
-11	-4	41.0897	1.4401	work
-10	-4	40.8400	1.7106	work
-9	-4	41.3195	1.1611	work
-8	-4	41.2988	1.1396	work
-7	-4	41.6149	1.2387	work
-6	-4	41.7485	1.0789	work
-5	-4	41.3084	1.1884	work
-4	-4	41.9314	1.2043	work
-3	-4	41.7922	1.1980	work
-2	-4	37.8563	20.2680	discharges
-1	-4	42.2476	1.0396	work
0	-4	42.2911	2.6090	work

Selection map

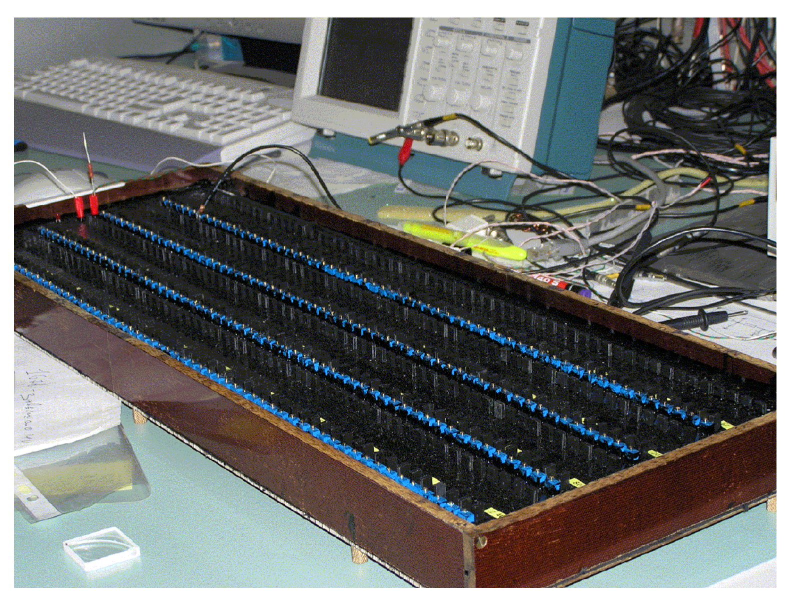


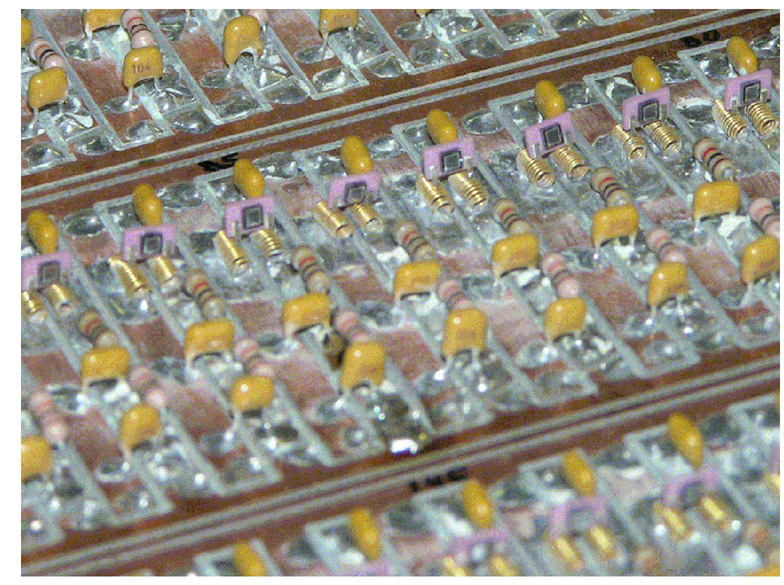
Max rate - 1000 SiPMs/day

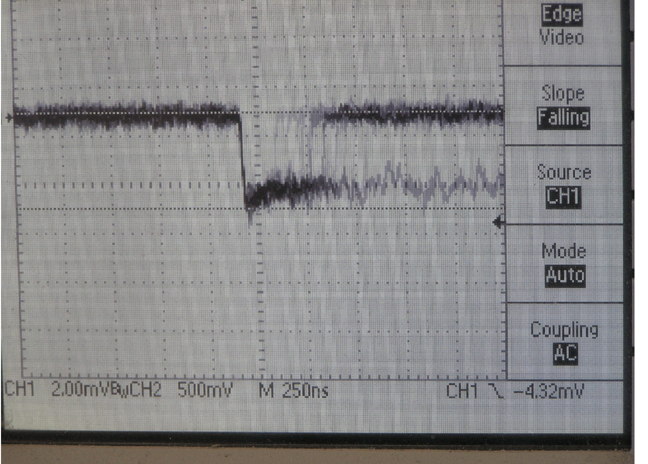
Long term stability

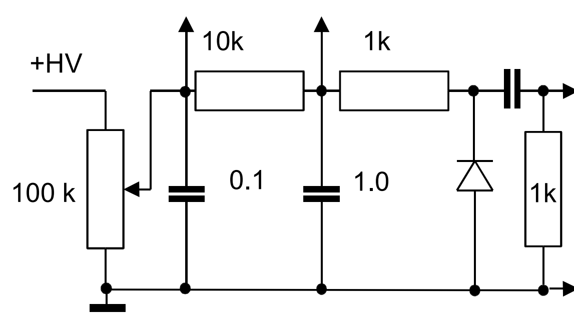
We have now the set-up to reject SiPM's after long term test (240 channels).

Individual bias voltage setting for each channel, outputs for current and pulse shape monitor

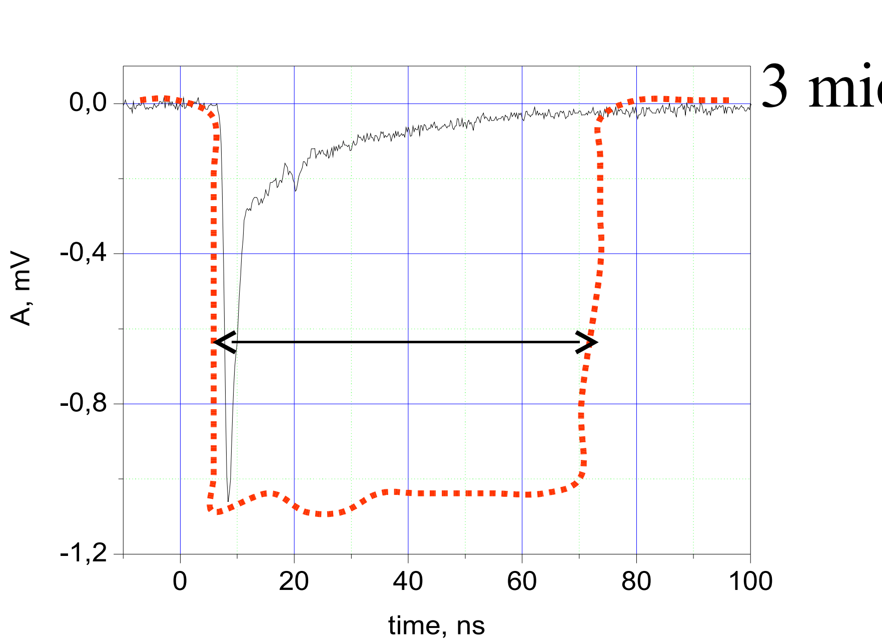


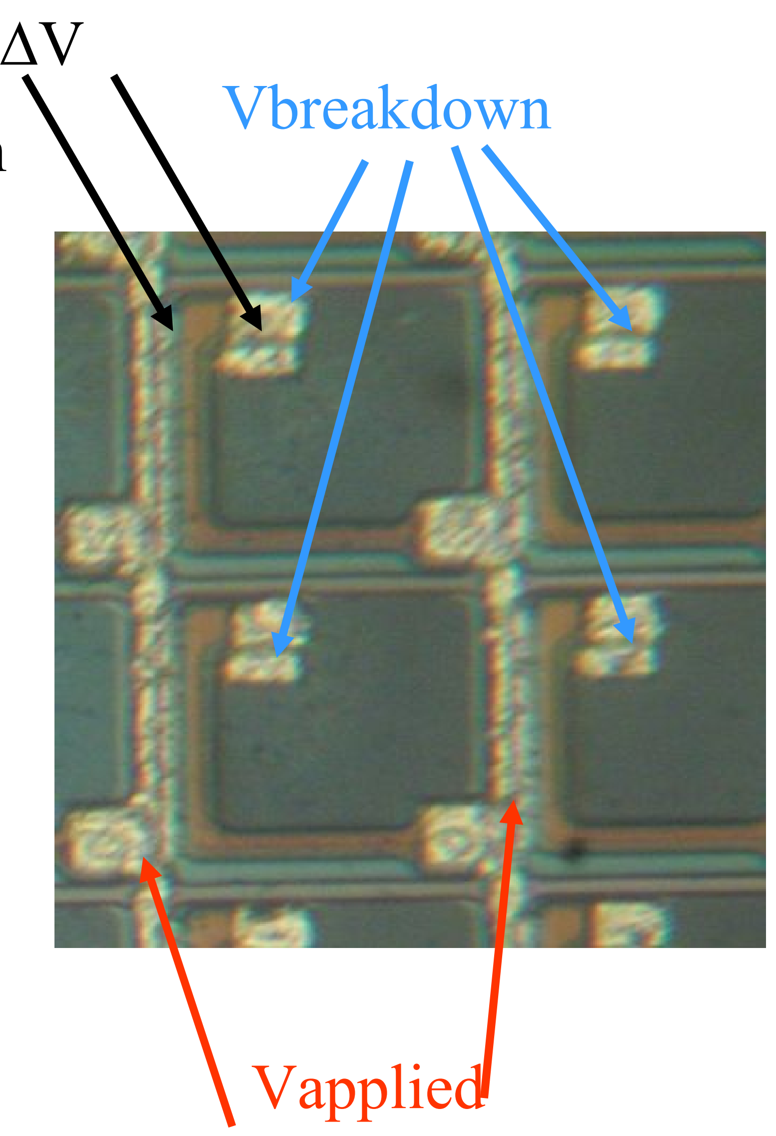






The study of LD origin





Random pulse length strongly increases with increasing of overvoltage

ΔV=Vapplied - Vbreakdown

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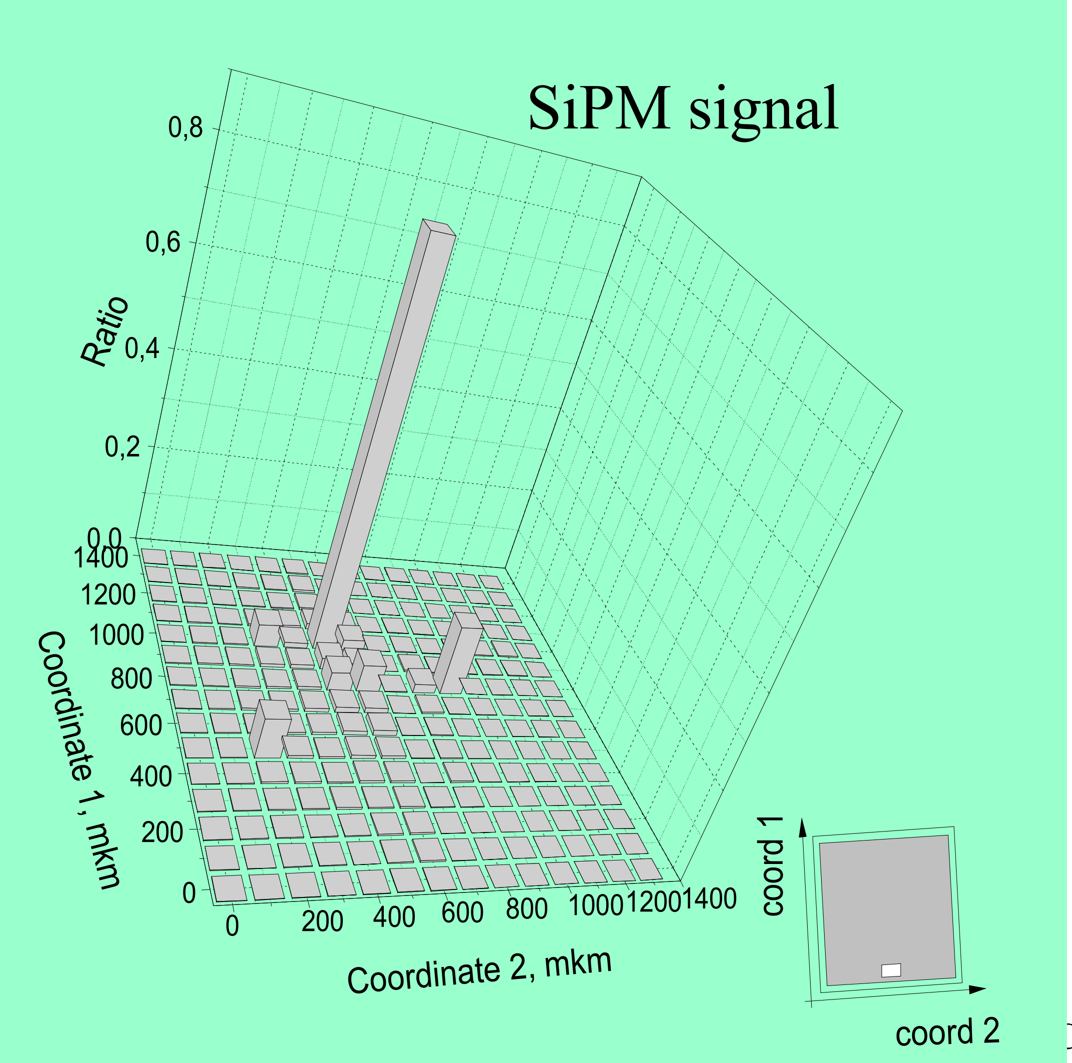
The special setup developed at MEPHI for scanning of the SiPM.

LED, optical fiber, step 100 micron



Localization of the problem region and investigation under microscope

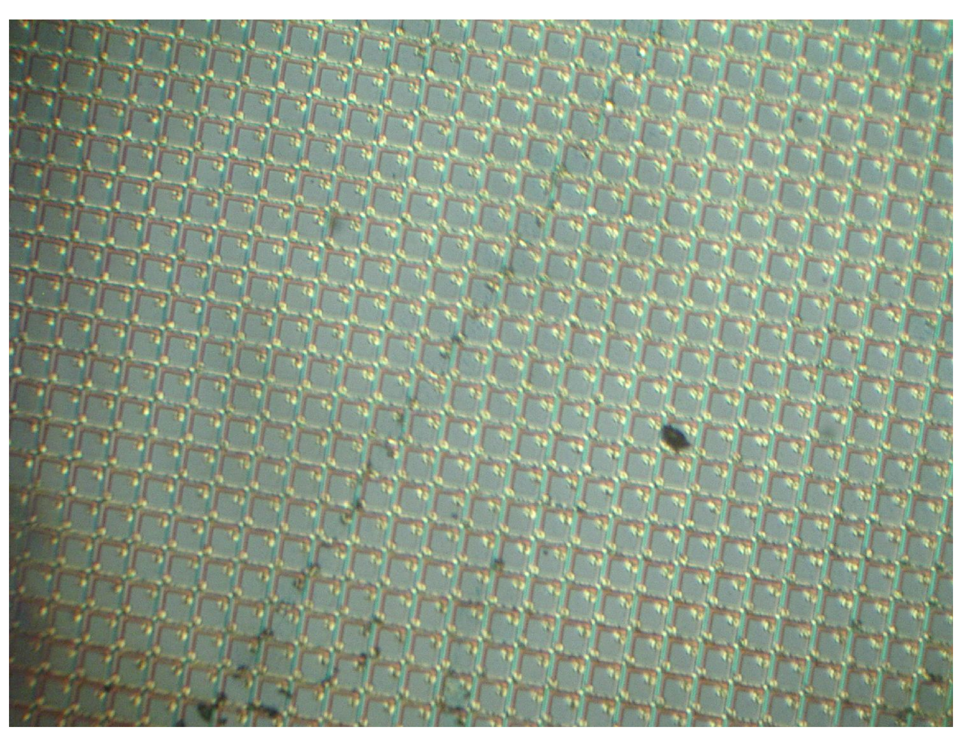
After scanning it became clear – Long Discharge come from local area – from 1 or few pixels

CE

ct 3090

Died SiPM (no signal and big current)

SiPM 2591



Big scratch

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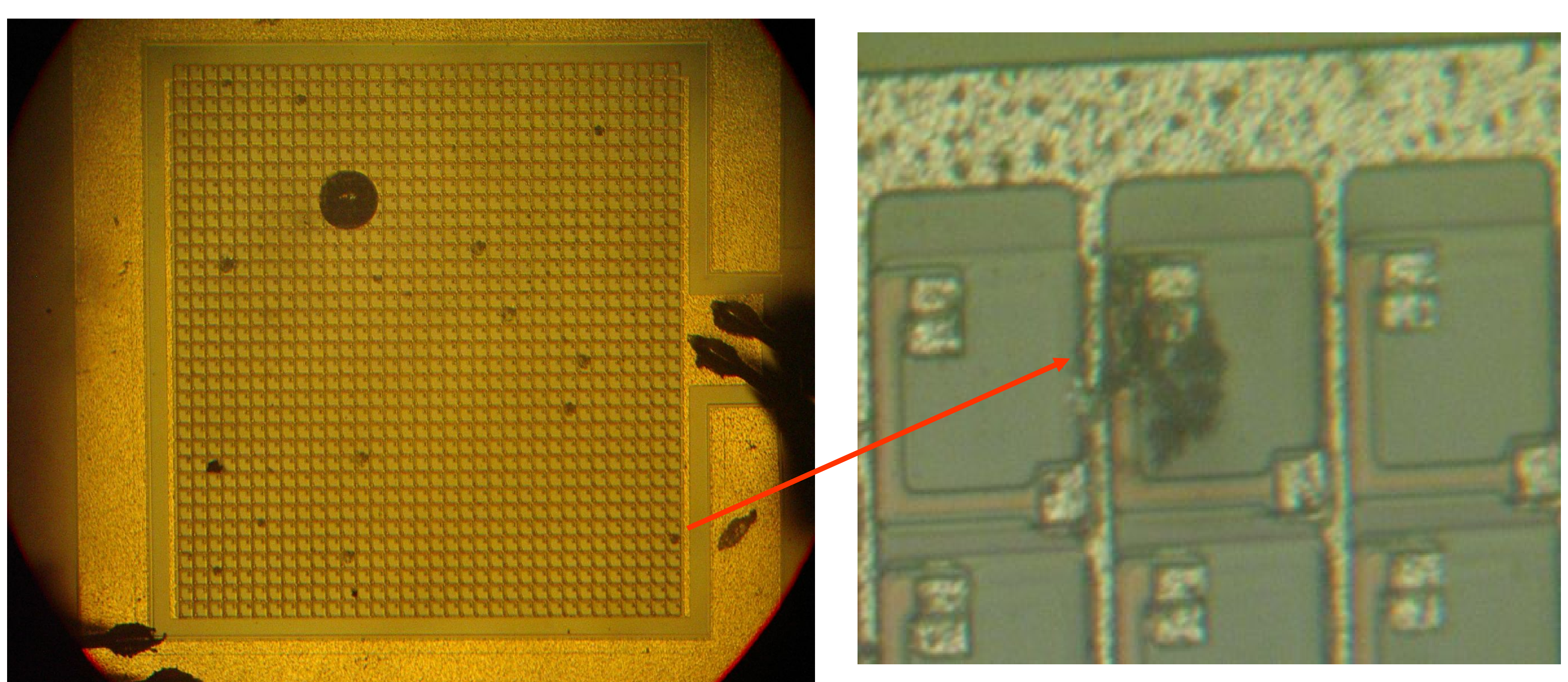
Died SiPM (no signal and big current)



Discharge between resistor and Al bus.
Damage of resistor and short circuit

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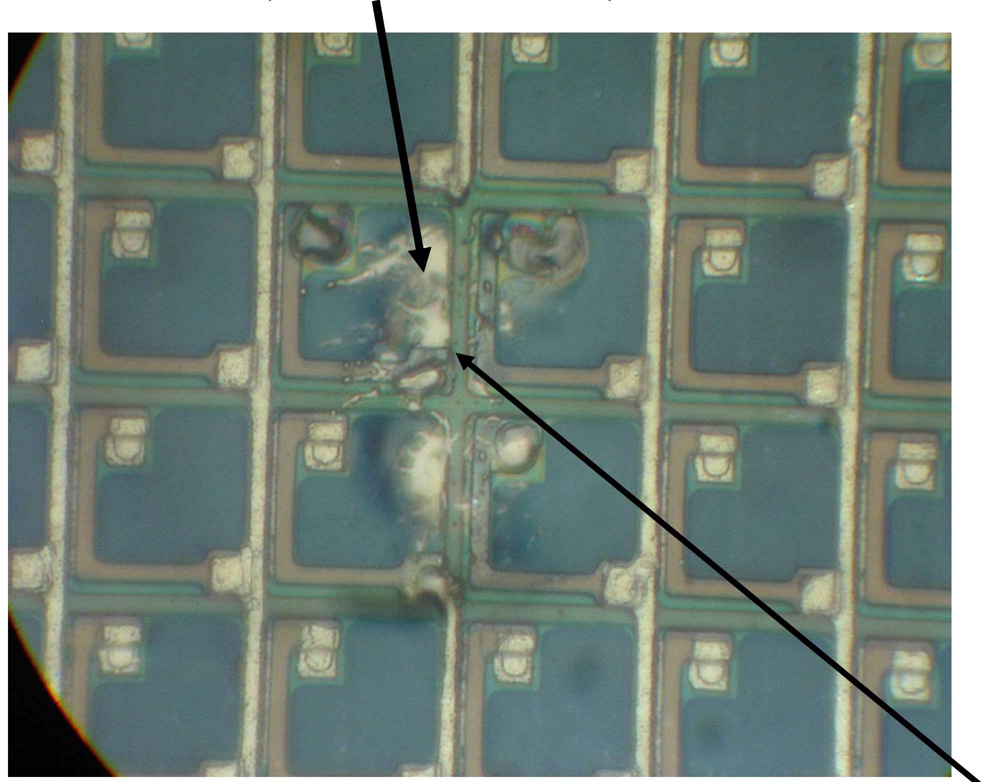
Another example of damages due to resistor-Al bus discharge

Al (short circuit?)



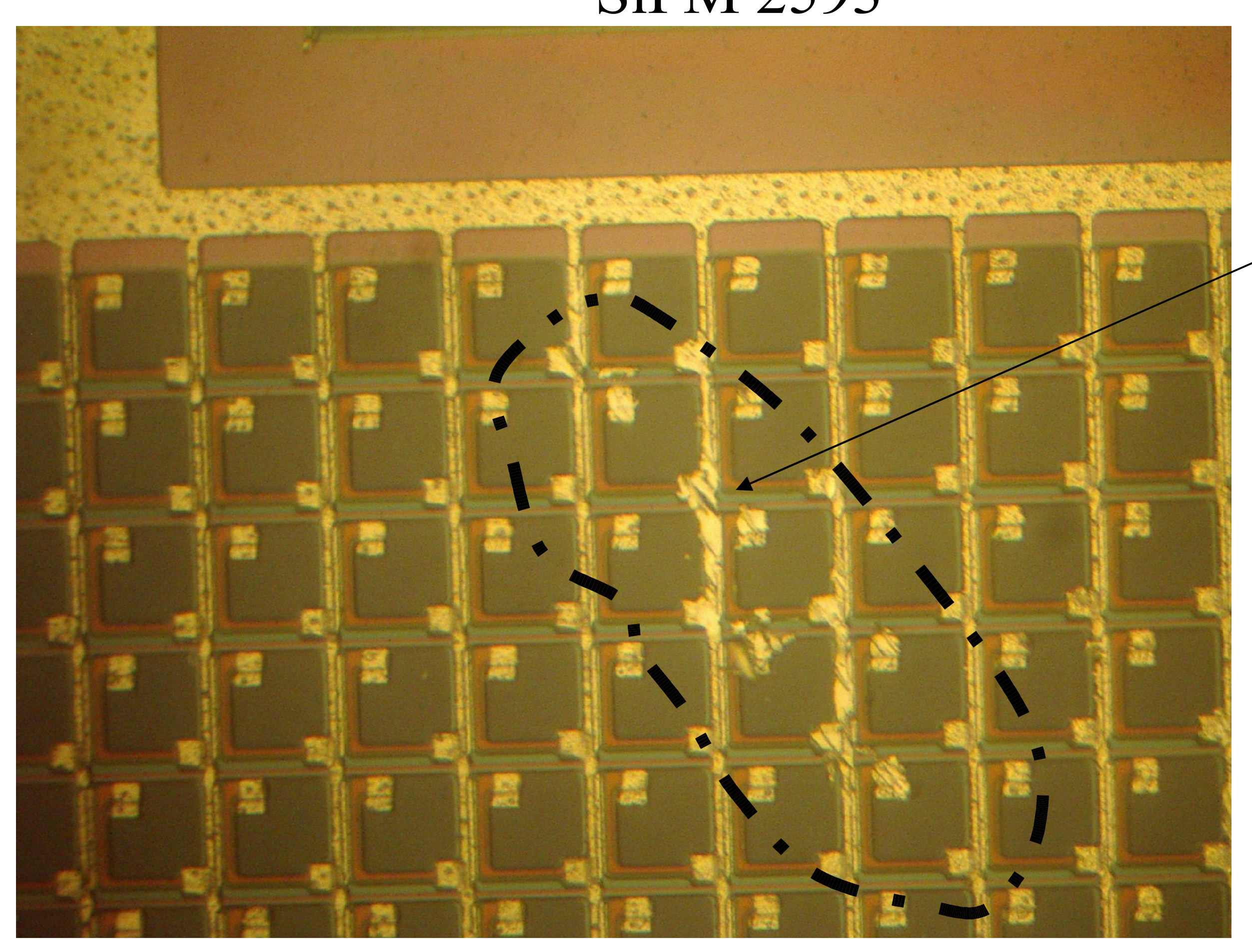
Such damages can appear as a result of

- big overvoltages for reverse bias
- High voltages for direct bias

No Al bus

SiPMs with LD were scanned and investigated under high gain microscope

SiPM 2593



LD area

Al short circuit due to scratch

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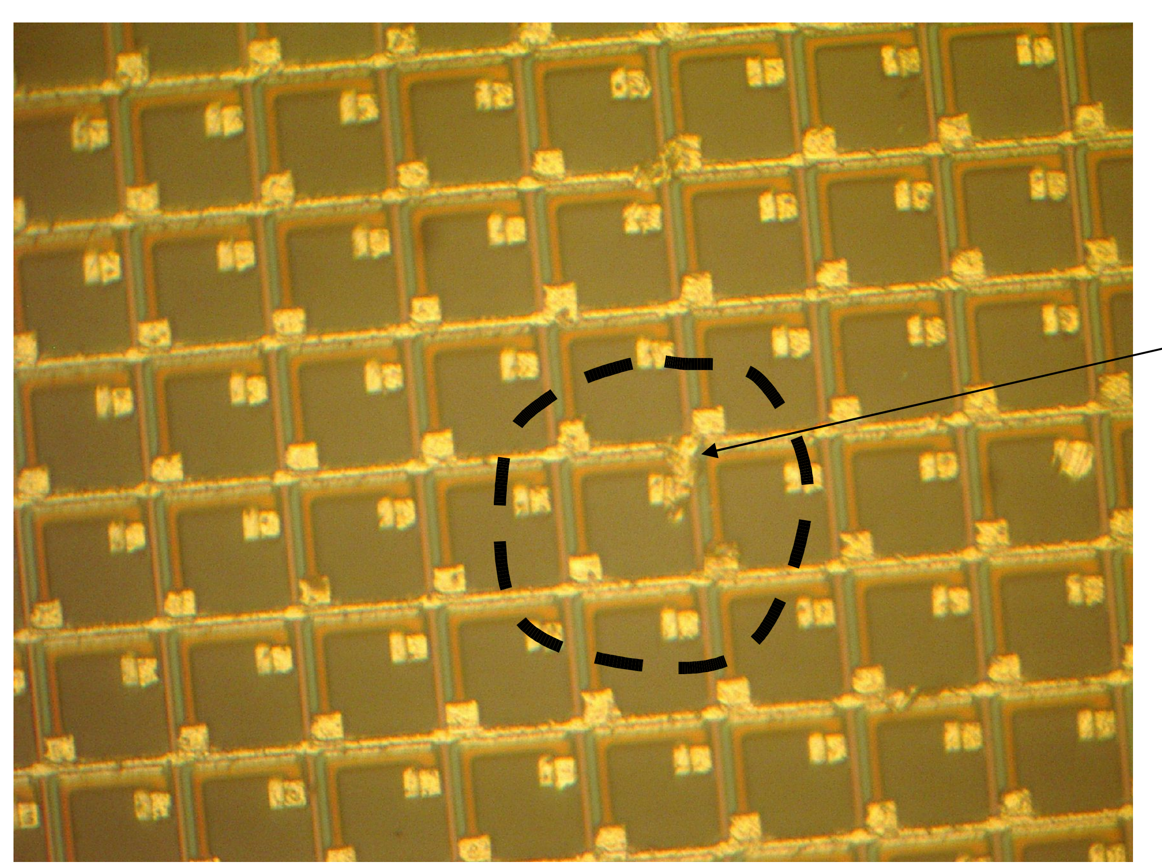
SiPMs with LD were scanned and investigated under high gain microscope

SiPM 2634



Pixel with LD

Al short circuit due to point like defect

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Conclusions:

1. SiPM is very sensitive to damaging during production and assembling operations.

   Actually each SiPM consists of ~1000 local points with very high electric field $3*10^4$ - $3*10^5$ V/cm.

2. There are a strong indication of SiPM surface damaging during production and assembling stages and also technological imperfections, which can lead to short circuits between Al buses and polySi resistor.

   ⟹ Now SiPM’s modification with additional SiO_2 layer for Al-polySi resistor isolation is under study.

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Conclusions:

3. We hope that we understand the main reason for LD problem so, the LD problem is close to be solved now in cooperation with ITEP and DESY

- We are checking all stage of SiPM production and assembling
- We are going to modify the SiPM selection criteria (MEPhI/PULSAR+ITEP+DESY)

SiPM mass production will be continued after checking the new selection methods (Nov 05)

Our plans for SiPM's production

	Oct 05	Nov 05	Dec 05	Jan 06	Feb 06	Mar 06	Total amount
SiPMs on wafer First batch	~ 10000						
SiPMs on wafer second batch							15000
Ceramic plates	~ 5000						13000
SiPM's on ceramic plates to ITEP	~2600						5000

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