

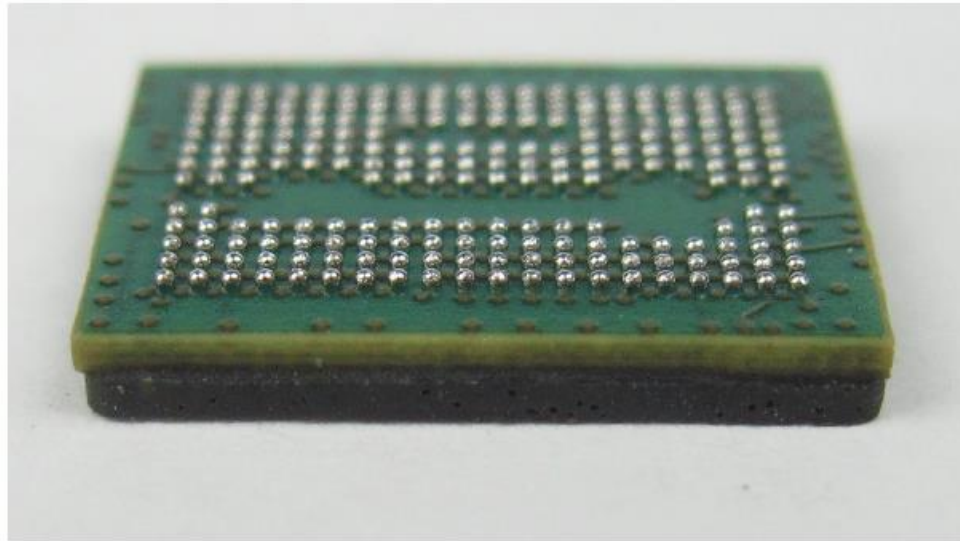
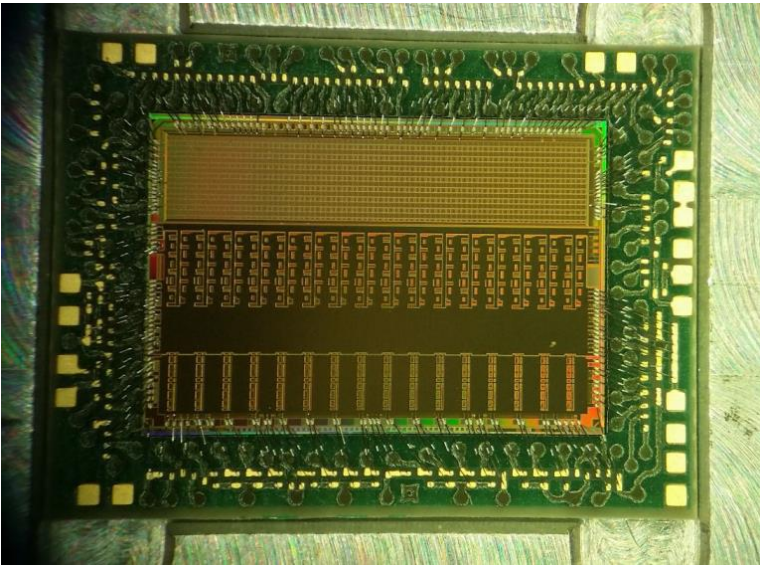
# Status of the TPC readout electronics

Status 9.2.2017

Leif Jönsson  
(representing the Lund group)  
Lund University

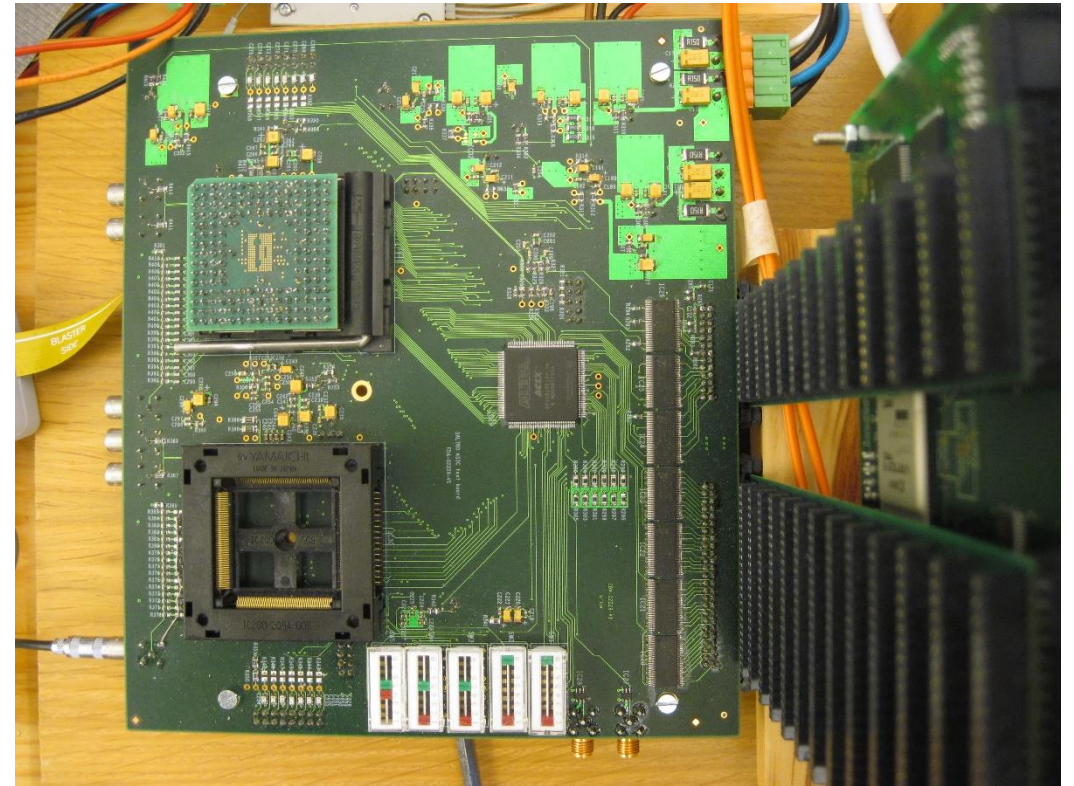
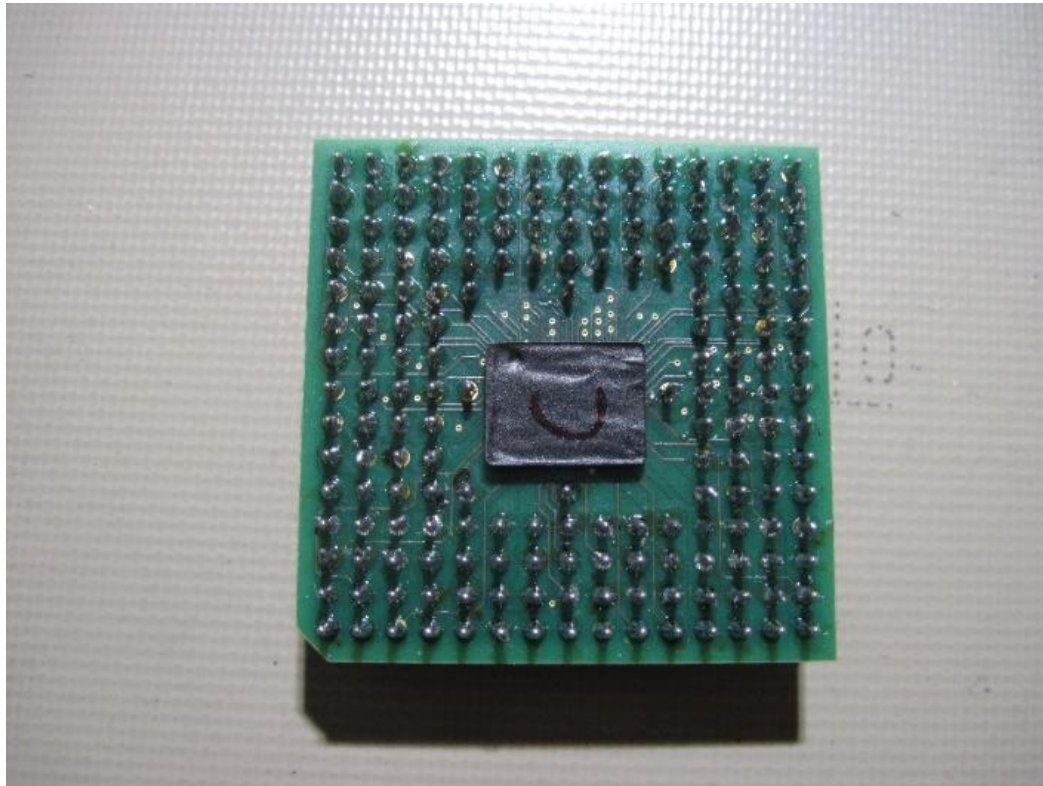
## History and present status:

- The SALTRO-chip, which integrates the analogue and digital processing in the same chip, is developed at CERN (size  $8.7 \times 6.2 \text{ mm}^2$ ).
- As we started the project there was no company which could offer packaging of the die in a small enough capsule ( $12 \times 9 \text{ mm}^2$ )  
⇒ Develop a carrier board onto which the die could be mounted.



## Test set-up with adaptor board

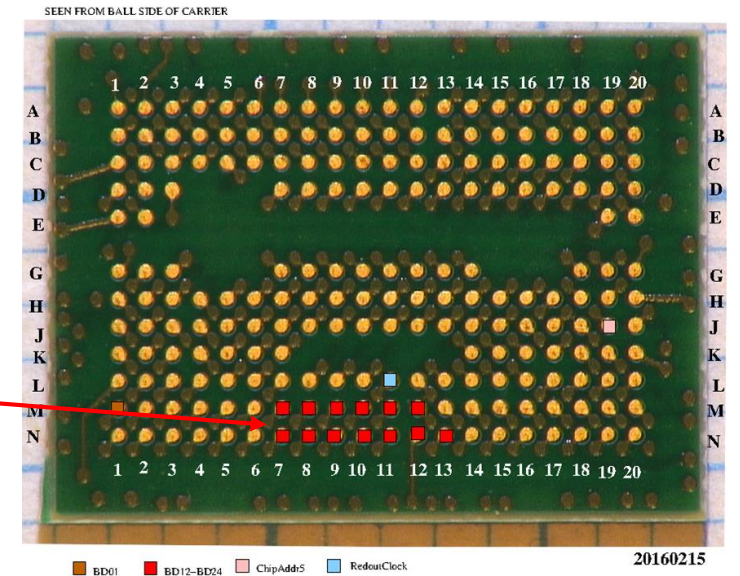
In order to test the functionality of the carrier board an adaptor board was designed onto which the carrier board was soldered. This adaptor board was plugged in on the CERN test board.





## Result of the 5th bonding trial:

- After bonding of the die tests were performed and all connections were confirmed.
- After application of the epoxy glob and the tin balls the connections were tested again and everything was ok.
- After soldering onto an adaptor board, for characterization, some connections were lost.

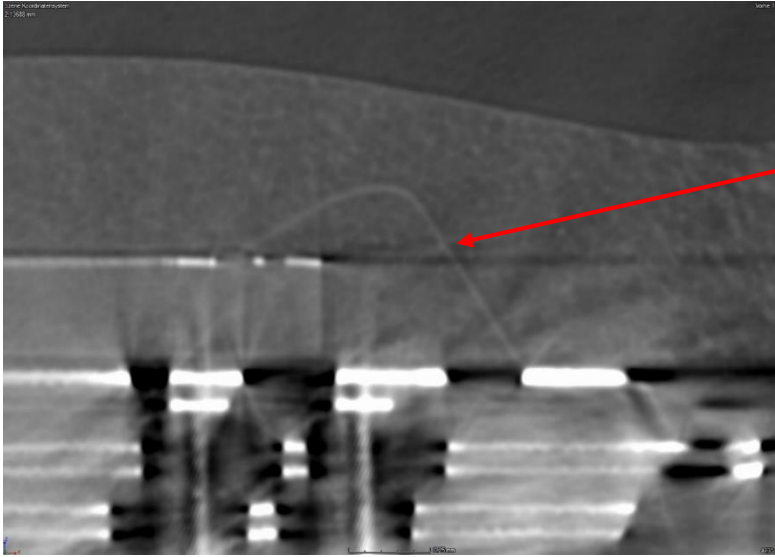


In order to find out what had happened we had the board **investigated by X-ray**.

At PETRA they have equipment for X-ray tomography

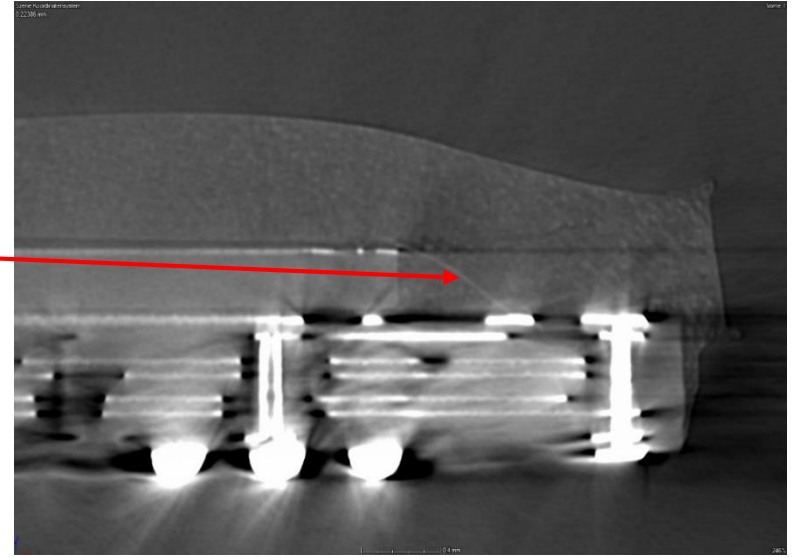
- 1st attempt: an Al-filter from the previous user had not been removed
- 2nd attempt: no bonding wires could be identified

⇒ Contact with **Fraunhofer Institute** in Izehoe

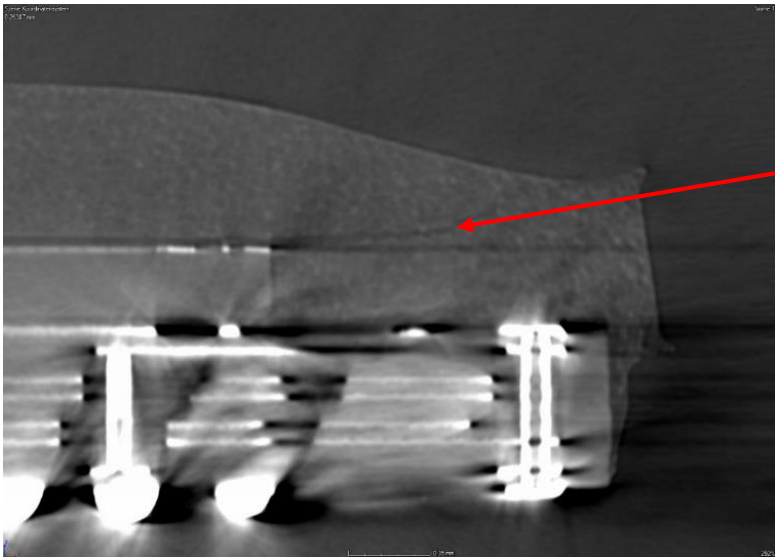


Normal bonding loop

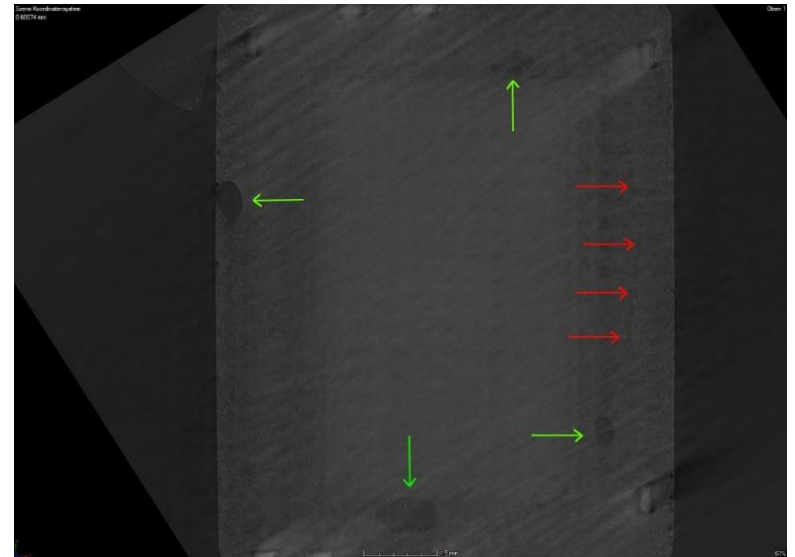
Bond wire without a significant loop



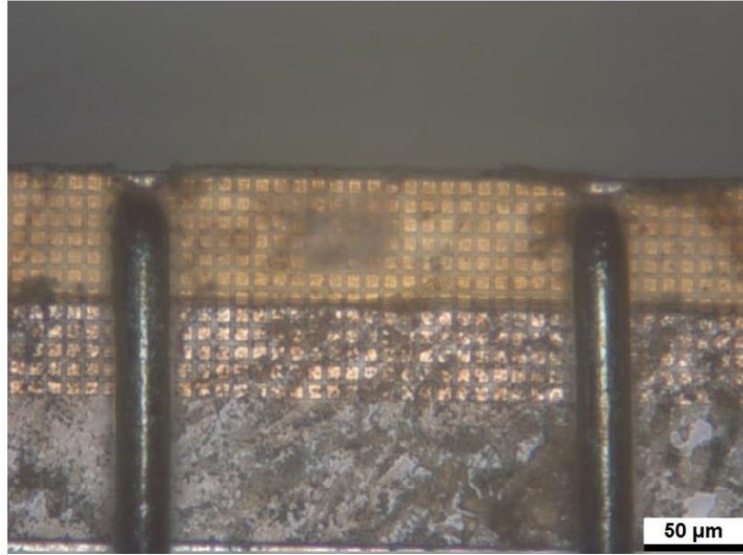
### Another important observation:



Cracks in the epoxy (red arrows) and air bubbles (green arrows).



In order to find out what impact this had on the bond wires it was decided to etch away the epoxy glob

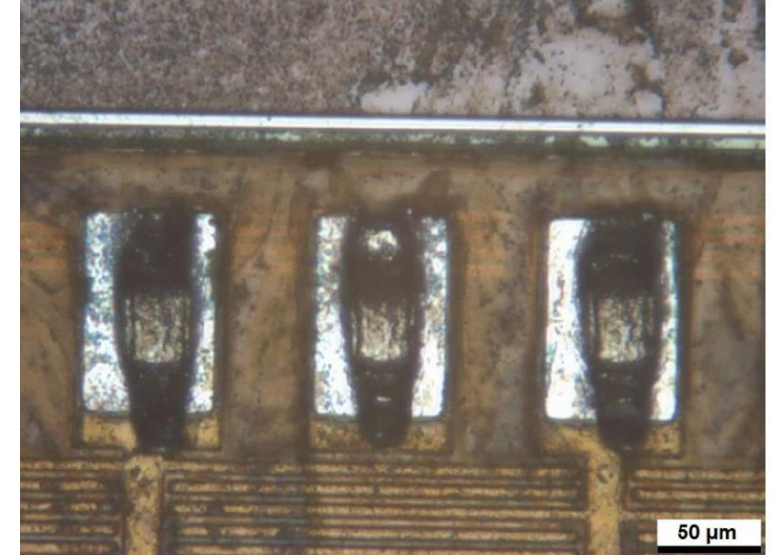


Left hand side picture:

The bond wires have been torn off at the edge of the chip. You may also notice that there is notches at the edge of the die.

Right hand side picture:

Some bond wires are broken already at the soldering point.



## Conclusion:

- There is nothing indicating an error in the design of the carrier board.
- The lost connections are due to the different expansions of the PCB and the epoxy material in the soldering process, which causes breaks in those wires where the wire loop is not sufficiently high.
- Another disadvantage of this method is that the surface of the epoxy layer is not flat enough to provide efficient cooling.

Possible way out: we have found a 3-D printing system which produces capsules with sufficiently thin walls to fit our carrier board.

## ON THE OTHER HAND

We have recently identified a company which claims that they can package our dies in a capsule of  $12 \times 9 \text{ mm}^2$ . An order has accordingly been submitted on a test sample (30 - 35 pieces).

**Consequence:** The design of the MCM-board, which was essentially ready for mounting of the carrier boards, has to be modified, dependent on the design of the substrate for the packaging.

**The DAQ system** is being developed using a prototype MCM-board, containing a single SALTRO-chip in a TQFP-package. Readout of data and configuration has been tested and is working. It, however, has to be improved and then implemented in a full DAQ system.