An SOI Monolithic Pixel Detector for Fine Measurement of Space and Time for the ILC Experiment

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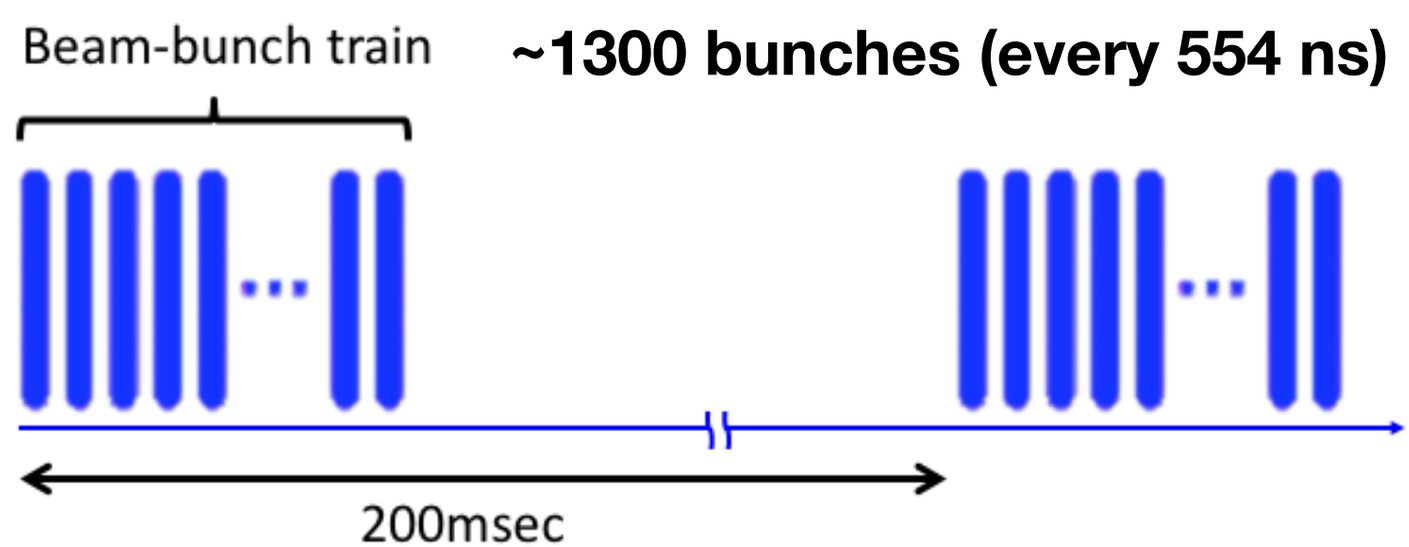
ILC Vertex detector

Requirements:

1) Single point resolution: better than 3 μm
   Pixel size: ~20 × 20 μm^2
2) Time resolution: single-crossing (554 ns interval) time resolution
3) Detector occupancy: < 2 %
4) Low material budget: $X \leq 0.1 - 0.2$ % X_0 / Layer
   corresponds to ~ 100 - 200 μm Si, including supports, cables and cooling
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year

We are designing and evaluating prototype pixel sensor with SOI technology to fulfill the requirements.



ILC TDR v4 Detector
LC Vertex / Tracking R&D 2nd Nov. 2015

SOI Pixel Detector

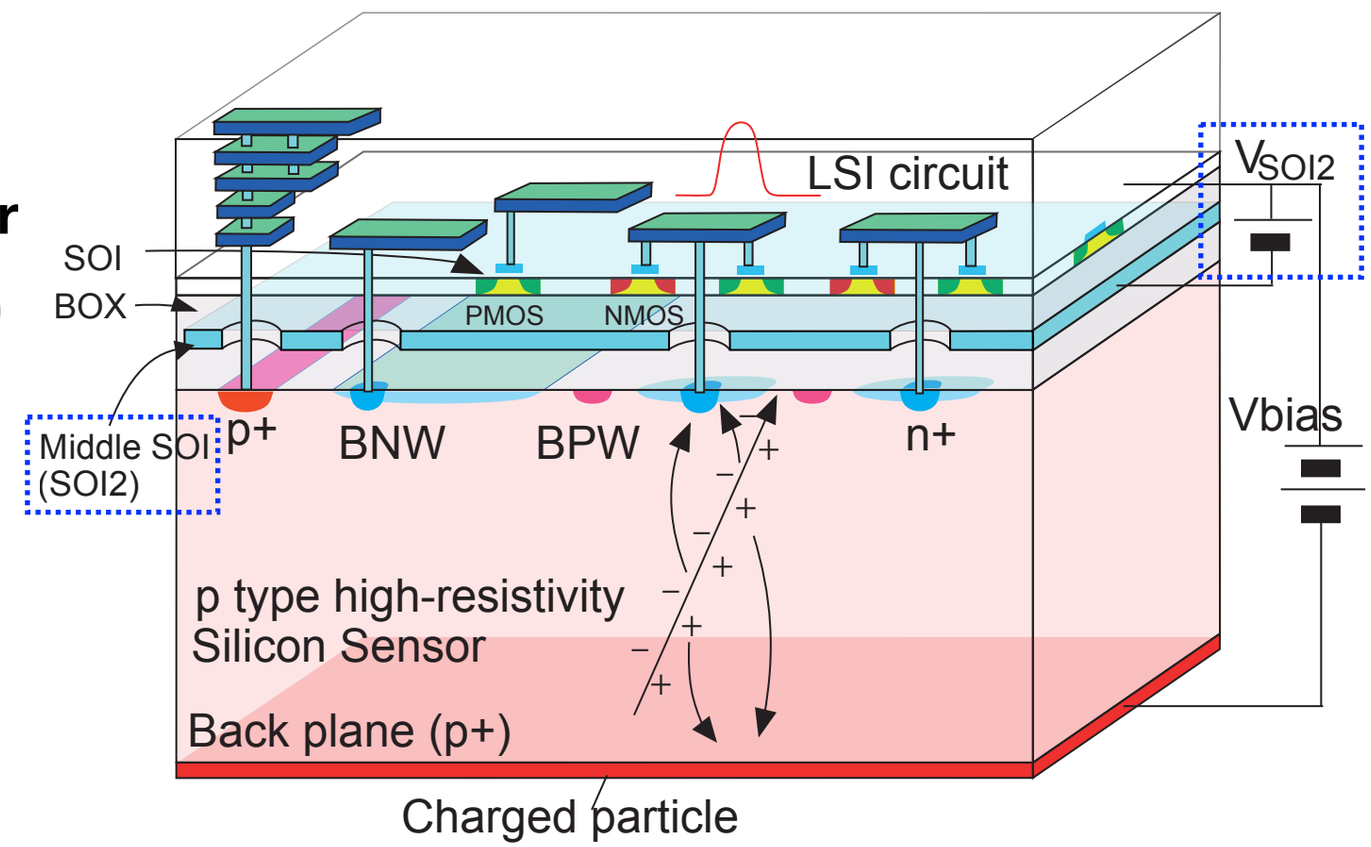
SOI: Silicon-on-Insulator technology

Utilize 0.2 μm FD-SOI CMOS process by Lapis Semiconductor Co. Ltd.

SOI Pixel Detector: Monolithic type detector

- LSI is processed on Buried Oxide layer (BOX)
- Smaller pixel size, complex circuit in pixel
- Low material budget
- High speed, low power
- Less single event effects (SEE) probability
- Low cost

Double SOI Pixel Detector



Illustrated by T. Tsuboyama (KEK)

Double SOI Pixel Detector

Middle Si layer suppresses

- Back gate effect
- Sensor-Circuit cross talk
  - Middle Si layer shields coupling between sensor and circuit.
  - It is useful for analog and digital mixed circuit in pixel.
- Radiation damage (TID)
  - It is able to compensate electric field generated by trapped holes in the BOX.
  - It can be used in high radiation environment (~1MGy).
  - (K. Hara, Vertex2017, Sep. 11-15, 2017, Las Caldas)

Sensor thickness: 50 - 500 μm
Sensor Resistivity: > 1 kΩ·cm
SOI2 thickness: 150 μm (n-type)
SOI2 Resistivity: < 10 Ω·cm

Functions for ILC Vertex Detector

Necessary functions for the ILC vertex detector:

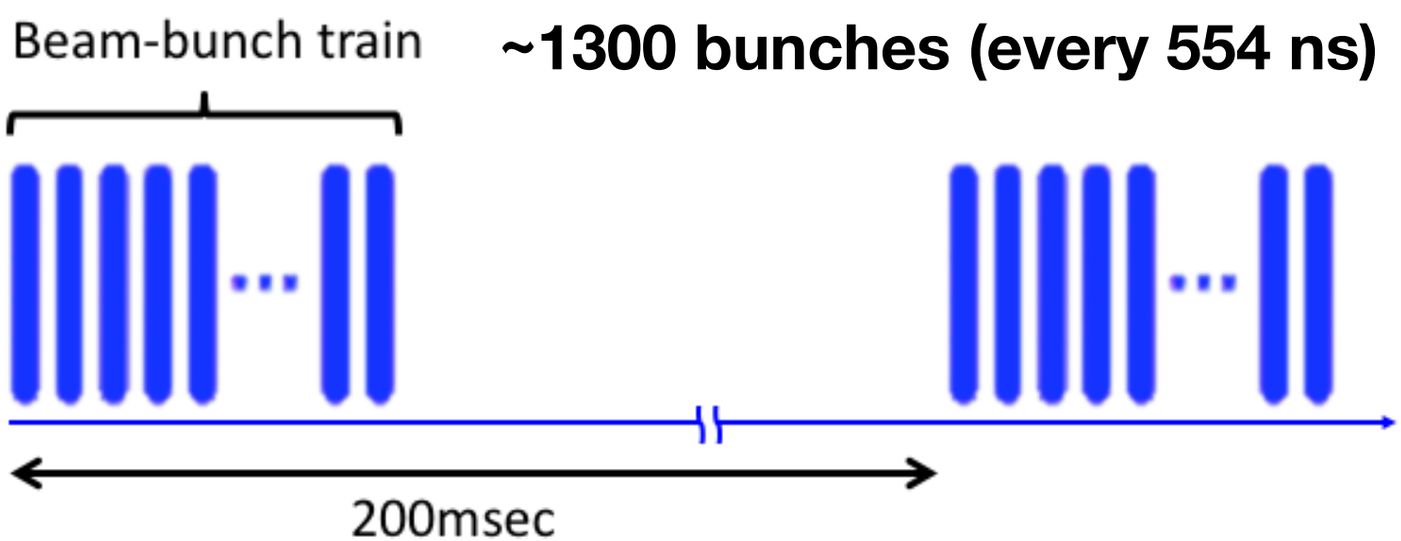
- Single point resolution
  Pixel size: less than 20 μm
  Calculate weighted center of charges (Charges are spread among multi pixels).
  → Record an analog signal of a hit.

- Timing resolution
  Bunch crossing occurs every 554 ns in 1-msec-long bunch train with an interval 200 ms.
  Identify a collision bunch of a hit to reconstruct a event.
  → Record a time stamp of a hit.

- Detector occupancy
  Hit information have to hold during 1 beam-bunch train.
  Increase detector occupancy.
  → Need multiple memories

- High speed data transfer
  Data have to be send to backend before next bunch train injection.
  → Reduce a data to transfer.

We designed a prototype pixel detector SOFIST.



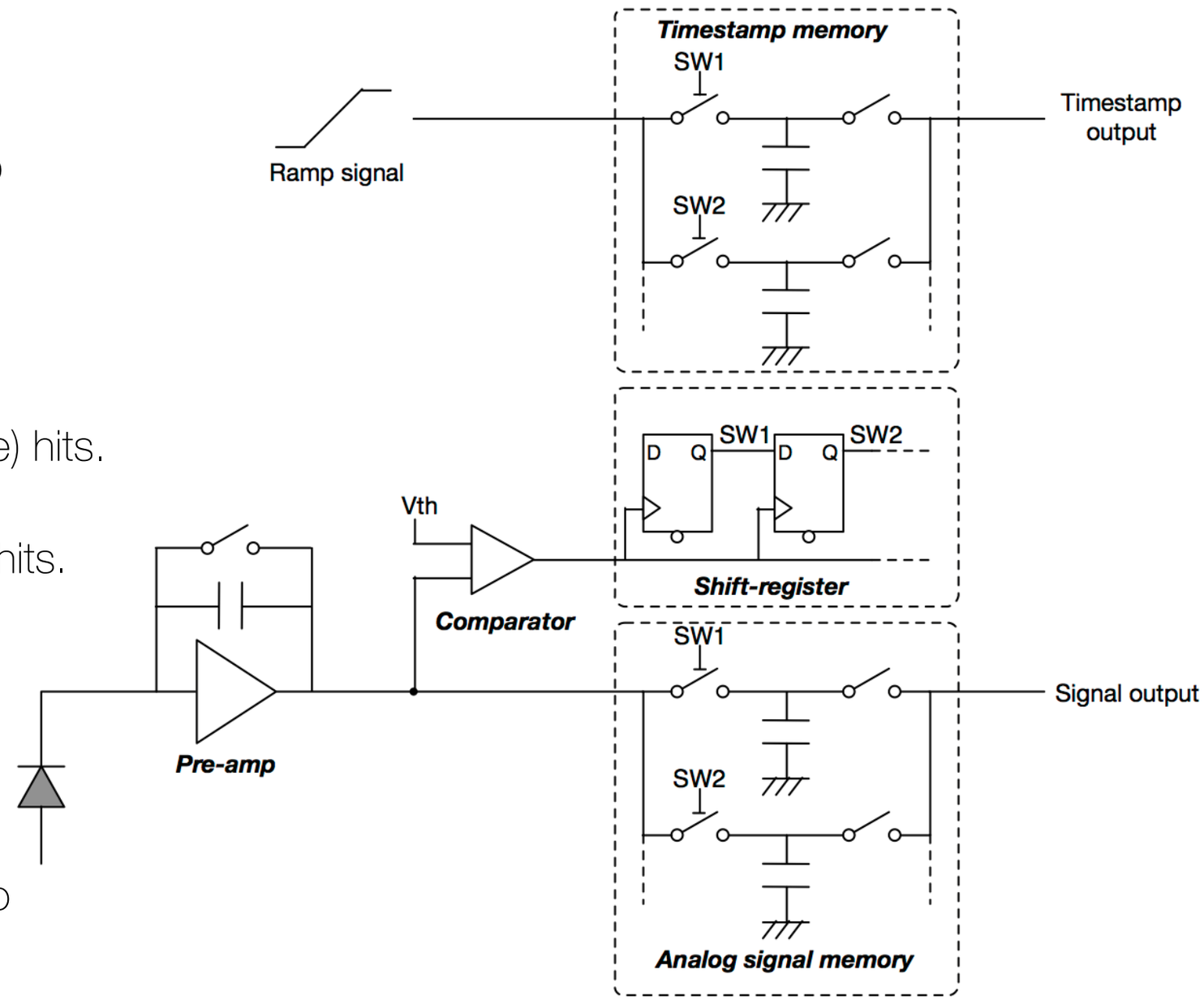
Architecture of SOFIST

In a Pixel

- Pre-amplifier
- Comparator
  Keep the analog signal and time stamp if a signal exceeds a threshold V_{th}.
- Shift register
  Latch for multiple memories.
- Analog signal memory
  Store signal charges up to two (or more) hits.
- Time stamp circuit
  Store time stamps up to two (or more) hits.

On Chip

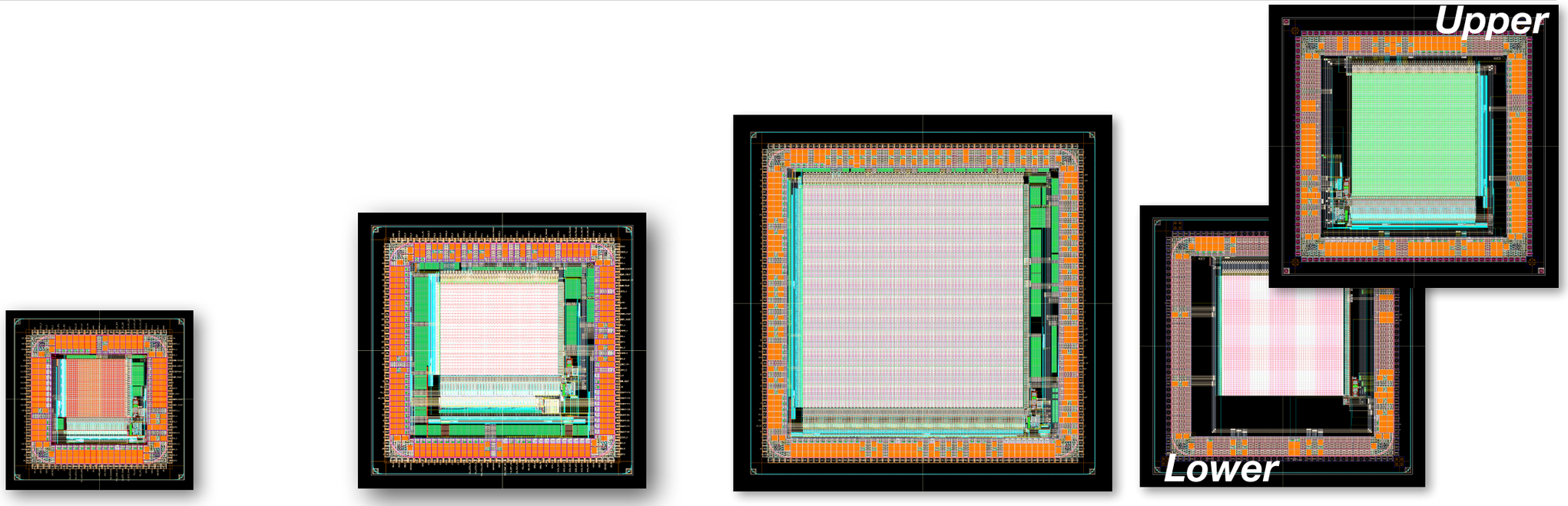
- Column ADC
  Digitize analog signal and time stamp.
- Zero-Suppression logic
  Extract hit pixels and reduce the data to transfer to backend.



Designed by S. Ono (KEK)

SOFIST Series

	MX1850	MX2040	MX2166	
SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)



Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n* -type (Single SOI)	Cz *p* -type (Double SOI)	FZ *p* -type (Double SOI)	FZ *p* -type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Under evaluation	Delivered (Jan. 2017)	Delivered (May. 2018)	will be delivered (Aug. 2018)

SOFIST ver.1

Pixel

- Pre. amplifier (Charge sensitive amplifier)
  gain: 32 $\mu V/e^-$
- Analog signal memories (two memories)

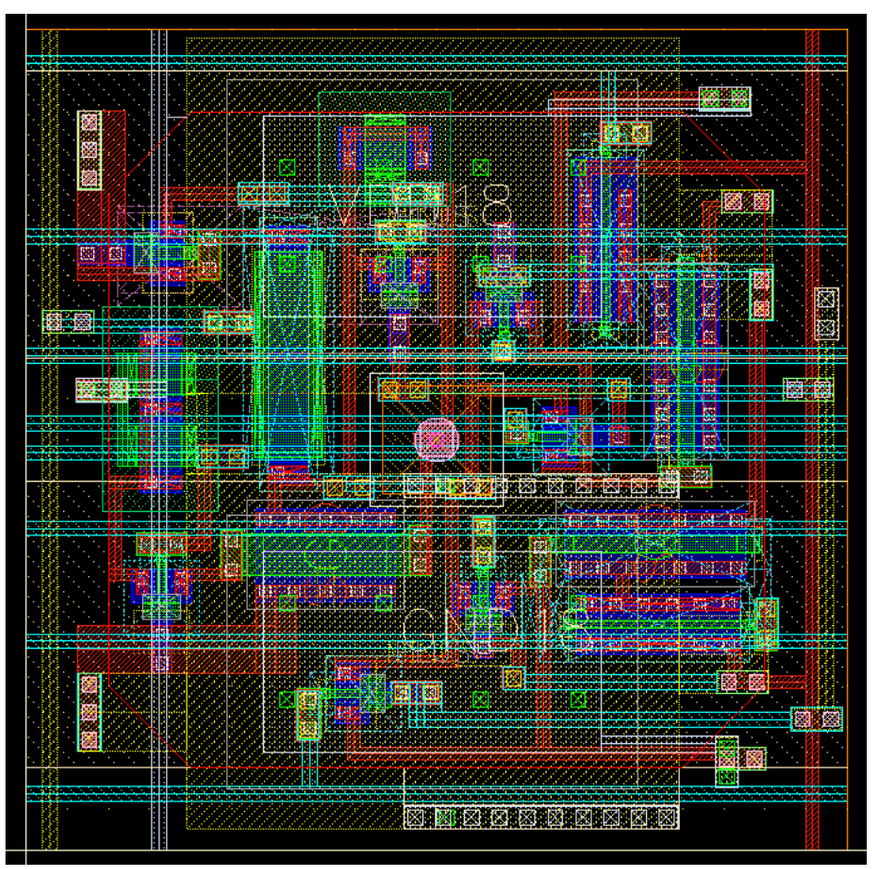
On chip

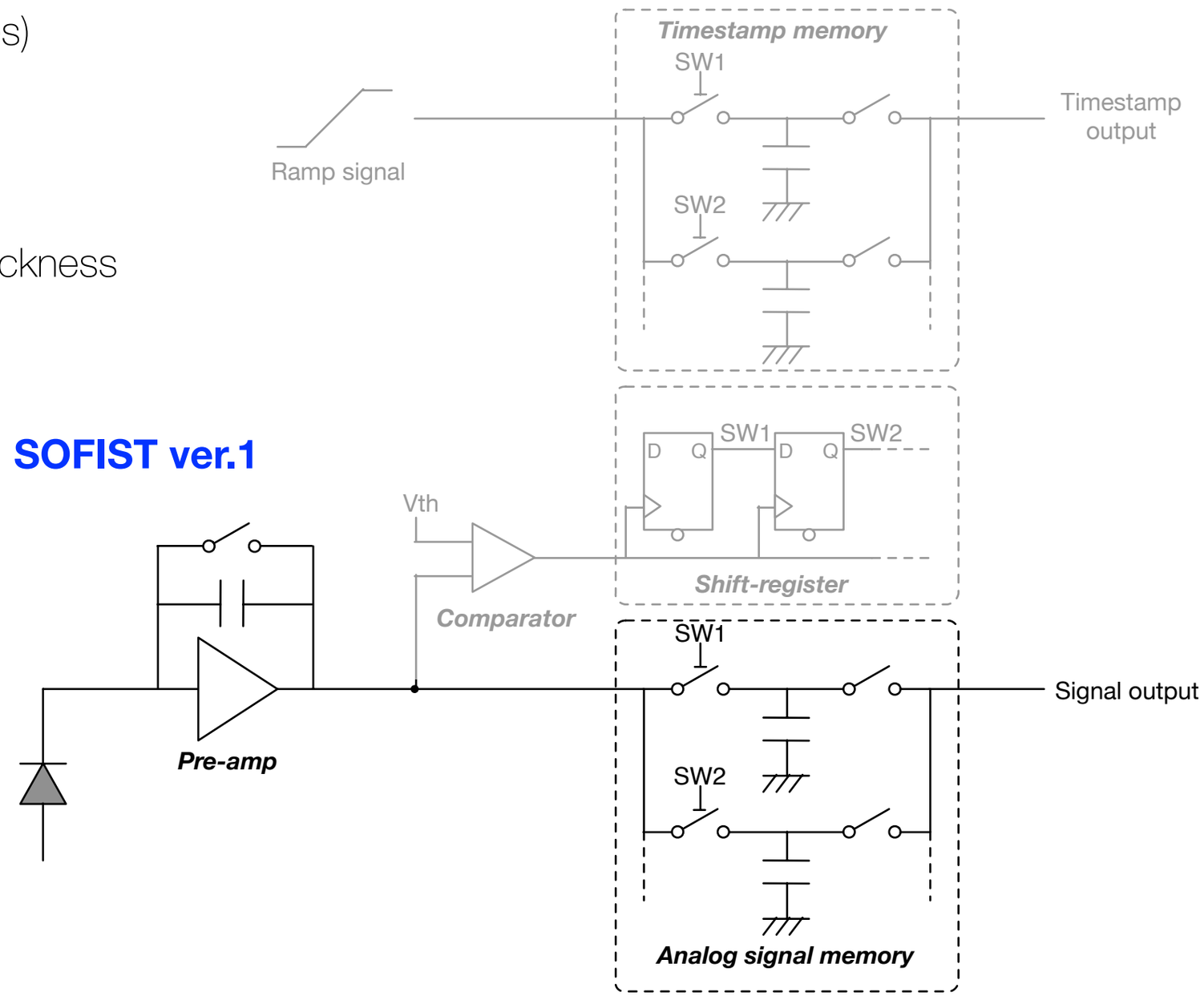
8 bit column ADC

Sensor

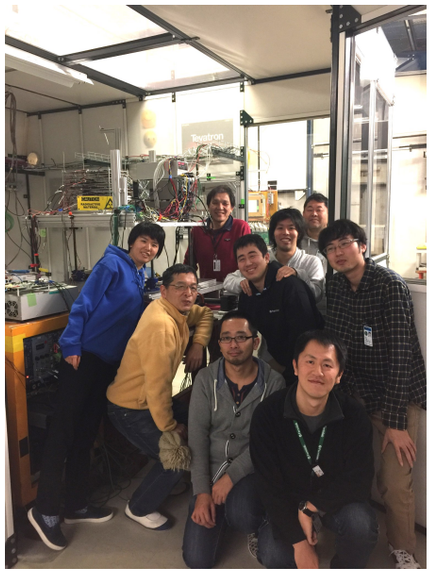
Single SOI
FZ-*n* type
500 μm thickness

Pixel size: 20 × 20 μm^2



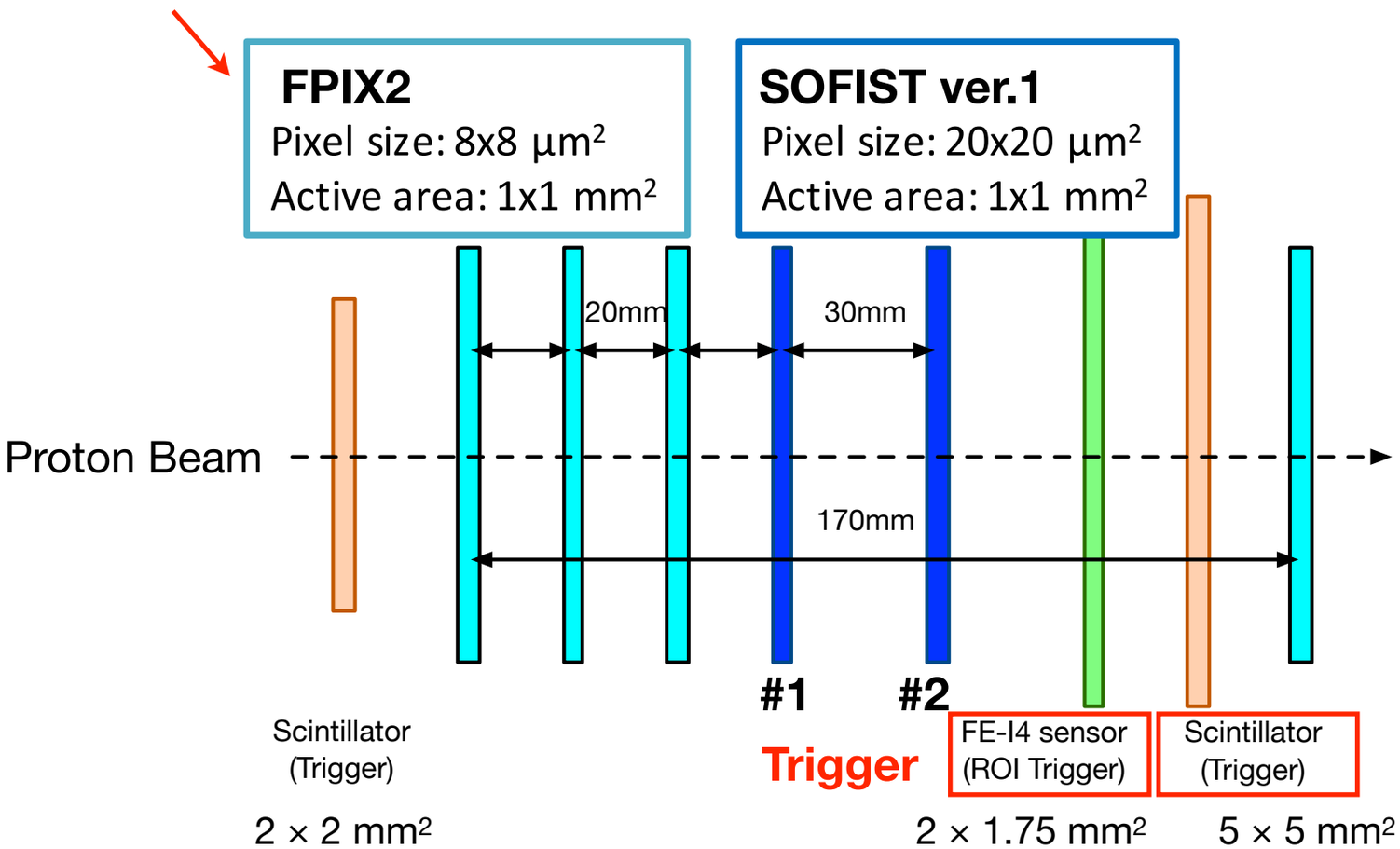


Beam Test

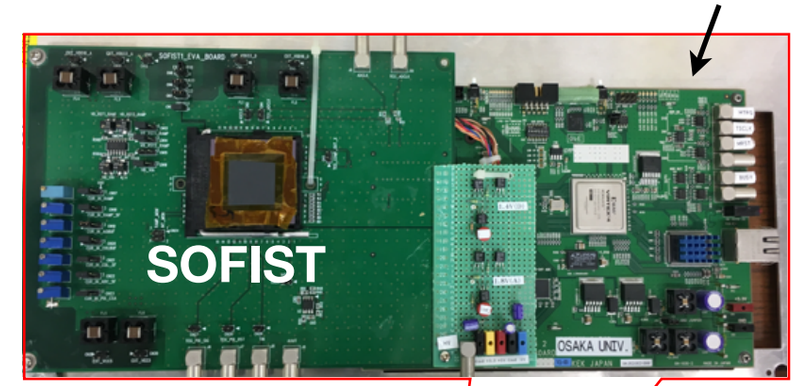


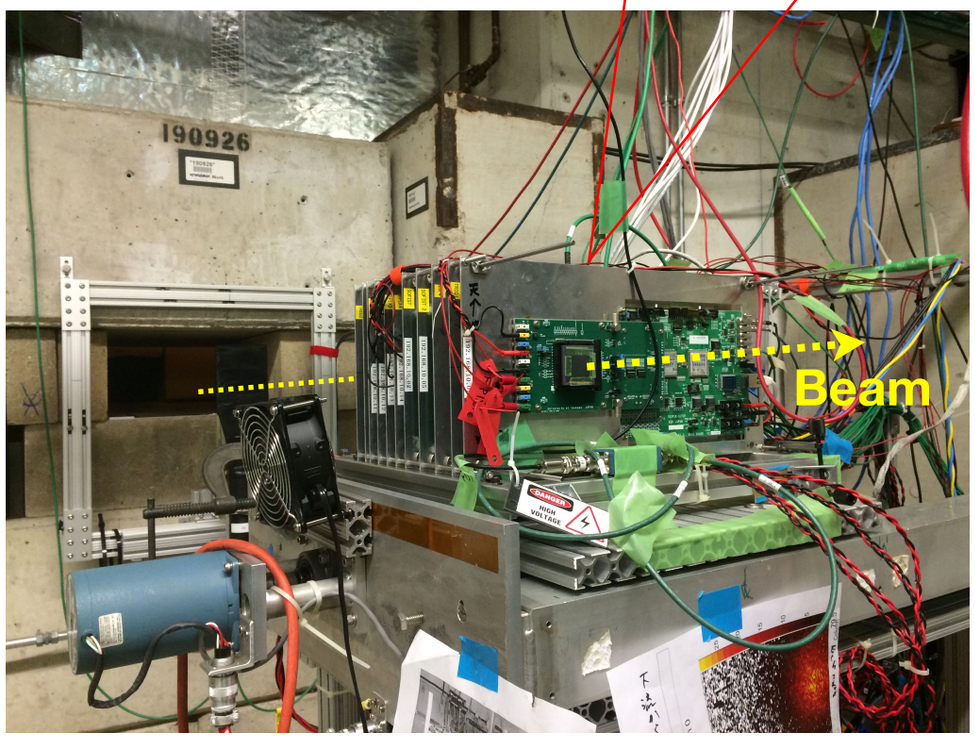
Beam: 120 GeV proton (Fermilab Beam Test Facility, Jan. 2017)
Trigger: ATLAS upgrade pixel sensor (FE-I4) && Scintillator (Downstream)
(Some data were taken by coincidence of two scintillators for checking the DAQ system.)
DAQ rate: ~300 events/s

FPIX2 (SOIPIX)
Telescope for SOFIST
Reconstruct track with four layers of FPIX2.
Spatial resolution: 0.65 μm (K. Hara, Vertex 2017)



DAQ board (SEABAS2)





S/N

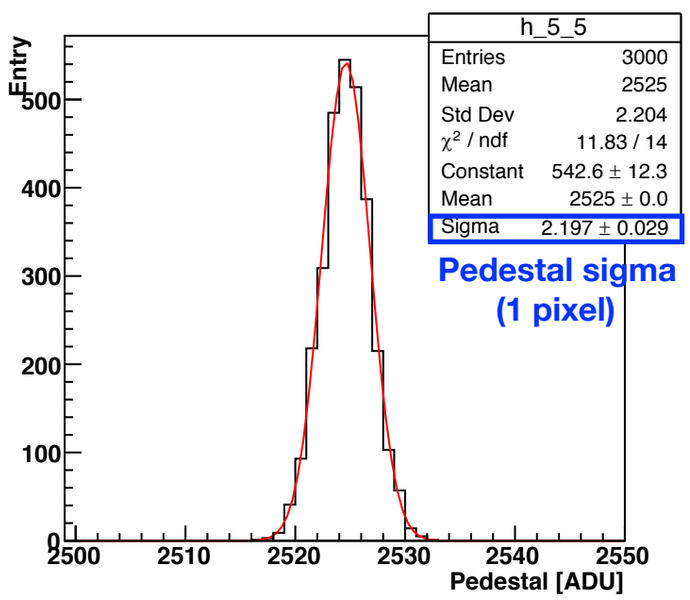
SOFIST setup

Readout: 12 bit external ADC (SEABAS2 onboard)
Sensor bias voltage = 130 V (Depletion depth ~ 500 μm)

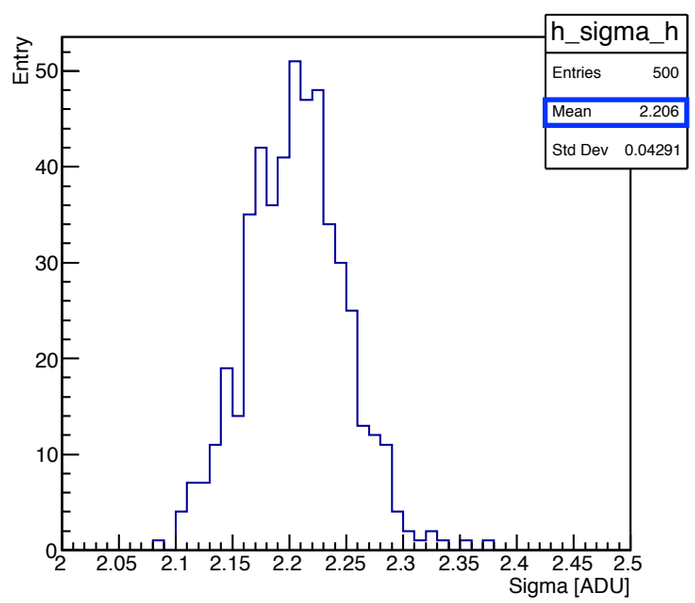
Clustering

1) find seed pixel which is ≥ 64 ADU.
2) add pixels which are ≥16 ADU to the cluster.
3) check 2) for 6 × 6 pixels centered on the seed pixel.

Pedestal (1 pixel)

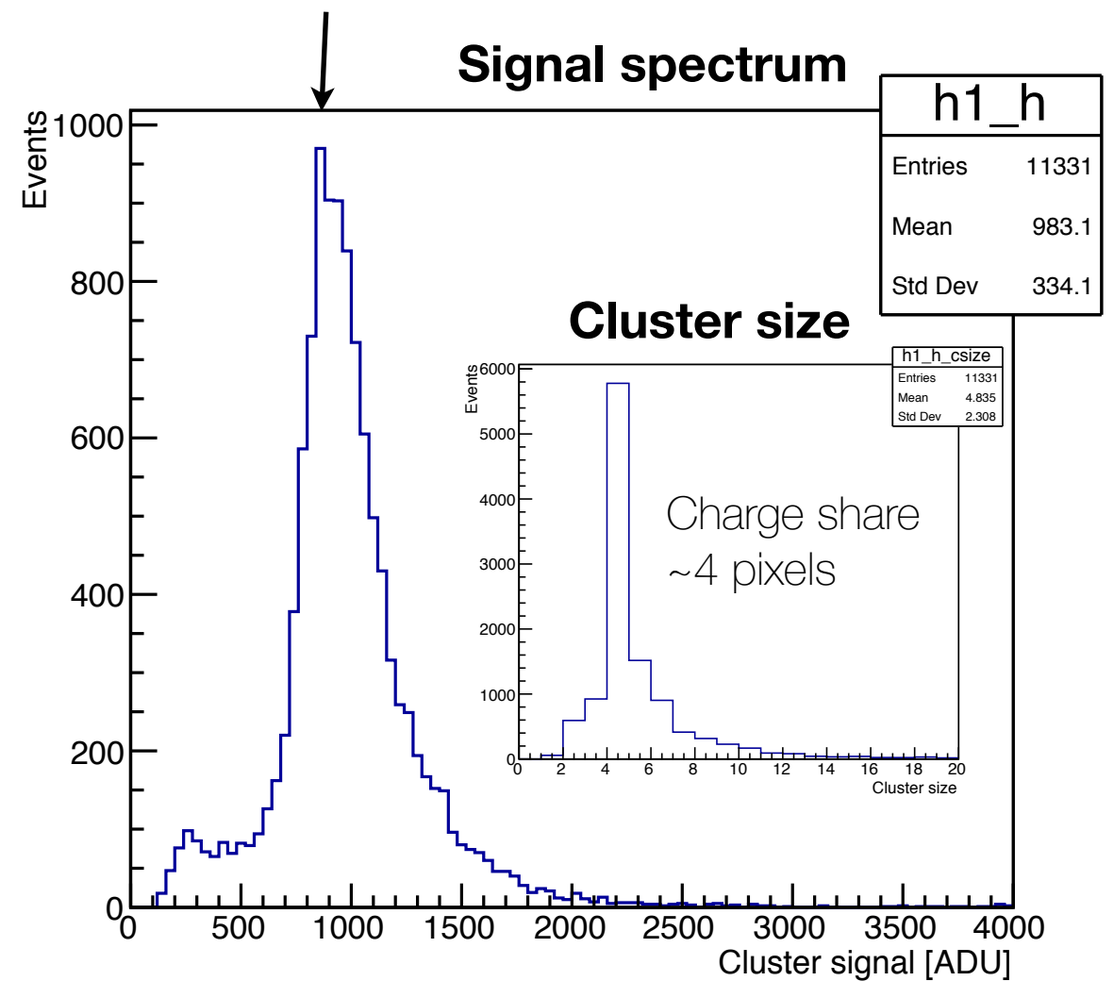


Pedestal sigma (Noise)
Mean = 2.2 (All pixels)



Cluster signal peak: ~800 ADU

Signal spectrum



Signal to Noise ratio

Signal peak = ~800 ADU
Pixel noise = ~2.2 ADU

⟶ **S/N ~ 360** (Full depletion of 500 μm thickness)

Position Resolution

Hit position reconstruction

Calculate weighted center of charges (6 × 6 pixels).

Track reconstruction

Find track candidates by four layers of FPIX.
The track that has the minimum chi2 is chosen for calculating the residual.

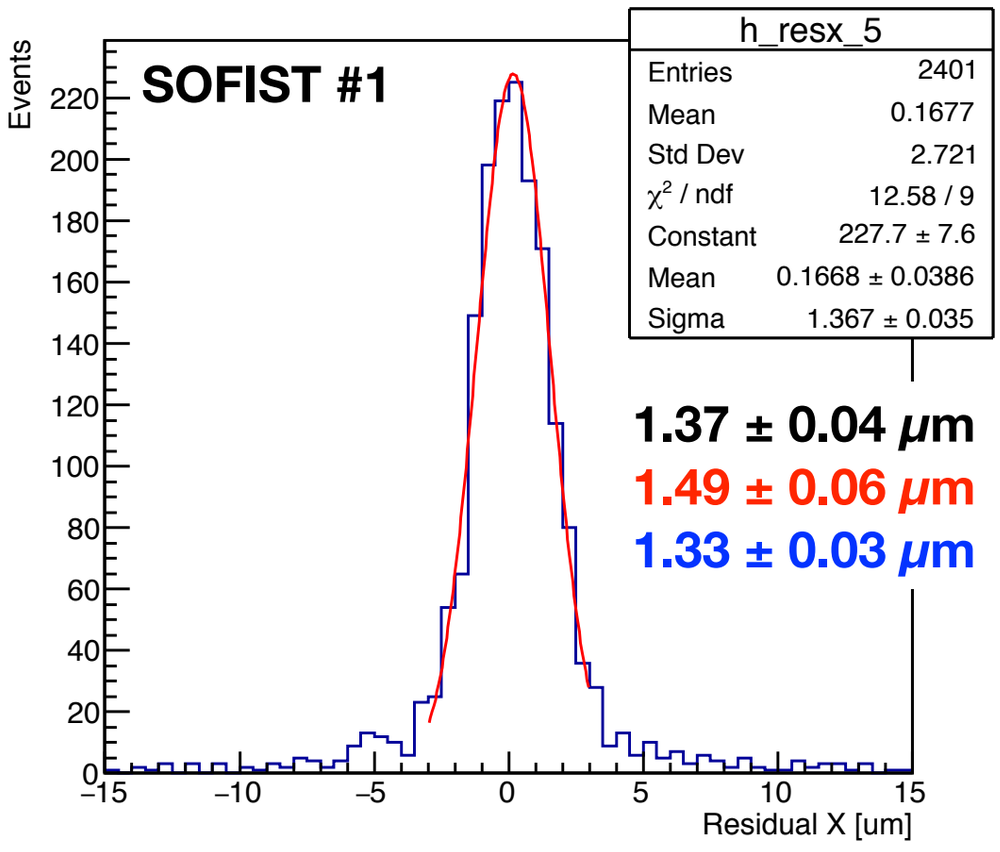
Residual

Difference between reconstructed track and actual hit on the SOFIST.

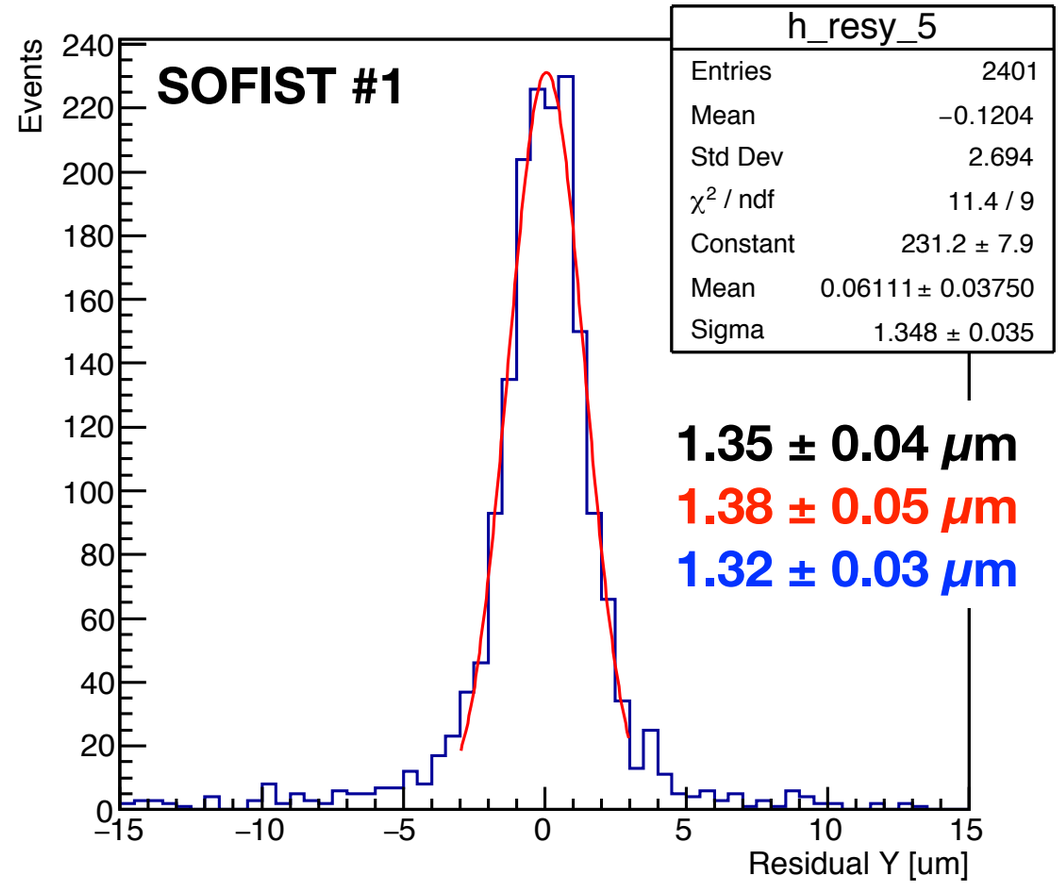
Readout and Sensor depletion layer

12-bit external ADC, 500 μm (Full depletion)
8-bit on-chip ADC, 500 μm (Full depletion)
12-bit external ADC, 200 μm (Partial depletion)

Residual X



Residual Y



SOFIST ver.2

Pixel

- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (two memories)
  or Time stamp memories (two memories)

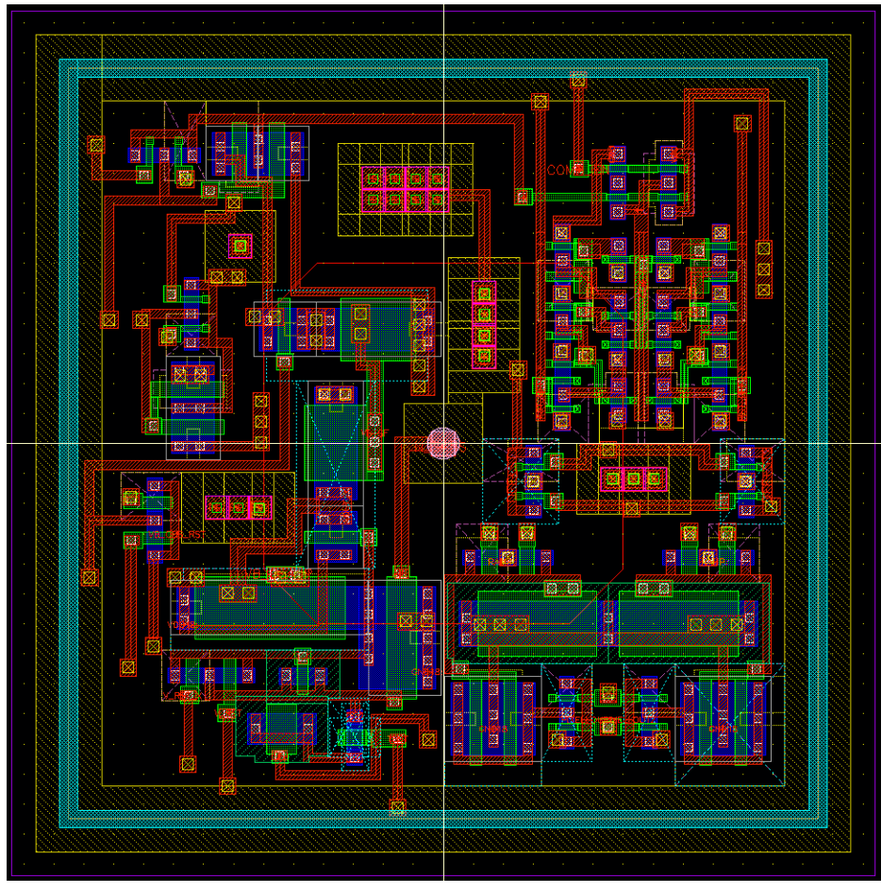
On chip

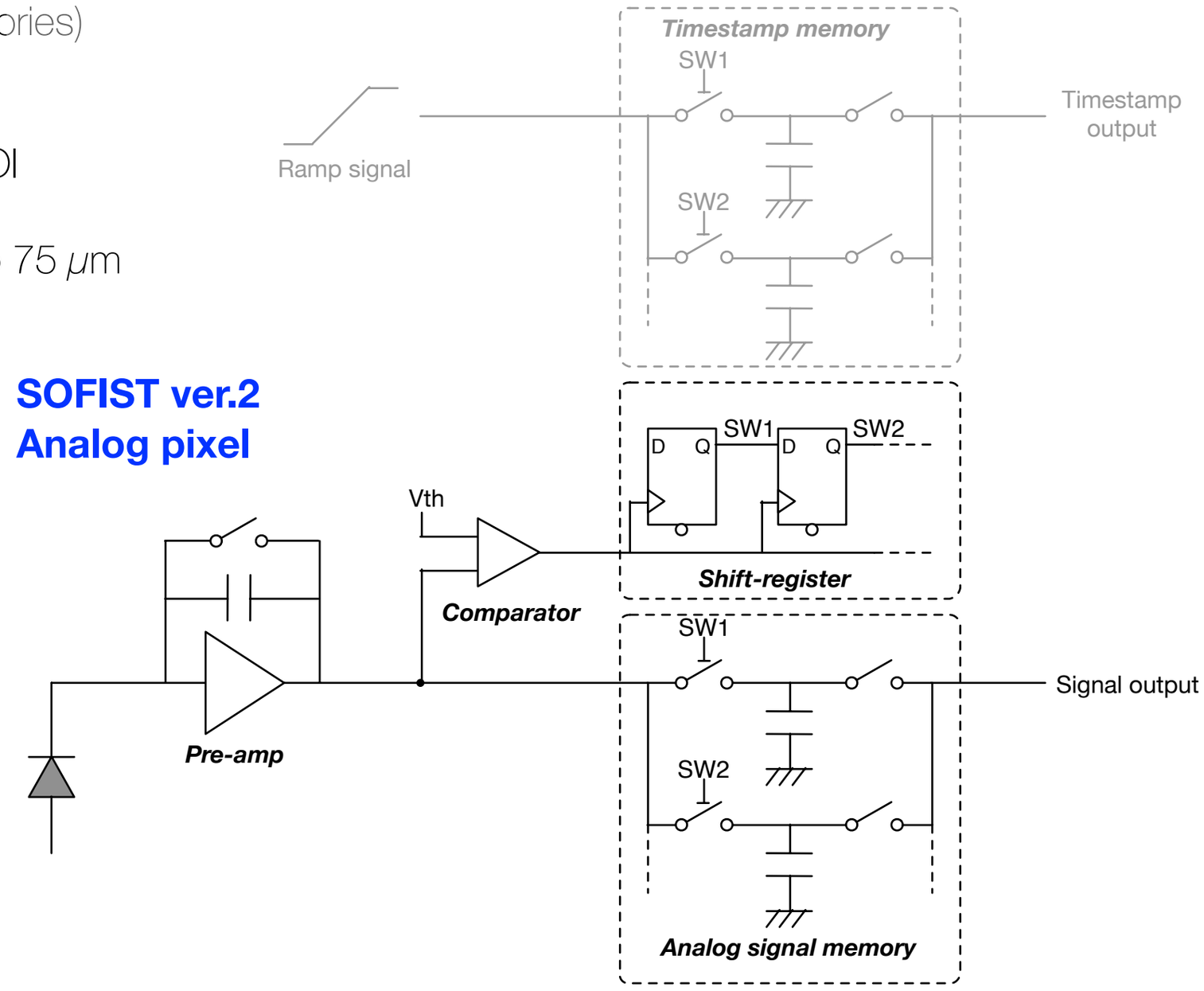
8 bit column ADC
Zero-suppression logic

Sensor

Double SOI
FZ-*p* type
Thinned to 75 μm

Pixel size: 25 × 25 μm^2





SOFIST ver.2

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8 bit column ADC
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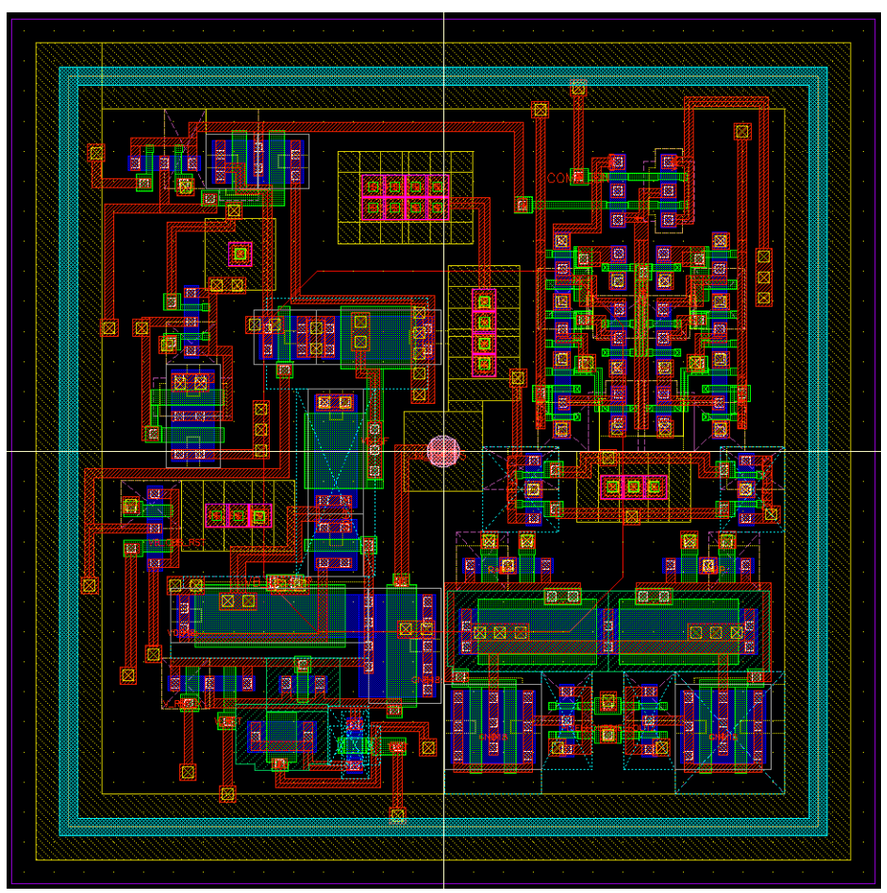
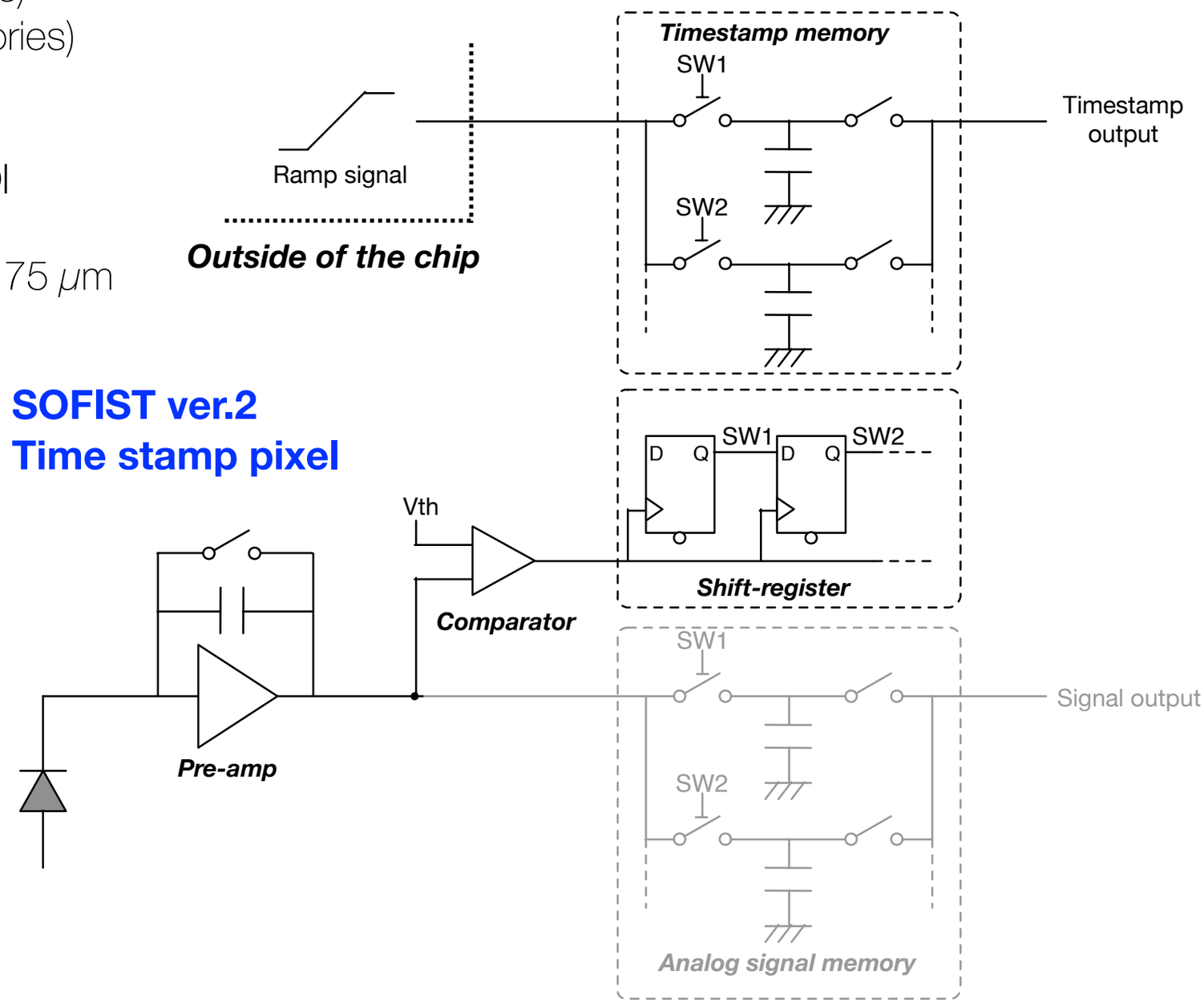
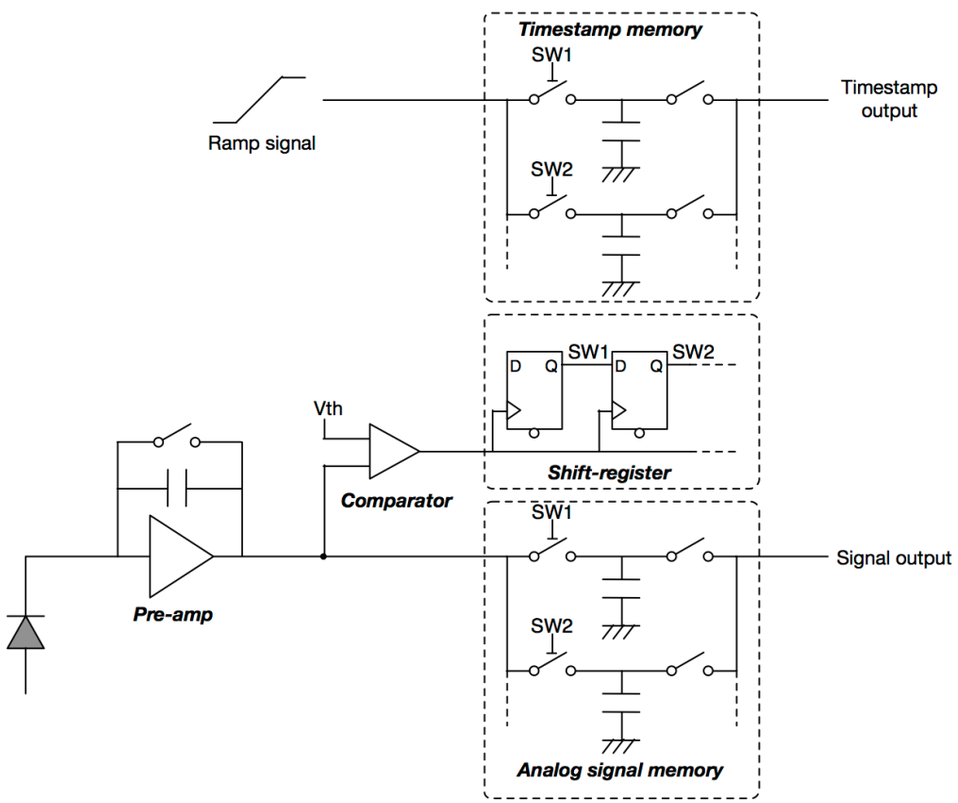
Thinned to 75 μm

Pixel size: 25 × 25 μm^2

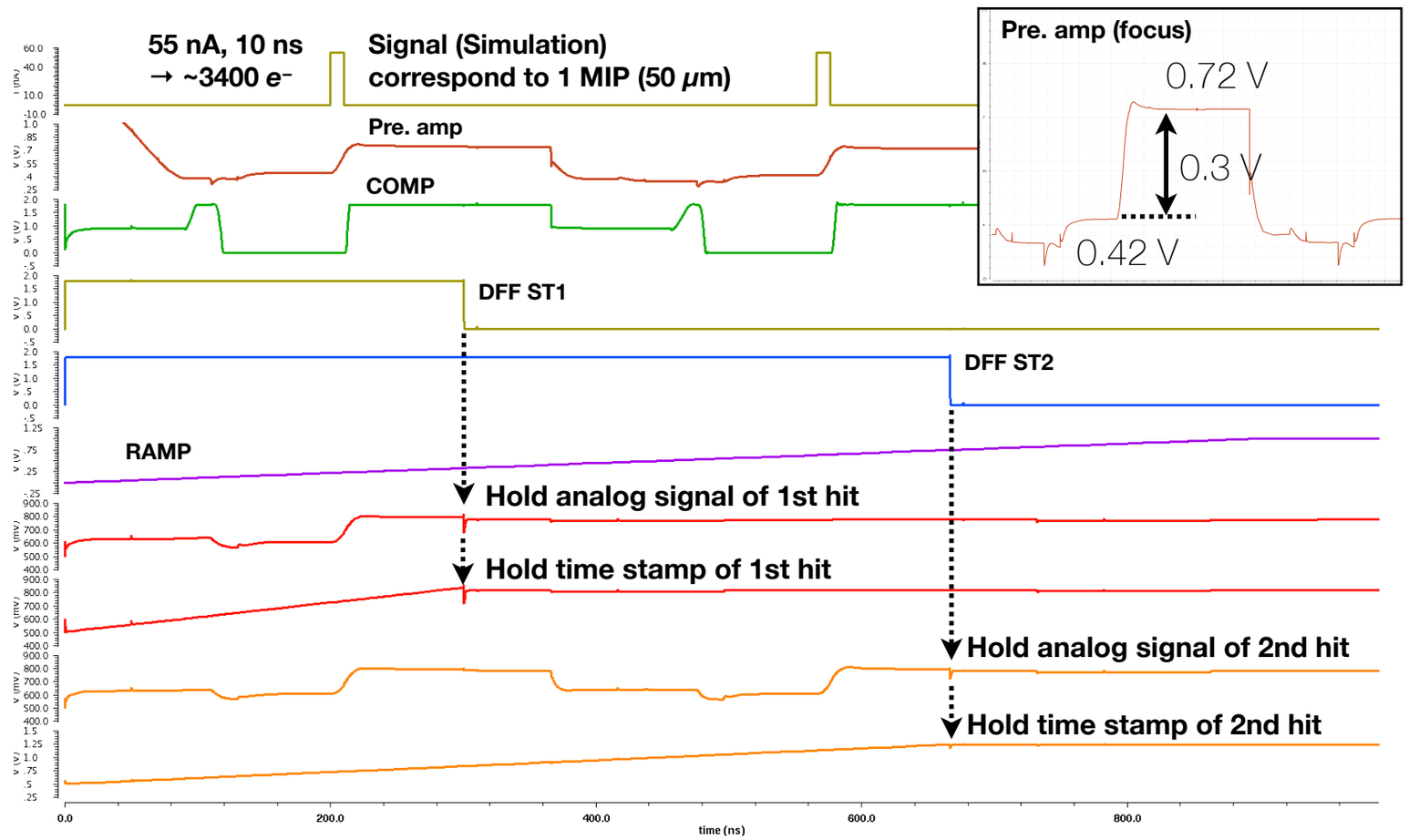




SOFIST ver.2 Pixel



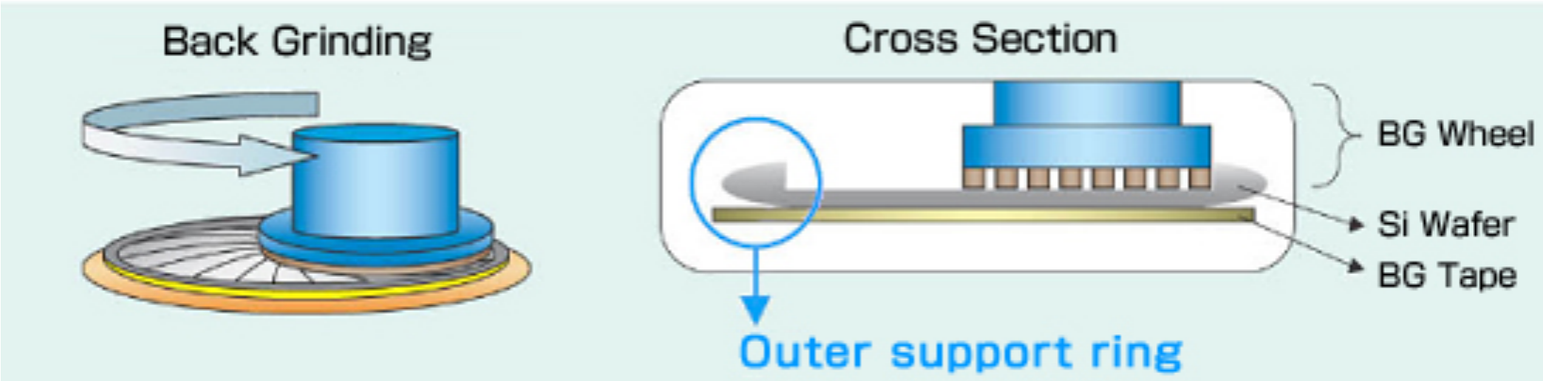
Simulation of the pixel circuit

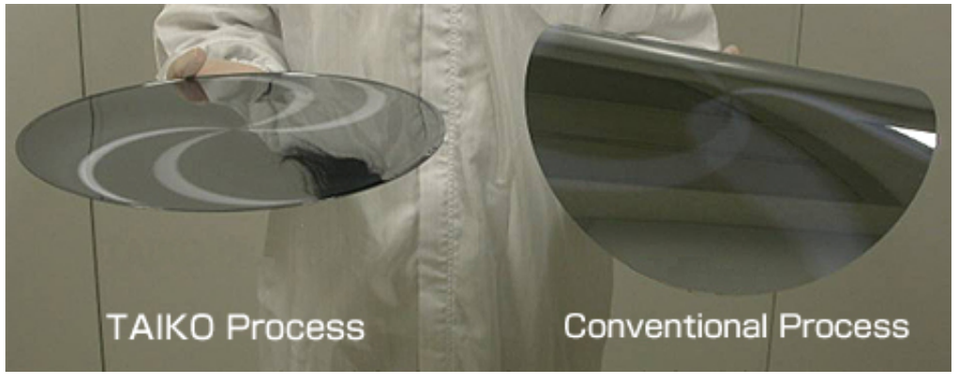


1) Input a RAMP waveform.
2) Open a store switch (SW1) when a comparator output changes to High.
3) Keep the voltage of RAMP to the time stamp memory as a time stamp.
4) in the same way for 2nd hit.

Wafer Thinning

TAIKO Process by DISCO Corporation (Japan)
https://www.disco.co.jp/eg/index.html

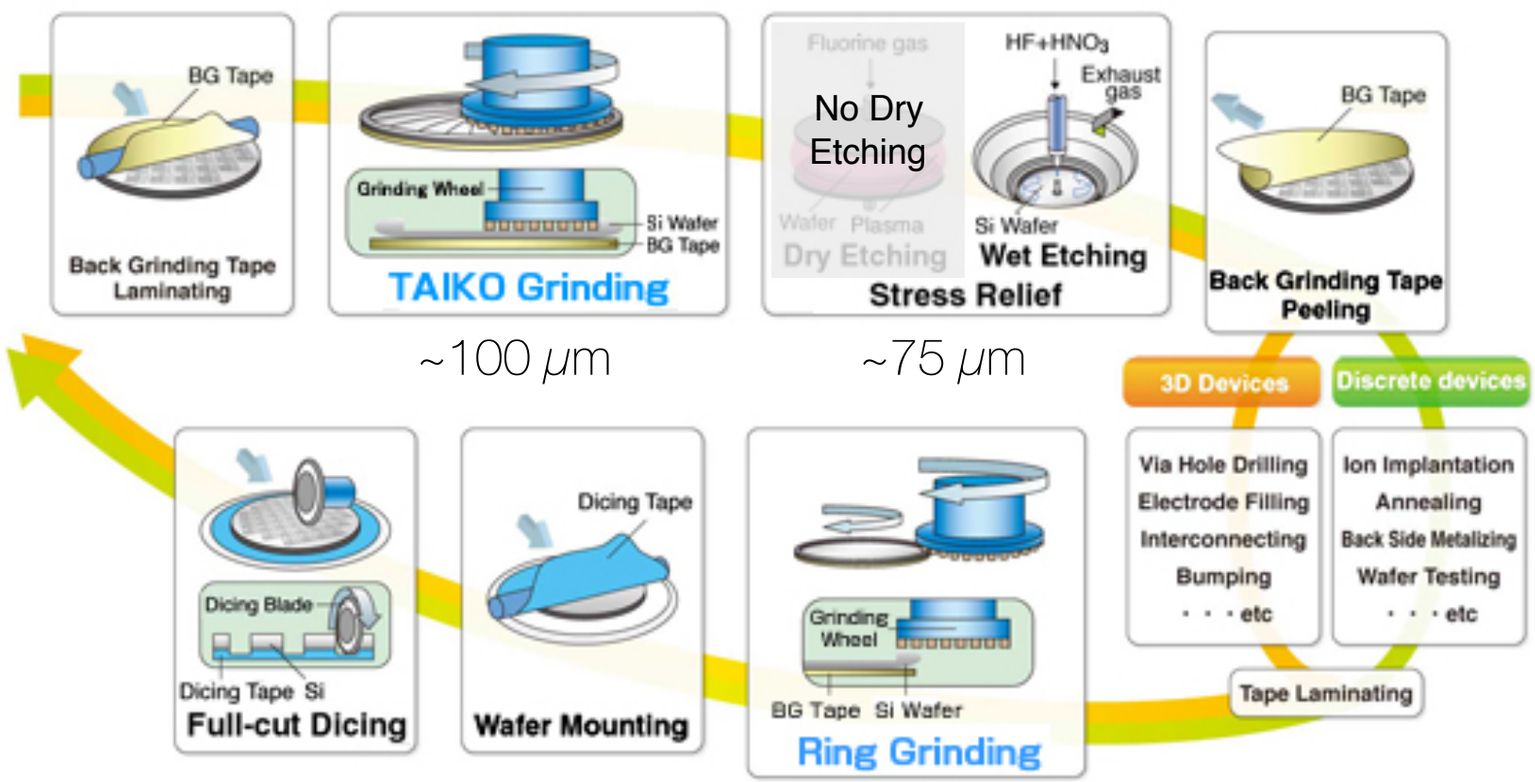




Stress relief with wet etching by
Mimasu Semiconductor Industry Co., Ltd. (Japan)

TAIKO Process
with outer support ring

- Lower wafer warpage
- Improve of wafer strength
- Easy wafer handling
- Easy backside processing (ion implantation, annealing, Metalizing etc) after thinning

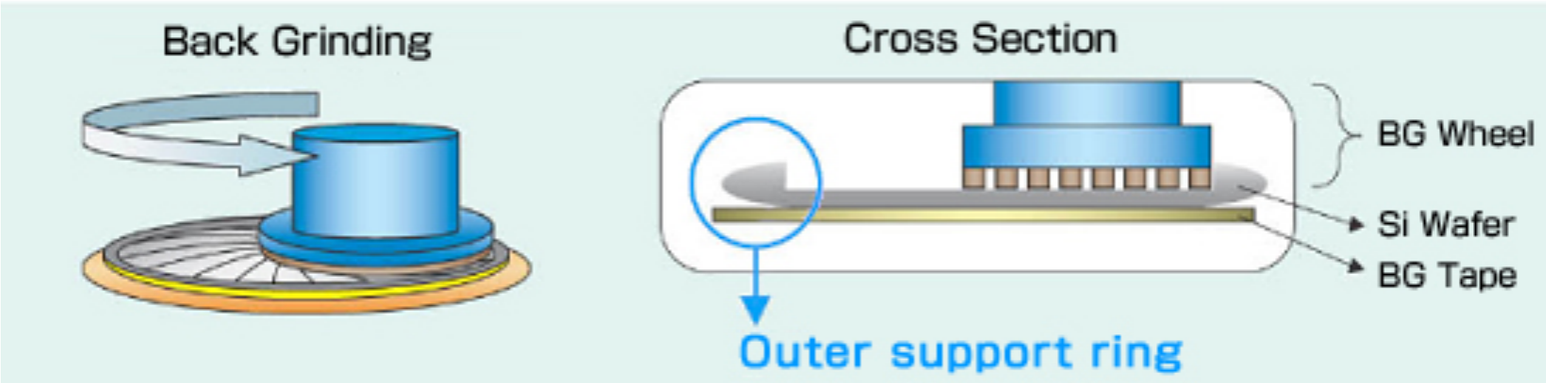


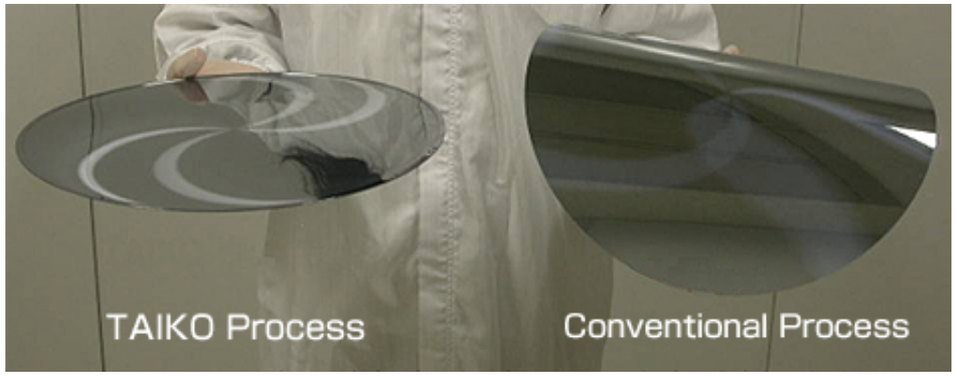
Back side process after thinning

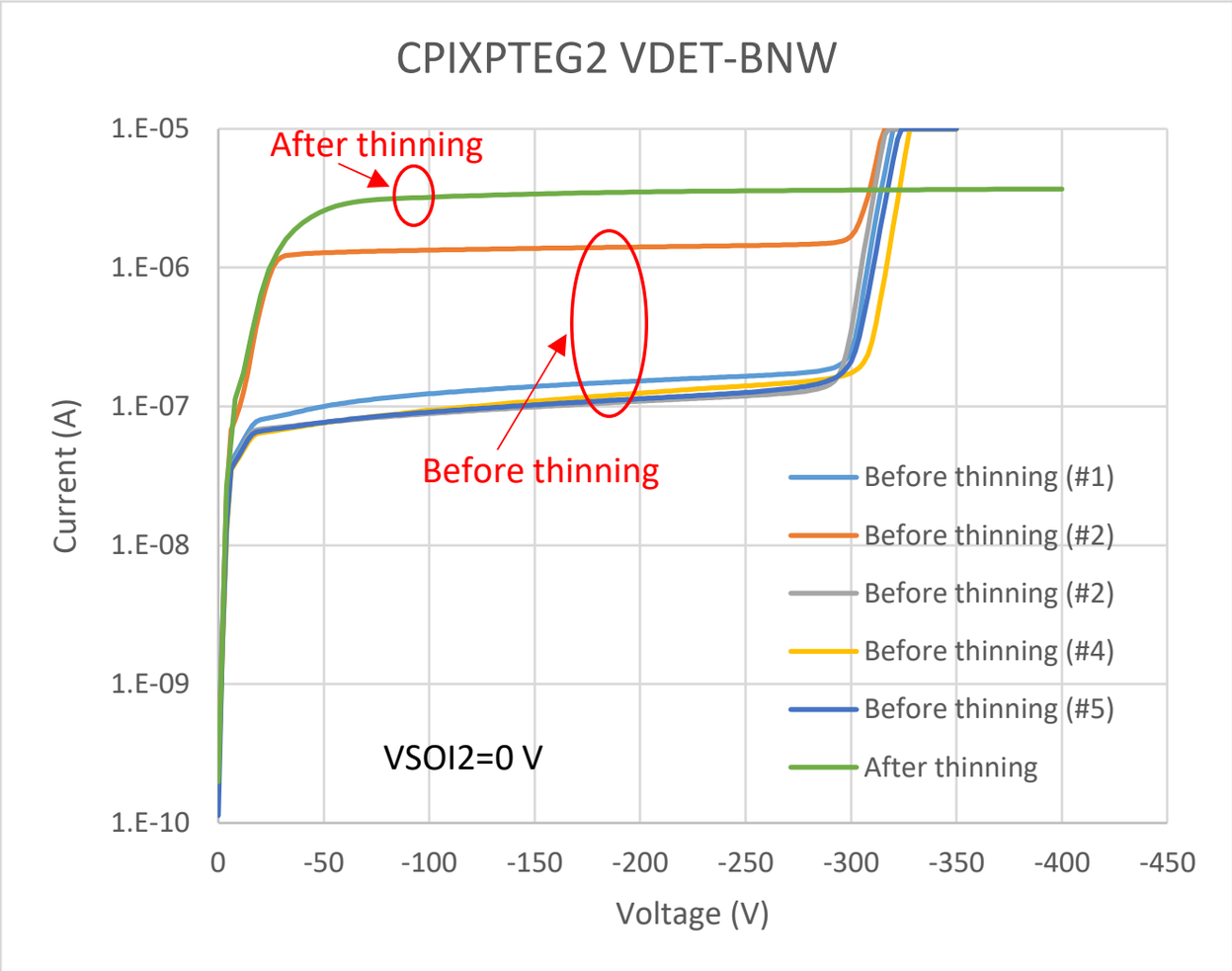
- Boron implantation (ULVAC, Japan)
- Laser Annealing (SHI, Japan)

Wafer Thinning

TAIKO Process by DISCO Corporation (Japan)
https://www.disco.co.jp/eg/index.html







Sensor I-V after thinning (other SOIPIX)

Leak current increased by ~1.5 orders of magnitude.
No break down by 400 V after thinning.

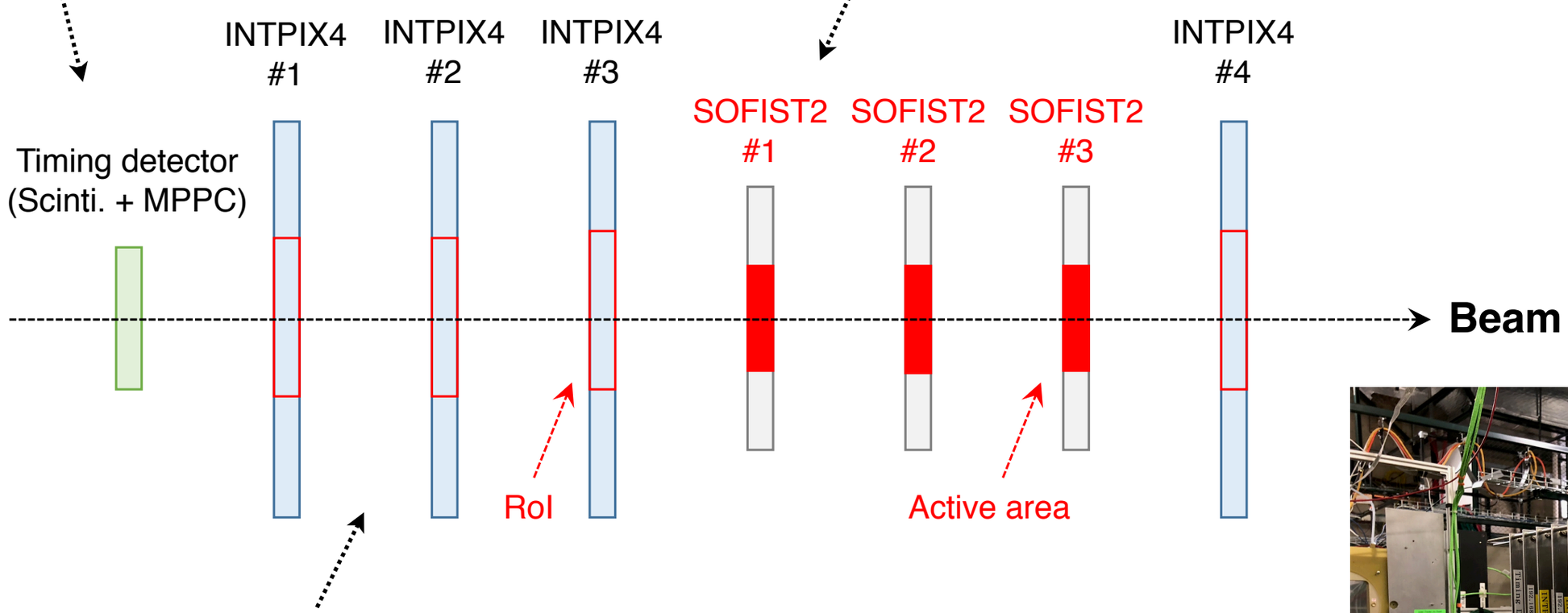
Still investigating these behavior.

Beam Test

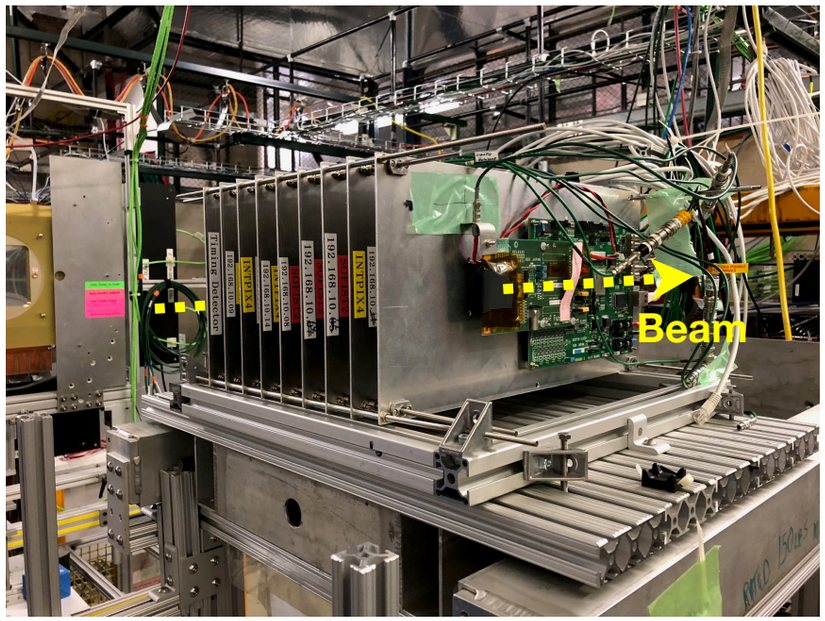
Beam: 120 GeV proton (Fermilab Beam Test Facility, Jan. 2018)
DAQ rate: ~120 events/s

Event Trigger and Timing detector
Record hit timing for checking consistency to SOFIST.
Scinti. size: 3 × 3 mm²
MPPC size: 3 × 3 mm²
Readout: Comp. + AND + NIM converter
(Signal is sent to Master DAQ, SEABAS2)

SOFIST ver.2
Pixel size: 25 × 25 μm²
Pixel array: 80 × 64 (2.0 × 1.6 mm²)
Readout: External 12-bit ADC (SEABAS2)
Sensor thickness: 75 μm

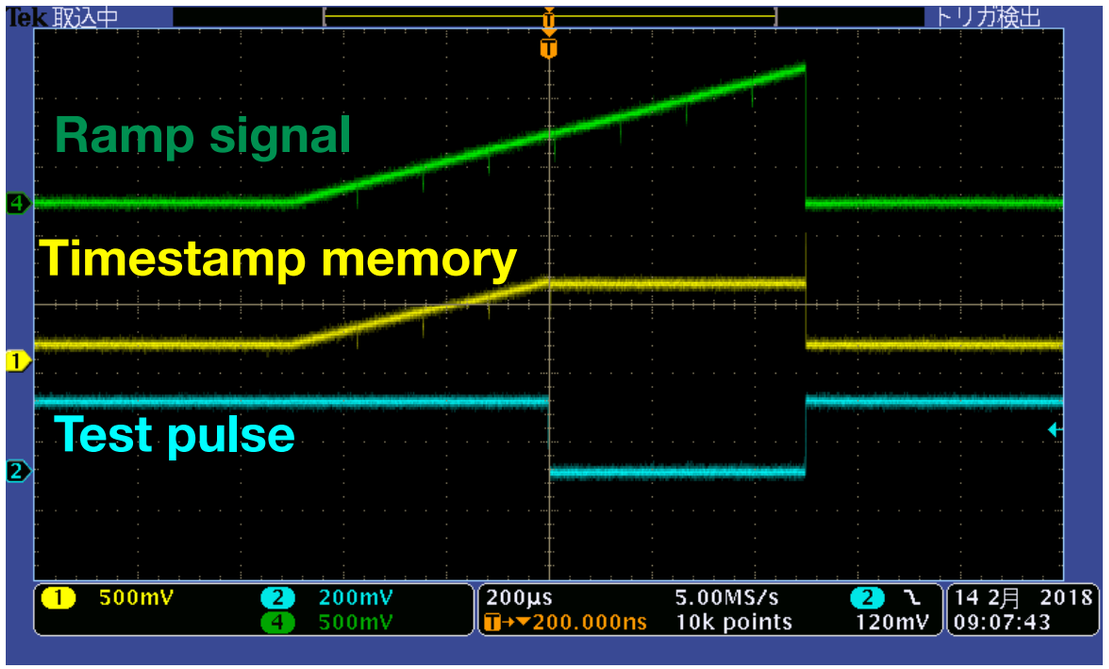


INTPIX4 (SOIPIX)
Telescope for SOFIST
Pixel size: 17 × 17 μm²
Pixel array: 832 × 512 (14.1 × 8.7 mm²)
Function: Region of Interest readout
Readout: External 12-bit ADC (SEABAS2)

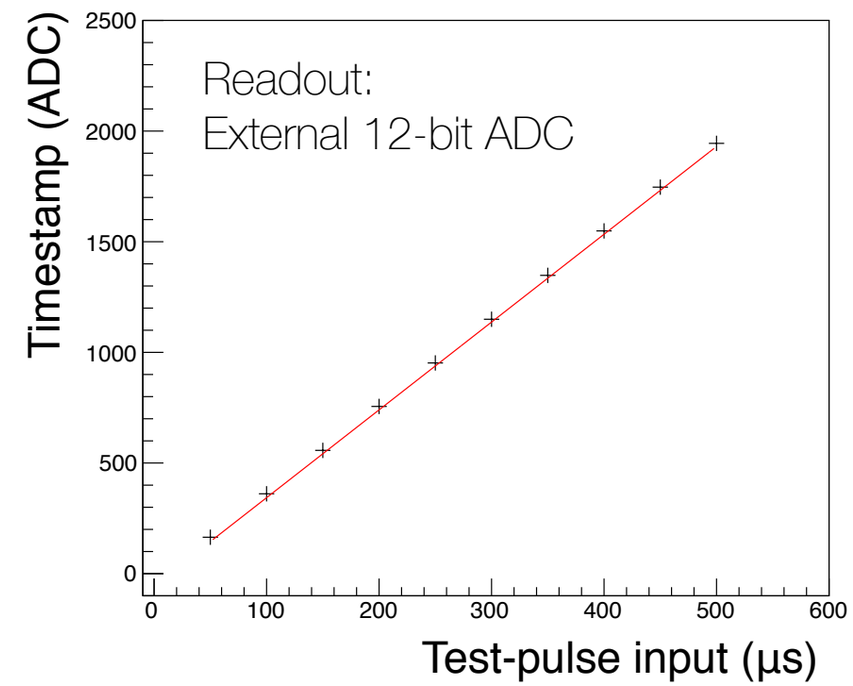


Time Resolution (Test Pulse)

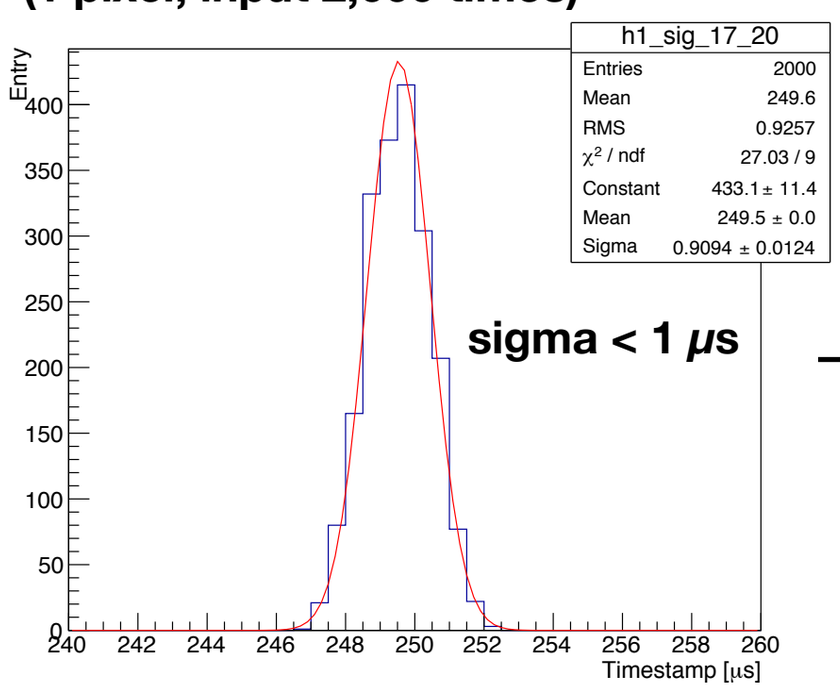
Timestamp Pixel output



Test-pulse input - Timestamp



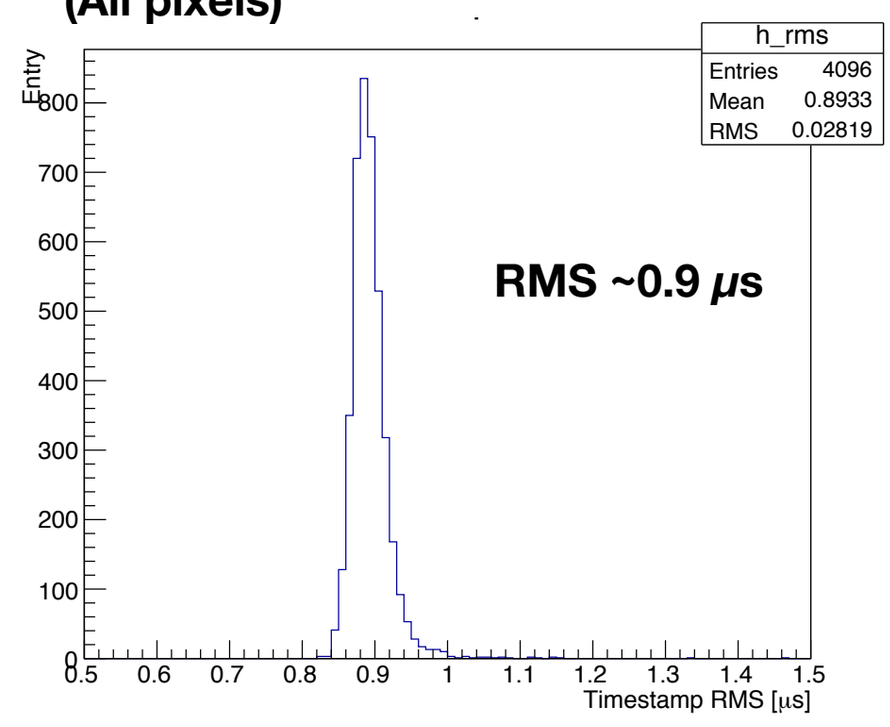
Fluctuation of timestamp (1 pixel, input 2,000 times)



All Pixels

Sigma

Fluctuation of timestamp (All pixels)



Time Resolution (Beam Test)

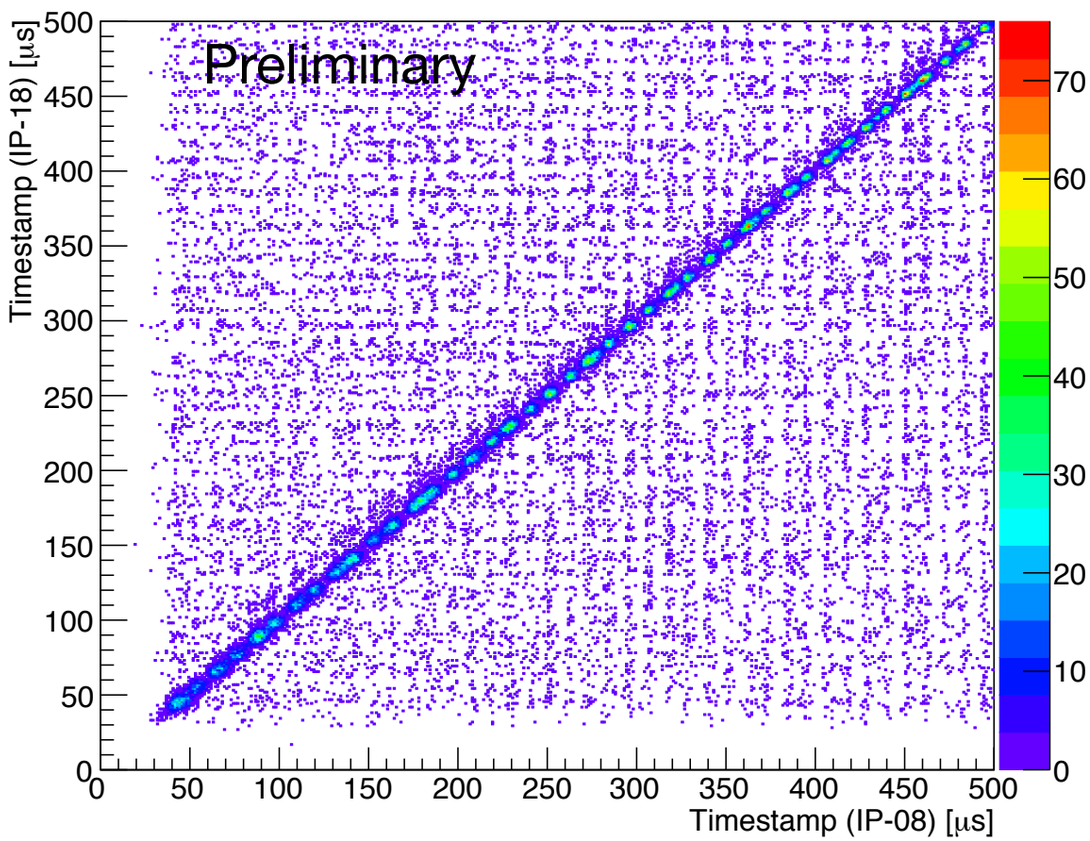
Alignment

Tracking by INTPIX4 is not performed.
Roughly aligned among SOFIST by hit position correlation.

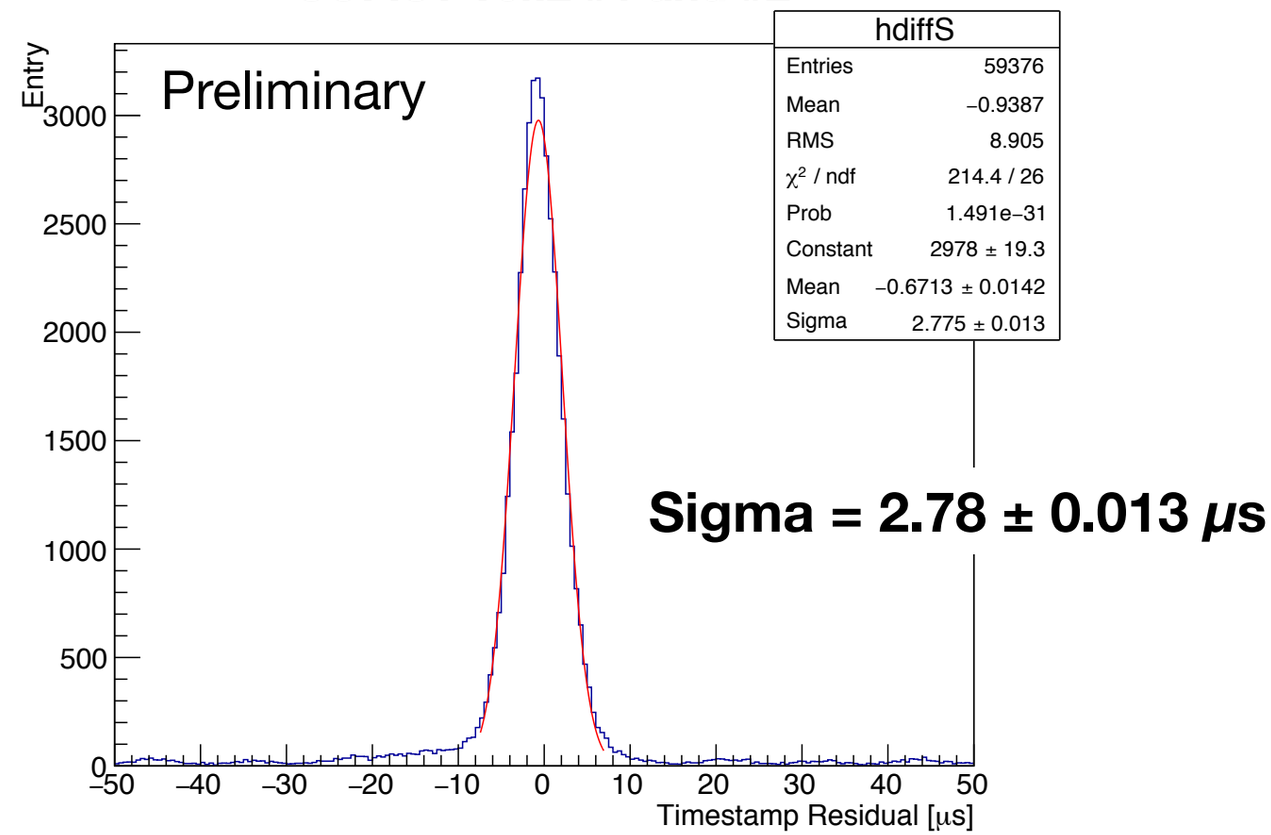
Timestamp residual

Timestamp difference between #1 and #2.
(Hit position of #2 is within 2 pixels of #1.)

Timestamp correlation between SOFIST ver.2 #1 and #2



Timestamp residual between SOFIST ver.2 #1 and #2



Intrinsic resolution: 2.78/√2 ~ 1.97 μs

Still investigating effect on time resolution

kT/C noise: Timestamp memory (25 fF) is designed by assuming 8-bit on-chip ADC.
Switching noise: Switching around memory
Alignment: Imperfect alignment. Tracking by telescope (INTPIX4) will be performed.

SOFIST ver.3

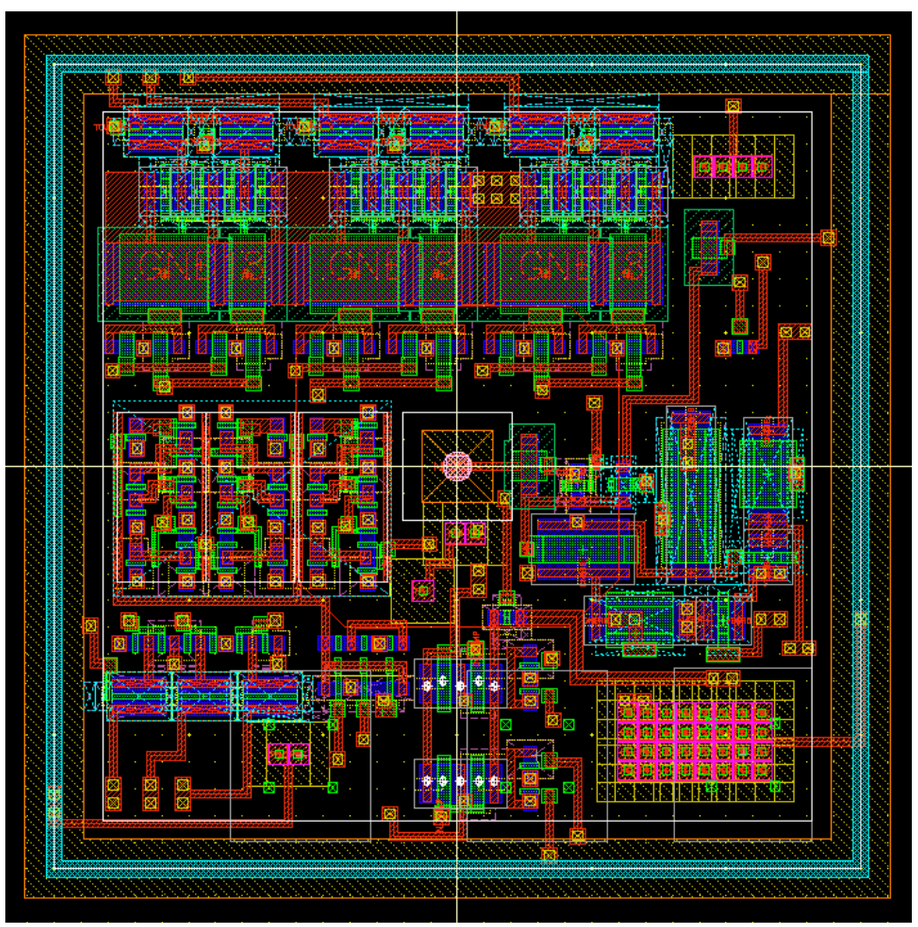
Pixel

- Pre. amplifier (Charge sensitive amplifier)
- Comparator (Chopper inverter)
- Shift register
- Analog signal memories (three memories)
- Time stamp memories (three memories)

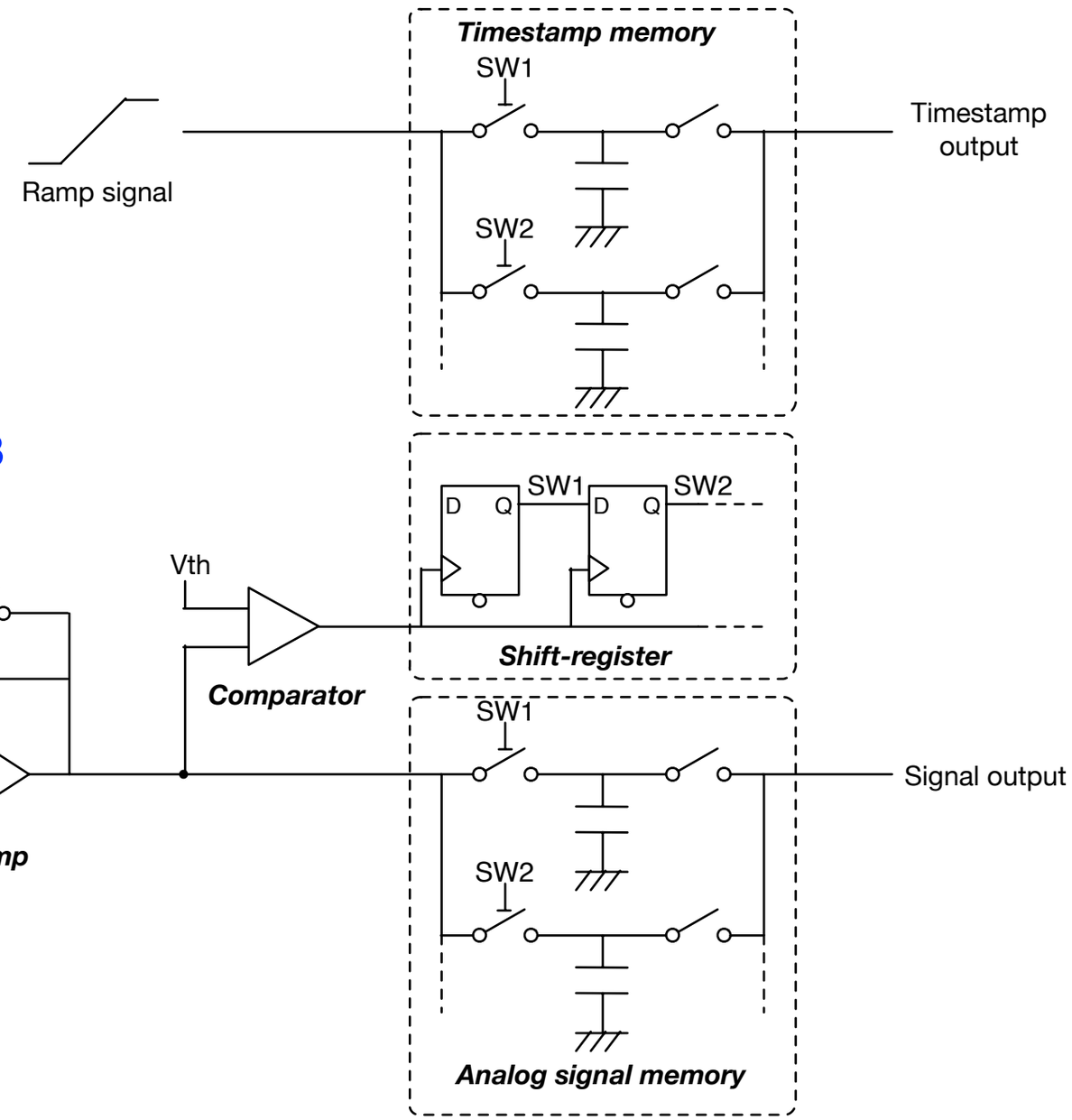
On chip

8 bit column ADC

Pixel size: 30 × 30 μm^2



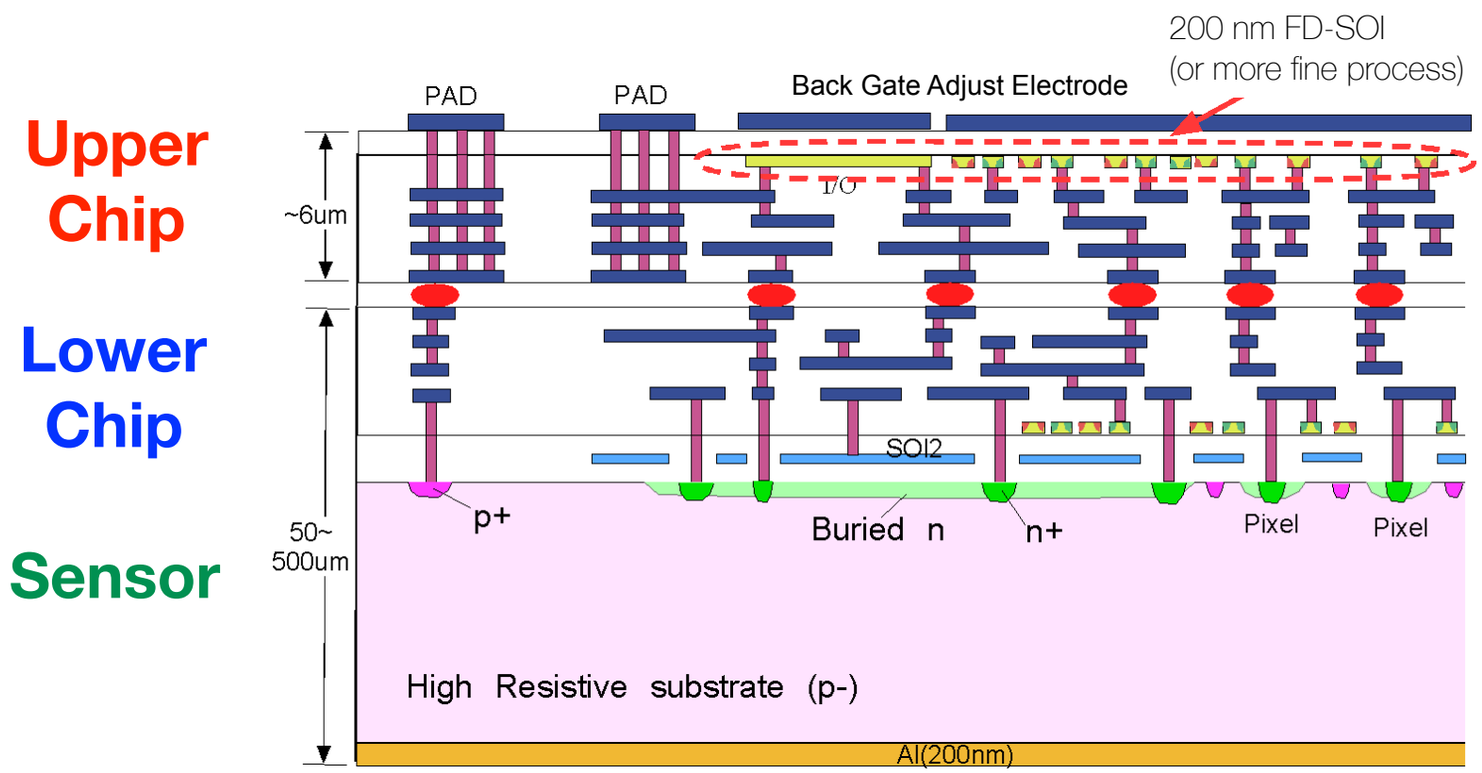
SOFIST ver.3

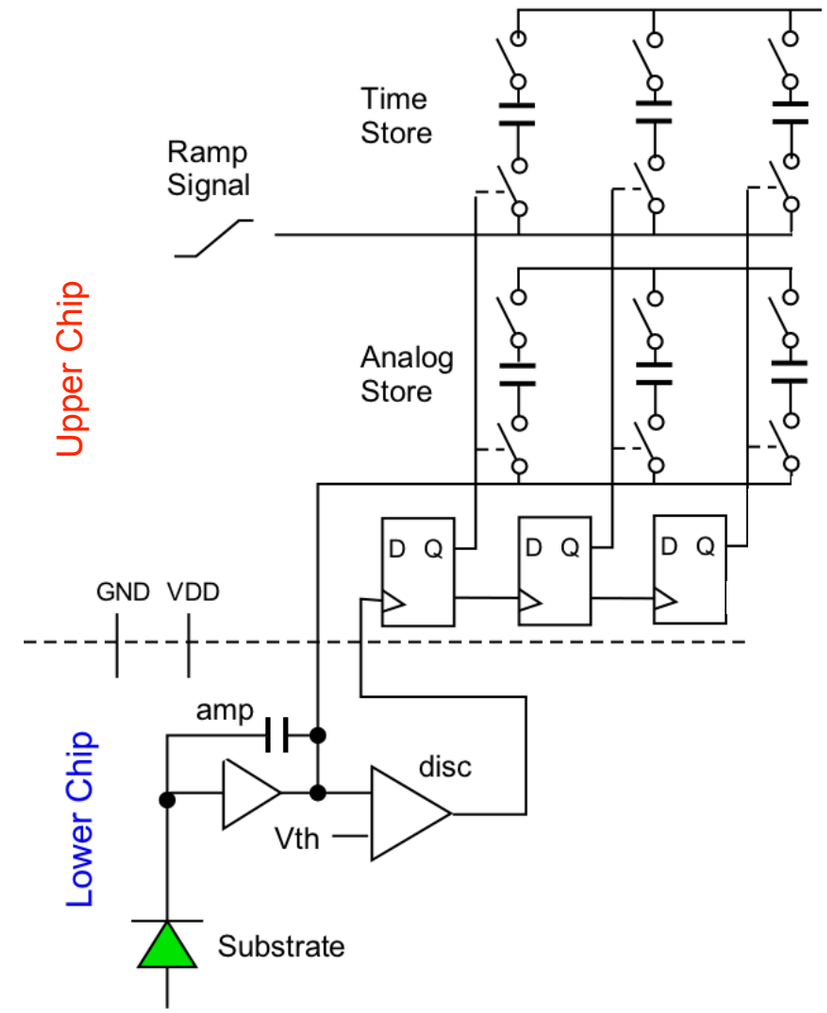


All the functions are implemented in a pixel to evaluate its functionality but lager pixel size.

SOFIST ver.4 (3D)

3D integration of SOI sensor
for implementation of complex circuit within 20 × 20 μm^2 pixel.



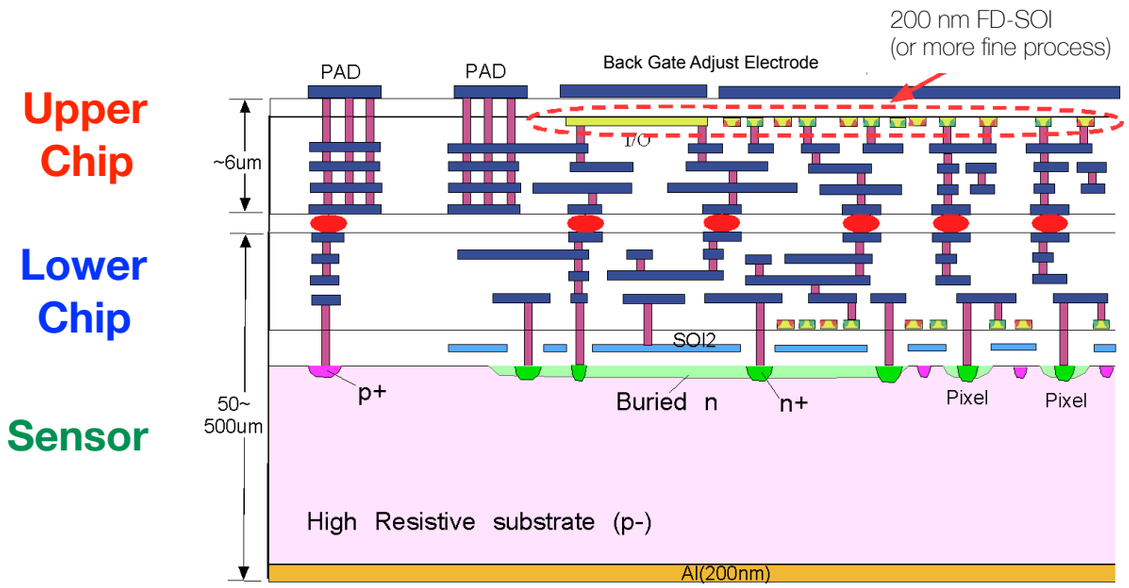


Illustrated by Y. Arai (KEK)

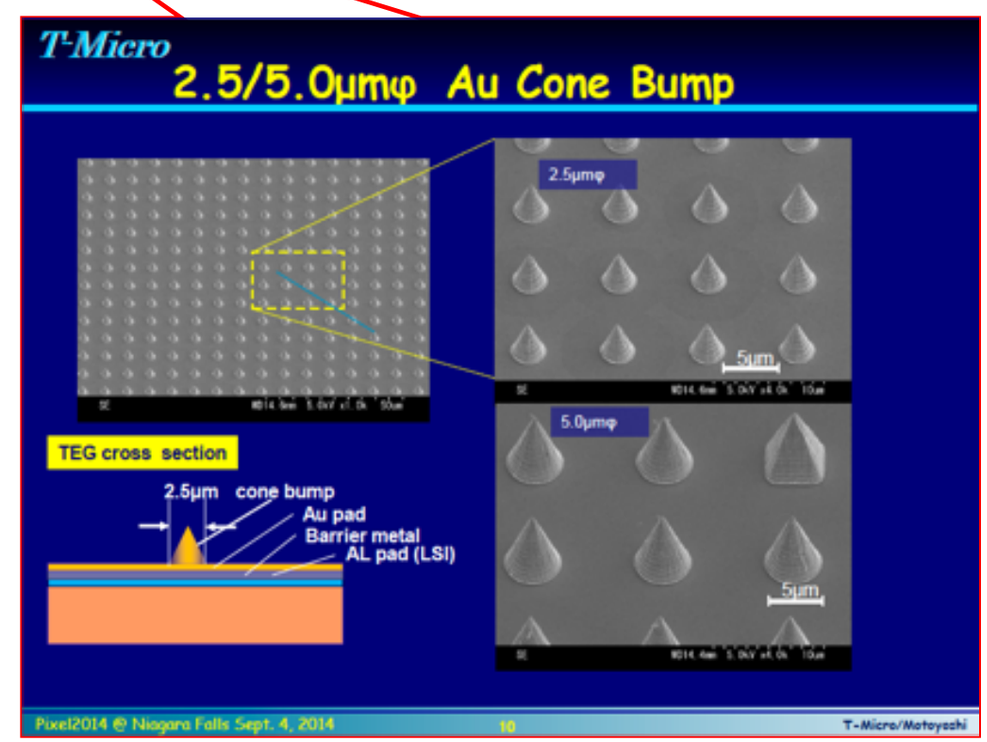
Upper chip: Digital part (D-FF, analog memories and timestamp memories up to 3 hits)
Lower chip: Analog part (pre.amp and comparator)

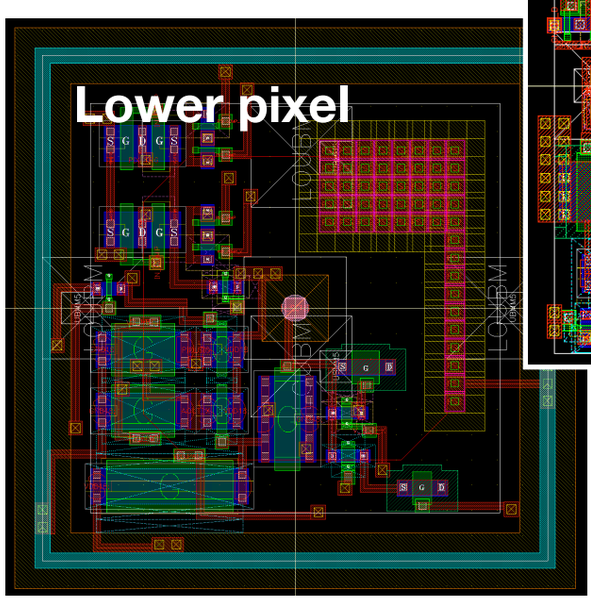
SOFIST ver.4 (3D)

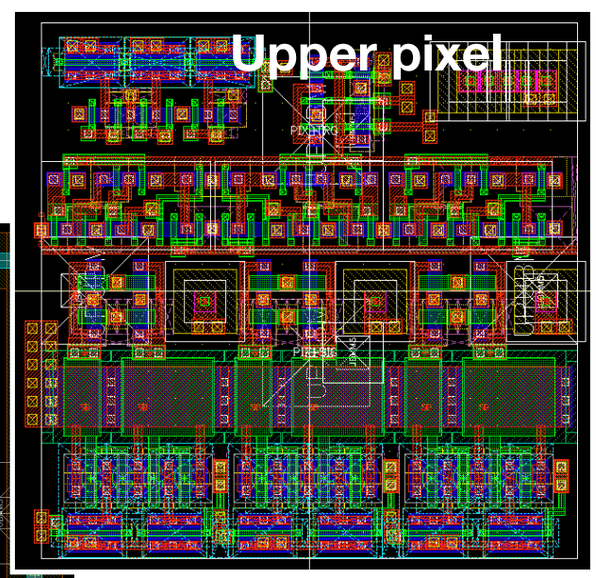
3D integration of SOI sensor
→Connect the upper and lower chip by Au cone bump (2.5 *μm*φ).



Tohoku MicroTec Co., Ltd.
http://www.t-microtec.com







Timestamp memory x 3
Analog signal memory x 3

3D integrated SOFIST ver.4
will be delivered in August 2018.

Summary

Requirements:

1) Single point resolution: better than 3 μm
   Pixel size: ~20 × 20 μm^2
   → SOFIST ver.1 achieved 1.4 μm

2) Time resolution: single-crossing (554 ns interval) time resolution
   → Preliminary: SOFIST ver.2 time resolution 1.97 μs (intrinsic)
   Currently time stamp memories are designed assuming on-chip 8-bit ADC.
   Need more precise memory and ADC (~12-bit).

3) Detector occupancy: < 2 %
   → SOFIST ver.2: 2 memories for analog signal and timestamp respectively
   Shift register is not tested yet.
   → SOFIST ver.3 and 4: 3 memories for analog signal and timestamp respectively
   Preparing DAQ system and waiting for finishing 3D integration.

4) Low material budget: $X \leq 0.1 - 0.2$ % X_0 / Layer
   corresponds to ~ 100 - 200 μm Si, including supports, cables and cooling
   → SOFIST ver.2: Timestamp function of the thinned sensor (75 μm) is working
   Spatial resolution is under studying.
   low-power ASICs (~ 50 mW/cm^2) + gas-flow cooling
   → SOFIST ver.2: Pixel array ~ 500 mW/cm2, Output buffer ~ 100 mW (14 bit)
   We will start to consider low power design/operation of pixel circuit.

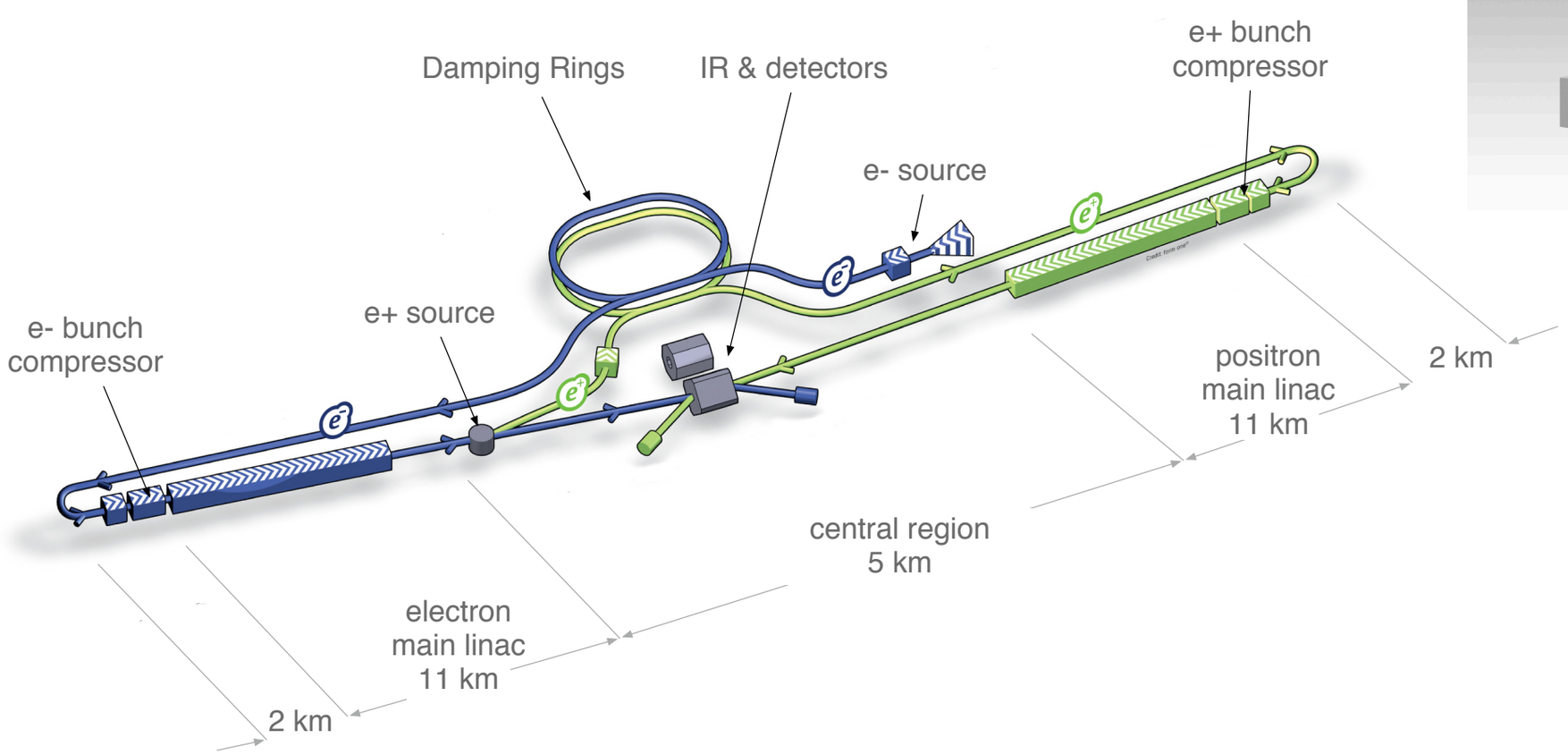
5) Radiation hardness:
   TID : < 1 kGy / year
   NIEL: < 10^{11} 1MeV n_{eq} / cm^2 / year
   → TID tolerance of 1 MGy is achieved by FPIX (SOIPIX) (K. Hara, Vertex 2017)
   Preparing irradiation test (^{60}Co gamma-ray) of SOFIST ver.2 (June, 2018)

Backup

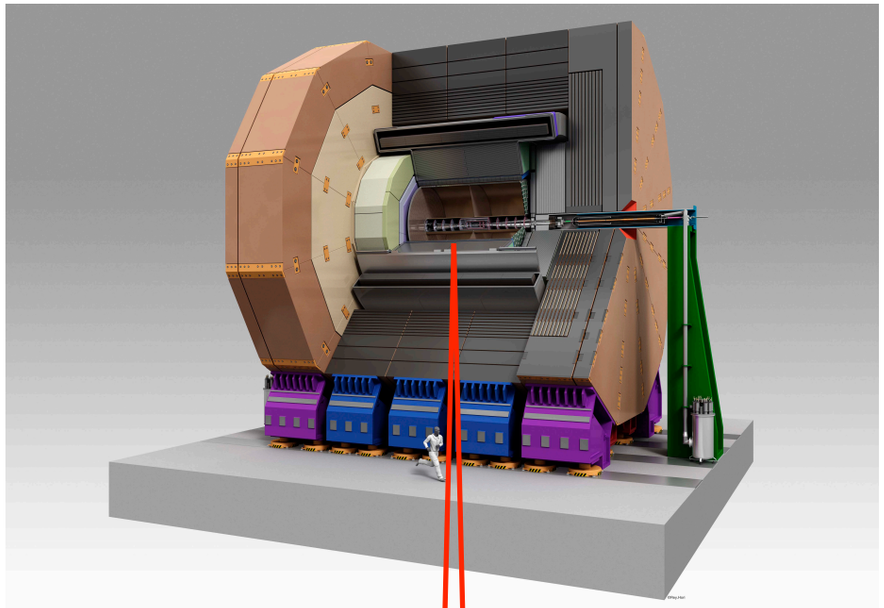
ILC Experiment

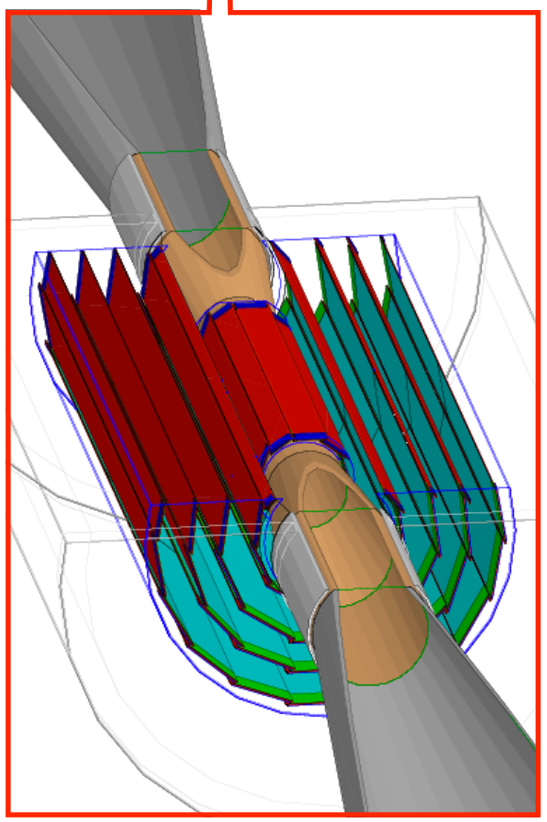
ILC Experiment

- e^+e^- linear collider
- Center of mass energy: 250 - 500 GeV (extendable to 1 TeV)
- Precise measurement of the Higgs boson
- Search for beyond the Standard Model



ILC detector concept (ILD)





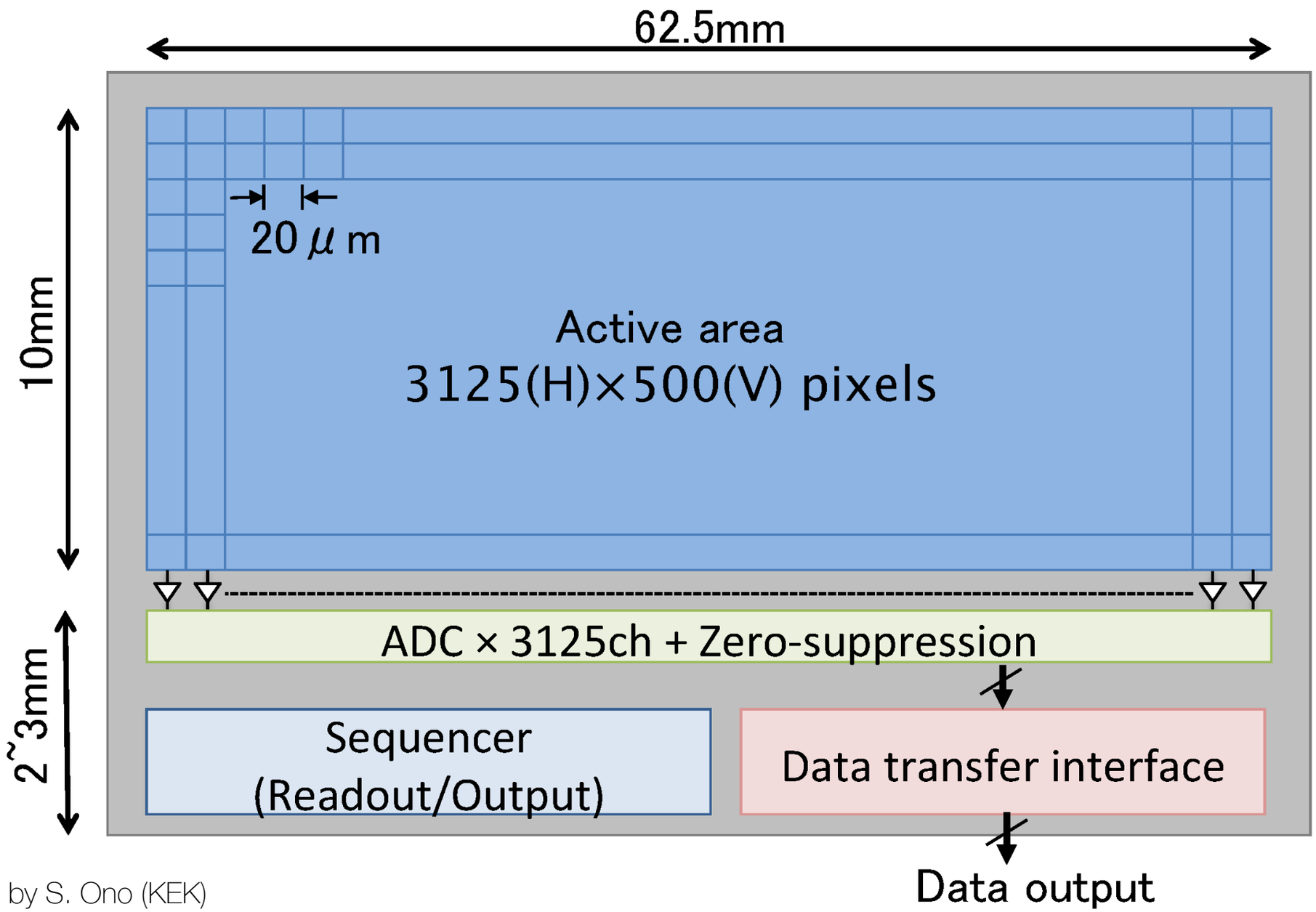
Vertex detector geometry (VTX-SL)

ILC TDR vol.4: Detectors
ILD Concept Group, T. Abe et al., arXiv:1006.3396 [hep-ex].

SOI sensor for ILC: SOFIST

SOFIST: SOi sensor for Fine measurement of Space and Time

Conceptual SOI pixel sensor for the ILC (inner most layer of the vertex detector).

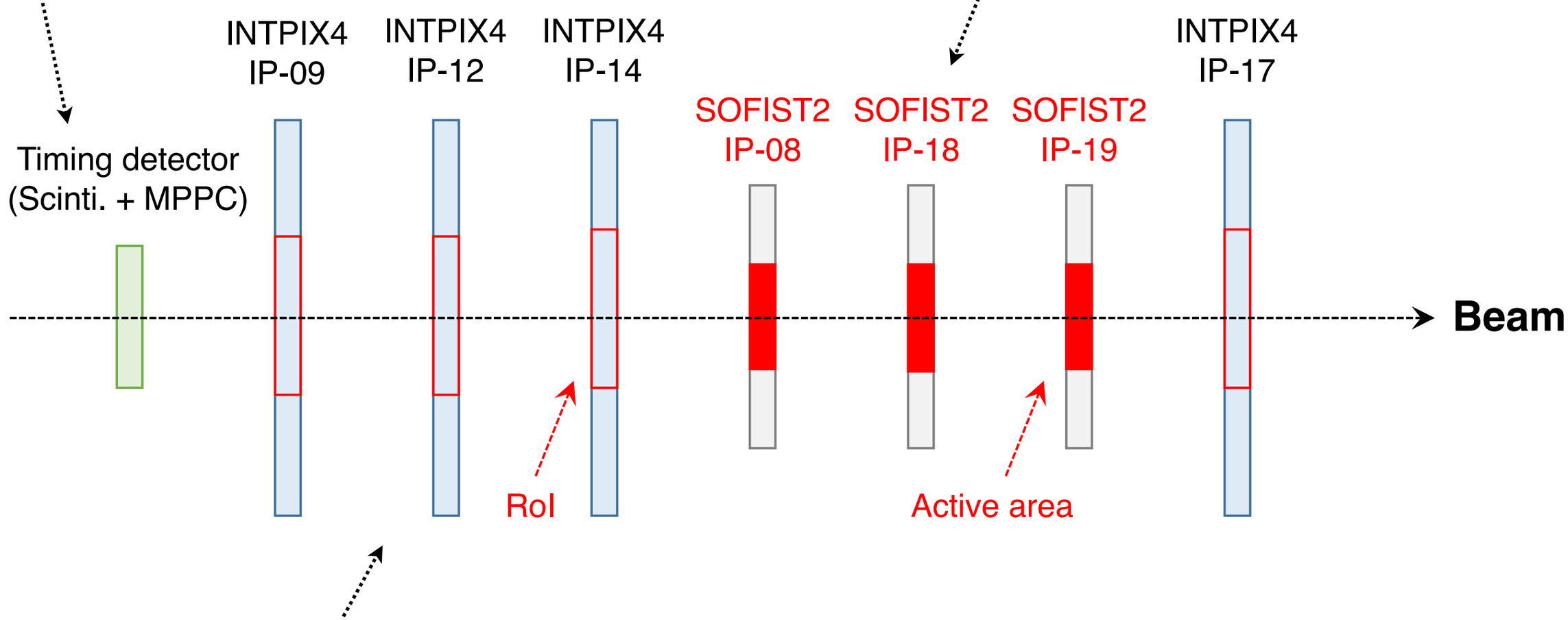


Designed by S. Ono (KEK)

Setup

Timing detector
Scinti. size: 3 × 3 mm^2
MPPC size: 3 × 3 mm^2
Readout: Comp. + AND + NIM converter
(Signal is sent to Master DAQ, SEABAS2)

SOFIST2
Pixel size: 25 × 25 μm^2
Pixel array: 80 × 64 (2.0 × 1.6 mm^2)
Readout: External 12-bit ADC (SEABAS2)

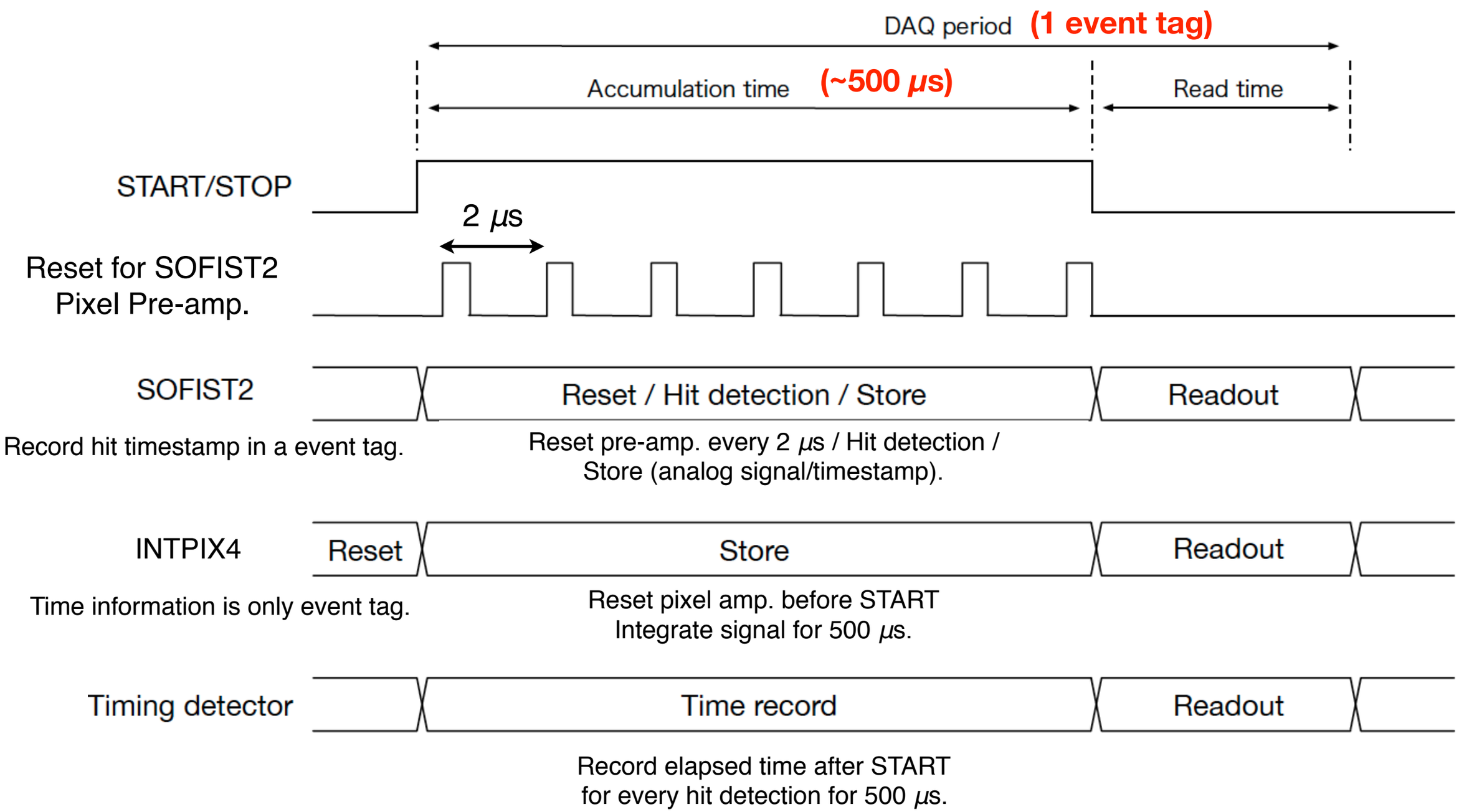


Telescope (INTPIX4)
Pixel size: 17 × 17 μm^2
Pixel array: 832 × 512 (14.1 × 8.7 mm^2)
Function: Region of Interest
Readout: External 12-bit ADC (SEABAS2)

INTPIX4 はピクセル数が多いので
1 frame 読み出すと時間がかかる.
SOFIST2 と同程度の領域だけを
読み出す（RoI）.

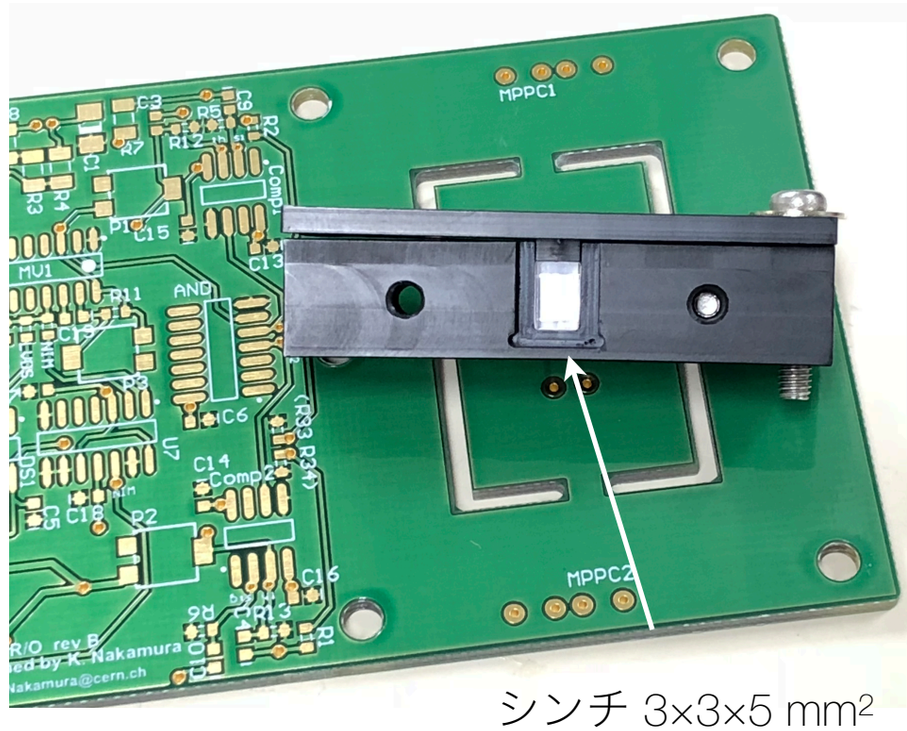
DAQ for Beam Test

Operation of each detector in 1 event tag (DAQ period)

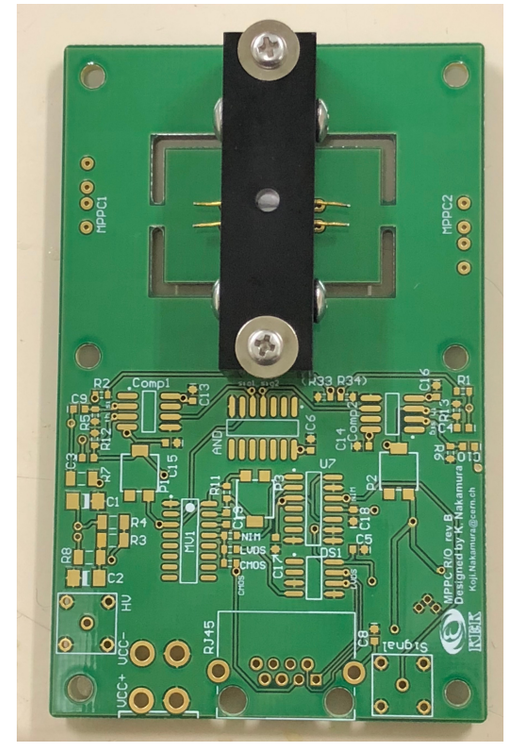


Timing Detector

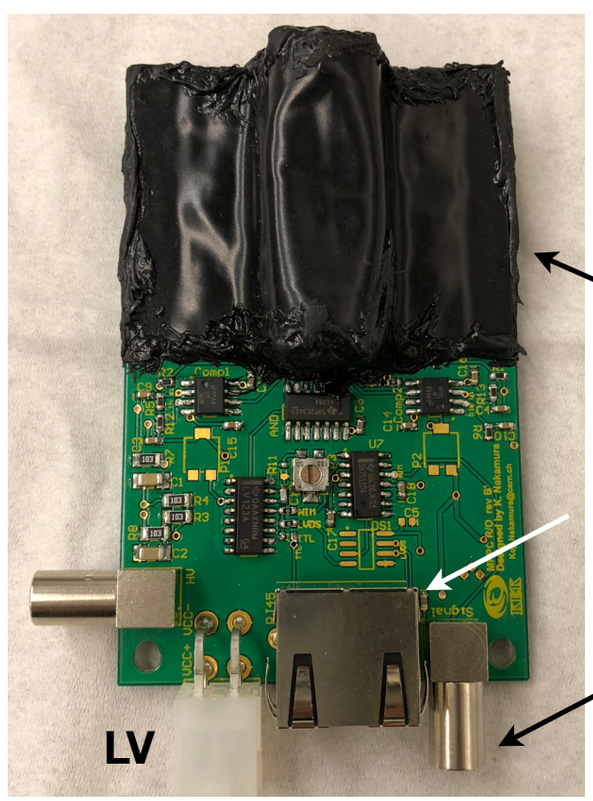
ブラックアクリル製のハウジング
シンチと MPPC を収める.
（飯村精密に工作依頼）



シンチ 3×3×5 mm^2



信号読出し基板は ATLAS グループが設計
（P 板.com で作製）



遮光のためブラックテープで巻いたあとに
シーラントで目張り

DAC control (DAC for COMP Vth)

HV

Signal (NIM)

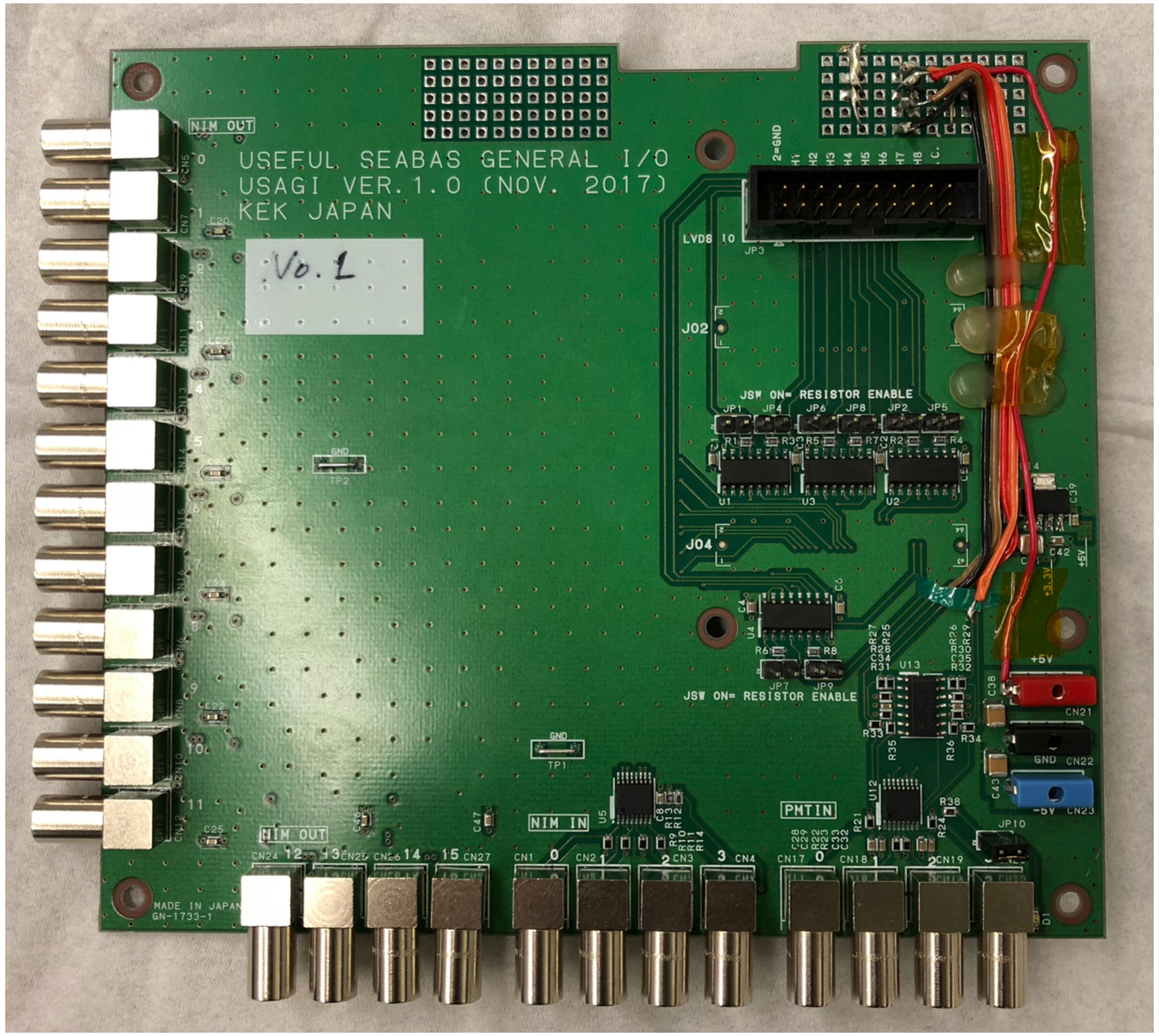
LV

USAGI I/O

SEABAS2 用 Fanin/Fanout ボード

NIM IN 8ch
NIM OUT 8ch
PMT IN 4ch
LVDS 8ch

電源: ± 5V



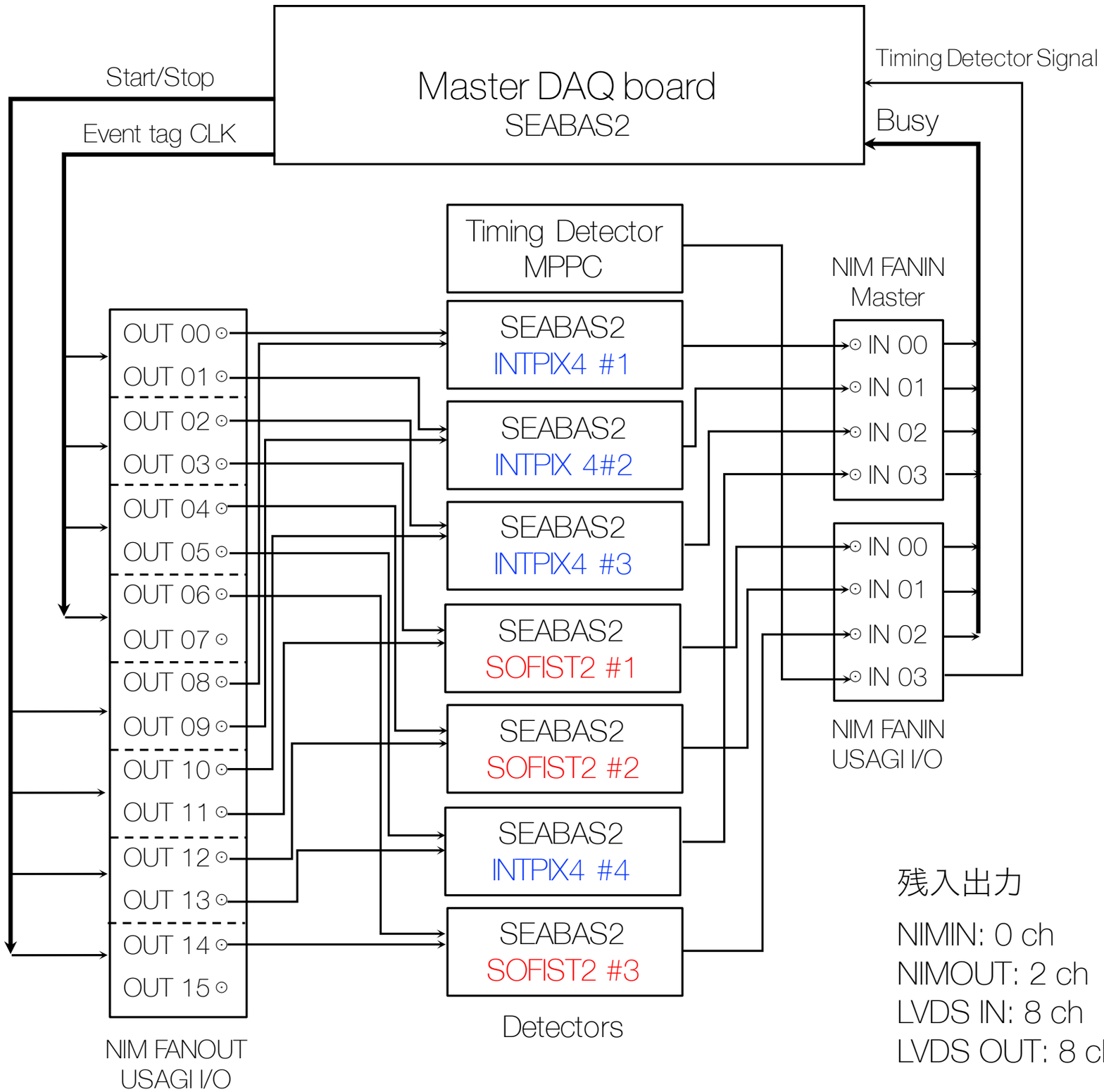
設計: 池上先生

作製: GND

全体構成

Master の入出力信号は

- Start/Stop
- Event tag CLK
- Busy
- MPPC signal



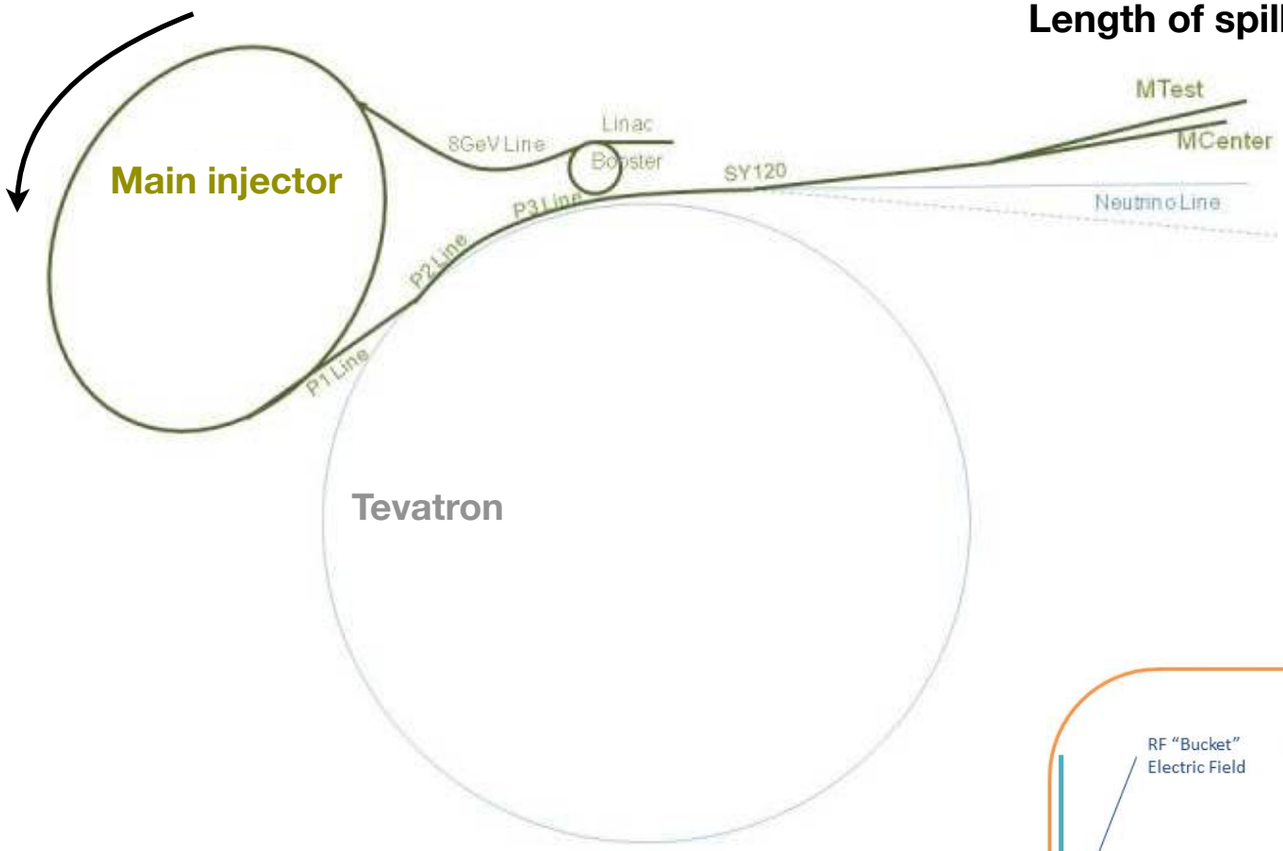
残入出力

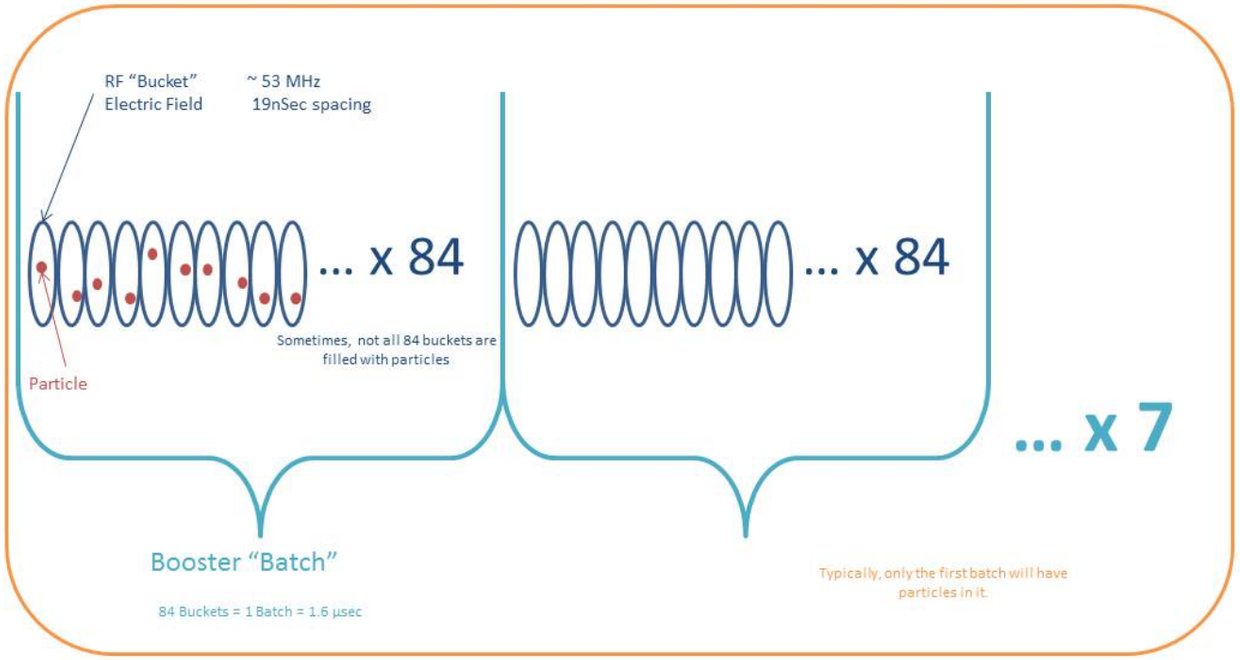
NIMIN: 0 ch
NIMOUT: 2 ch
LVDS IN: 8 ch
LVDS OUT: 8 ch

Beam

The size of main injector: 11 *μs*

Beam test@FTBF (MTest)
Length of spill: 4 s

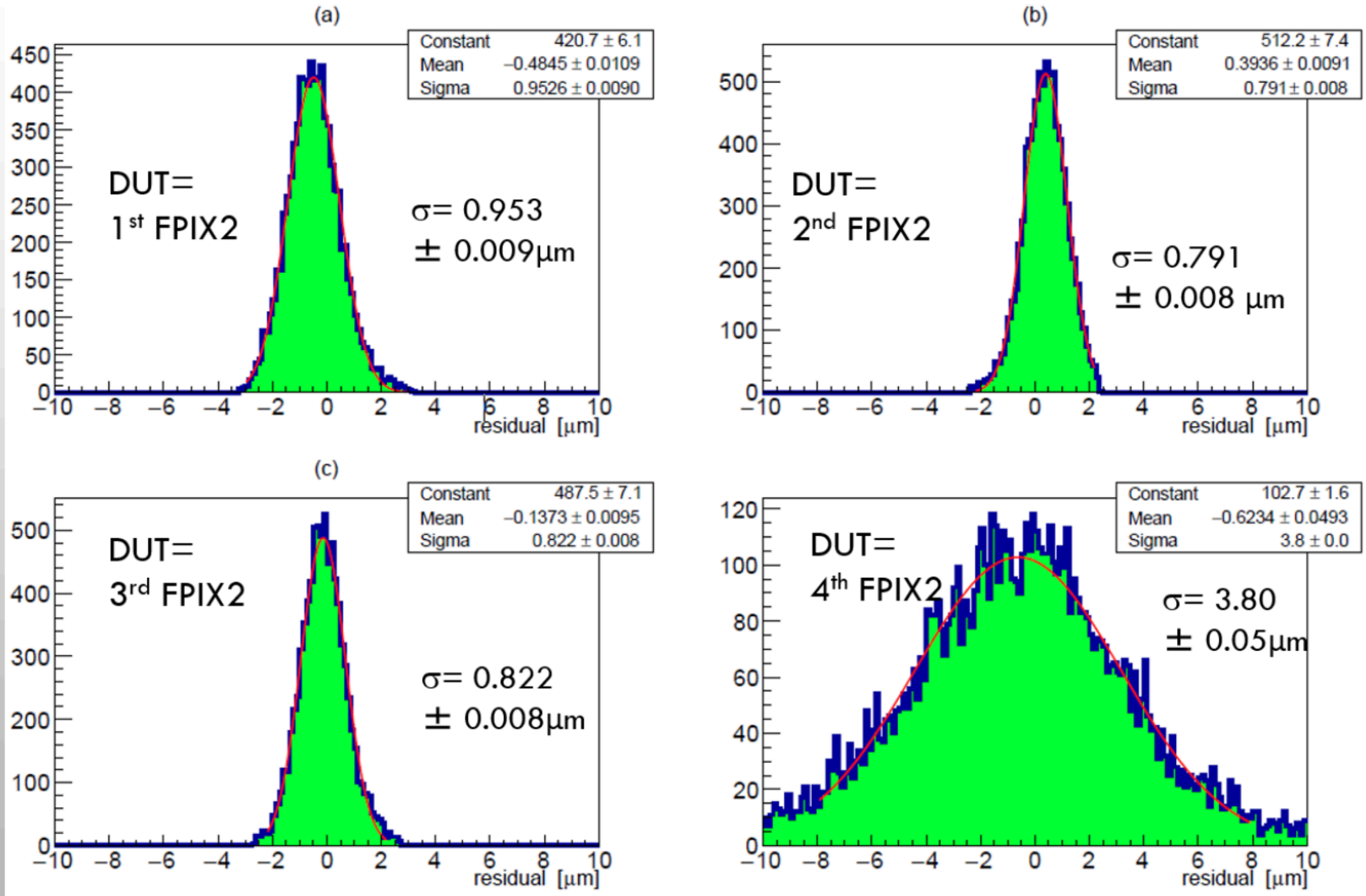




7 Batches = 1 MI Cycle = 11.2 microSec

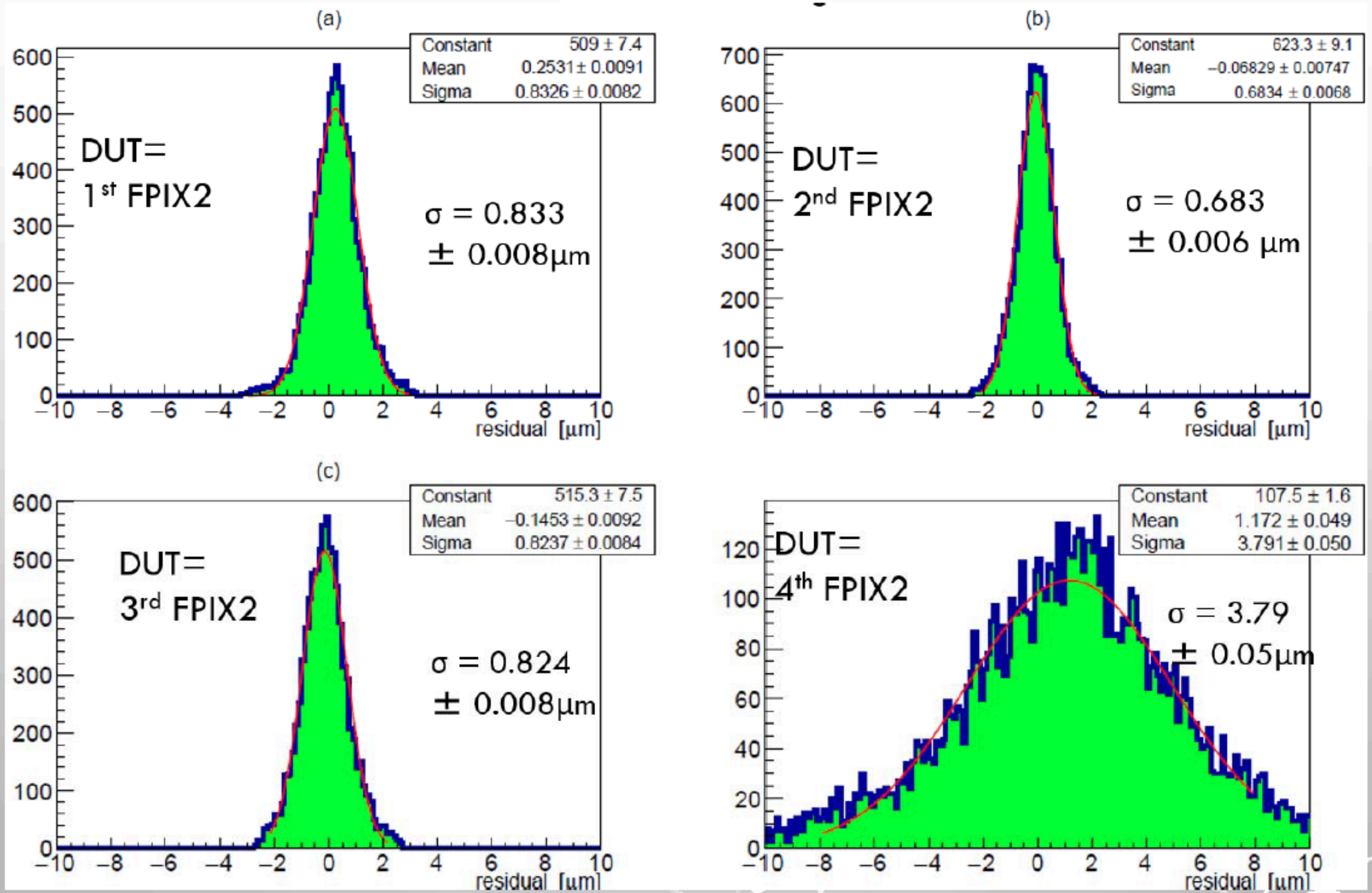
RESIDUALS in X

- Residuals of DUT hit wrt the track reconstructed using other three FPIXs



RESIDUALS in Y

Residuals of DUT hit wrt the track reconstructed using other three FPIXs

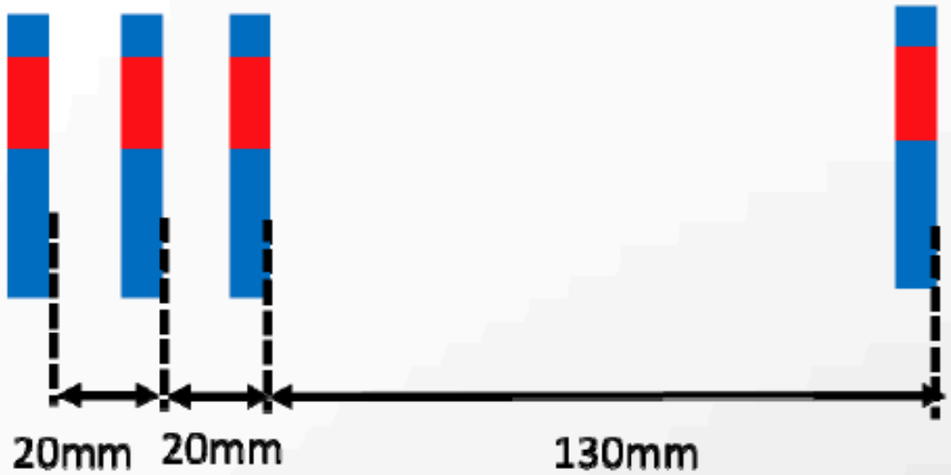


INTRINSIC SPATIAL RESOLUTION

- Observed residual spread: σ_{obs}

$$\sigma_{\mathrm{obs}} = \sqrt{\sigma_{\mathrm{int}}{}^2 + \sigma_{\mathrm{track}}{}^2}$$

under an assumption all four FPIXs have the same intrinsic resolution and contributions of misalignment/ multiple scattering are negligible (=conservative σ_{track} value), we can calculate σ_{int} analytically



	1X	2X	3X	4X
Measured residual	0.953 ± 0.009	0.791 ± 0.008	0.822 ± 0.008	3.80 ± 0.05
Intrinsic resolution	0.711	0.648	0.703	0.75
	1Y	2Y	3Y	4Y
Measured residual	0.833 ± 0.008	0.683 ± 0.006	0.824 ± 0.008	3.79 ± 0.05
Intrinsic resolution	0.622	0.600	0704	0.75

Intrinsic resolution:
0.65~0.71 μm in X
0.60~0.70 μm in Y
(effect of imperfect alignment included)