Study for Retriggers of SiW-ECAL

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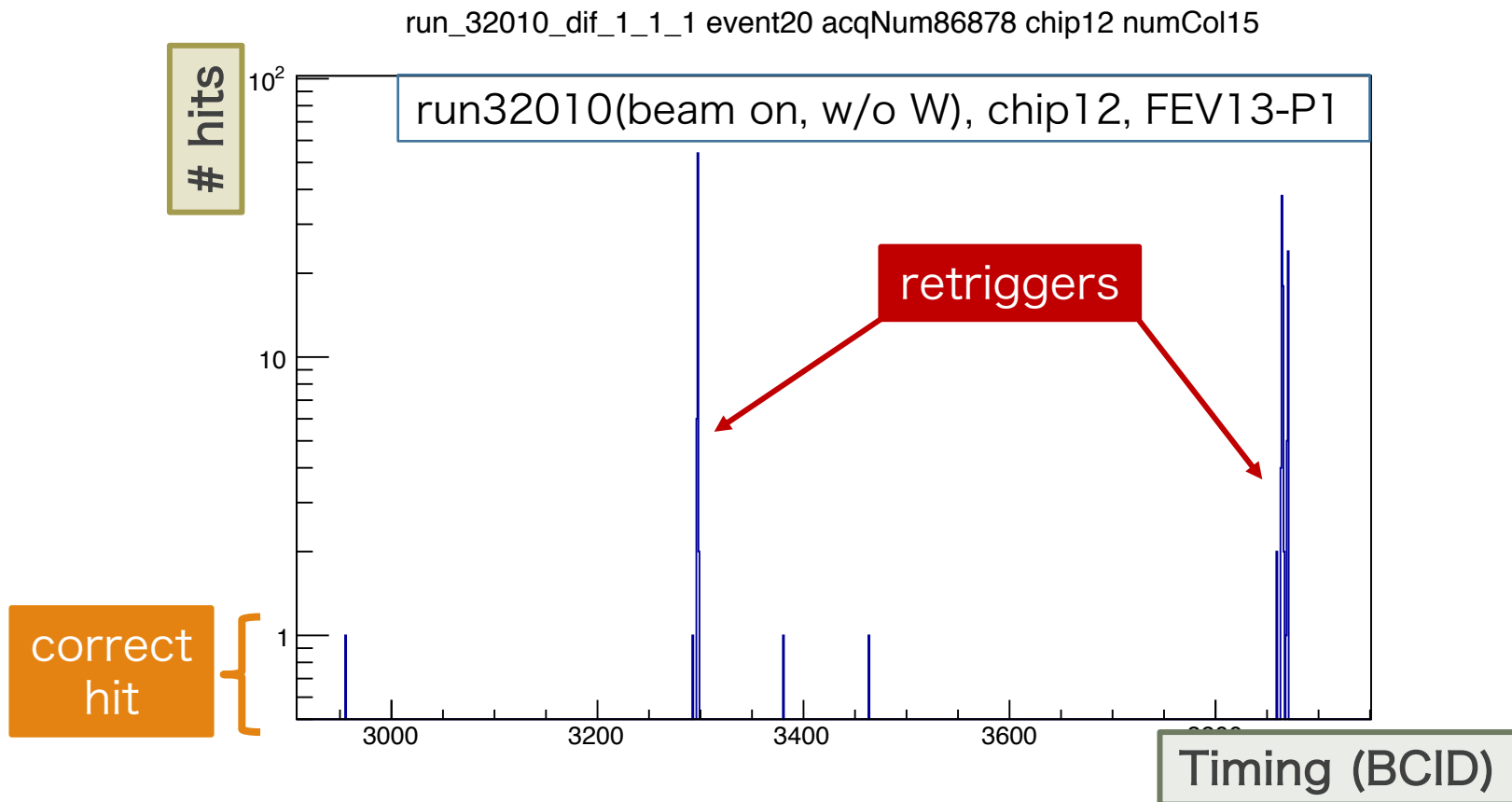
The University of Tokyo

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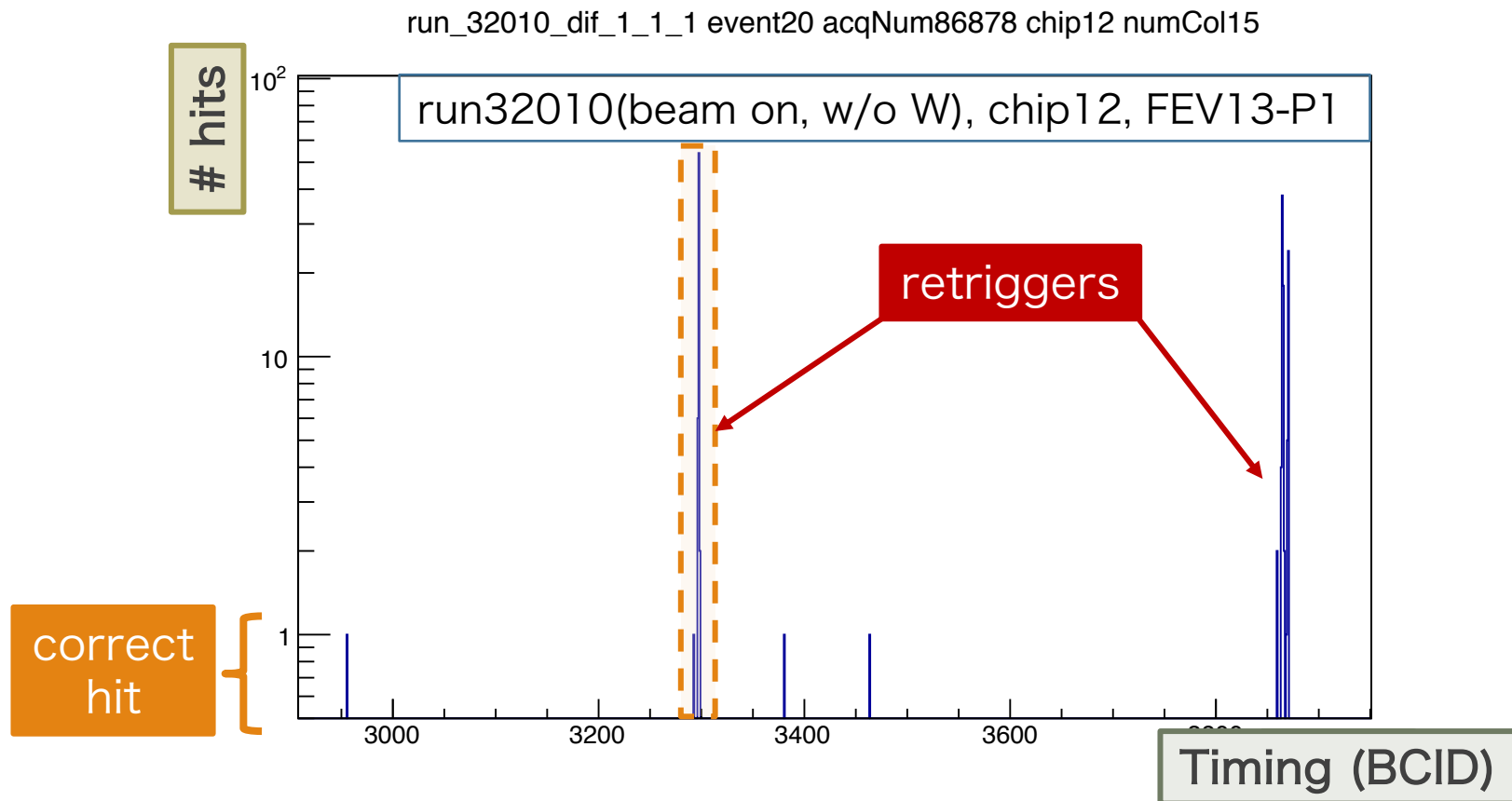
What are Retriggers?

➢ SiW-ECAL technological prototype has an issue called "**retriggers**".
  - many fake hits just after correct hit(s)
  - consecutive BCIDs

➢ **Memory cells are occupied by retriggers and may fail to store normal events.**

run_32010_dif_1_1_1 event20 acqNum86878 chip12 numCol15

run32010(beam on, w/o W), chip12, FEV13-P1

retriggers

correct hit

hits

Timing (BCID)

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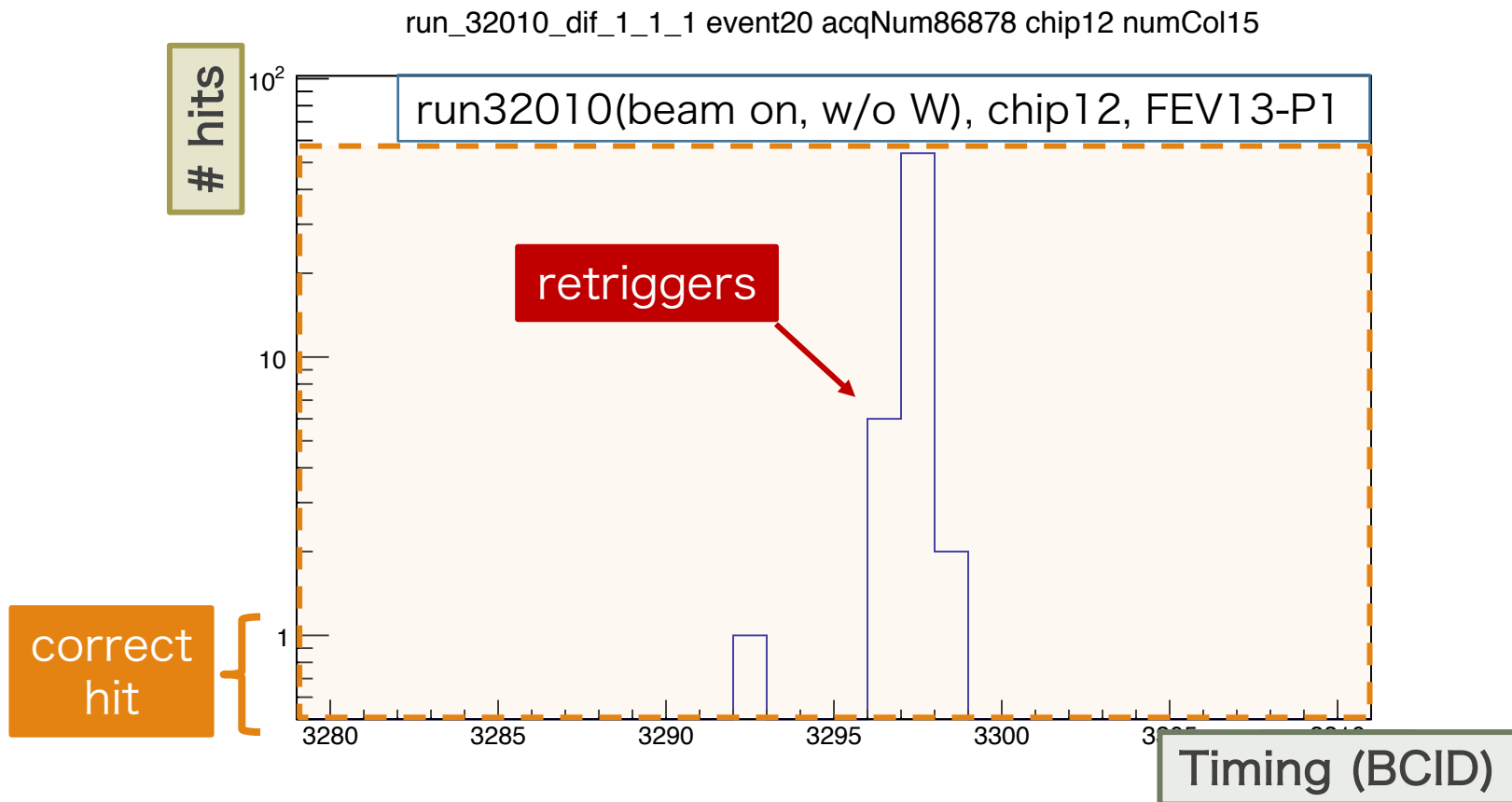> **Memory cells are occupied by retriggers and may fail to store normal events.**

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Target of this study

> ➢ Develop retrigger discrimination method
> ➢ Evaluate retriggers
> ➢ Consider its cause

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run32010(beam on, w/o W), chip12, FEV13-P1

hits

retriggers

correct hit

Timing (BCID)
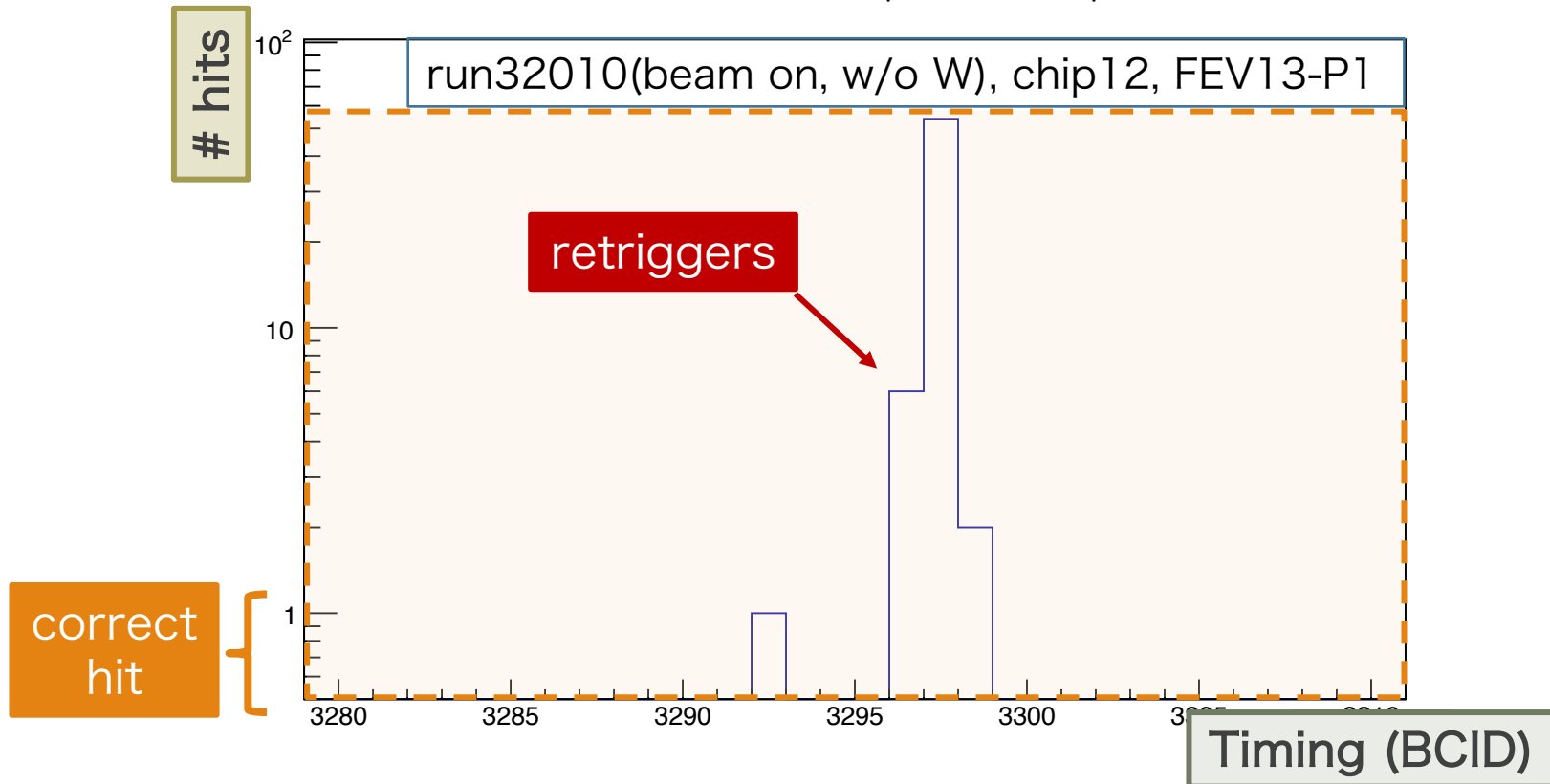
Data acquisition mechanism of SiW-ECAL

- ● **Geometrical structure**
  - ◦ Si pixel: 5.5×5.5 mm^2
  - ◦ $32 \times 32 = 1024$ ch / slab
  - ◦ 16 ASICs / slab
  - ◦ 4 Si wafers / slab

- ● **Readout information**
  - ◦ Bunch Crossing ID (**BCID**)
    - f = 5 MHz, $\Delta t = 0.2$ μs
  - ◦ Hit bit
    - ◦ self-triggered by each channel
  - ◦ Analogue output (Any two of the three)
    - ◦ Charge [1]High/[2]Low gain, [3]Timing

One ASIC
One channel
★ Hit
Data acquisition area
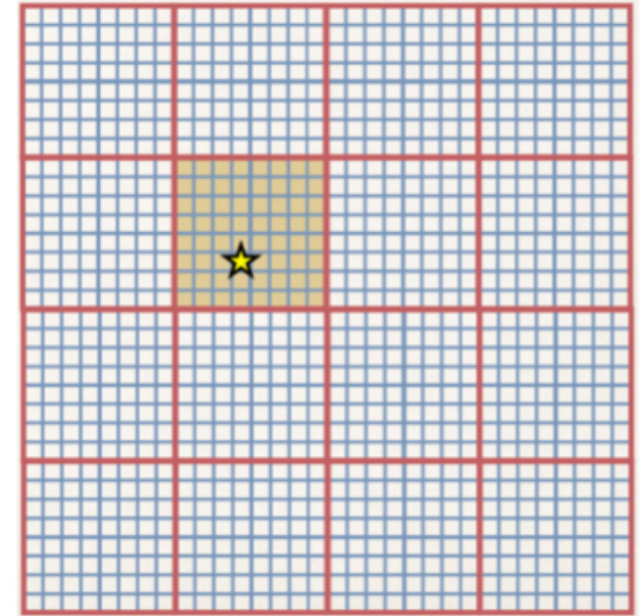
- ● **Readout mechanism**
  - ◦ independently on each ASIC
  - 1. Some tracks are triggered within one BCID interval (0.2 μs).
  - 2. Analogue outputs from all channels are stored in memory cells (15 SCAs).
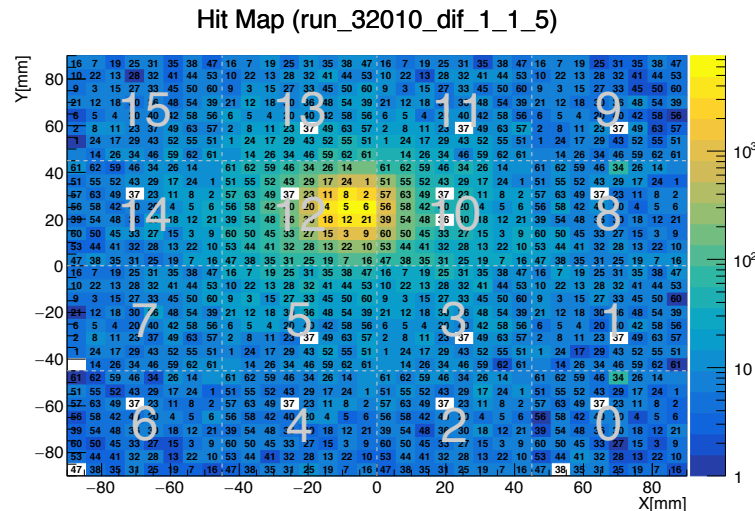 - 3. After the acquisition phase(5 Hz, ~ 2.5 ms), all stored data is read out.

Studies for retriggers

● Setup

◦ We used following data in this talk.

◦ The data used for evaluation was obtained in TB2019 @ DESY.

◦ All the results are based on FEV13-K2 so far.
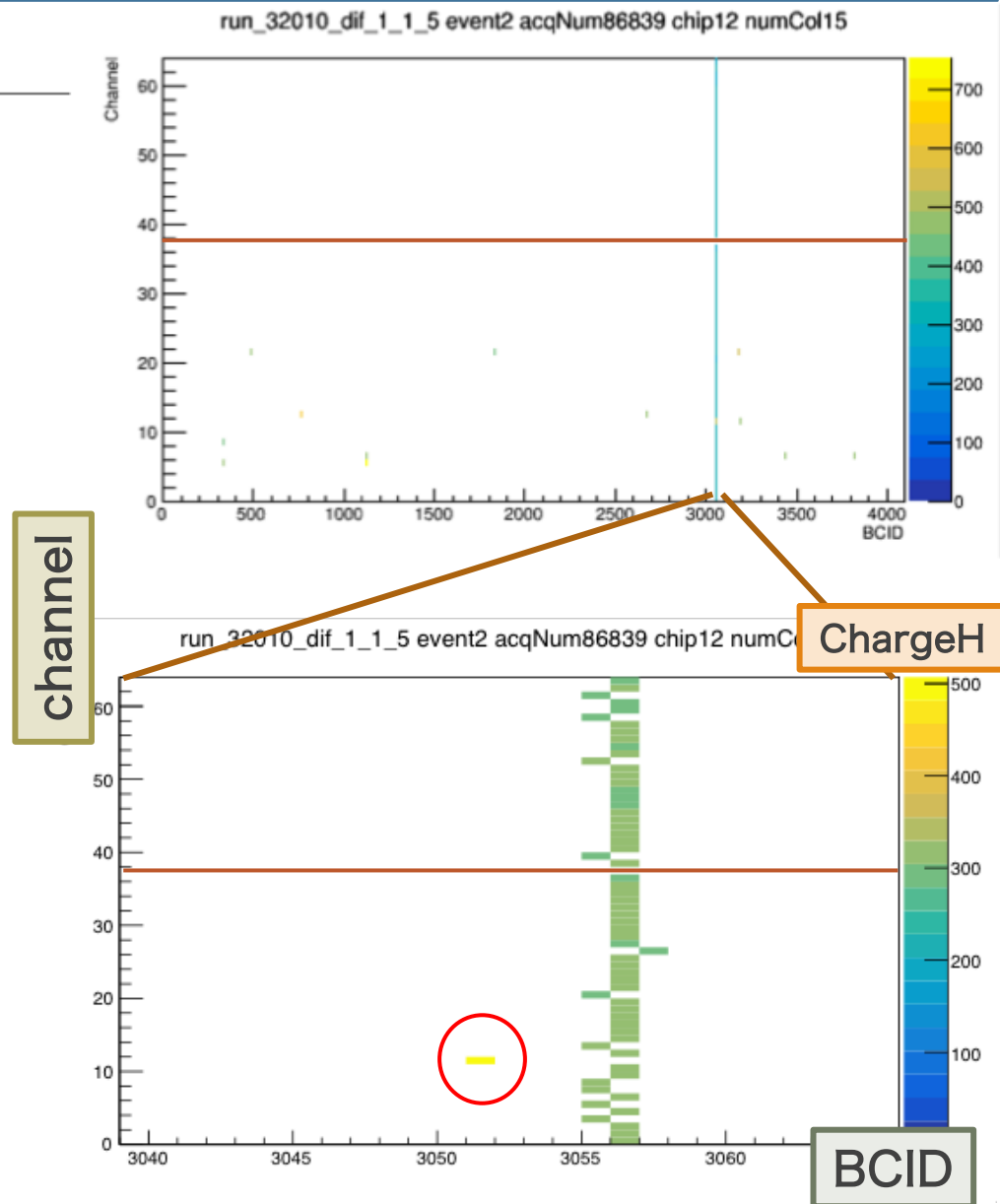
run	beam	Output mode	W absorber
32010	On (e- 3 GeV)	ADC	None

ADC mode: Charge High(×10) & Low(×1)

Hit Map (run_32010_dif_1_1_5)

Retriggers: Structure

BCID vs Triggered channels

● The retriggers looks "line".

➢ Almost all channels are triggered.
  • except <u>masked channel</u> (ch. 37)
  • sometimes one or two channels do not triggered.

● Many consecutive hits occur after 4 - 6 BCIDs from the hit that looks normal. → "**Induction**"

run_32010_dif_1_1_5 event2 acqNum86839 chip12 numCol15

channel

ChargeH

run_32010_dif_1_1_5 event2 acqNum86839 chip12 numCo

BCID

Discrimination Method

- Previous one
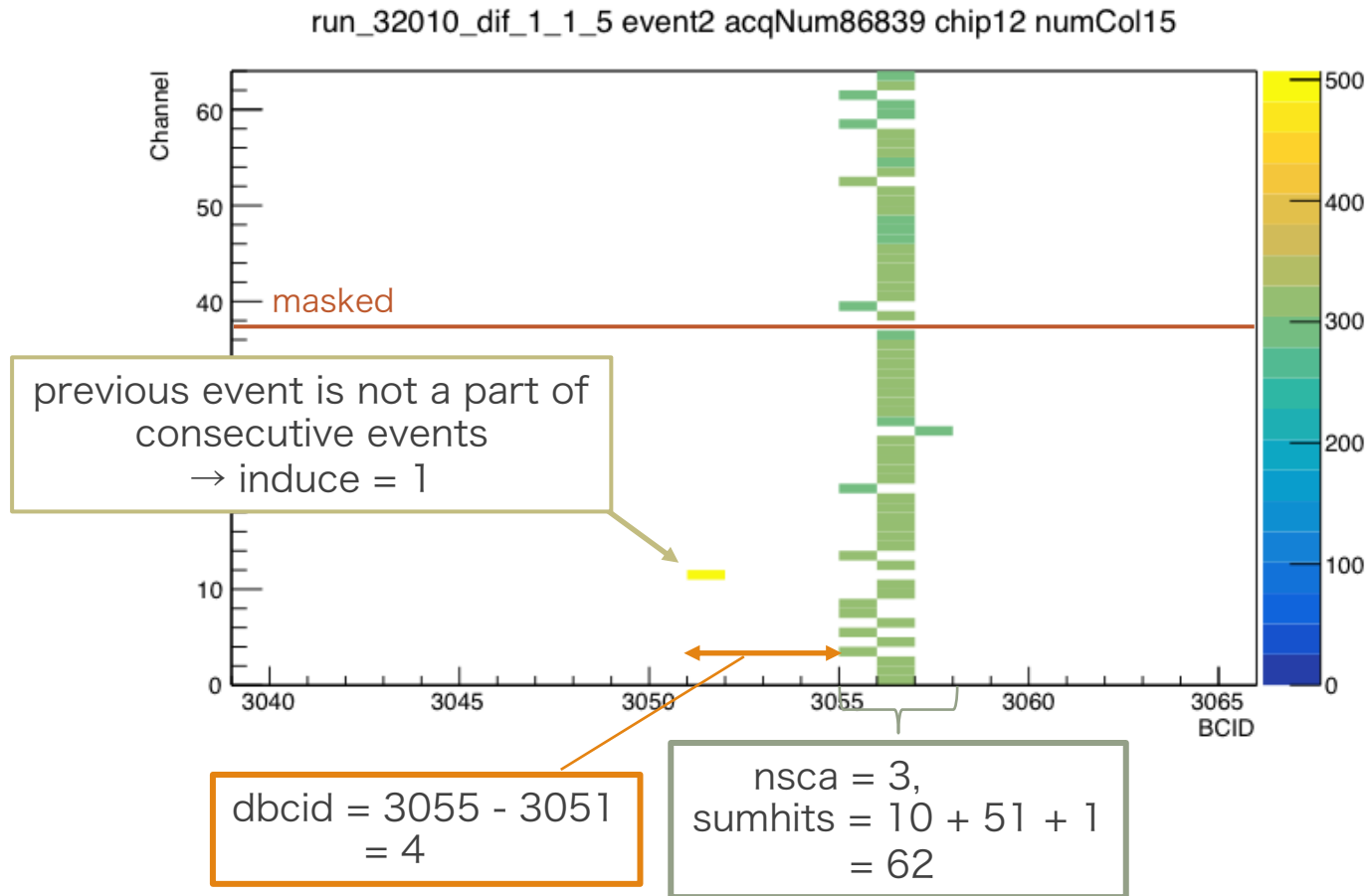 - ➤ Δbcid is less than 15 (adjustable) in 3 consecutive events
  - To extract only normal hits undoubtedly
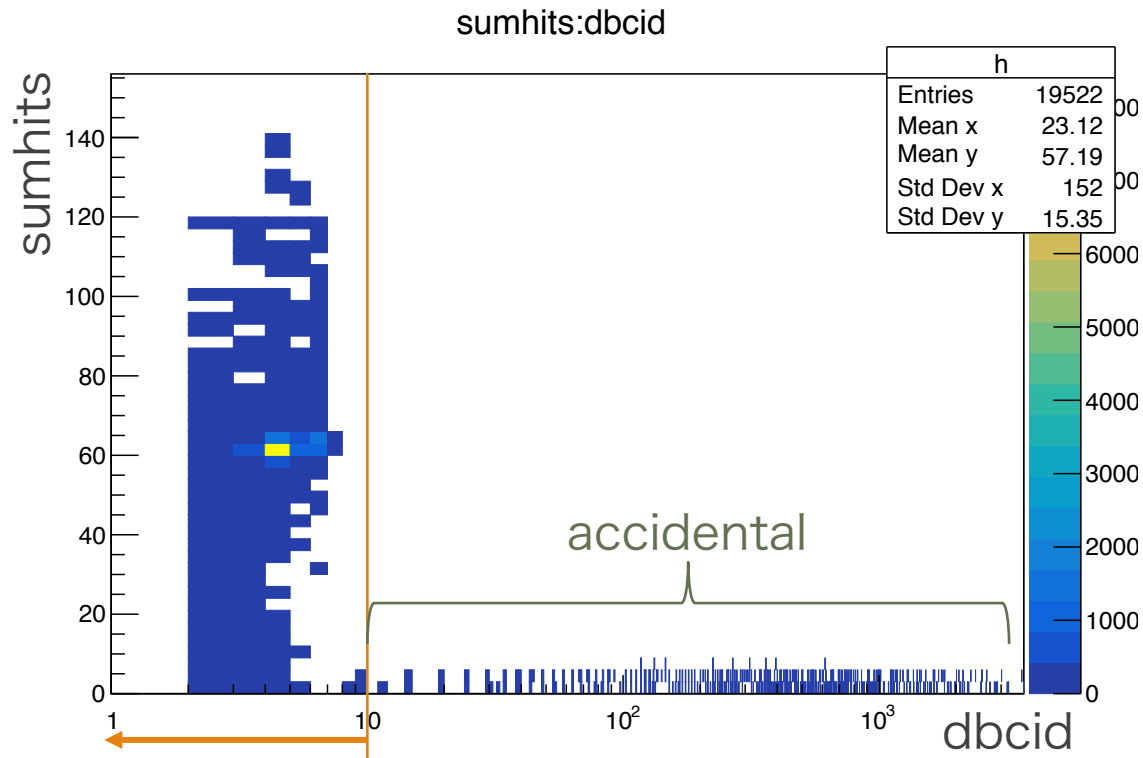   - Exclude even the induction events

- Developing one
  - To identify retriggers
  1. Merge triggers recorded by consecutive bcid
  2. Make the variables below to evaluate whether retrigger
     - nsca: Number of merged memory cells
     - sumhits: Total number of hits
     - dbcid: bcid interval between the induction and the start of the merged triggers
  3. Set some condition to discriminate normal / induction / retrigger
     - currently: dbcid < 10
     - work in progress

Discrimination Method

- Example:
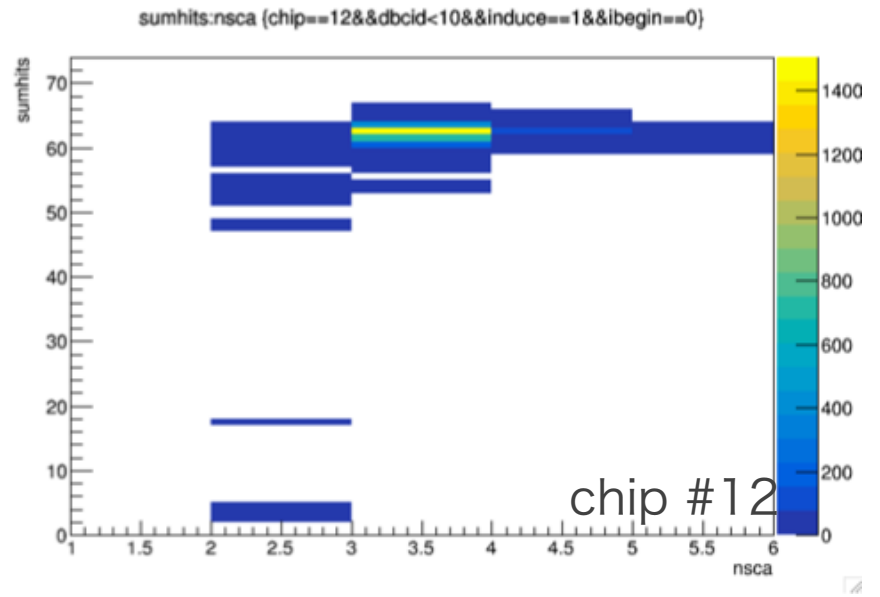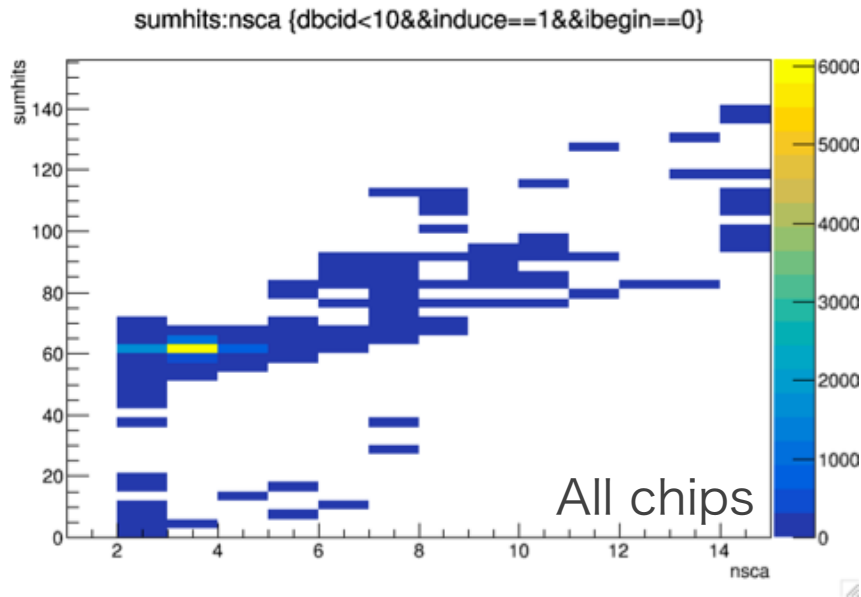 - The variables are saved in each time consecutive bcids are found.

run_32010_dif_1_1_5 event2 acqNum86839 chip12 numCol15

previous event is not a part of consecutive events
→ induce = 1

masked

dbcid = 3055 - 3051 = 4

nsca = 3,
sumhits = 10 + 51 + 1 = 62

dbcid vs sumhits

sumhits:dbcid

h	
Entries	19522
Mean x	23.12
Mean y	57.19
Std Dev x	152
Std Dev y	15.35

- Cut by dbcid is necessary to exclude accidentally consecutive events.
- dbcid < 10 (preliminary)

nsca vs sumhits

sumhits:nsca {dbcid<10&&induce==1&&ibegin==0}

All chips

sumhits:nsca {chip==12&&dbcid<10&&induce==1&&ibegin==0}

chip #12

- Basic cut is applied.
  - dbcid < 10, induce = 1, not the begin of acquisition
- In all chips result, there are a few events in which both variables are large.
  - They would be multi-retriggers.
- In only the irradiated chip, almost all the entry is [nsca = 3 & sumhits =62].

Hit Map (run_32010_dif_1_1_5)
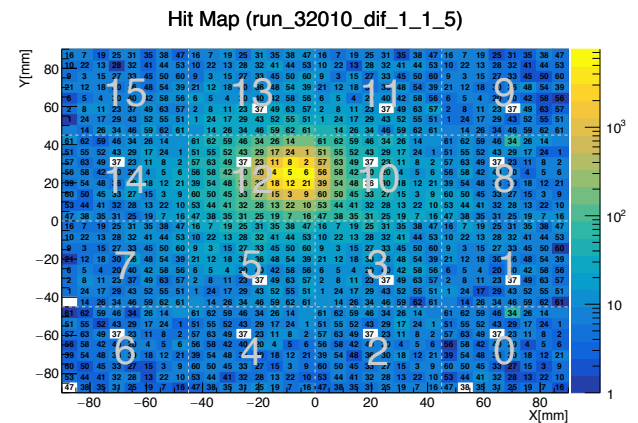
Retrigger Rate

run_32010_dif_1_1_5_retrigger.txt
RESULT
Acq Cycle: 14469, Acq Recorded: 7068

Triggered = Empty + Retriggers + Normal
Normal ⊃ Induction

Chip	Triggered	Empty	Retriggers	Induction	Normal	FullSCA	Rate(Induction/Normal)
0	2819	70	1907	297	842	93	0.353
1	3225	59	2224	350	942	84	0.372
2	2928	66	2007	322	855	77	0.377
3	5421	154	3567	653	1700	104	0.384
4	2855	73	1984	305	798	76	0.382
5	5288	175	3230	667	1883	83	0.354
6	2439	76	1661	238	702	80	0.339
7	3319	87	2274	374	958	89	0.390
8	3763	361	2249	425	1153	87	0.369
9	2905	83	1938	286	884	87	0.324
10	18520	788	10149	1895	7583	196	0.250
11	4809	123	3215	521	1471	107	0.354
12	61283	2635	13688	3805	44960	1769	0.085
13	5280	172	3288	635	1820	93	0.349
14	4116	96	2778	488	1242	74	0.393
15	2642	86	1666	309	890	78	0.347

- Many retriggers are occurred in the irradiated chips.
  - The electron tracks should induce the retriggers.

- The rate of induction/normal seems to be higher in chips far from beam spot.
  - Is there any causes other than the tracks?

Comparison of triggered charge

chip #12
Normal
Induction
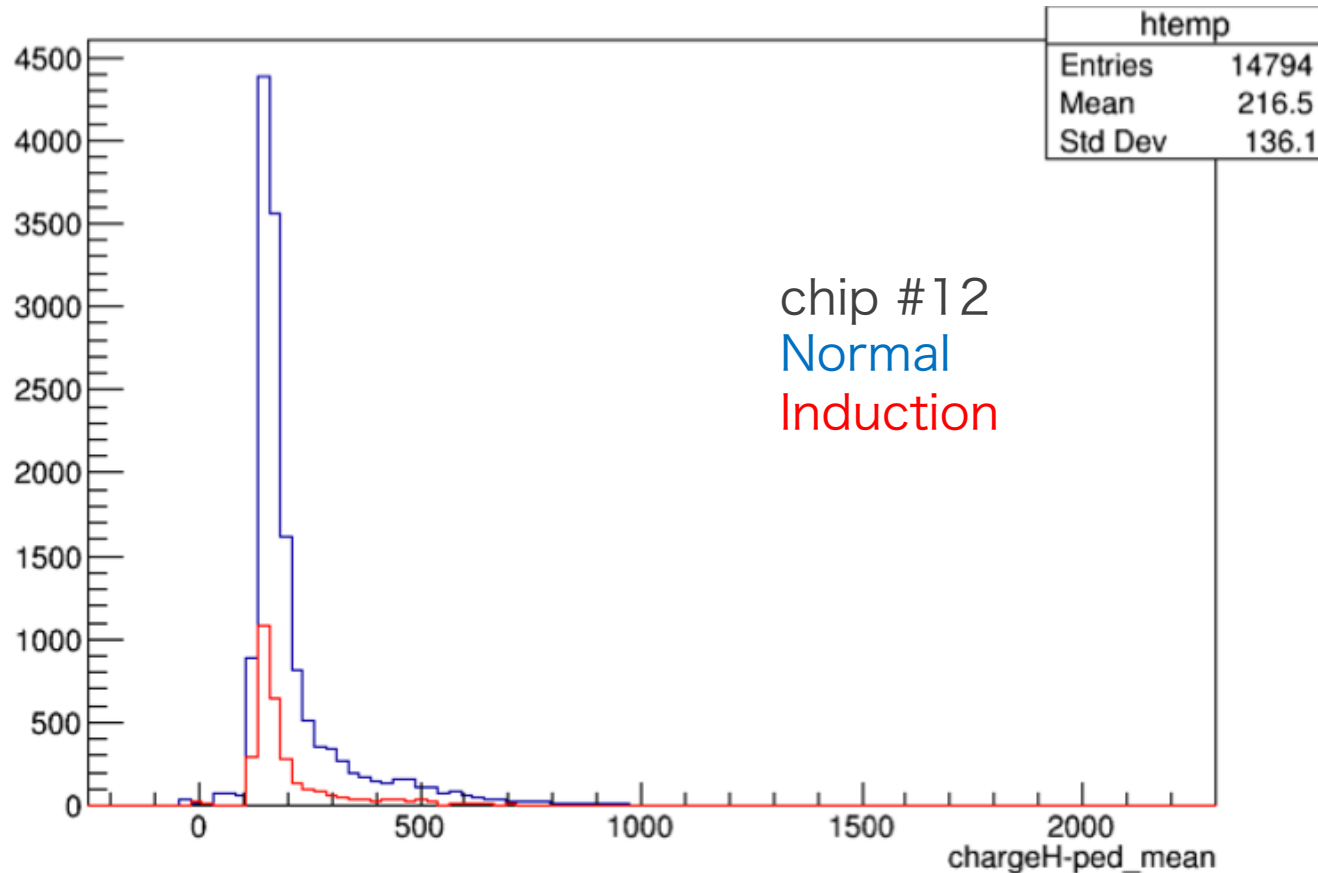
- No significant difference between normal and induction distribution.
  ◦ Induction can be treated as a normal hit? (Previously excluded.)

Summary

- New method to discriminate the retriggers is under developing.
- The retrigger rate is evaluated using current method.
- Many retriggers are occurred in the irradiated chips.
  - ➢ The electron tracks should induce the retriggers.
- The rate of induction/normal seems to be higher in chips far from beam spot.
  - ➢ Is there any causes other than the tracks?
- No significant difference of charge distribution between normal and induction.
  - ◦ Induction can be treated as a normal hit? (Previously excluded.)

To do

- ☐ Update the method which can identify the multi-retriggers.
- ☐ Comparison of the pedestal between normal and induction.
- ☐ Check the effect between each chips in the board.
- ☐ Verification using a test board
  - • after the situation of COVID-19 calms down.

additional

SiW-ECAL technological prototypes

Vincent Boudry, LCWS2019 Sendai

Major changes in FEV11→13

➤ ASIC: SKIROC2 → 2A
– individual threshold control
– improvement on TDC resolution

➤ Separation of power layers
– power supply for analogue and digital
– improvement on noise level

➤ Capacitor for Power Pulsing
– 0.4 mm thickness, 40 mF x 6
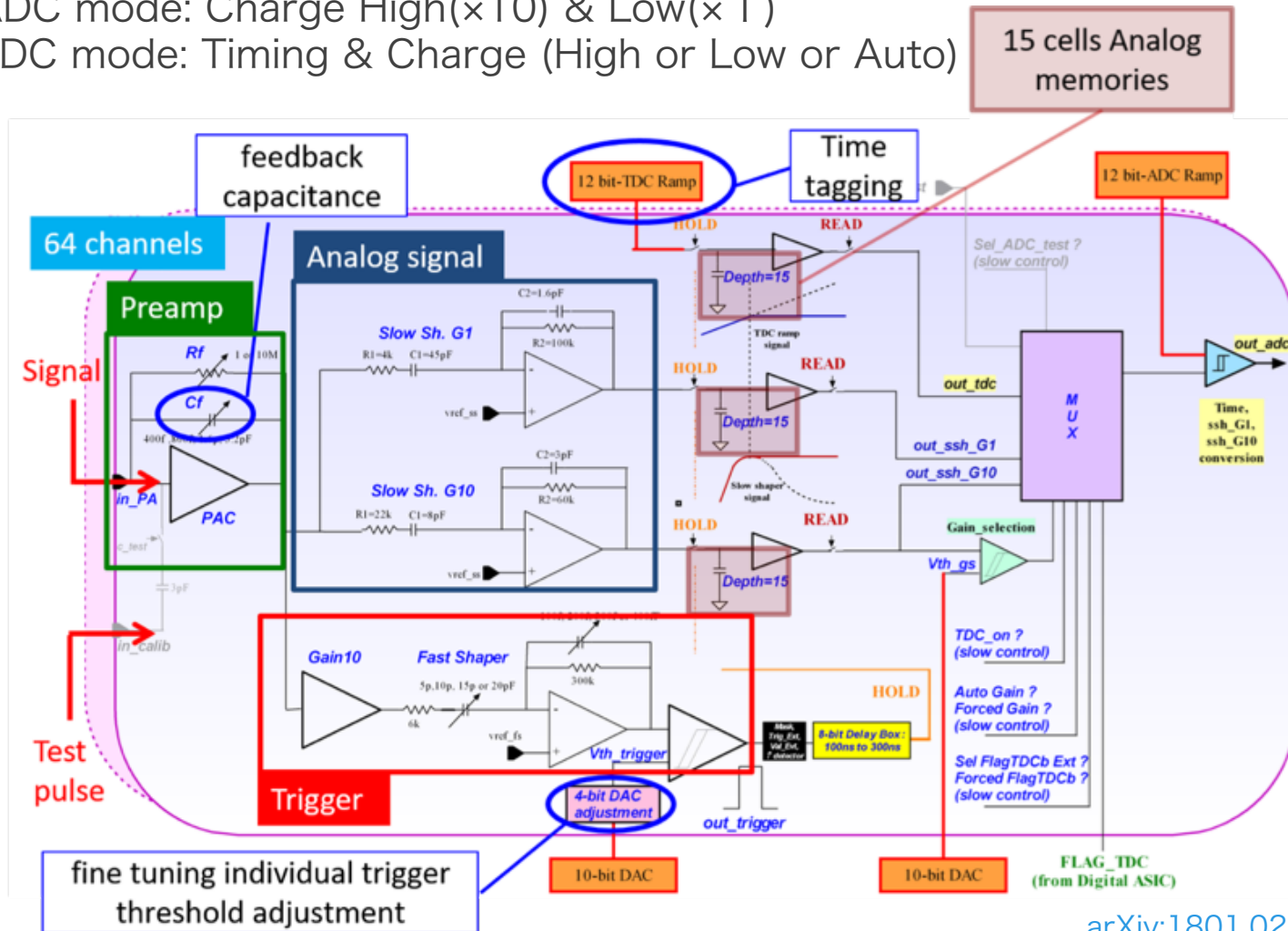
➤ Carbon fiber frame/cover

➤ Smaller SMB footprint

FEV13

Carbon

FEV

SMB

DIF

Carbon
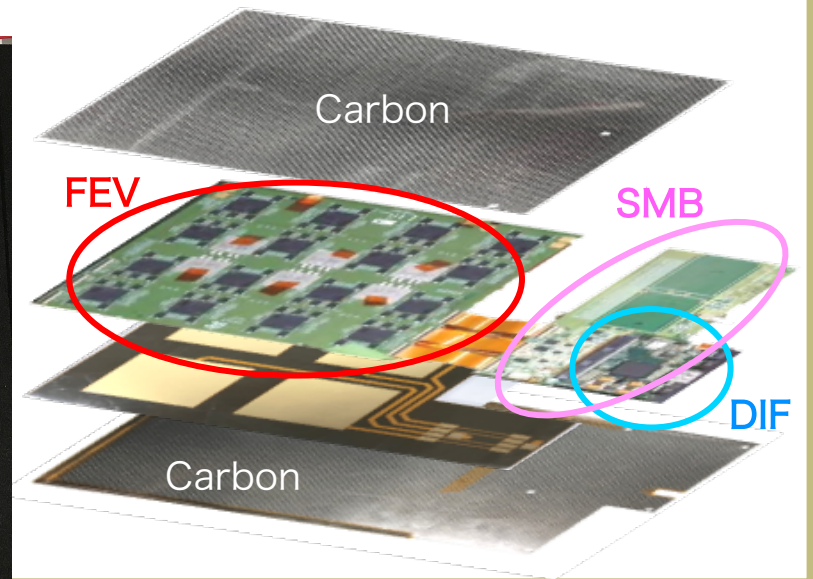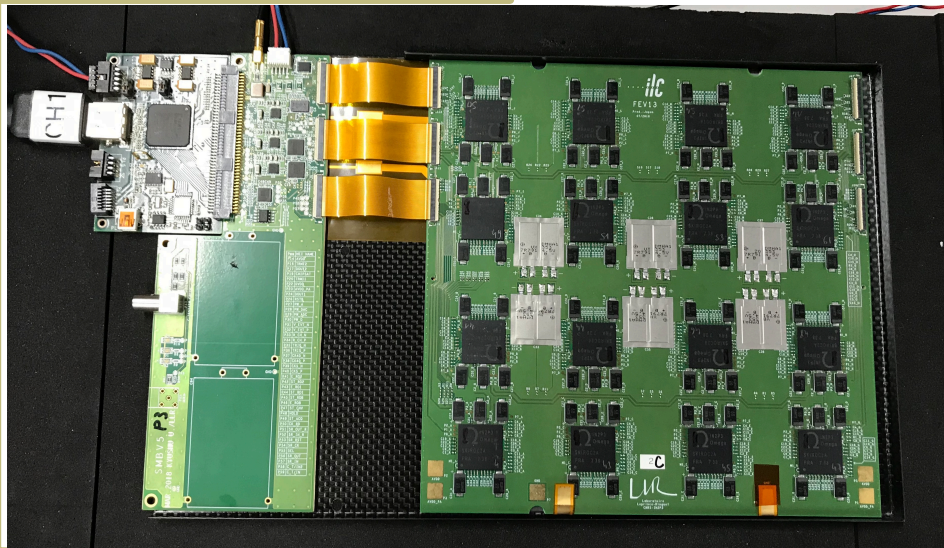
Analogue core: SKIROC2A

➤ Outputs
  ◦ ADC mode: Charge High(×10) & Low(×1)
  ◦ TDC mode: Timing & Charge (High or Low or Auto)

arXiv:1801.02024
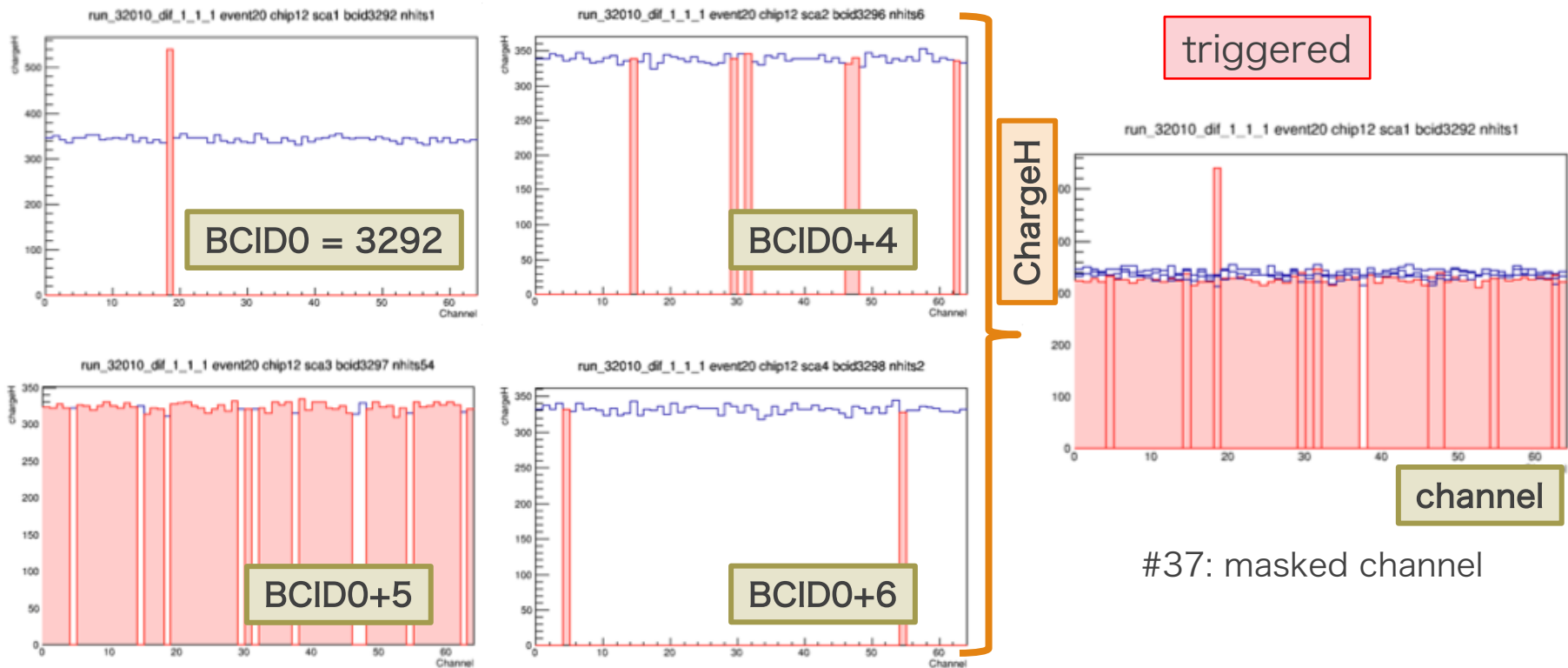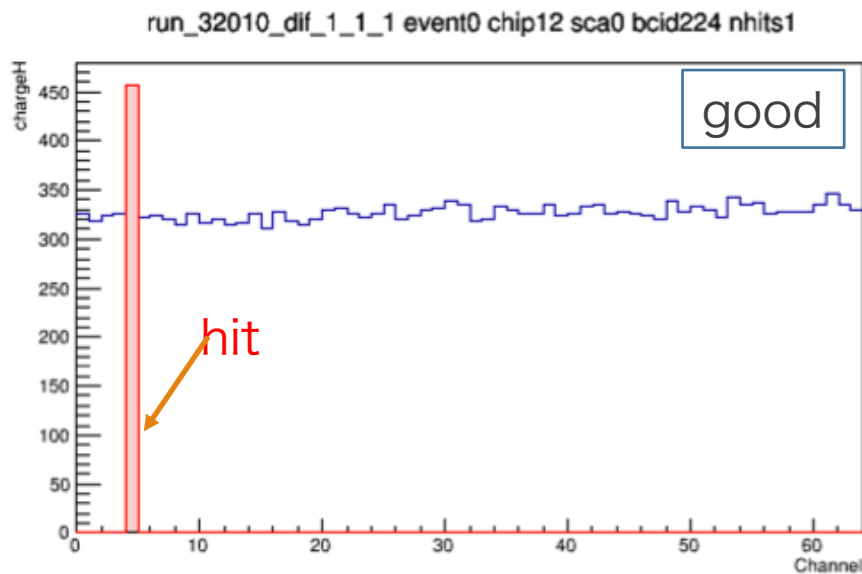
Retriggers: Structure

Trigger & Charge   run32010(beam on, w/o W), chip12, FEV13-P1

- Even the channels which charge is around pedestal level are triggered.
- ➤ Fast shaper (trigger line) is presumed to be affected by retriggers.

triggered

BCID0 = 3292

BCID0+4

BCID0+5

BCID0+6

ChargeH

channel

#37: masked channel

Retriggers

● trigger vs charge
  ◦ Which shaper has problems that cause retriggers?
  ◦ The charges and hits are compared between good/retrigger events.
  ◦ Even the channel which charge is lower than pedestal is triggered.

➢ Fast shaper has some problems in retrigger?

Charge of Induction hits

chargeH-ped_mean {chip==12}

htemp	
Entries	3156
Mean	211.7
Std Dev	138.5

beam on (chip12)

chargeH-ped_mean

htemp	
Entries	238
Mean	239.4
Std Dev	511.6

beam off