Si-W ECal with Integrated Readout

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Chicago
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Si/W ECal R&D Collaboration

SLAC: M. Breidenbach, D. Freytag, N. Graf, R. Herbst, G. Haller, J. Jaros

KPiX readout chip, downstream readout, simulations, mechanical design and integration

U. Oregon: J. Brau, R. Frey, D. Strom, undergraduates.

Detector development, readout electronics

UC, Davis: B. Holbrook, R. Lander, M. Tripathi, undergraduates.

Interconnect issues: Flex cable development, bump bonding, conducting films

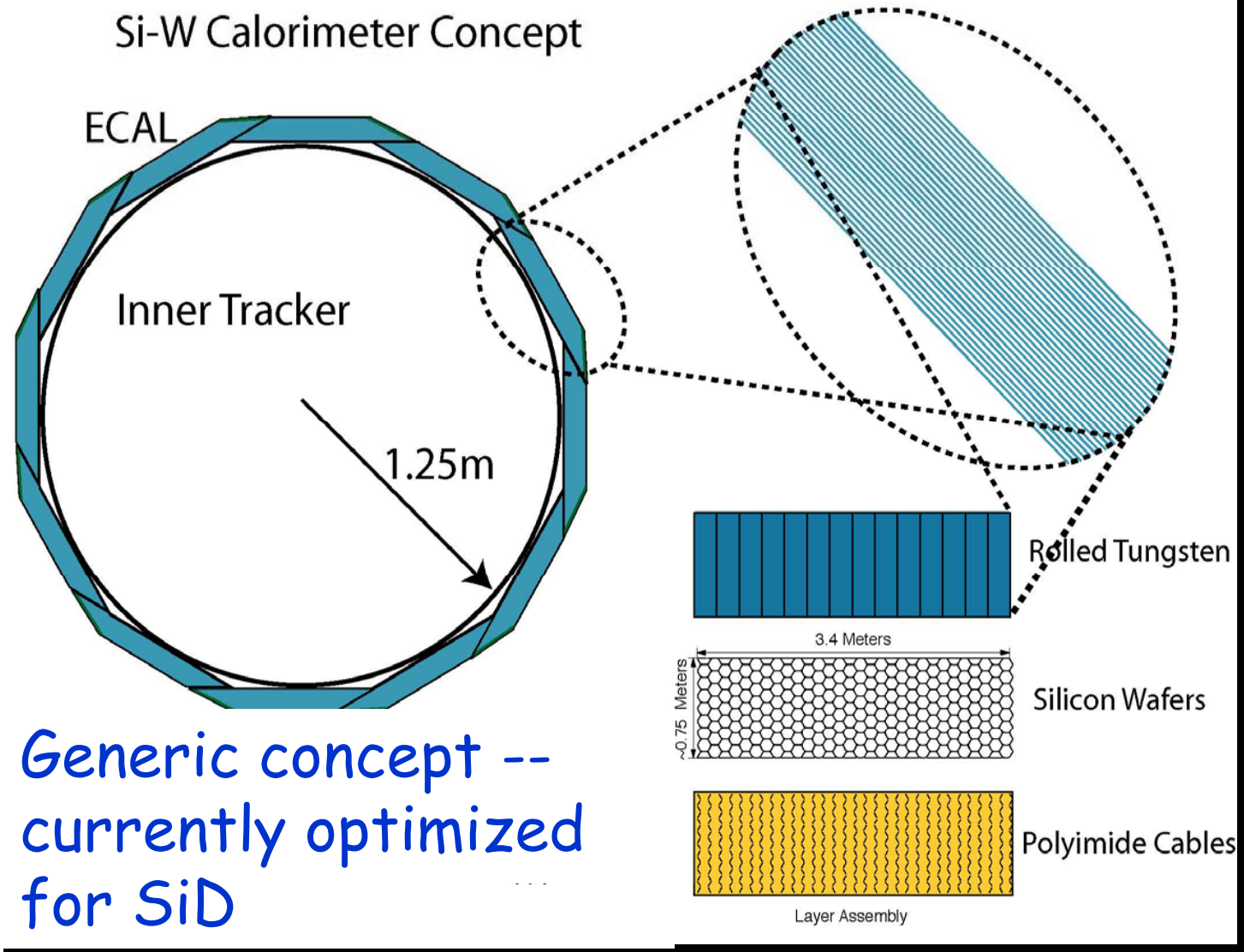
BNL: V. Radeka

Readout electronics

LAPP Annecy: S. Adloff, F. Cadoux, J. Jacquemier, Y. Karyotakis

Mechanical design and integration

Si-W Calorimeter Concept



Generic concept -- currently optimized for SiD

Baseline configuration:

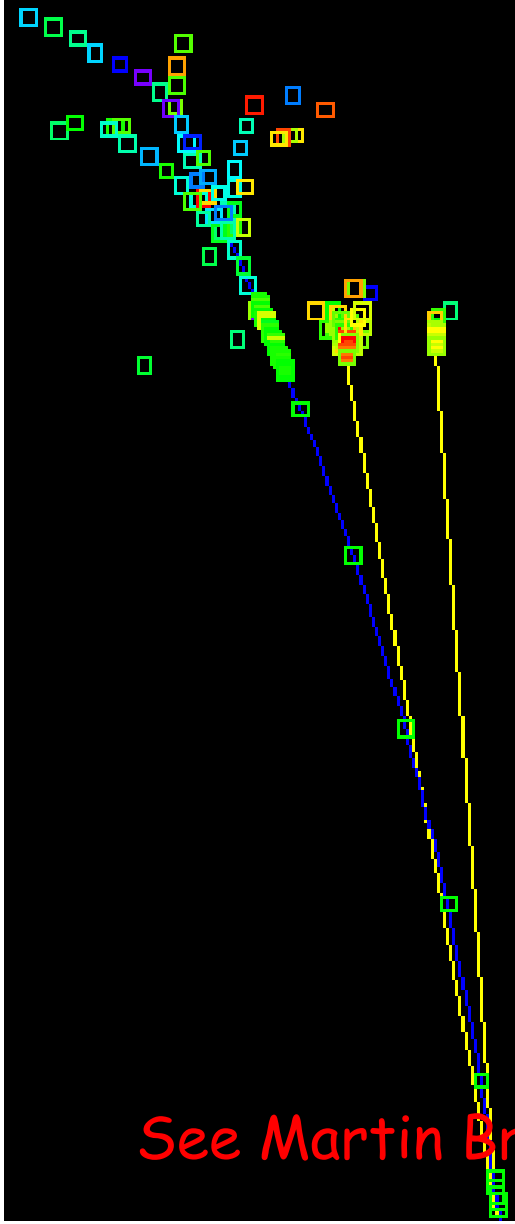
- transverse seg.: 13 mm^2 pixels
- longitudinal seg:

  (20 x 5/7 X_0) + (10 x 10/7 X_0)

⇒ **17%/sqrt(E)**

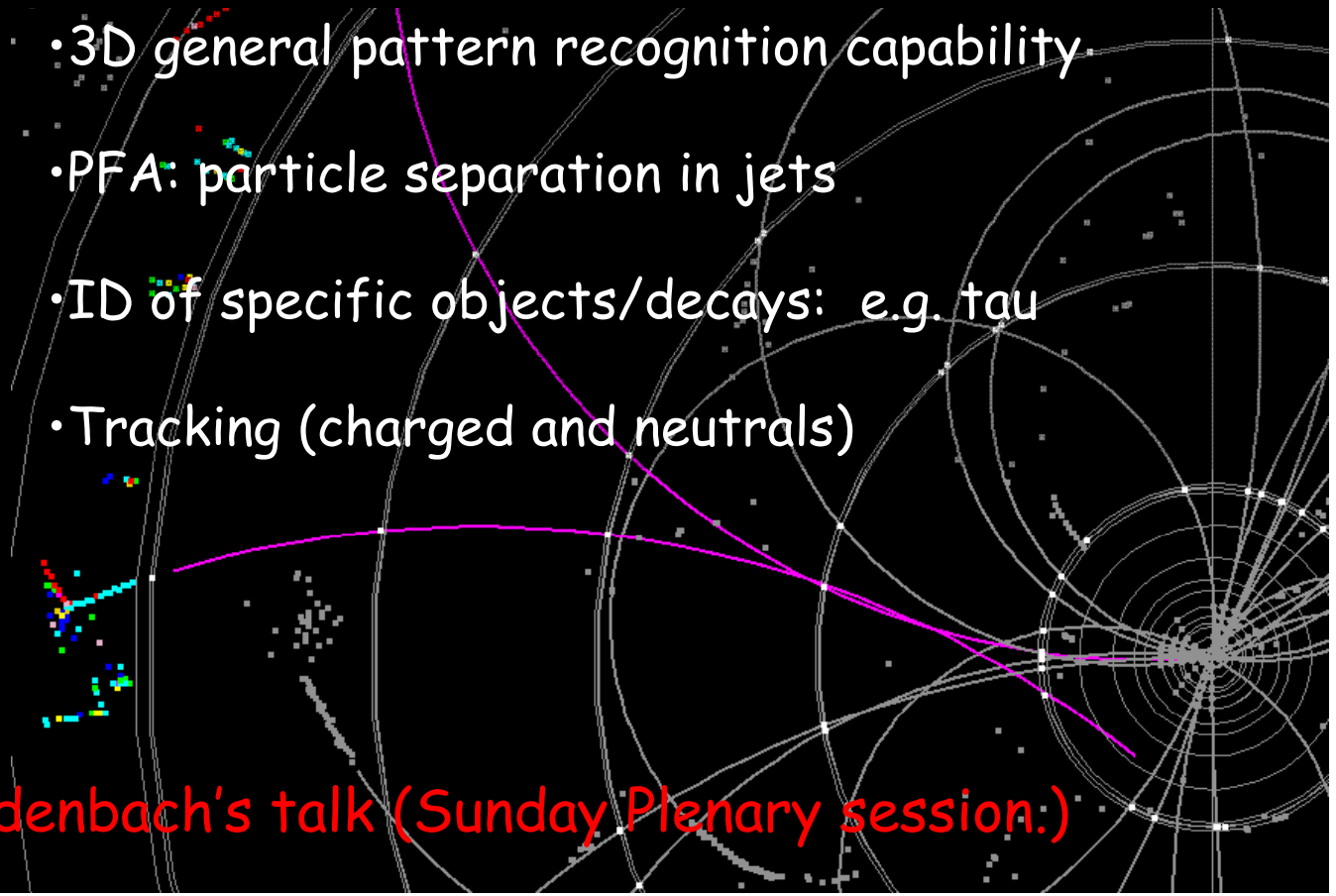
- 1 mm readout gaps ⇒ 13 mm effective Moliere radius

An Imaging Calorimeter



High Degree of Segmentation ⇒

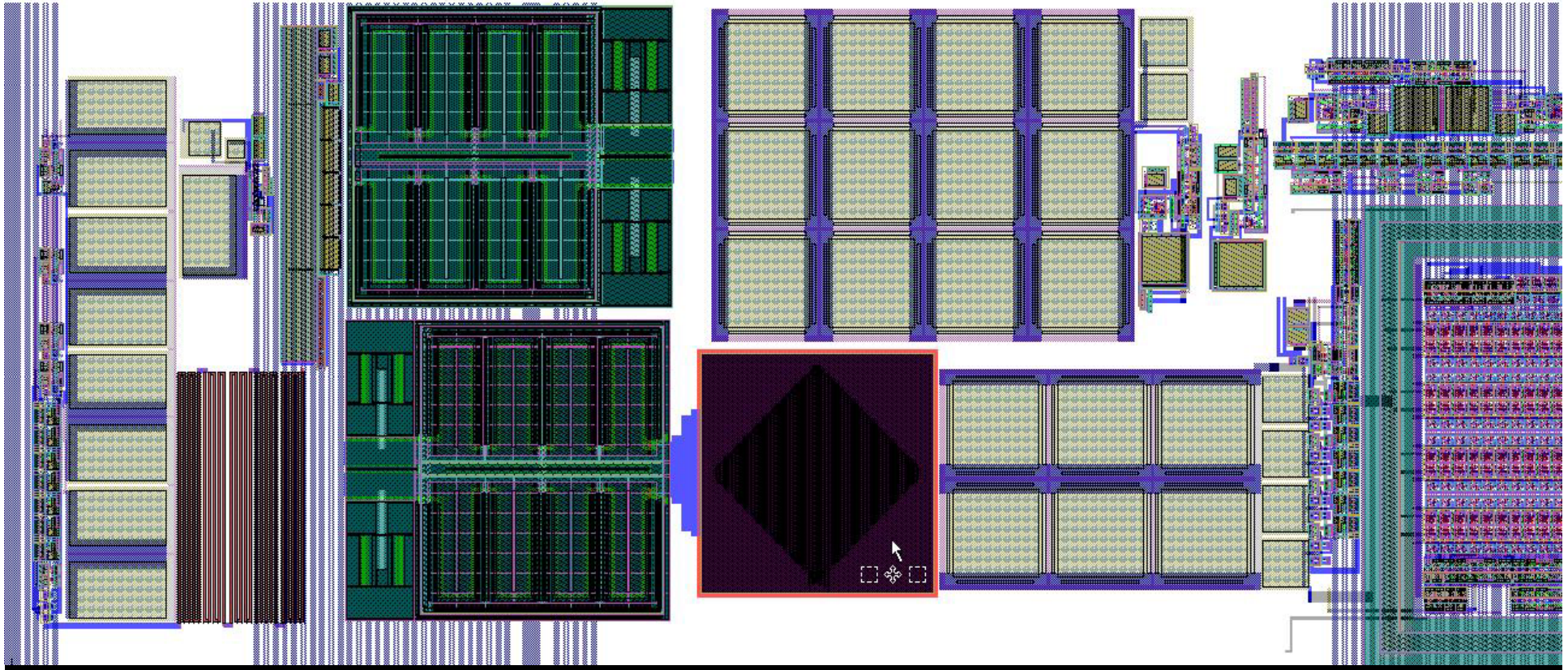
- 3D general pattern recognition capability
- PFA: particle separation in jets
- ID of specific objects/decays: e.g. tau
- Tracking (charged and neutrals)



See Martin Breidenbach's talk (Sunday Plenary session.)

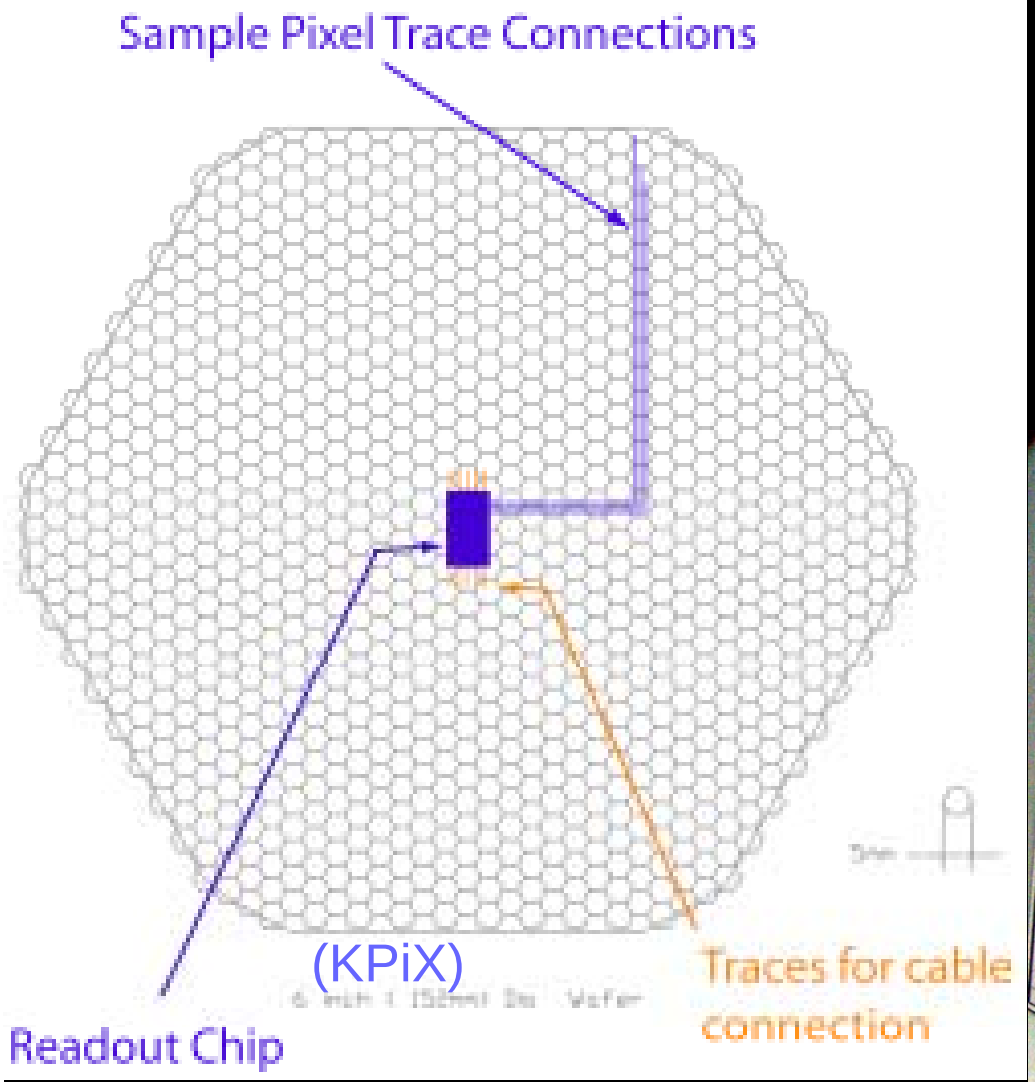
KPiX Development

Complexity and A large number of functions => several rounds of prototyping. A 64-channel prototype (version 7) is currently under test.



See talk by Ryan Herbst (Tues 8:30 am Data Acquisition session)

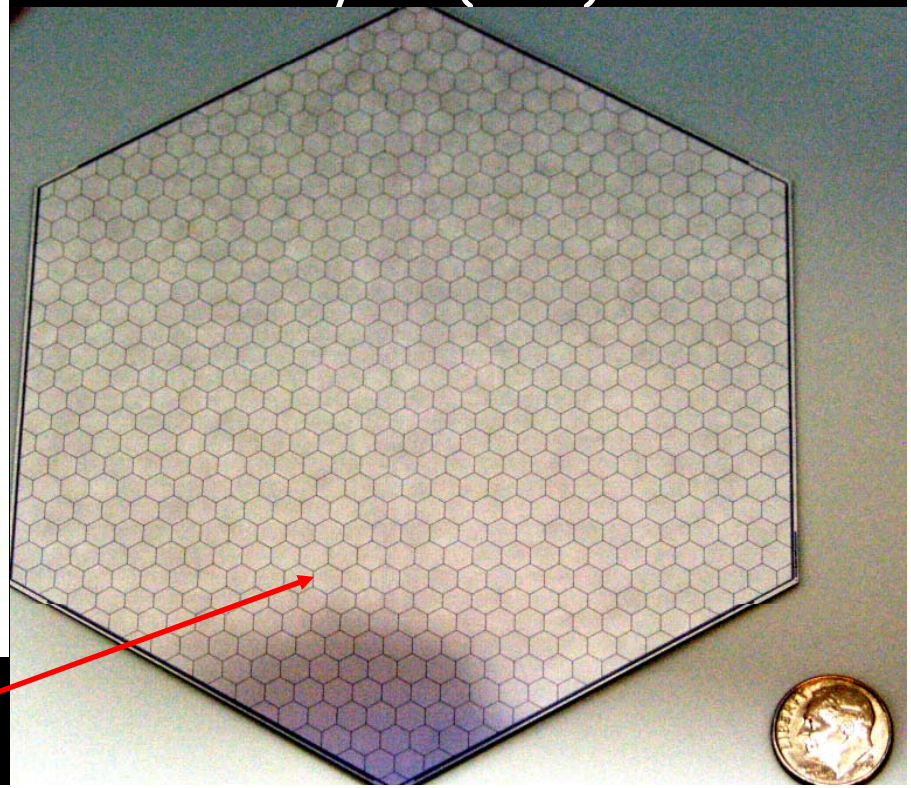
Si detector: layout & segmentation



One KPiX readout chip for the sensor (1024 pixels, 6 inch wafer)

Limit on segmentation from chip power (~20 mW per chip).

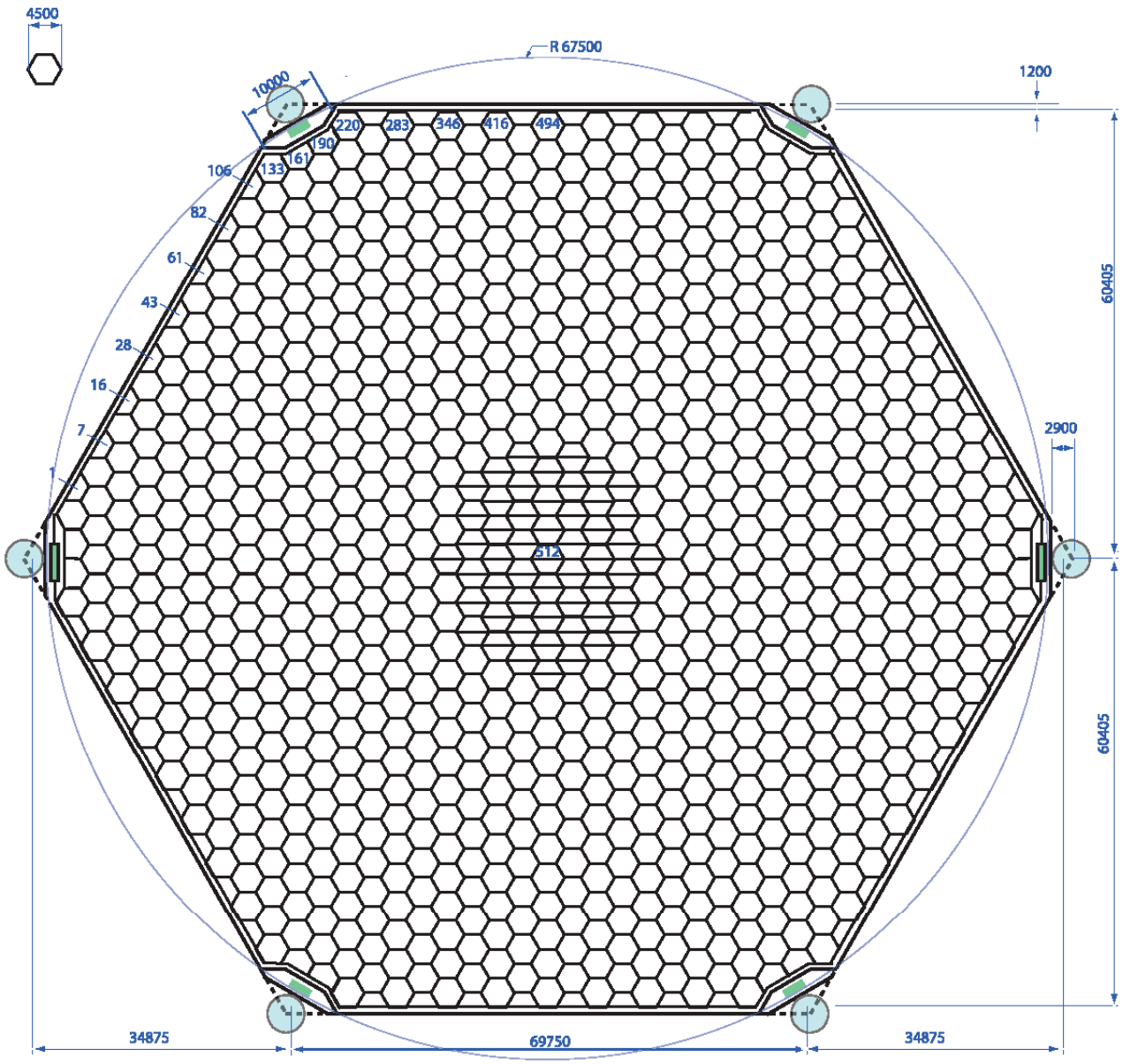
Use DC-coupled detectors: only two metal layers (cost)



Fully functional v1 prototype (Hamamatsu)

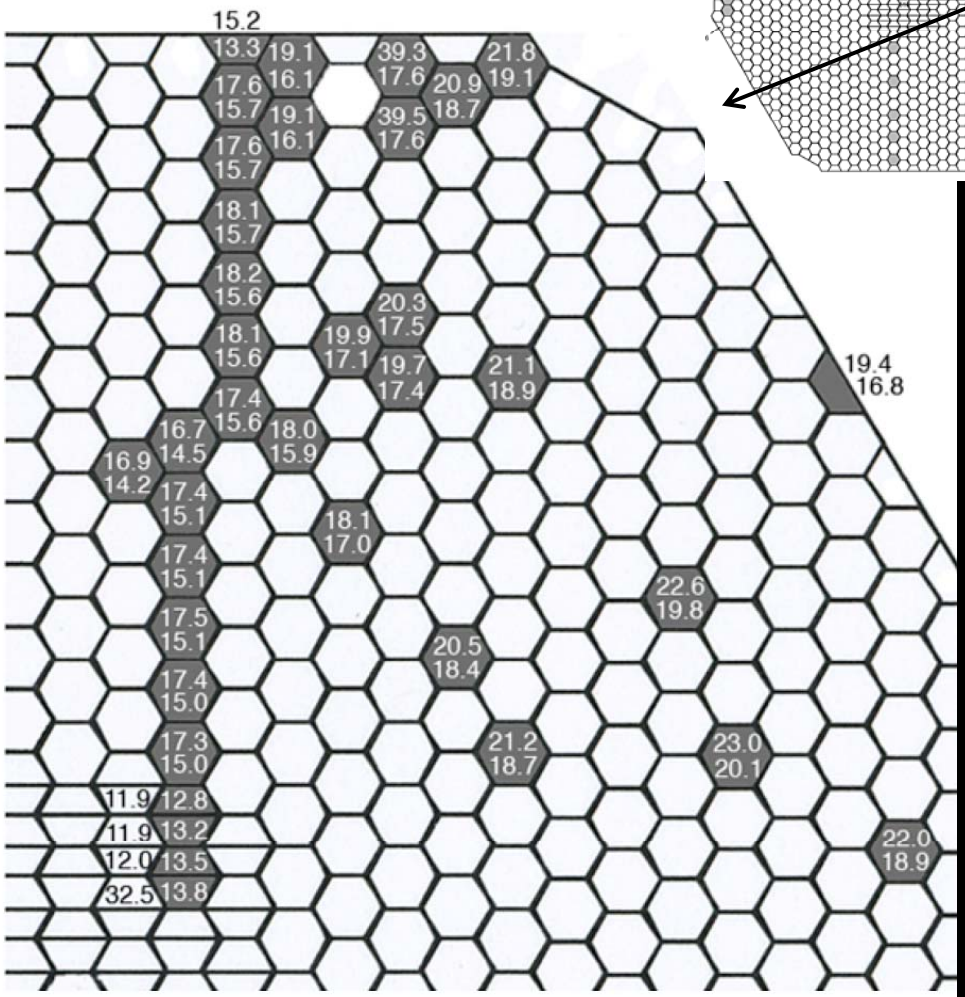
Si detector –Version 2

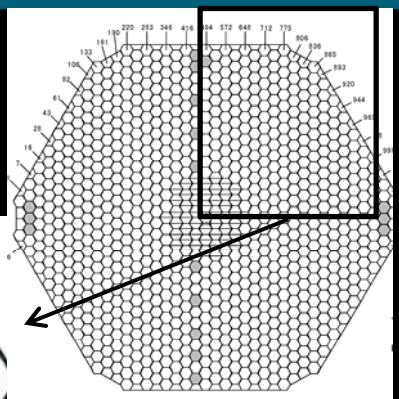
- Intended for full-depth test module
- 6 inch wafer
- 1024 13 mm² pixels
- improved trace layout and split pixels near KPiX to reduce capacitance
- 40 good + 20 NG sensors in hand fromHamamatsu

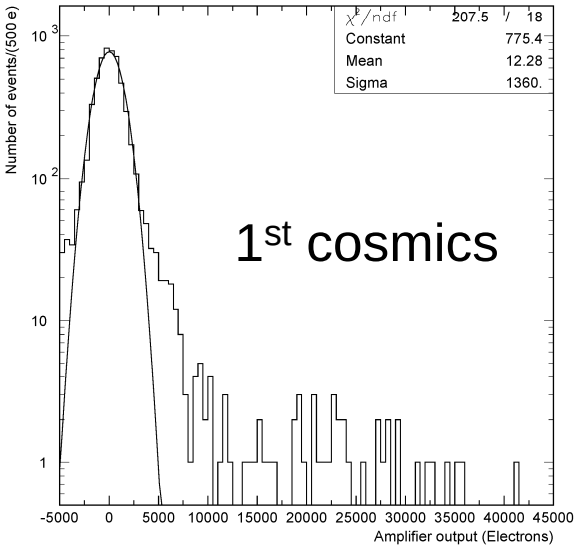


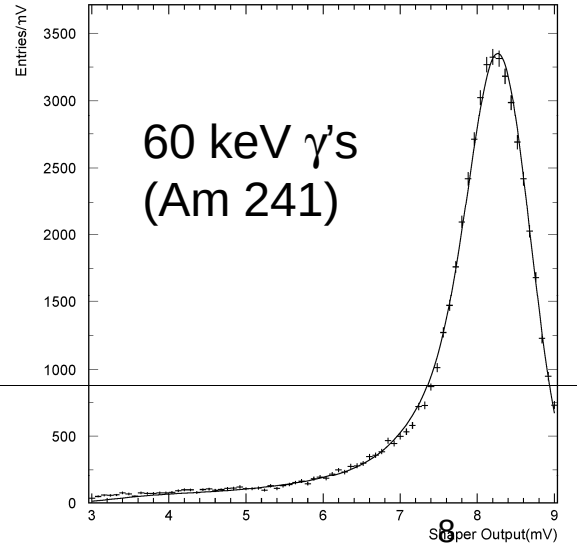
Initial studies of version 2 sensors

Capacitance:
expected/measured

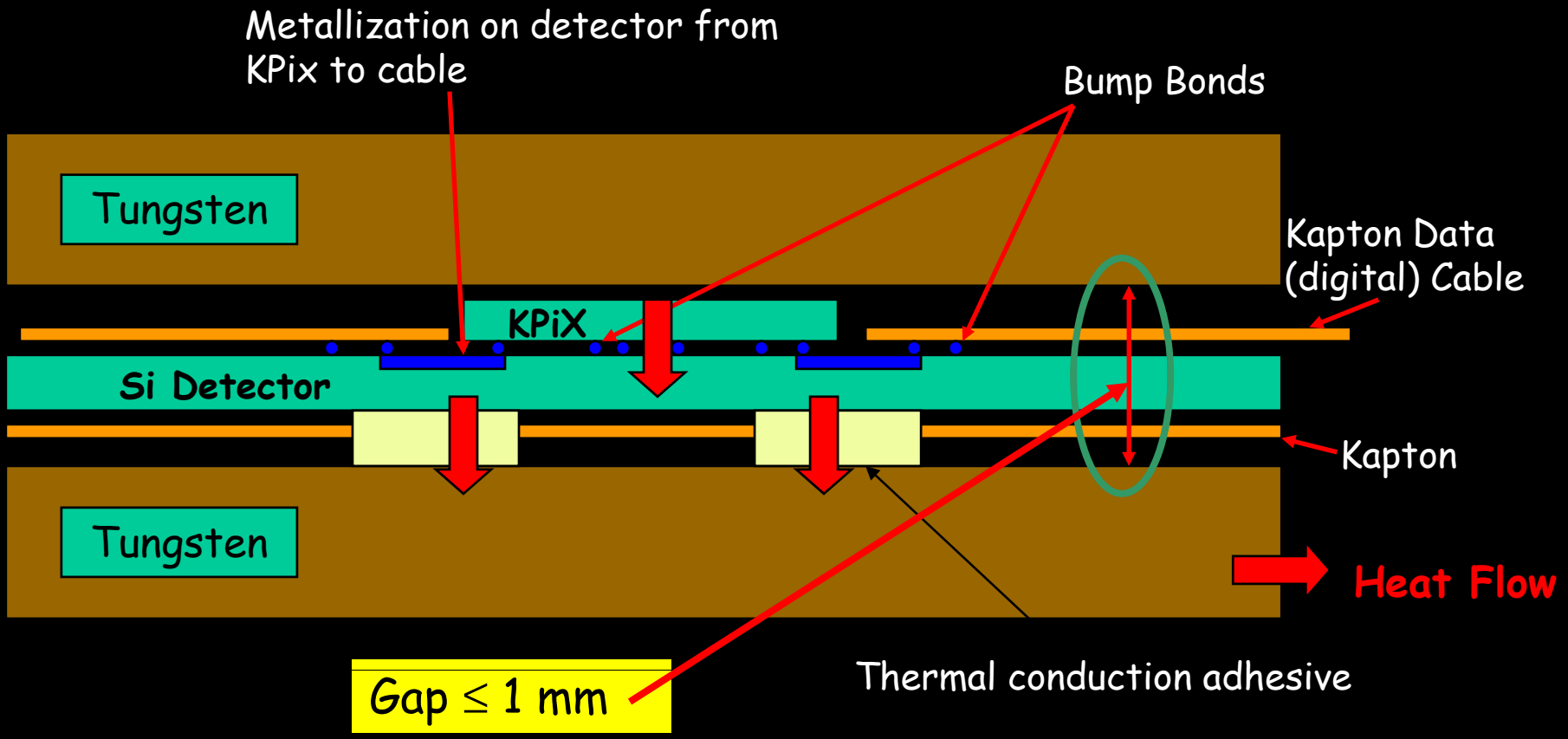




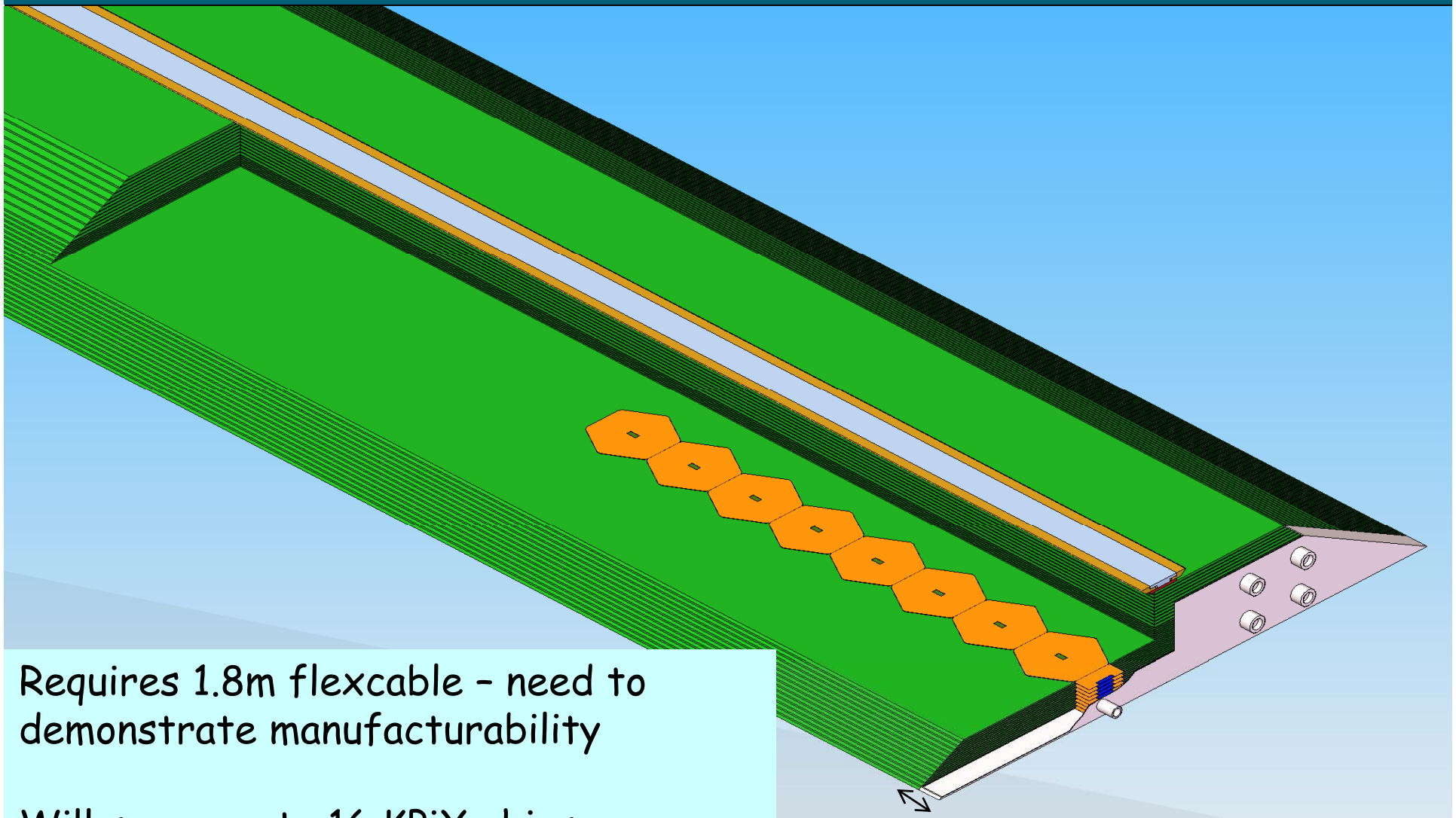




Readout gap cross section (schematic)



Module Design: New Layout (Marco Oriunno)

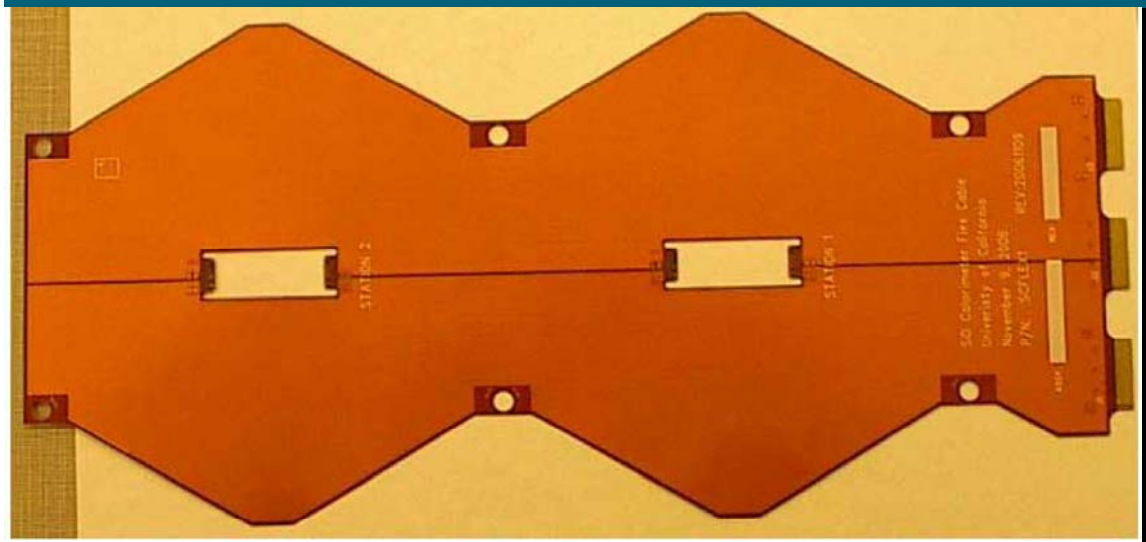


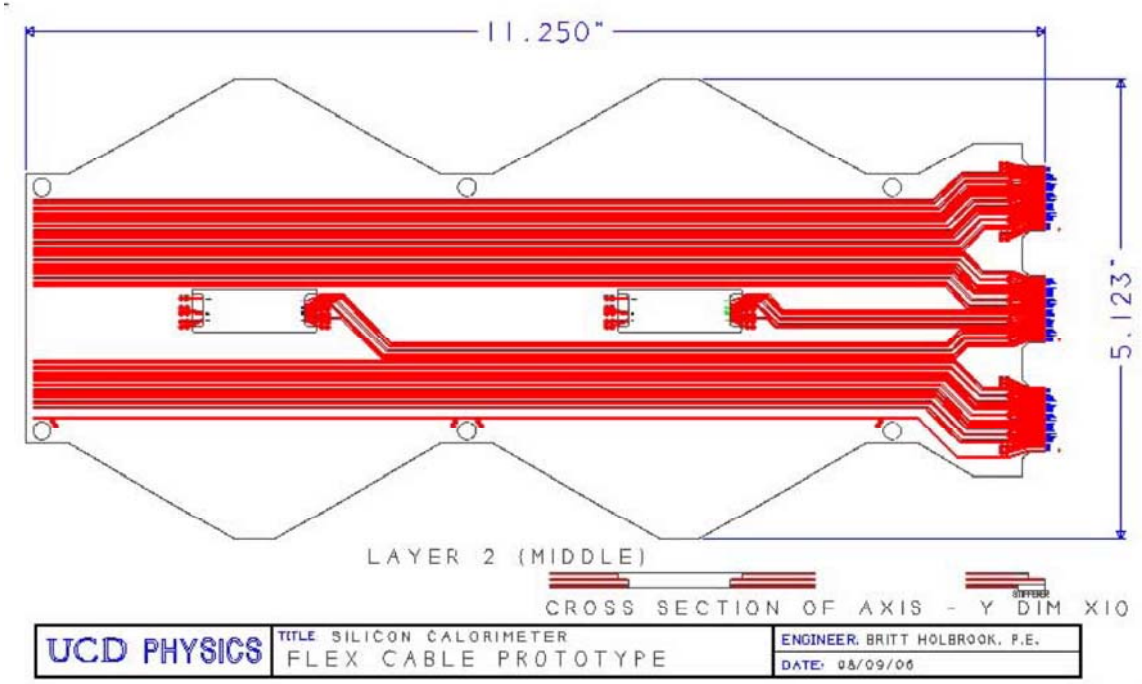
Requires 1.8m flexcable – need to demonstrate manufacturability

Will serve up to 16 KPiX chips

~200 cables/connectors per side

Readout flex cable





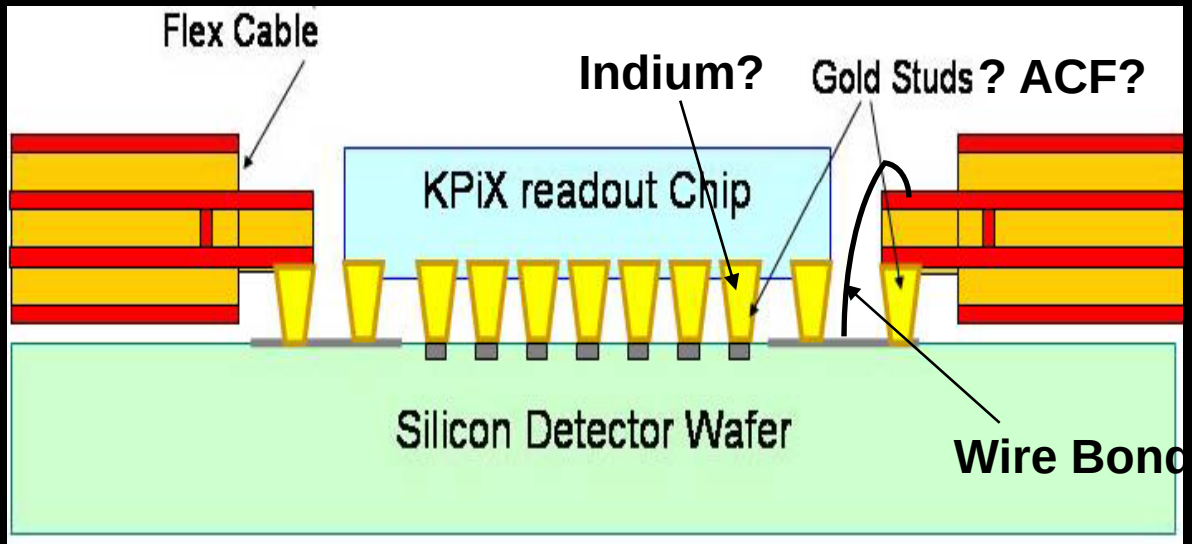
- Second prototype tested well with no problems:
  - 2 chip stations
  - Buried digital signal layer between power and ground planes
  - Two "lips" per KPiX from the buried layer.
  - Wire-bonded to KPiX test-board (for now)
- For 16 station cable:
  - A second vendor identified (produced long cables for EXO).

Interconnect issues

Technologies being considered:

KPiX to Sensor: Indium Bump Bonding
Gold Stud Bonding

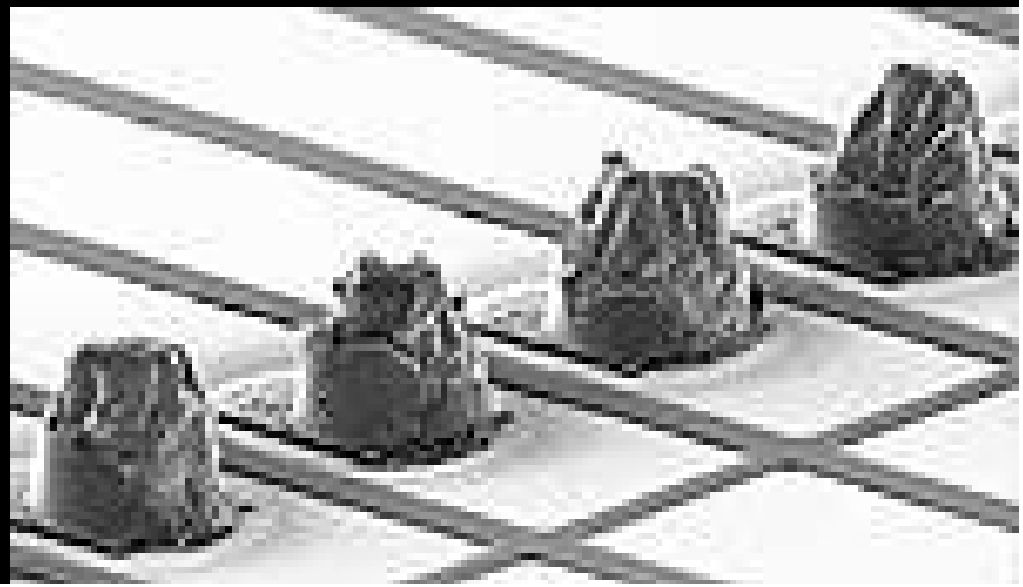
Flex Cable to Sensor: Wire Bonding
Z-axis Conducting Film
Gold Studs



Indium Bump Bonding

Indium Bump Bonding is a mature/commercial technology. UC, Davis has developed the process for prototyping purposes. Our facilities include a Class 100 clean room (10,000+ sq. ft.) and several pieces of specialized equipment. All the steps are done in-house:

- Photoresist spinning
- Mask making
- Alignment, UV exposure
- Ti/W sputtering
- Indium deposition
- Flip-chip bump bonding

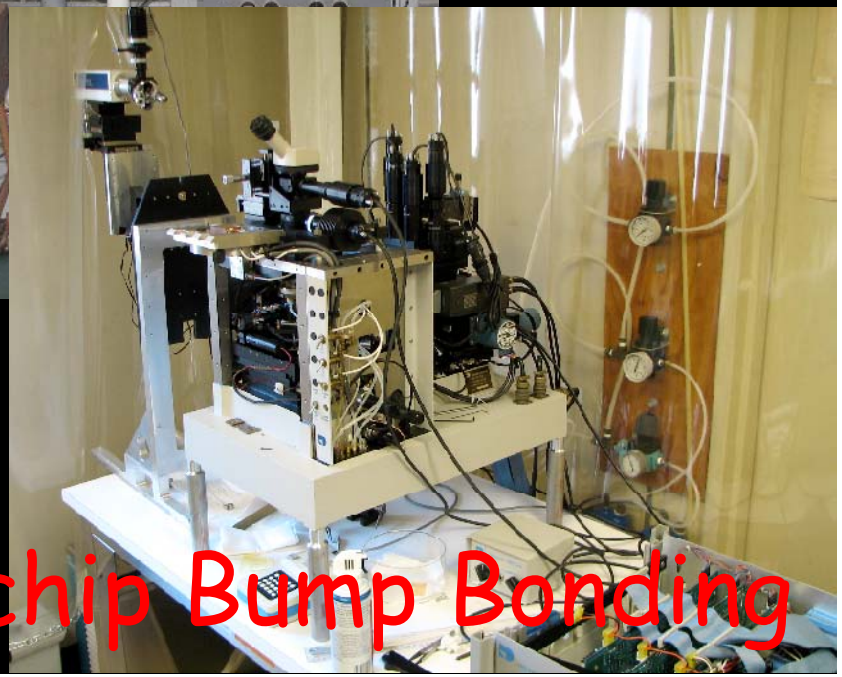


Indium Bumping Process

UV Exposure

Indium Deposition

Ti/W Sputter



Flip-chip Bump Bonding

Gold Stud Bump Bonding

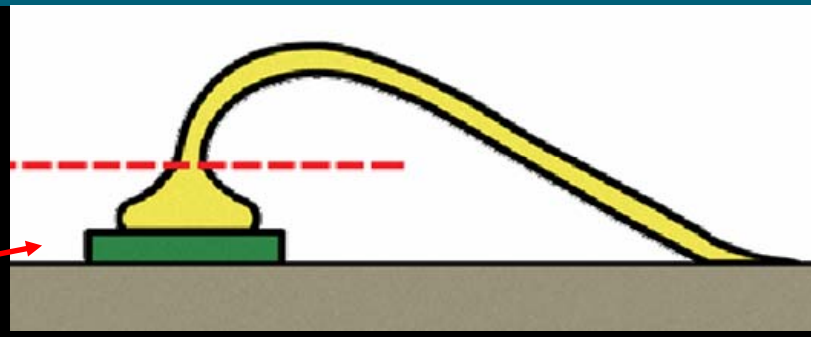
Palomar Technologies
Vista, Ca.

An attractive option for prototyping because individual small chips are difficult to handle for Indium bumping.

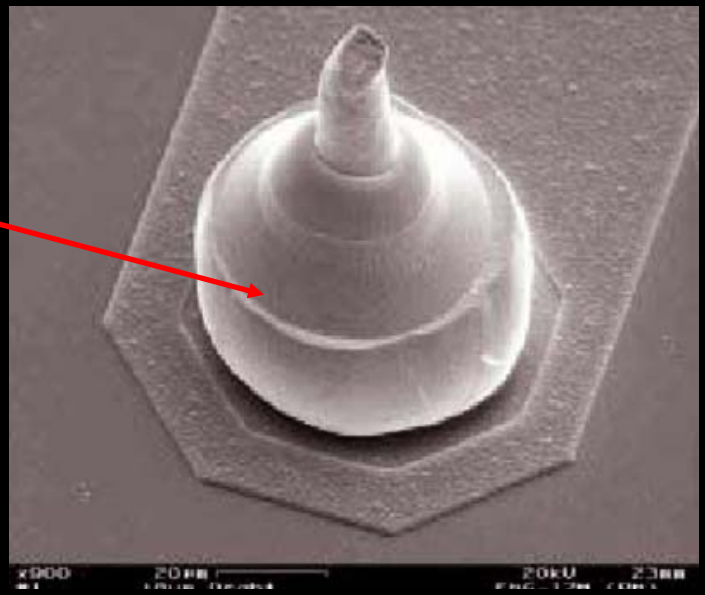
Gold Stud Growth

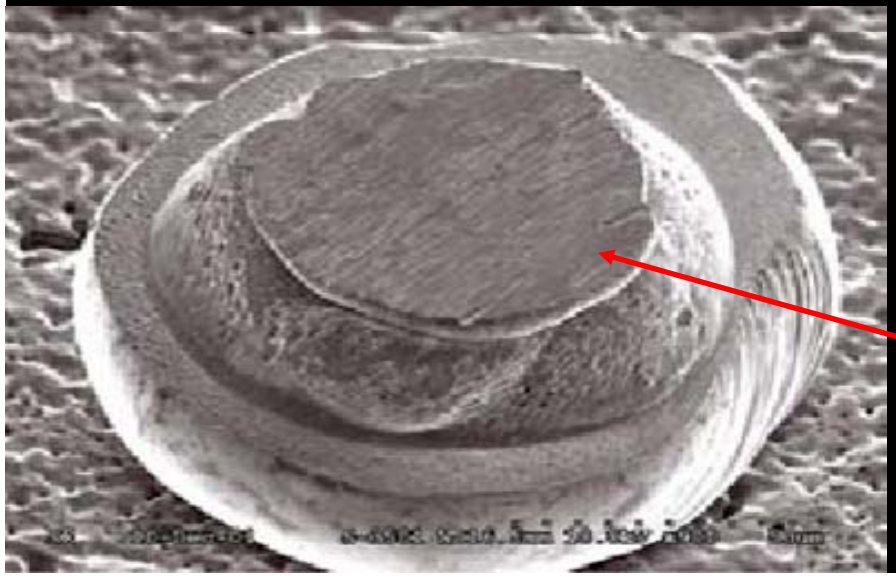
Palomar Technologies:

Step 1: A ~25 μm gold wire is bonded to the pad.



Step 2: The wire is snapped off leaving a stud behind.





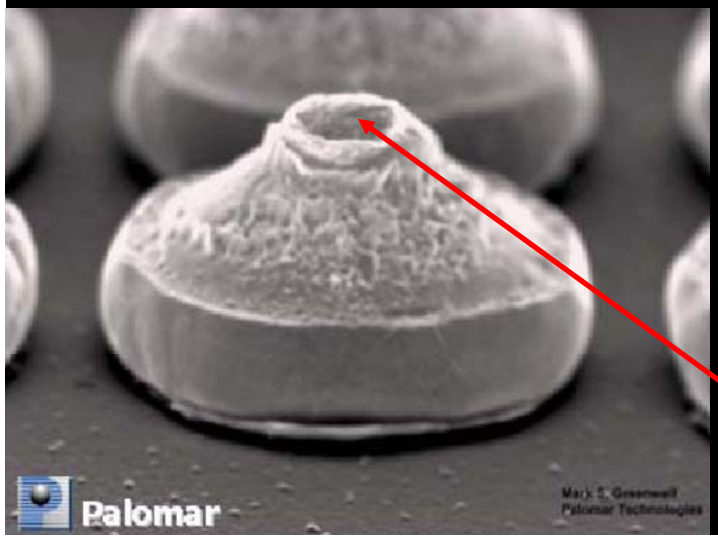
Step 3: The stud is "coined" (flattened) to provide a better shape.

Adhesive Attachment

Palomar Technologies:

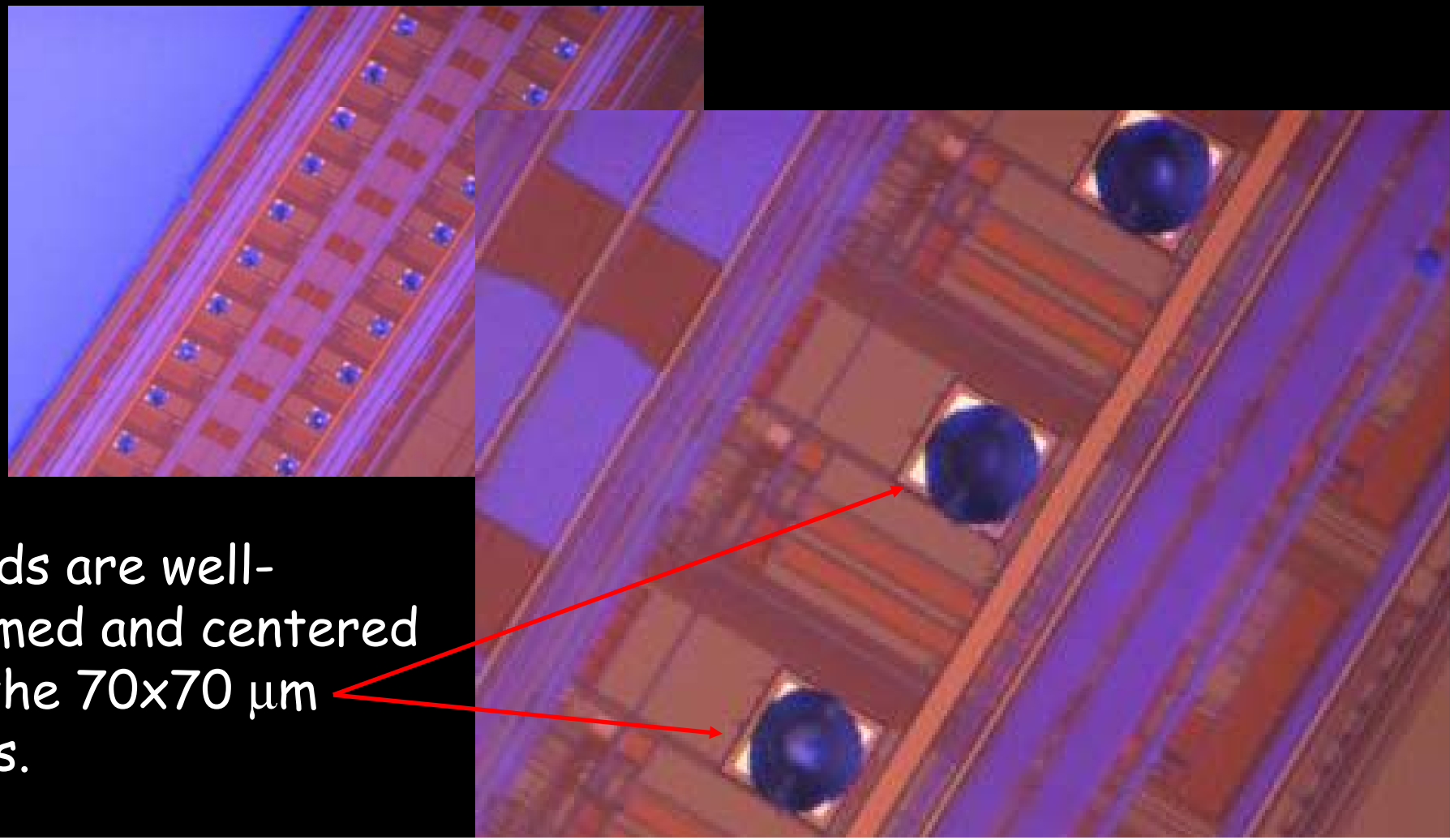
The tips of the studs are dipped into a conductive epoxy.
(Alternately, epoxy "dots" can be dispensed on the opposite wafer).

After a flip-chip alignment, the chips are compressed.



An optimum stud shape for adhesive attachment has been developed. Instead of "coining" the wire is pushed back into the ball after snapping. The result is a matted surface.

KPiX with Gold Studs

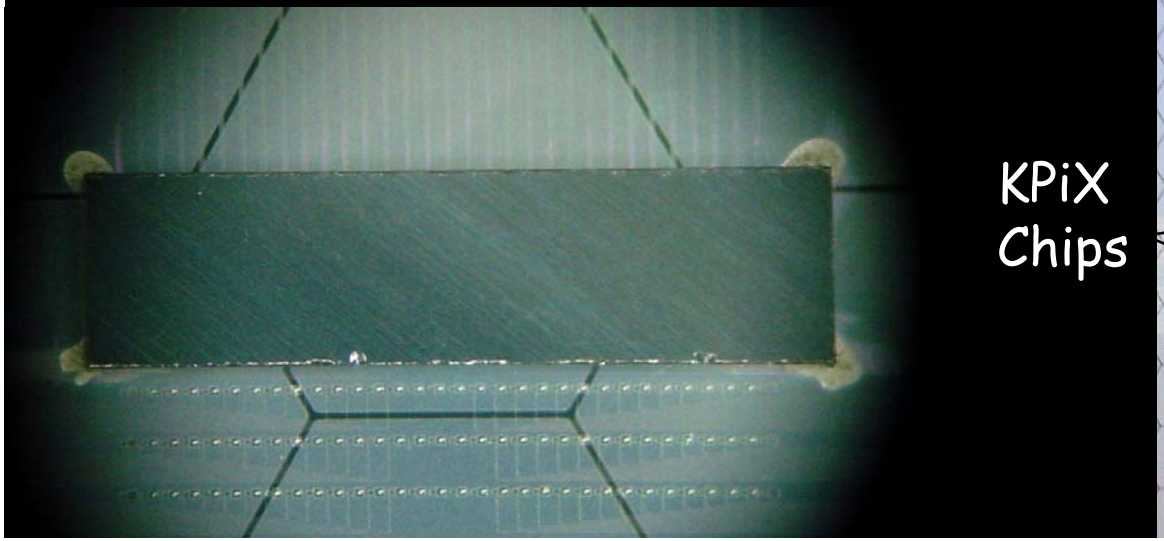


Studs are well-formed and centered on the 70x70 μm pads.

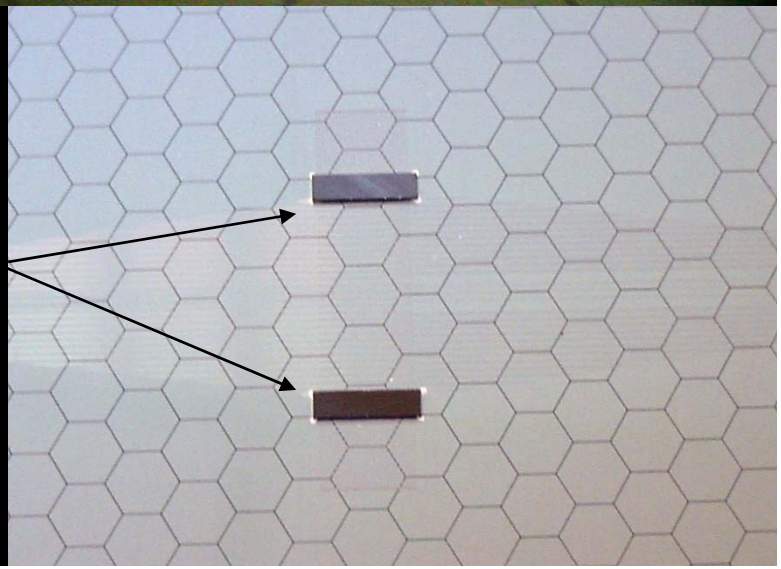
Si-W Bump Bonding

•Initial gold-stud bump-bonding trials had mixed results due to surface oxidation.

•Trials using titanium-tungsten treatment of Hamamatsu sensors and KPiX-7 are underway.



KPiX Chips



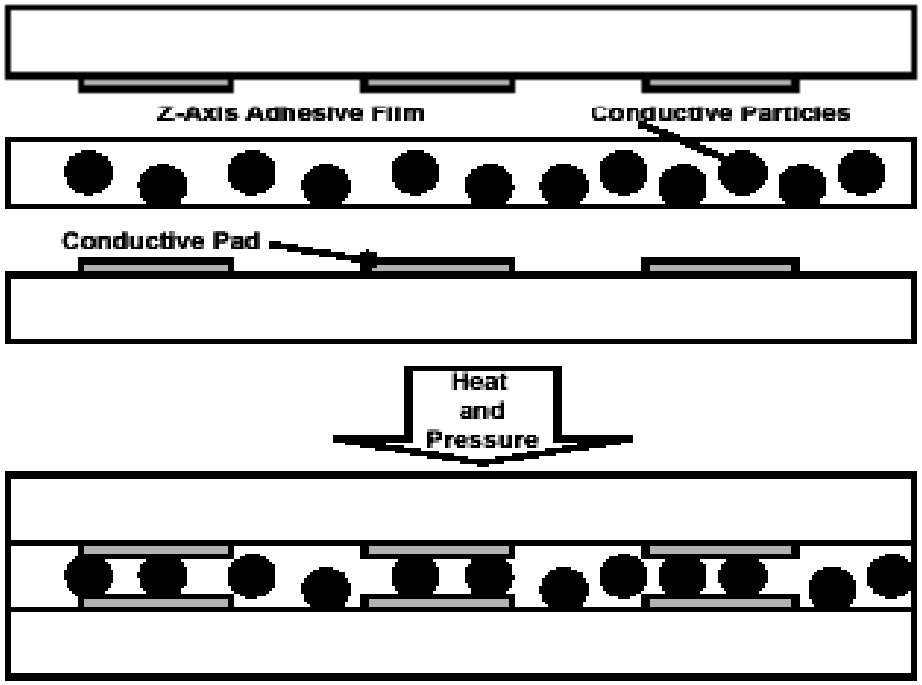
Z-Axis Conducting Adhesive

3M: 7303 ACF Adhesive

~45 μm particles
~75 μm film thickness

≥250 μm pad pitch

Bonding Conditions:
140°C @ 260 PSI for 25 secs



Cairns et al, SID Digest, 2001

Contact resistance ≤0.2 Ω (for flex-cable to PC board).
≤0.2 Ω maintained after 80°C for 1000 hours or 25°C for 4 yrs.

Flex cable to Wafer attachment is not common => R&D.

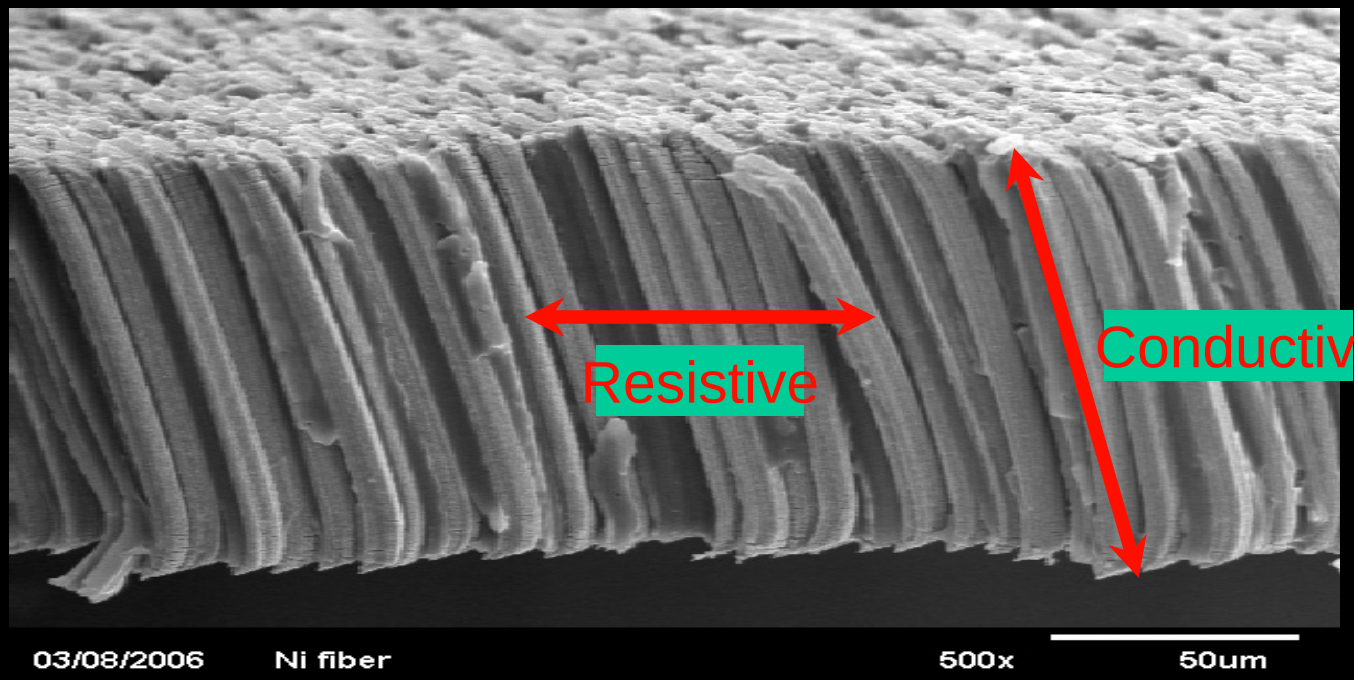
Thermoplastic Conducting Adhesive

Btechcorp:

Metal fibers in a matrix
~2 x 10^7 fibers/in^2

≥11 μm pad pitch

Low Cure pressure: 50 psi

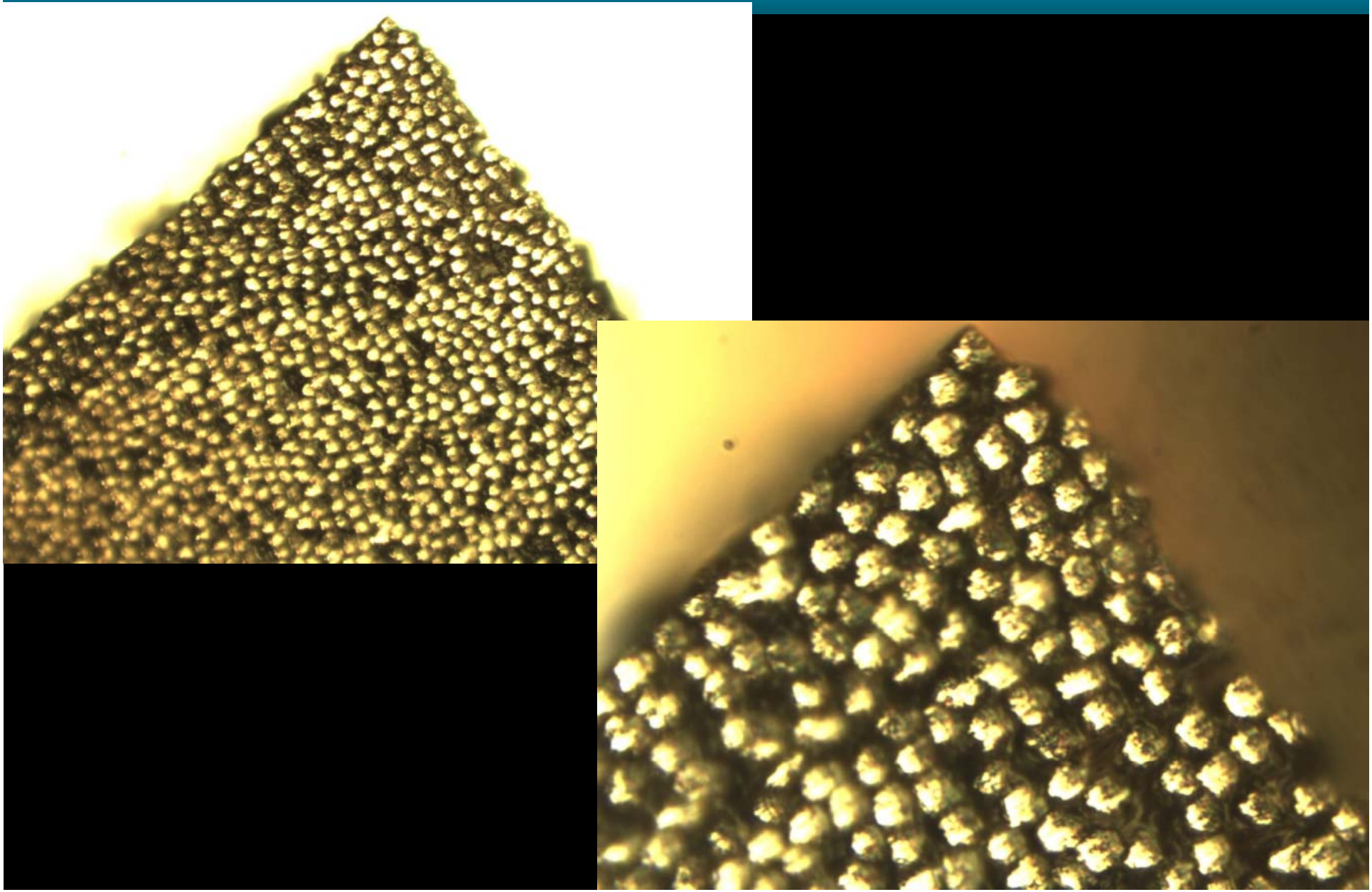


Nickel fiber structure.

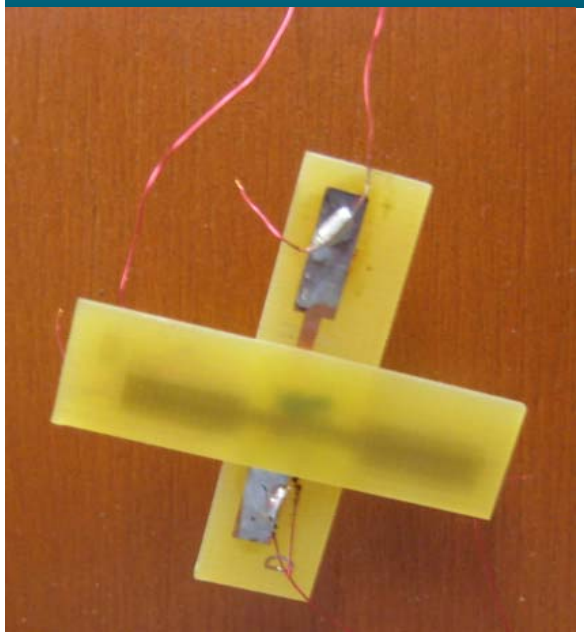
Thermal Conductivity ≥ Cu. Smaller resistance

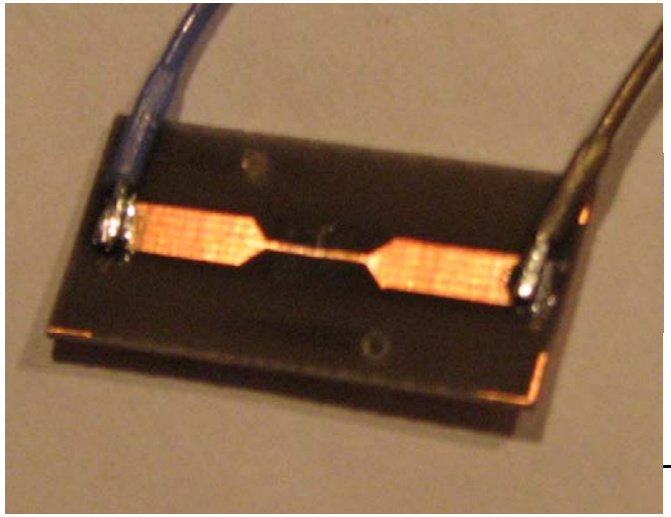
Cheaper. Candidate for both KPiX to Sensor and Flex cable to Sensor attachment => Further R&D.

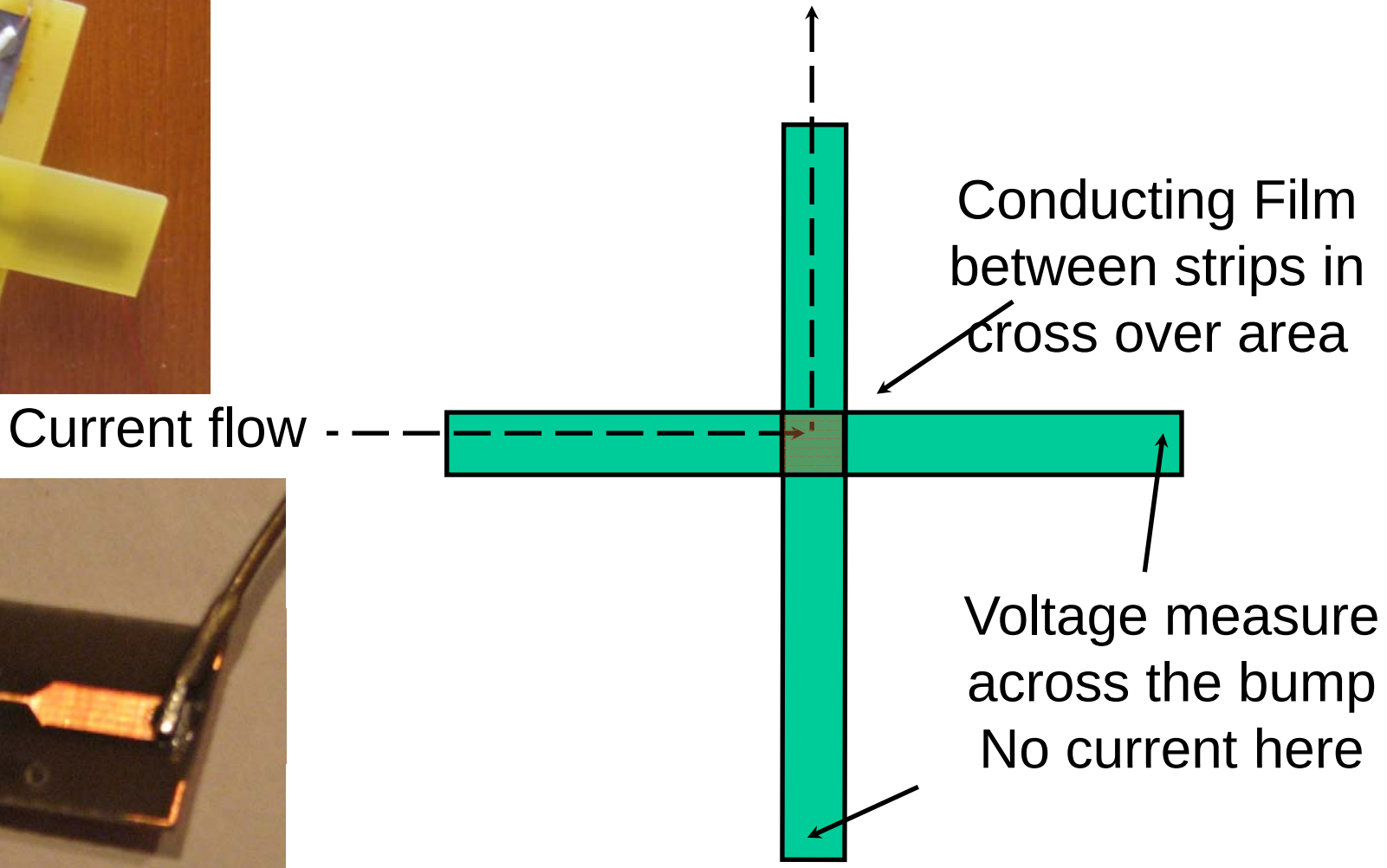
ACF: Cross sections



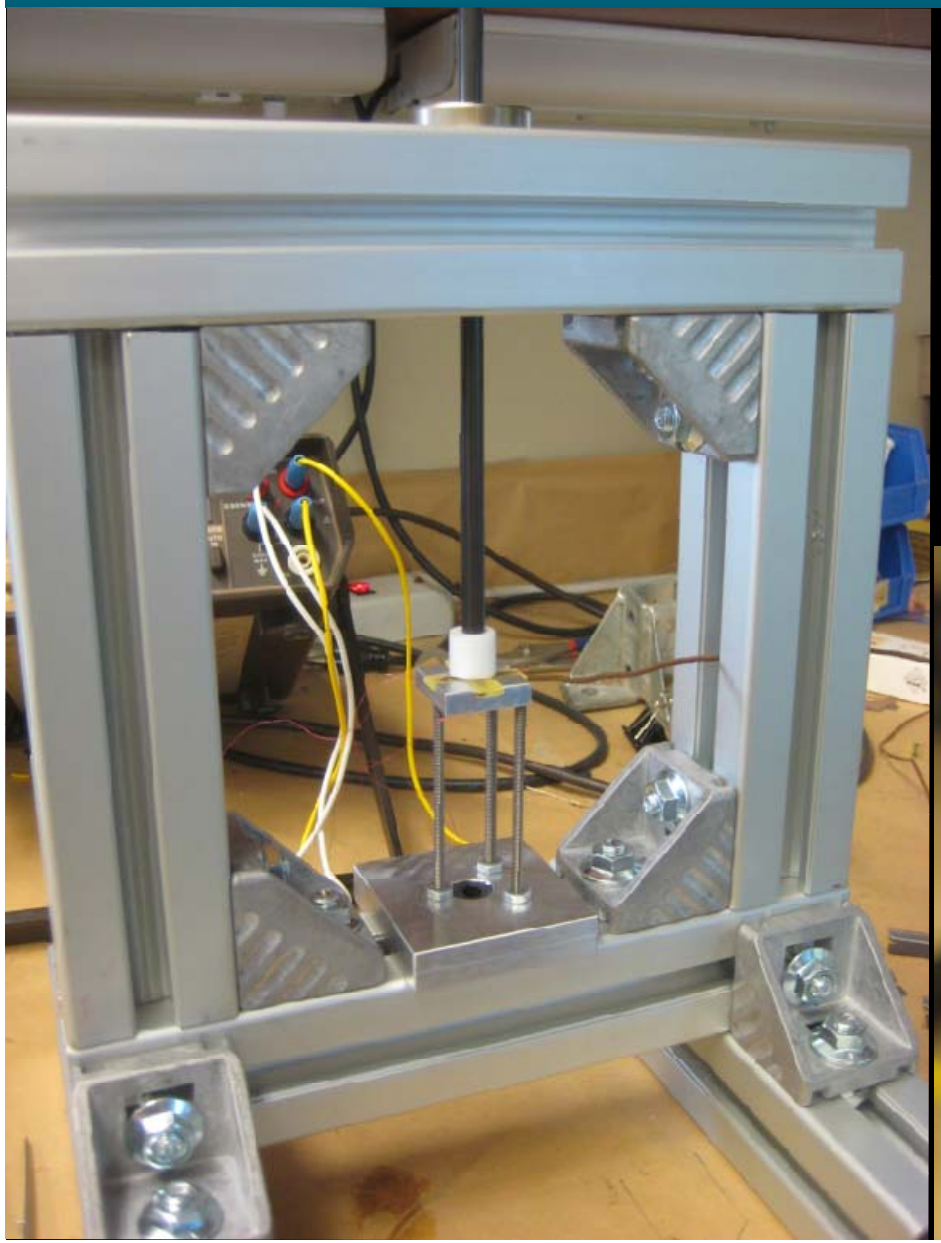
Test Setup: “4 point” R measure





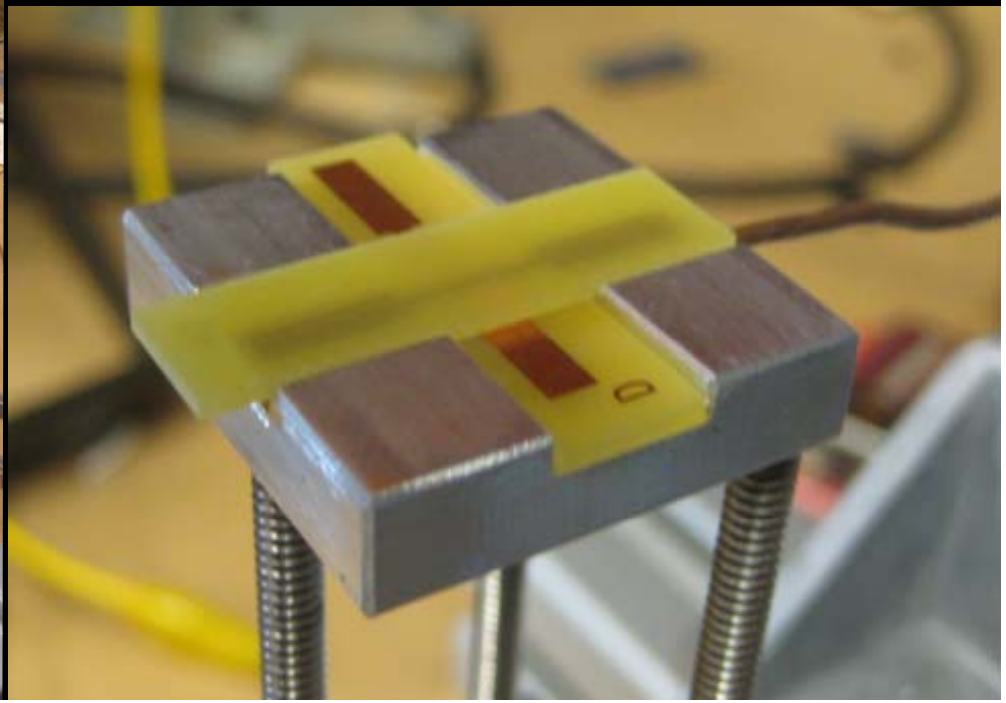


Jig for Forming the Connection

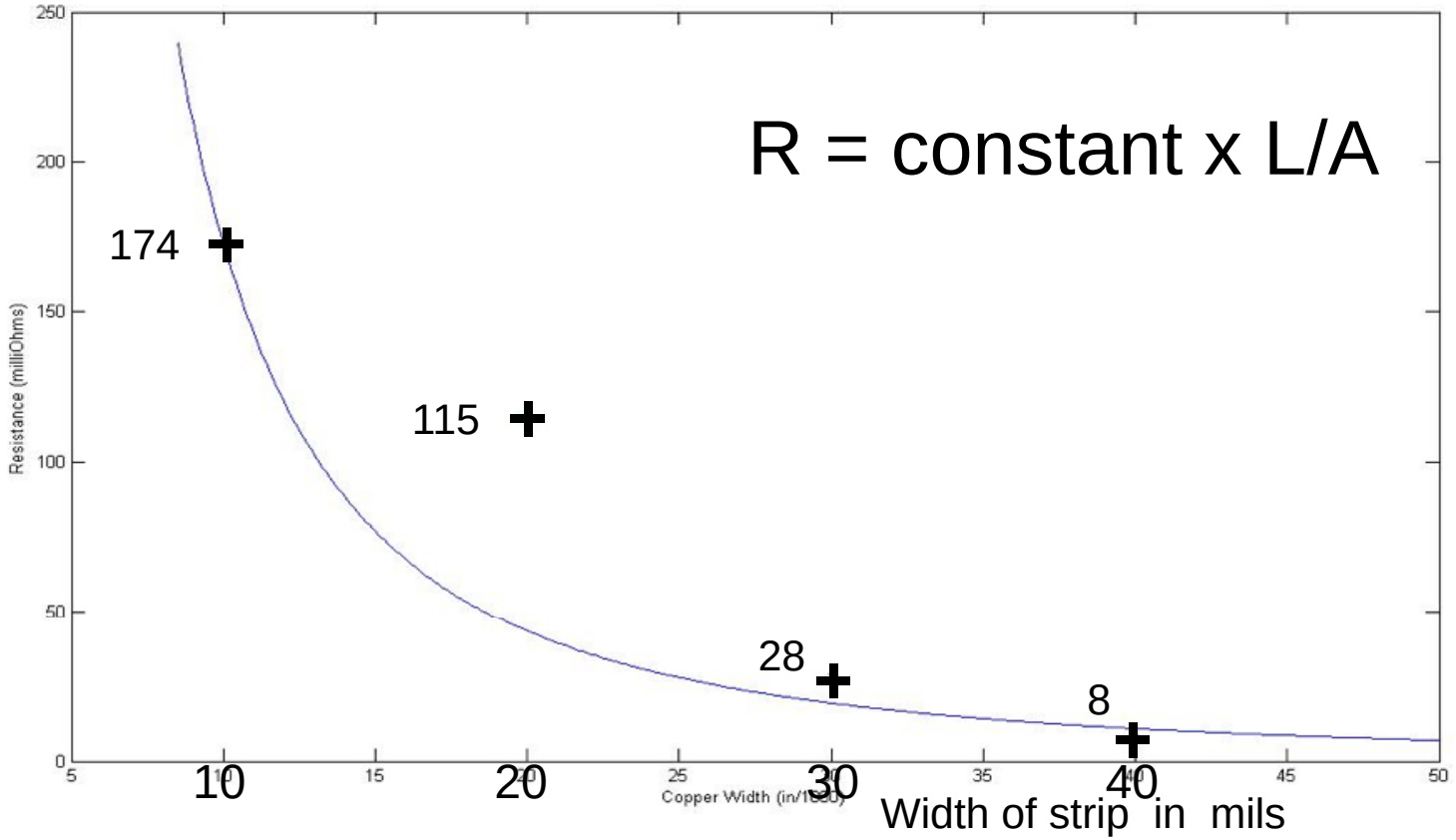


Temperature and pressure control and readback.

Duration and ramp-up/ramp-down are also factors.



Initial Results

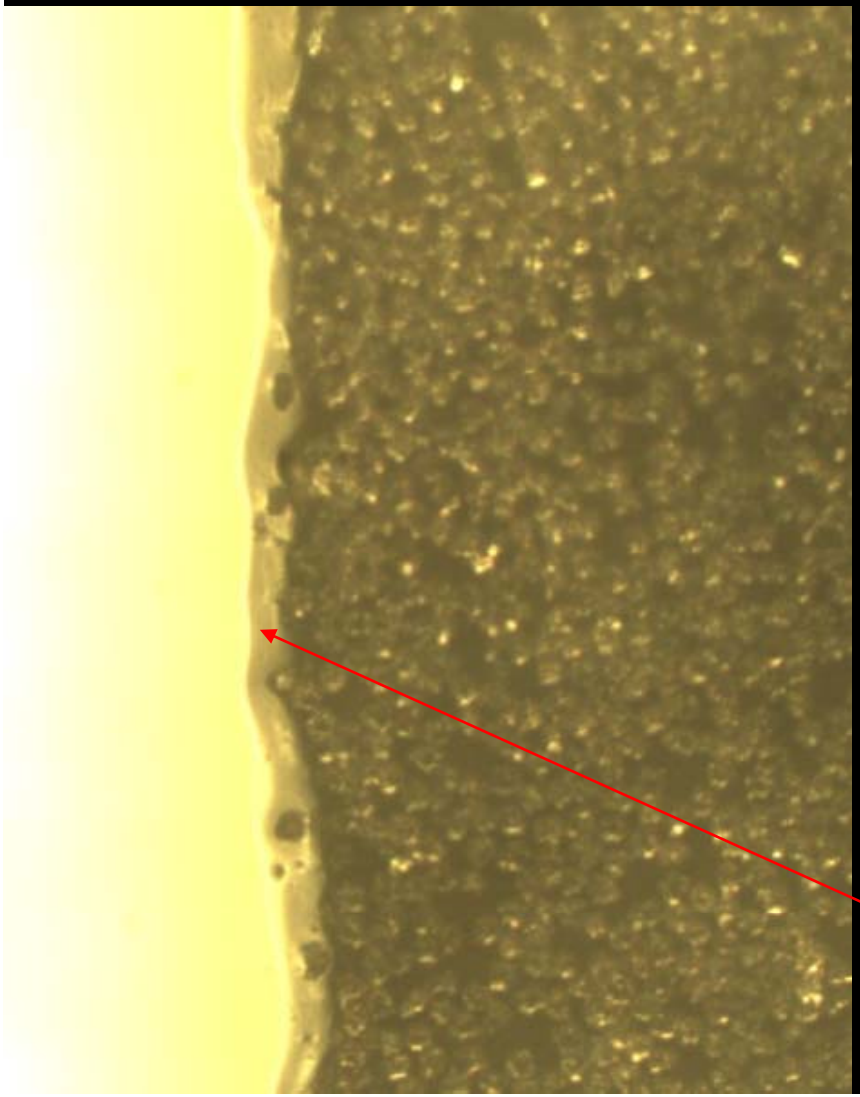


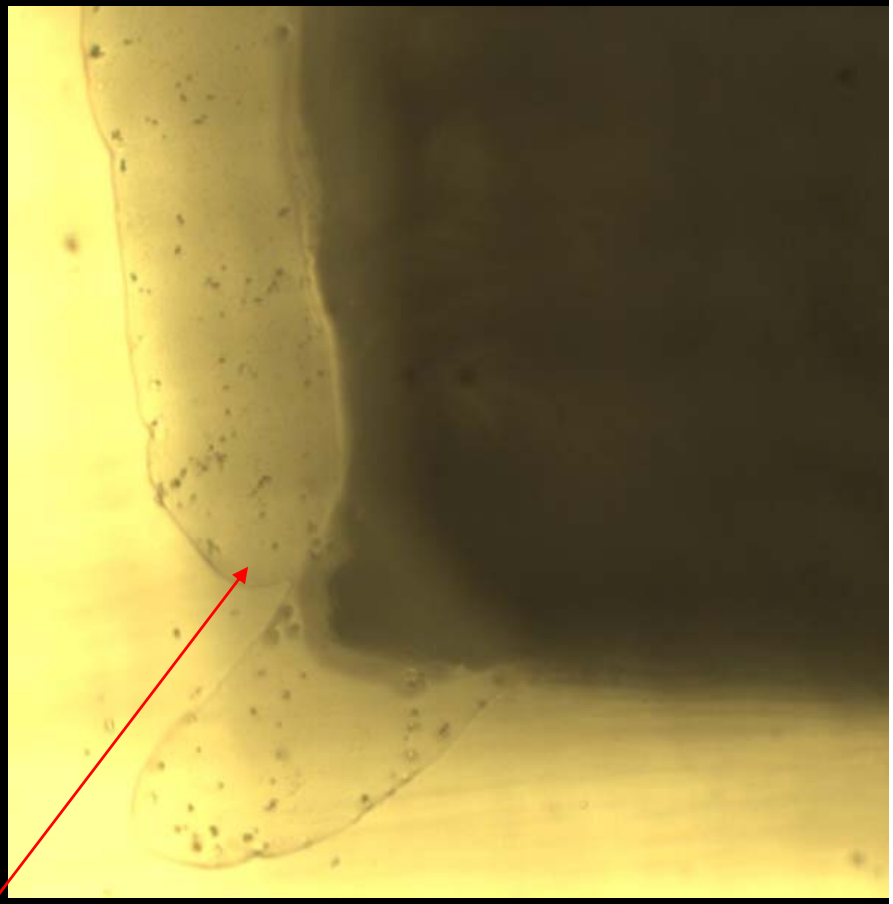
The results are promising.

One anomalous data point => more study of process parameters is needed.

ACF between glass cover slips

- Allows for observation under a microscope.





"Oozing of adhesive needs to be studied and controlled.

Summary

- The R&D for Si-W ECal technology is progressing steadily.

Near-term Goal:
Construct a "Tower": full-depth (30 layer), single-wafer wide module with 1024 channel KPiX chips bonded to sensor wafers and read out via flex cables. => Test Beam.