Status of the construction of a $1m^3$ Digital Hadron Calorimeter prototype

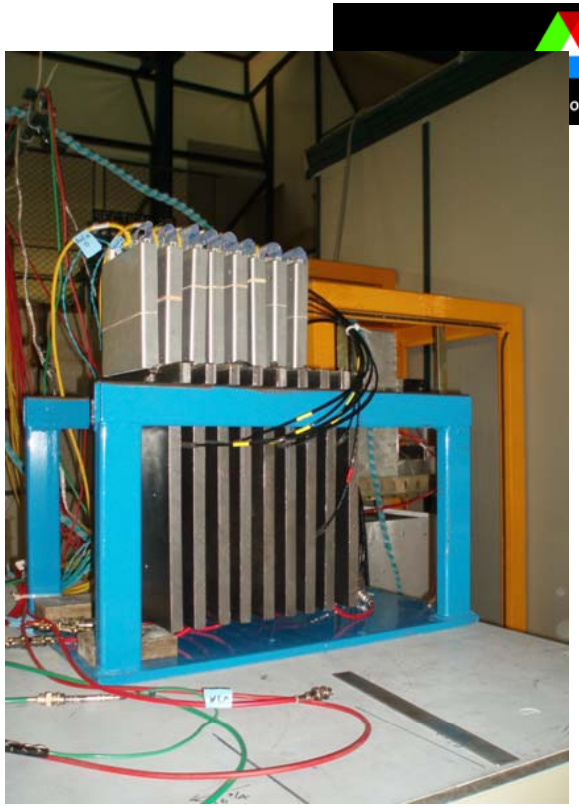
Lei Xia

ANL-HEP

Outline

- We had a very successful beam test (slice test) with a small DHCal prototype, using RPC as the active medium
  - Muon sample analysis done
  - Other analysis on-going
- After beam test, the slice setup was turned into cosmic ray running and became our very useful test stand
  - Complete test and debugging of electronic readout
  - Test of new readout prototypes
  - RPC aging test, running condition tests
  - Test of large RPC, readout components, and daq for $1m^3$
- Construction of the $1m^3$ prototype
  - DCAL III
  - New readout components (FE, Pad boards, DCon)
  - Multiple DCol running + daq/off-line software upgrade
  - Large RPC construction and testing
  - Gas mixing and distribution system
  - HV control and distribution
  - Gluing machine
  - RPC cassette
- Timeline

DHCal Slice Test

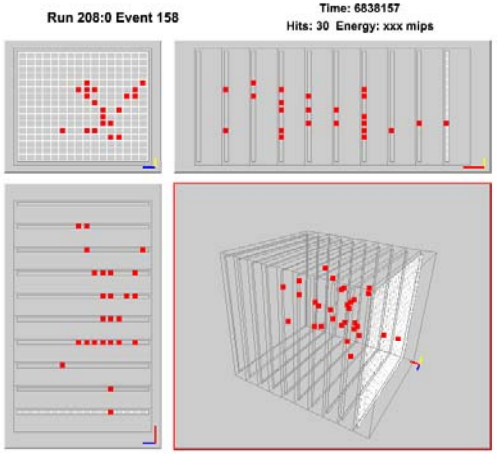


Vertical Slice Test with up to 10 RPCs (20 x 20 cm^2)

Tests included the entire electronic readout chain
Extensive tests with cosmic rays and in Fermilab test beam
3 papers in refereed journal

Finished analysis

Muon data sample -- DONE
RPC property measurements: efficiency, multiplicity
Calibration scheme for a DHCal
Paper published on JINST



On-going analysis

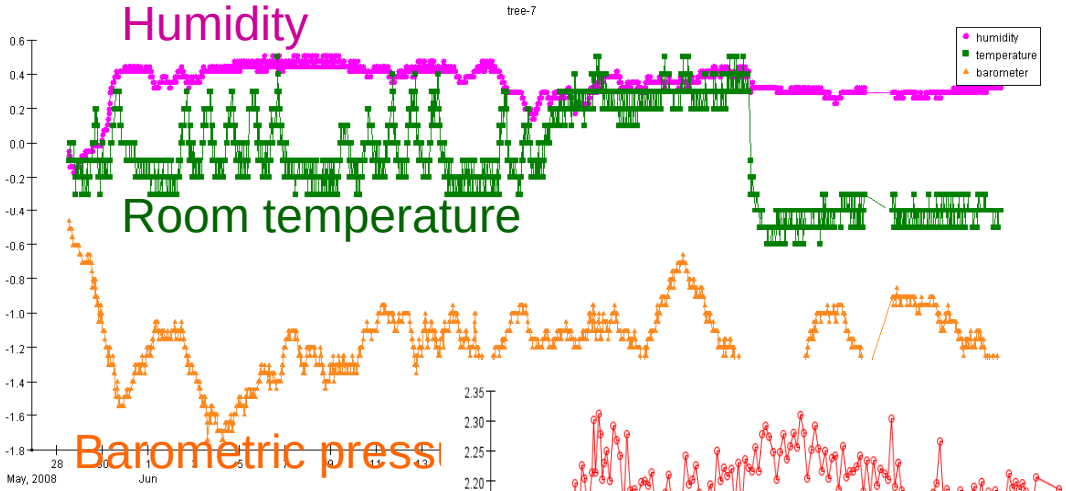
Positron data: almost done
Pion data: started
Rate measurement: started, a lot of progress

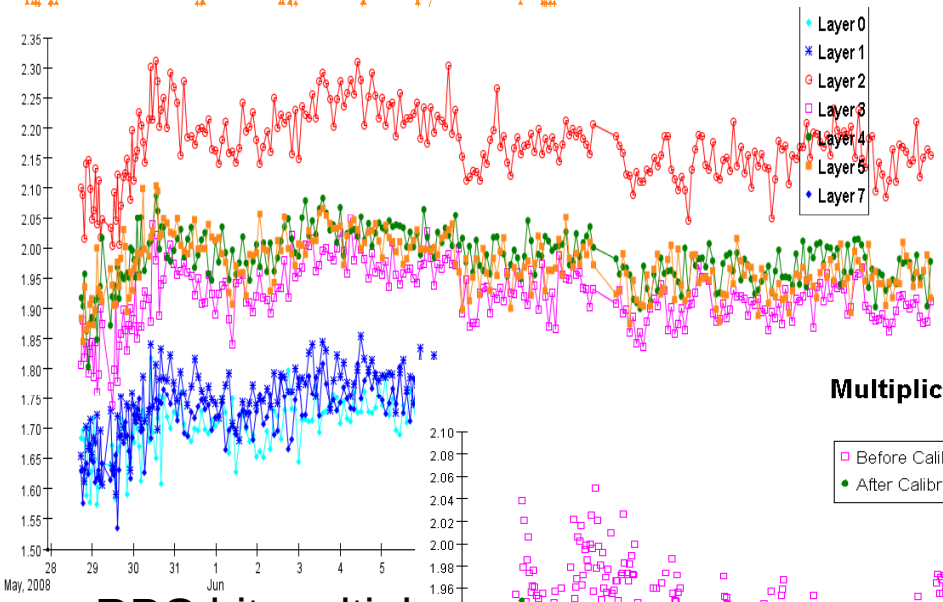
Details on analysis progress: next talk (Jose Repond)

Cosmic rays test stand

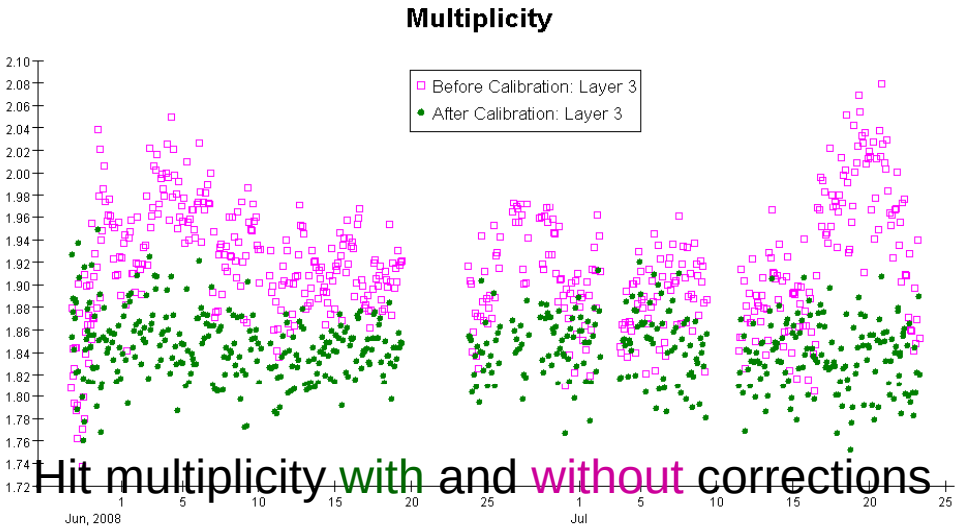
- After a successful beam test, we took a lot of time to understand our system better
  - Data errors has been identified and understood (~13 error modes)
  - Most errors has been eliminated by system improvements (grounding, noise reduction, firmware improvements, etc.)
  - Current error rates < 0.000n%
- We studied running conditions for a larger system
  - Gas distribution & flow rate
  - Environmental impact
- Aging tests
  - No aging seen after 1.5 years running
  - All chambers in great shape: low and stable noise rate, including ‘exotic’ RPC
  - (a few chambers damaged for known reason – not related to aging)
- We also used the test stand to test new components for 1m^3 construction

Weather condition and RPC running





RPC hit multipl

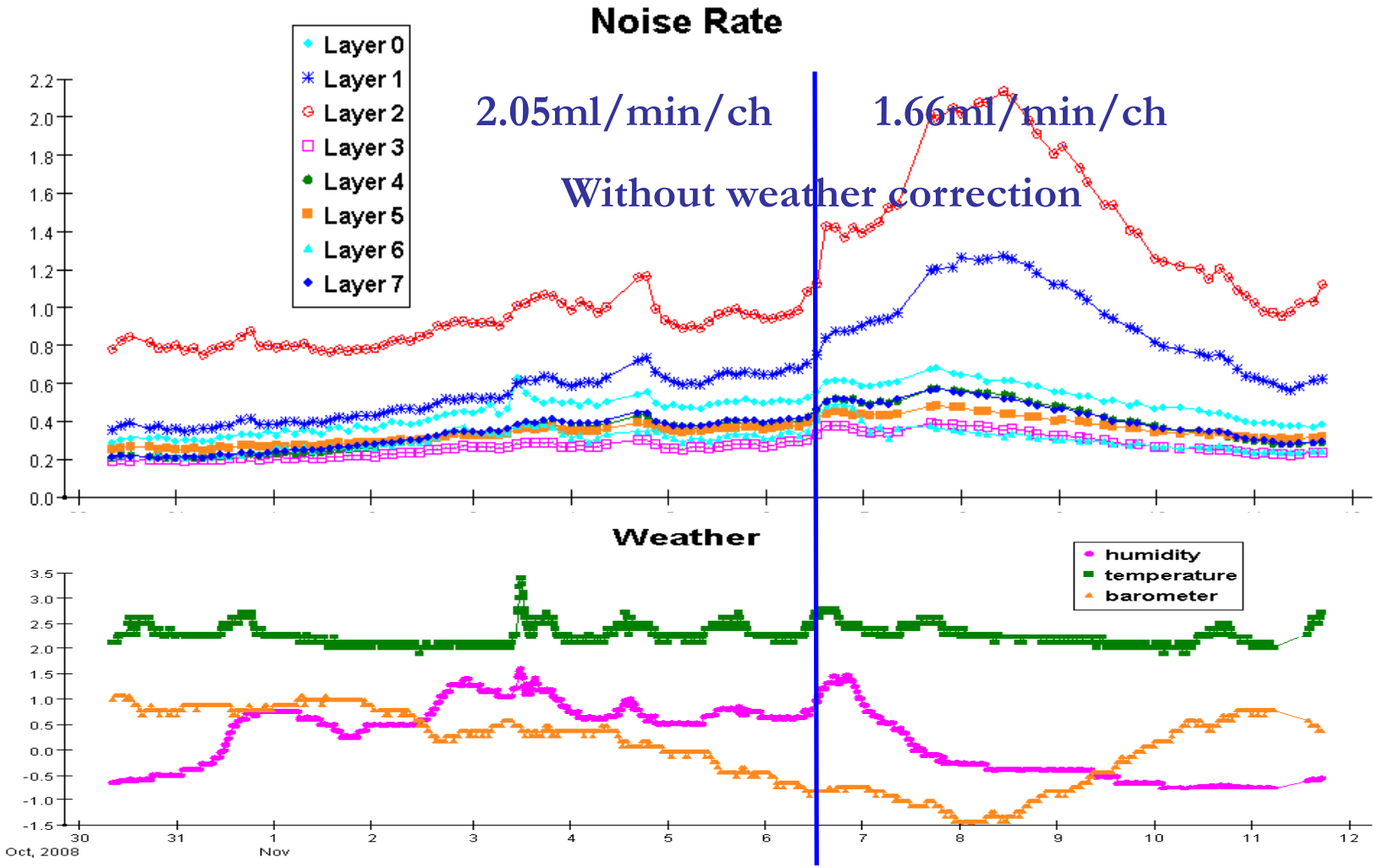


Hit multiplicity with and without corrections

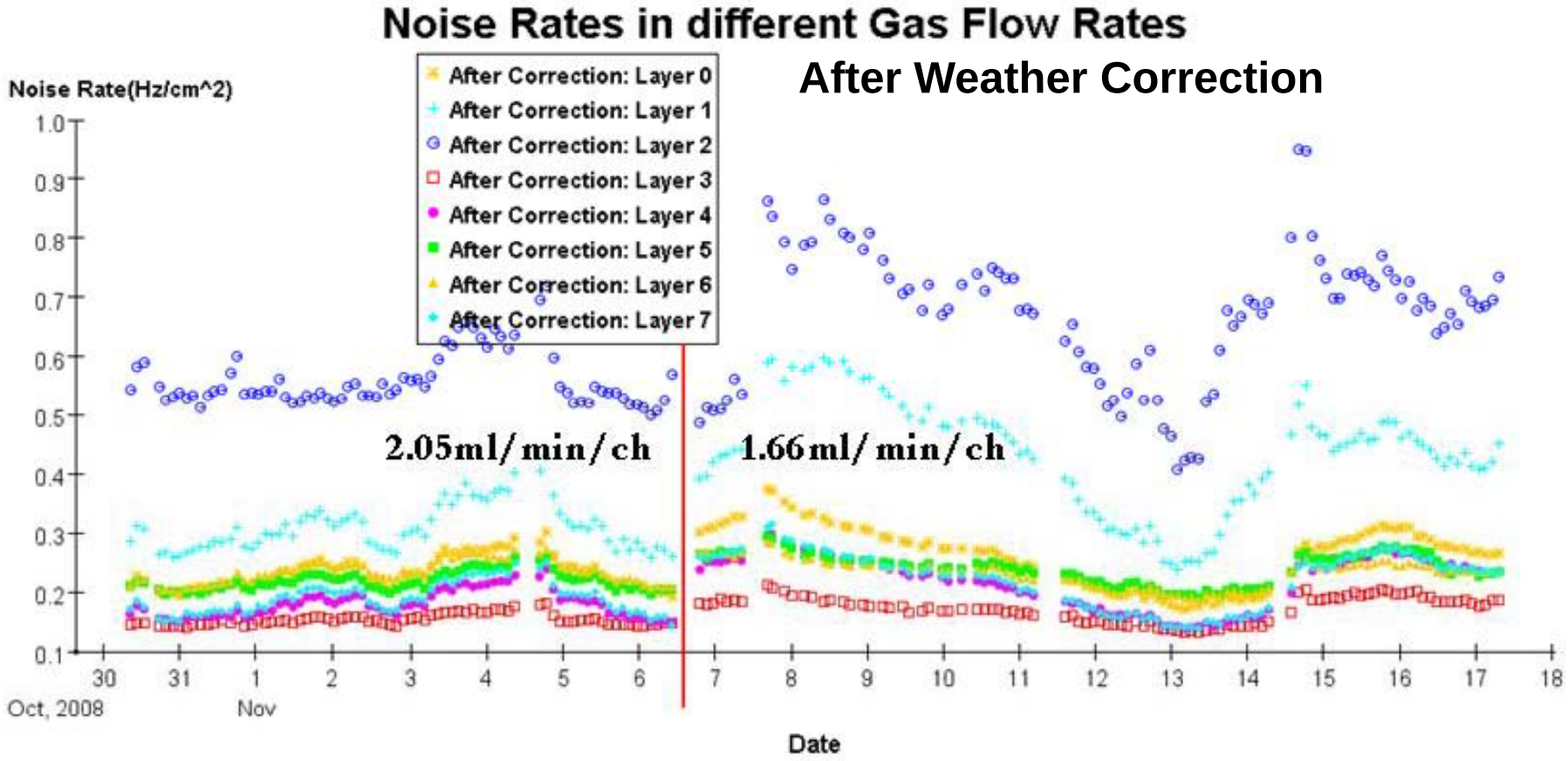
Qingmin reported detailed results this morning

Gas flow studies

- What is the minimum gas flow rate to avoid damaging RPCs?
- How long can gas travel inside RPC gas volume without being too contaminated?



Gas flow studies



With weather correction, effect from gas flow rate becomes clear

Recipe for 1m^3 prototype

	Slice Test	1m^3 Prototype
RPC	~10, 20x20 cm^2 Frame machined	~120, 32x96 cm^2 Frame extruded
DCAL ASIC	~50, DCAL II	~6,000, DCAL III fixed bugs in DCAL II
FE & Pad board	~10, 256ch, 4 DCAL II Glued by hand	~240, 1536ch, 24 DCAL III To be glued by machine
Data concentrator	~10, handle 4 DCAL II	(handle 24 DCAL III) (Build into new FE board)
Data collector	1, handle 12 DCON	~20, same design
Trigger & timing module	1 (1 per VME box)	2, same design
HV system	~10ch, Manual control/monitor/record	~120ch, computer control/monitor/record
Gas system	~10ch, pre-mixed gas	~120ch, real time gas mixing system
DAQ software	Stand-alone: used in test beam Calice based: tested, current default	Calice based will be used Moderate change needed
Analysis software	Stand-alone	Dramatic change needed (To be calice compatible?)

The DCAL III: fixing issues in DCAL II

Jim Hoff and Gary Drake

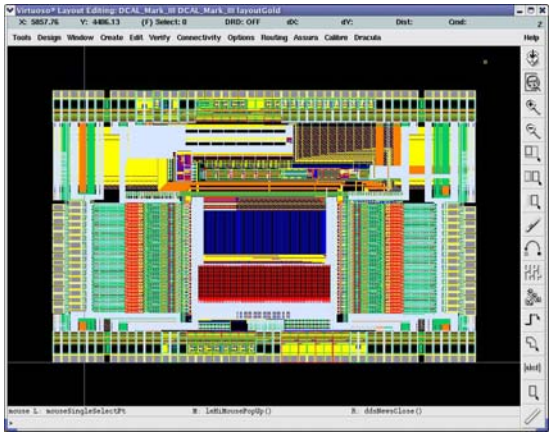
1. Problem Saving Data to Output FIFO
   - For DCAL II, when Output Buffer is empty, it missed the first write operation of data 50% of the time
   - Problem due to Sync/Status circuitry – the steady state data stream from the chip. During the Sync phase, the circuitry ignored new data write cycles. → ***Fixed***

2. Problem with Reading Slow Control Data
   - For DCAL II, could not connect read slow control data lines to a common bus as intended.
   - Problem: enable for output drivers for reading slow control data did not use chip select. → ***Fixed***

3. Changes to Mask & QINJ Registers
   - For DCAL II, Mask & QINJ Registers were embedded into each front end channel, loaded serially with a 64-bit data stream. Each register implemented as an edge-triggered flip-flop. These registers were write-only, and could not be read.
   - Problem: Registers appeared to be reset unintentionally during a data acquisition run, at least partly correlated with chamber sparking. Best guess is that noise from the sparking caused the edge-triggered flip-flops to reset.
   - The Fix: the edge-triggered flip-flops were removed and standard-type SR flip-flops were put in, situated in the slow control section (away from the front-end channels.) This topology is more robust to noise, and should be less susceptible being moved away from the front-ends. The registers are now readable (16 new registers, plus one control register to perform the load operation.) → ***Fixed***

All changes implemented

Design completed in July

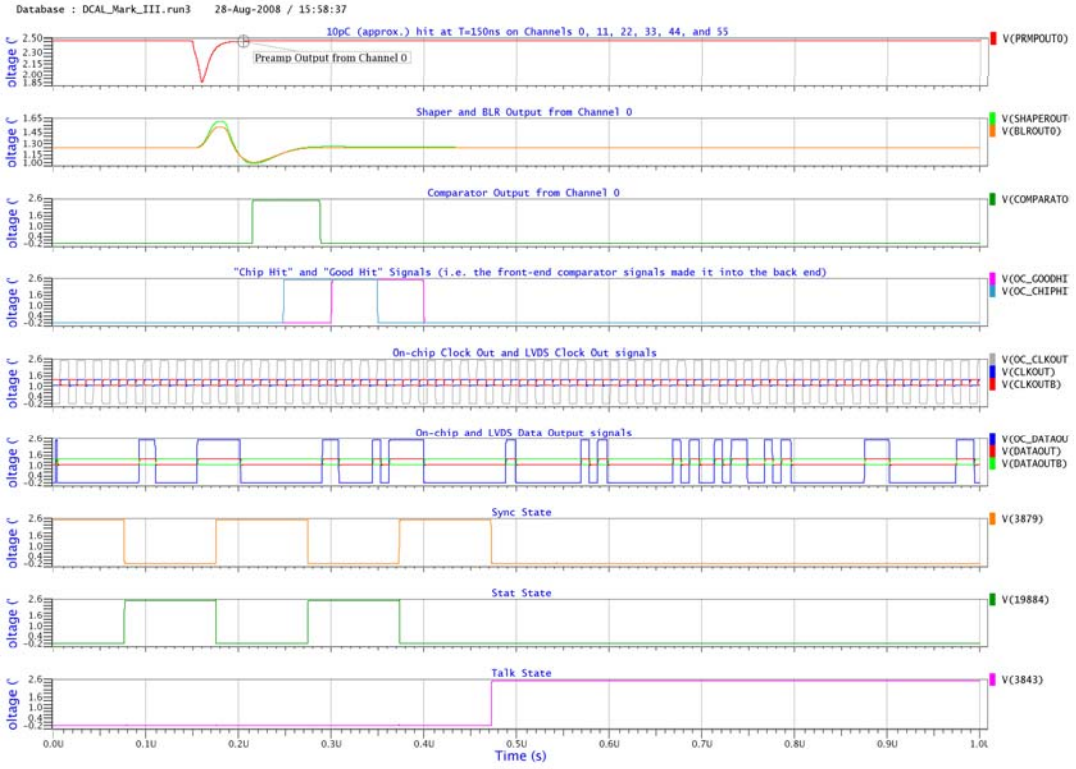


Simulation done

Financing of production sorted out

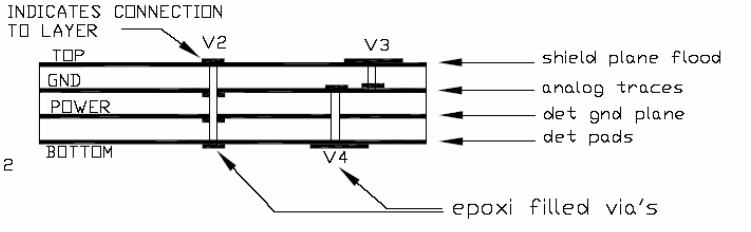
Cost ~ $150,000 (for mask) + $50,000 (for >9 wafers) + $20,000 (for packaging)
Argonne – Fermilab contribute ~ 50:50

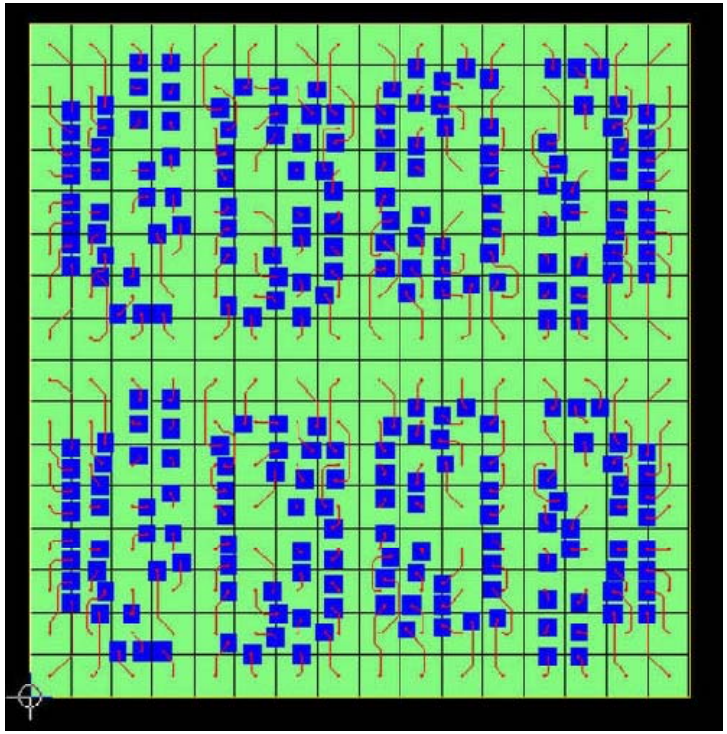
Submission last month



Slice Test Pad Board & Front End Board

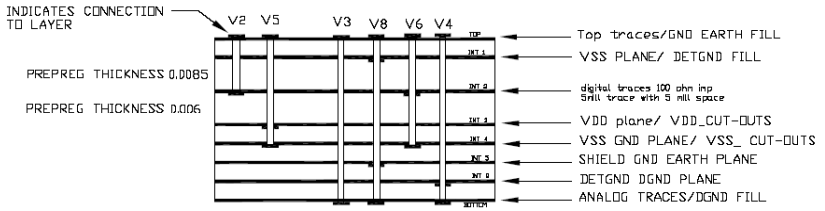
4-layer Pad-board (3 shown)

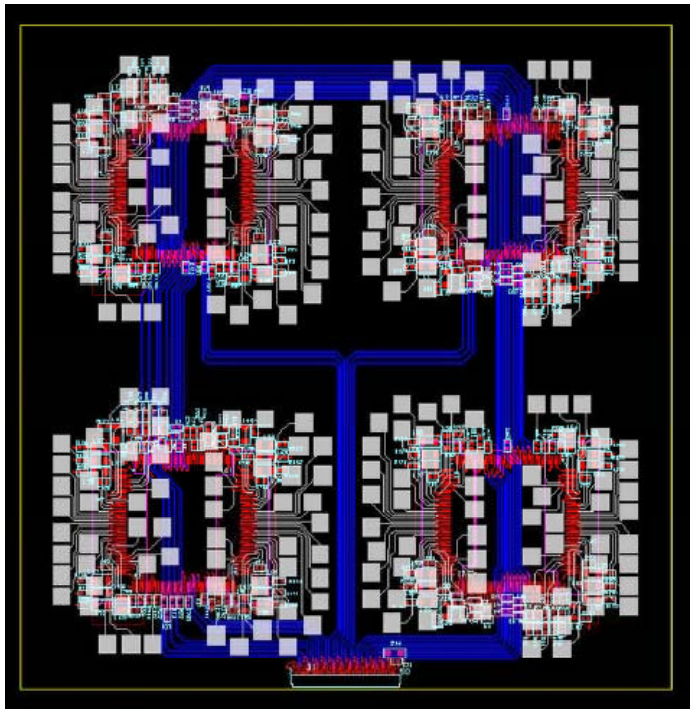




Blind vias to route sensitive signals to glue pads – needed to minimize contact with digital lines in FEB

8-layer FE-board (3 layers shown)





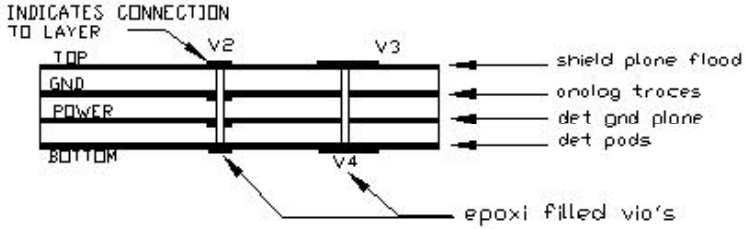
Also has blind vias
→ Very complex board design to minimize crosstalk & digital noise pickup

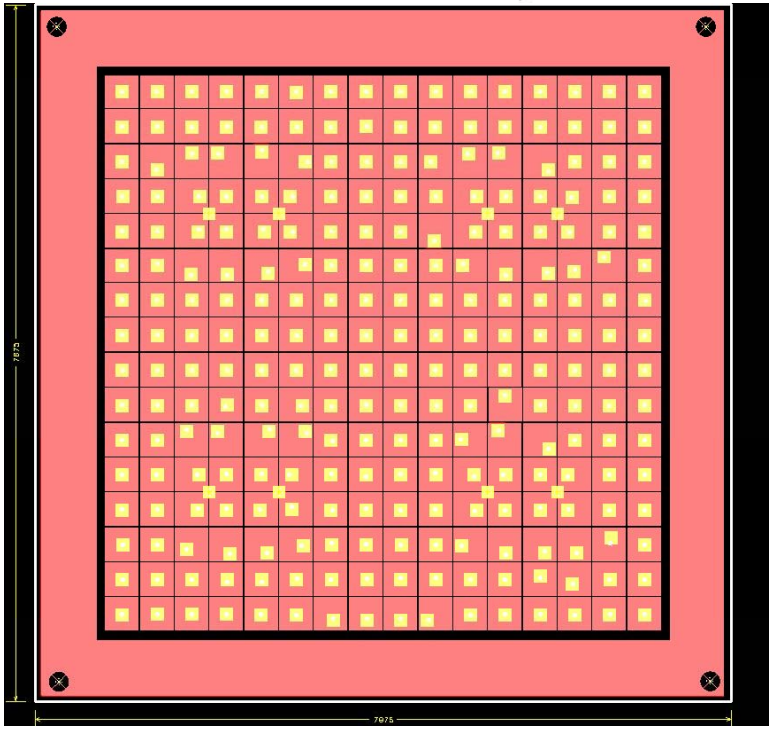
Front End Board - Work in Progress

- FE board and Pad board are glued together to avoid buried vias
- Current design has extremely good noise performance
  - Noise floor: only 10 – 15 DAC count (low gain)
  - System comfortably runs @ 30 DAC count or even lower (normal runs @110 DAC count)
  - Left a lot of head room for cost reduction
- Have designed and produced new 16 cm x 16 cm FEB with ***NO*** blind vias
  - Still 8 layer
  - Still has ground shielding layers to protect charge signals
  - Primary change: now ALL vias come down to glue pad layer (bottom)
- Have designed and produced ***Two*** new 16 cm x 16 cm Pad Boards also with ***NO*** blind vias
  - One is 2 layer, with no internal ground plane
  - One is 4 layer with 2 internal ground layers
- Tests show that new boards have the same excellent noise performance
  - Noise floor of two boards (FE+pad): 11 – 12 DAC counts
  - This will simplify large FE board and Pad board fabrication

New Pad Board & Front End Board Design

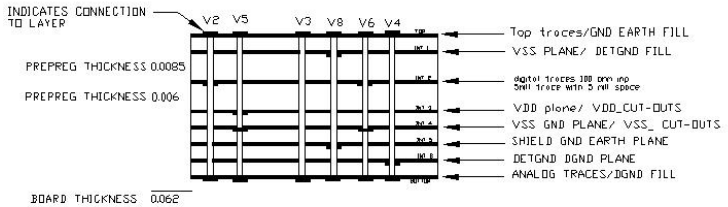
4-layer Pad-board (3 shown)

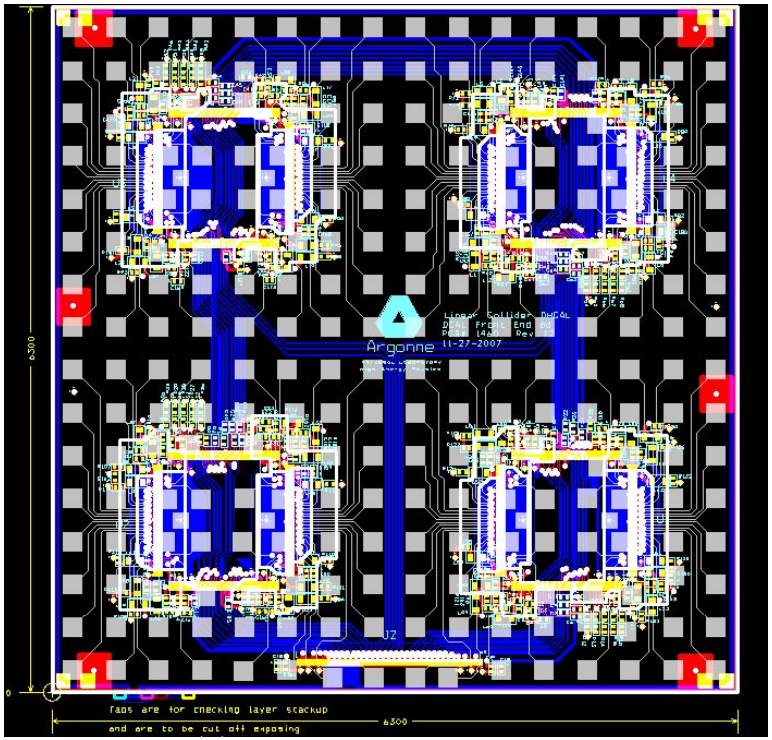




No blind vias

8-layer FE-board (3 layers shown)

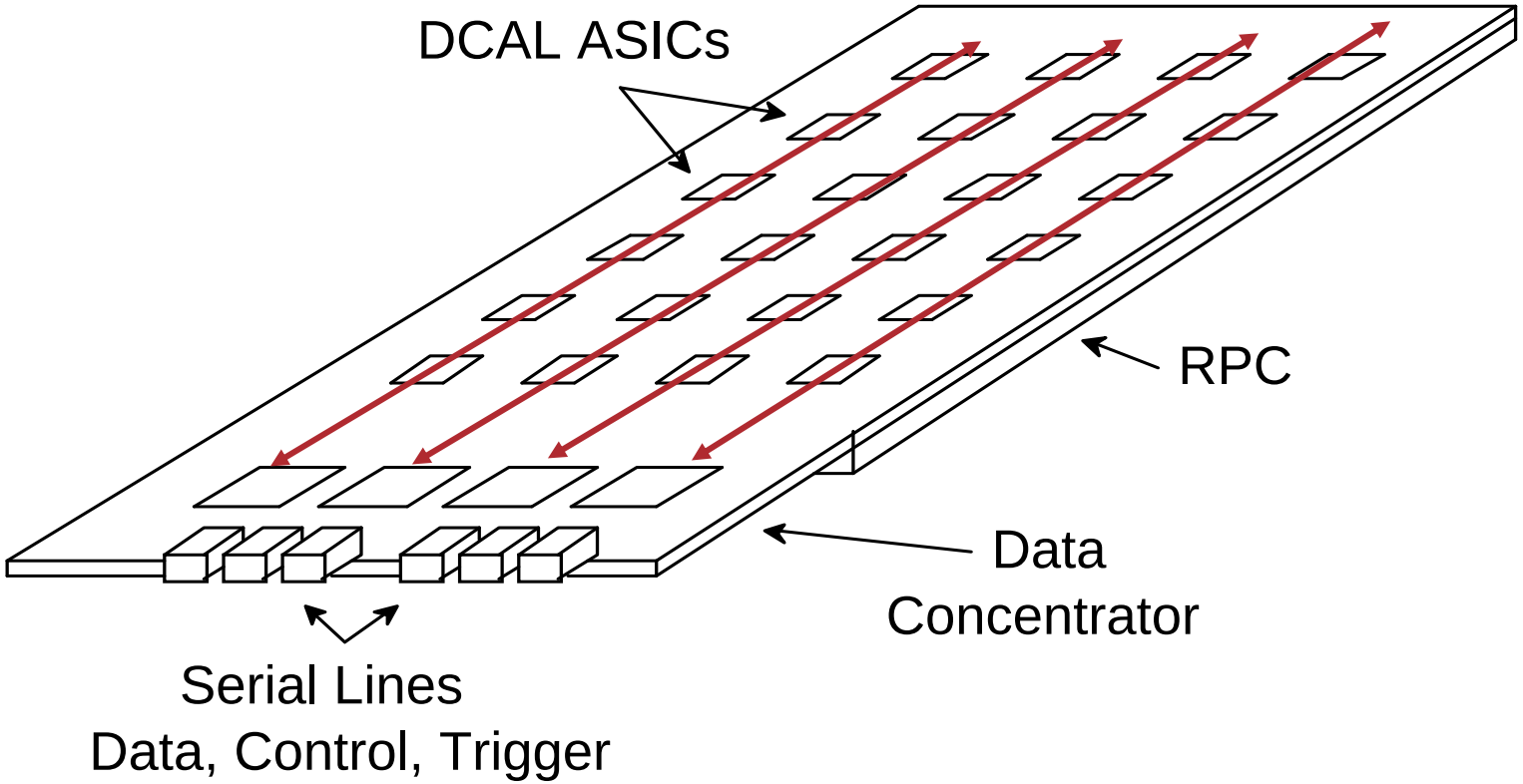




No blind vias

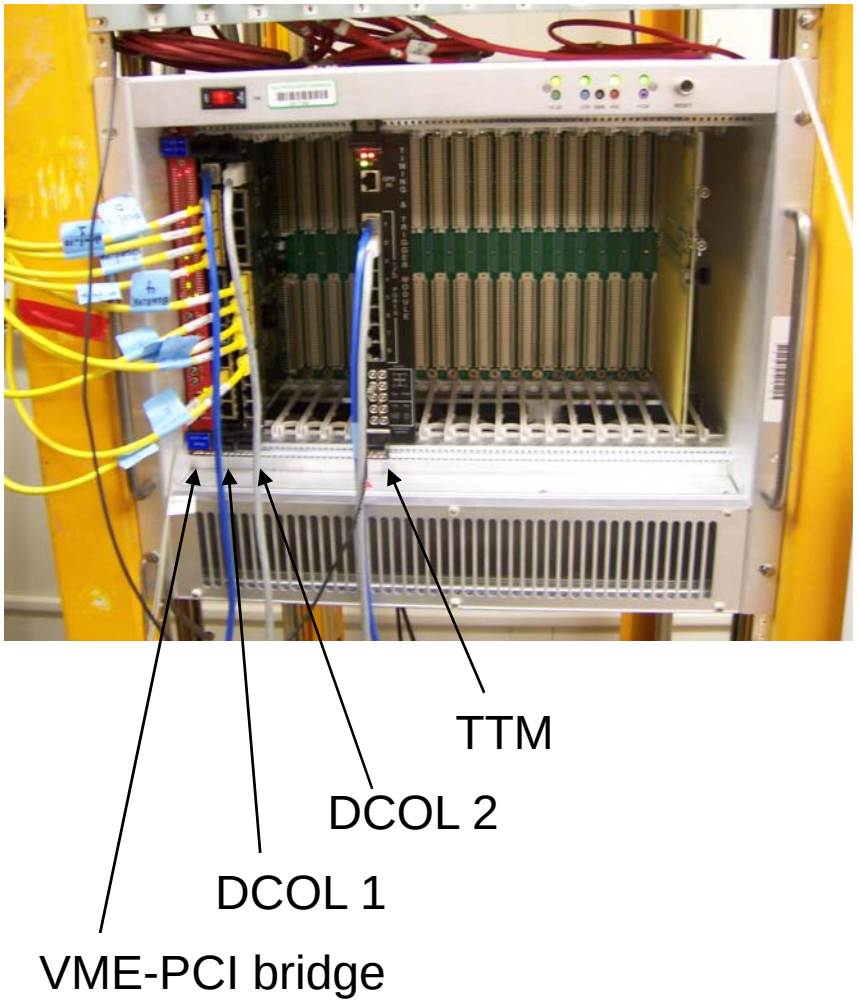
FEB & Data Concentrator – Work in Progress

- New Data Concentrators – One services 24 chips
  - Idea: Column Architecture
- Going a step further: Make FEB & Data Concentrator Monolithic...



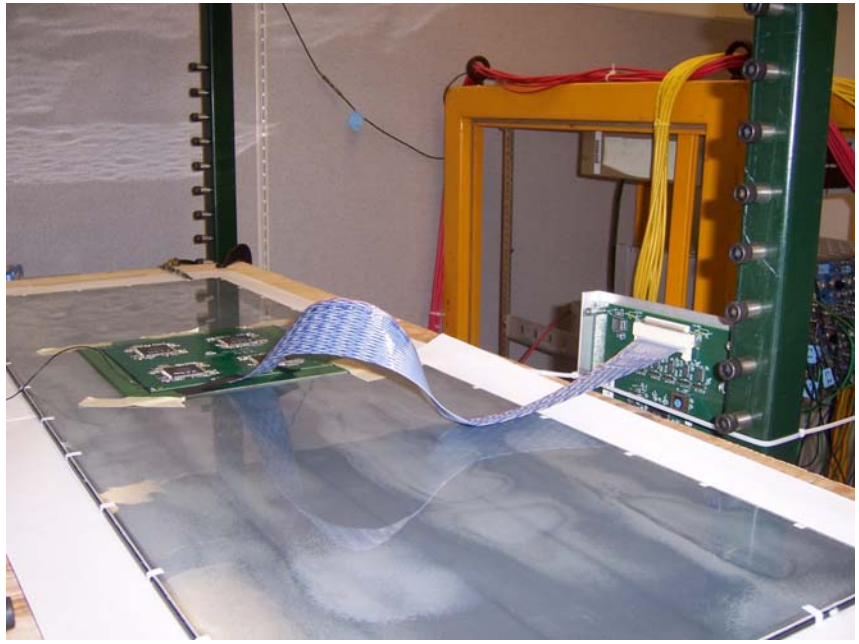
DAQ/Analysis software and 2 DCOL test

- Test beam was done with single data collector
  - Data are nicely in time order
  - Simple home cooked daq
  - Simple event building logic (but became very complicate when dealing with errors)
- New daq based on CALICE frame work
  - Added DHCAL specific run types
  - Tested and became default for data taking since June
  - Tested with 2 data collectors
  - Capable of running $1m^3$ prototype, with limited modifications
  - A lot of tests needed for $1m^3$
- New event builder: dramatic changes needed
  - Error handling significantly simplified
  - Event building logic becomes complicated
  - Most likely will evolve with detector configuration

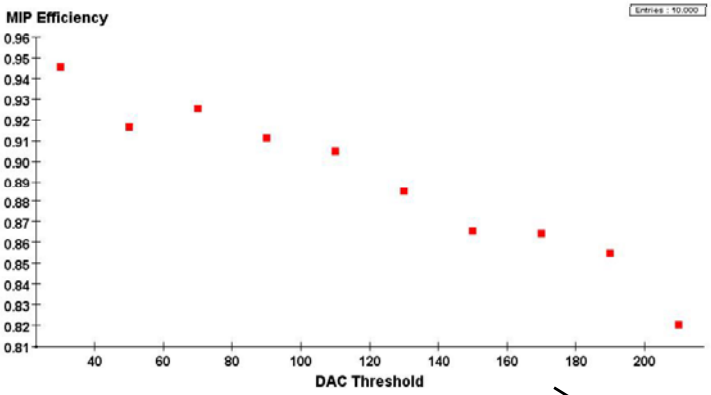


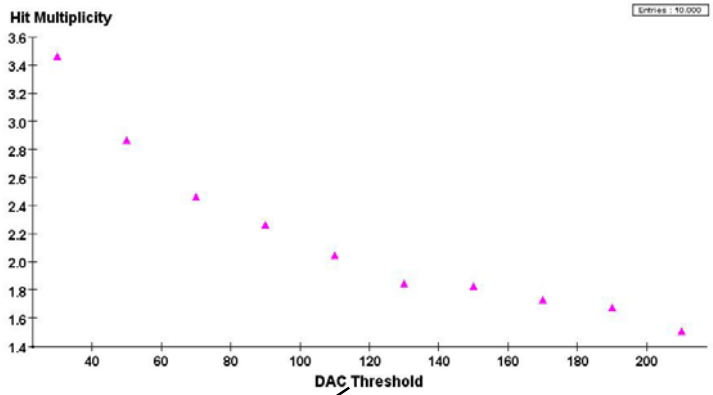
Large RPC production: 1st RPC finished and tested

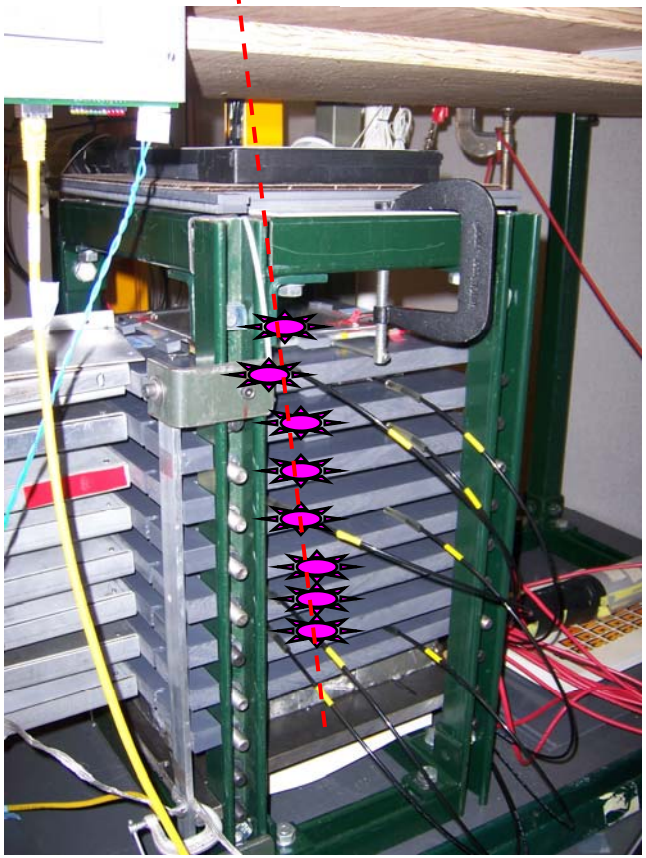
- 1st full size RPC constructed for 1m^3
  - Used 1.2mm glass, 96cm x 32cm
  - (VST: 1.1mm glass, 20cm x 20cm)
- Frame for 1m^3 RPCs extruded
  - Slice test RPC frames were machined
  - 1m3 RPCs uses extruded frames
  - Better control on critical dimensions
- Slightly modified assembly procedure works for large chamber
  - Chamber is gas tight (~ 5 meters long glue trace!)
  - Chamber is relatively stiff, deformation doesn't affect gas tightness
  - Good for large scale production
- Chamber dead area: 4.7%
  - Frame: 3.3%
  - Fishing line: 1.4%

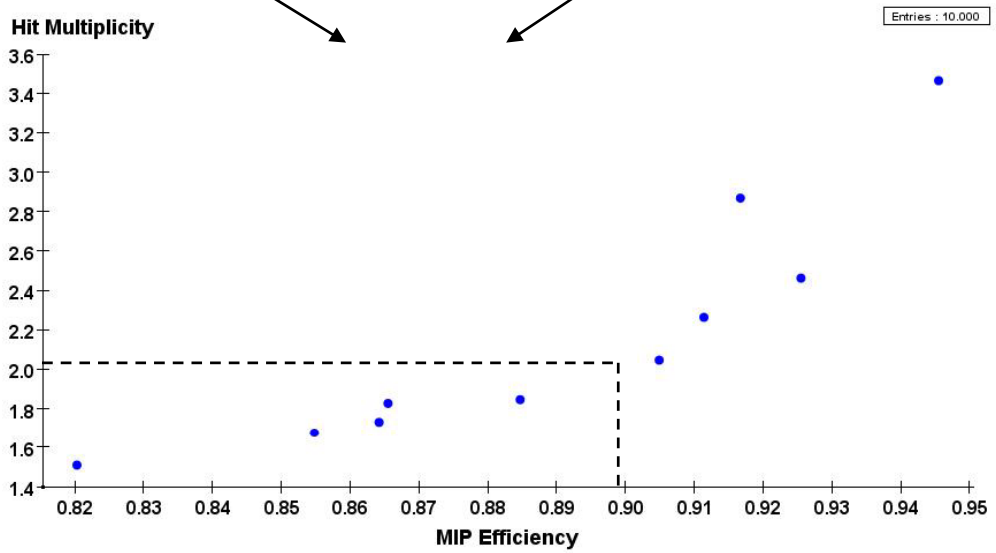


Test of 1st large RPC





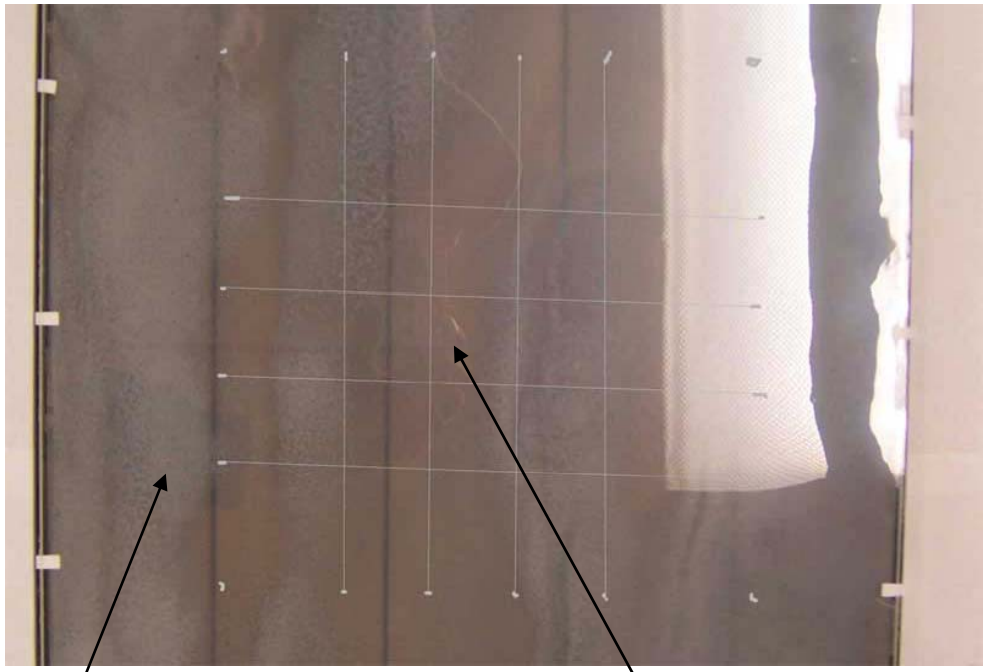




At 90% efficiency, hit multiplicity ~ 2.0
(compare to slice test: 1.5 – 1.7)

Lei Xia

Test of 1st large RPC



White area: 0.2MOhms/square

Transparent area: 1.MOhms/square

0.99	0.93	0.96
0.96	0.94	1.01
1.04	1.05	1.11

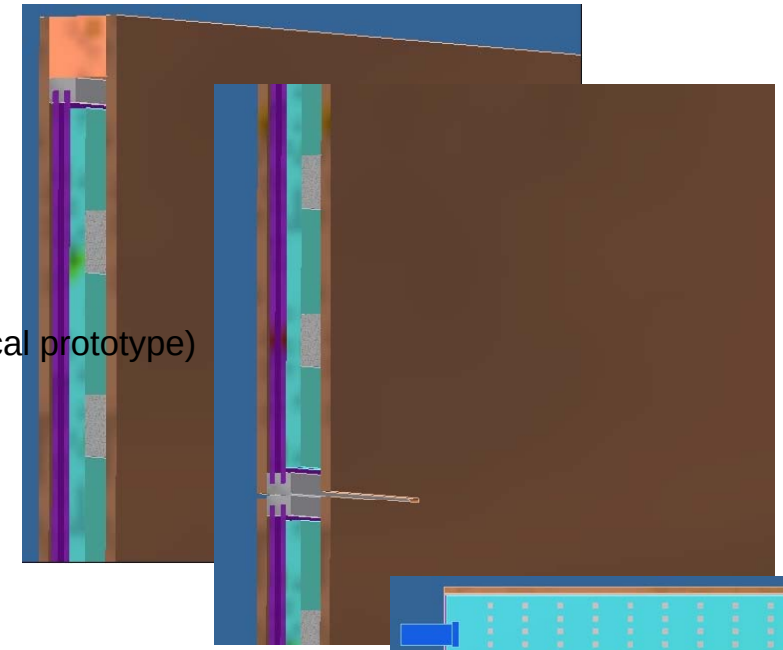
Hit multiplicity
(normalized to average)

Suggests correlation between surface resistivity and hit multiplicity
(agrees with our previous measurements)

RPC Cassettes and Gluing Machine

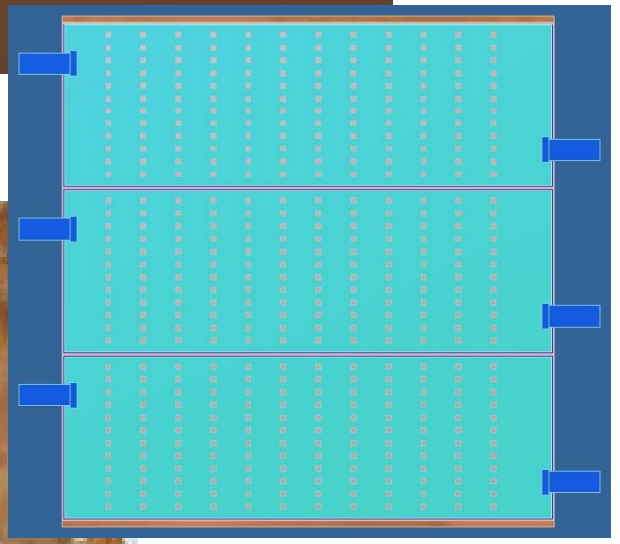
Cassettes

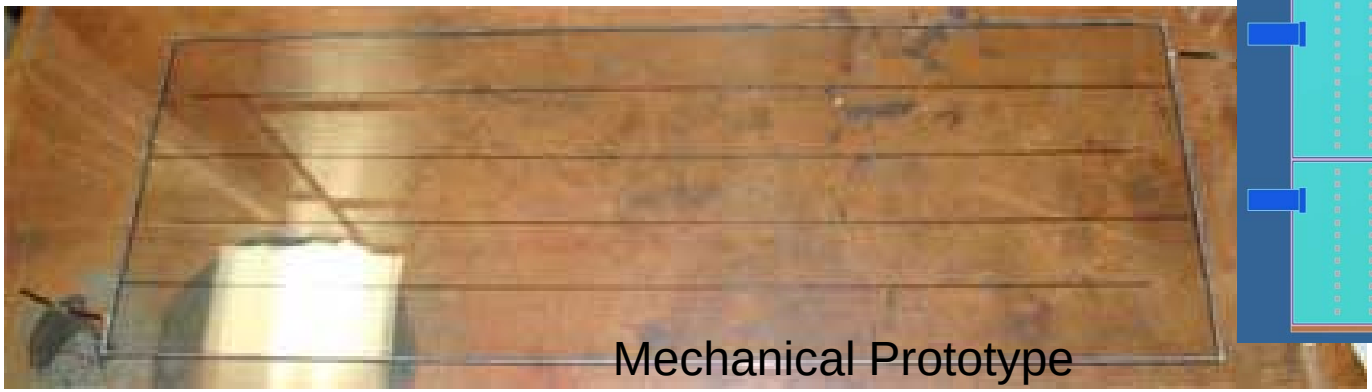
Design of 1 x 1 m^2 cassettes complete
Material for (few) cassettes in hand
Assembly of 1st (fake) cassette started
3 large RPCs produced for cassette tests (mechanical prototype)



Gluing machine

x-y moving stage to locate the glue syringe
Solenoid in z to move up (travel) – down (deposit)
Electric relay to dispense glue
Control elements: 2 stepping motors and amplifiers + controller + solenoid





Mechanical Prototype

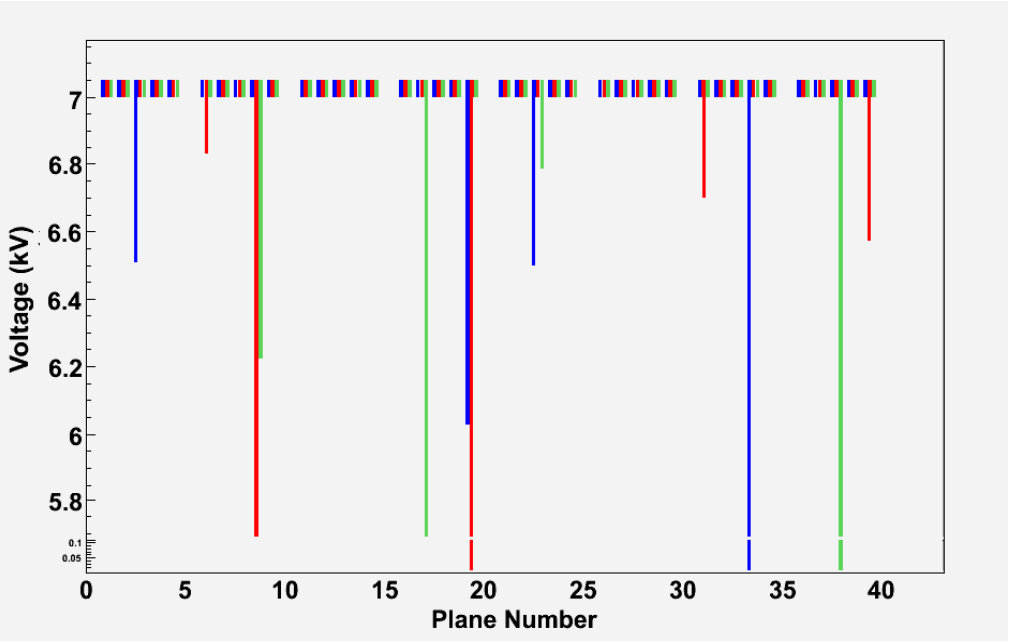
Gas and High Voltage system

Gas mixing and distribution system

Premixed gas in small tanks (as used for slice test) not adequate for larger system
Required flow rate ~ 10 liters/hour
Started assembly of mixing system (94.5:5.0:0.5)
Eventually will need to recycle (purify) gas (but not for 1 m^3 prototype section)

High Voltage system and display

Will use LeCroy 32-channel High Voltage unit
Control interface/program done and tested
Display program for 120 channels written
Example: HV set to 7 kV with a few problematic channels



(David Northacker and Ed Norbeck)

LCWS08

Time Table

Month	9	10	11	12	1	2	3	4	5	6	7	8
RPC production	Build #1 and test	Build #2 #3 #4	Test									
Cassettes			Assemble 1st layer	Design layout of supplies								
DCAL chip	Design and simulate	Submit for production	Prepare packaged chip tests	Start testing								
Readout system	Complete tests of PadB and FEB Develop gluing techniques		Initiate design of new DCON Gluing test		Prototype combined FEB & DCON							
DAQ		Test with multiple DCOL		Modify DAQ SW for 1 m^3								
HV and gas	Develop HV control SW Initiate assembly of gas mixing system				Complete gas mixing system							
Miscellaneous												
System						Test layer #1						

Ready for production

Conclusion

- $1m^3$ construction has started!
- A lot of fun ahead…
  - Provide solid proof for Digital HCal concept
  - Detailed shower shape measurement and comparison with simulation
  - Comparison with CALICE scintillator - analog HCal concept

We will reuse CALICE AHCAL structure

- Collaborators: ANL, BU, Fermilab, Iowa, IHEP(Beijing), UTA, …