

RPC based Semi-Digital HCAL with an embedded readout

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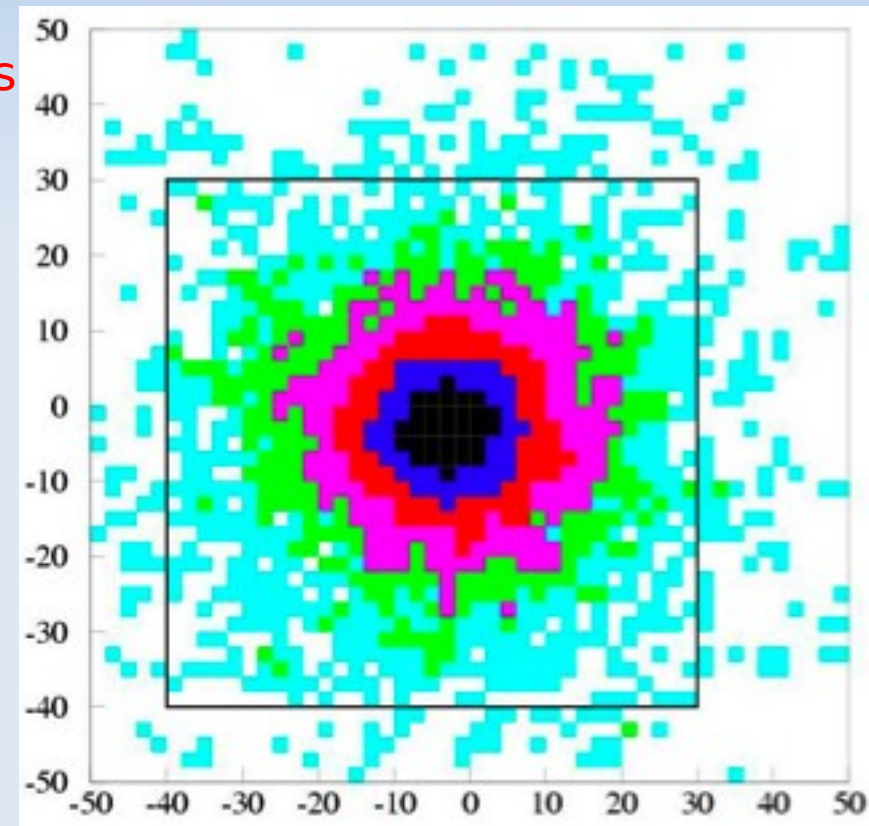
LM



- Case for a digital calorimeter
 - Detectors :
 - ▶ RPC, MGRPC
 - ▶ μ MEGAS, GEMs
 - Digital Readout by embedded ASICs
 - ▶ HARDROC
 - ▶ DIRAC
 - Integration & Debug Card: DHCAL1 & readout
 - Cosmic tests
 - Beam tests
- 1 m² prototype
 - ▶ Validation of large surface detector & readout
 - 1 m³ prototype
 - ▶ First use of 2nd gen DAQ
 - ◆ see V. Bartsch talk
 - *Efforts of integration in ILD & SiD*
 - ▶ *Mechanical & simulation*

Case for a **D**igital **H**Adronic **CAL**orimeter

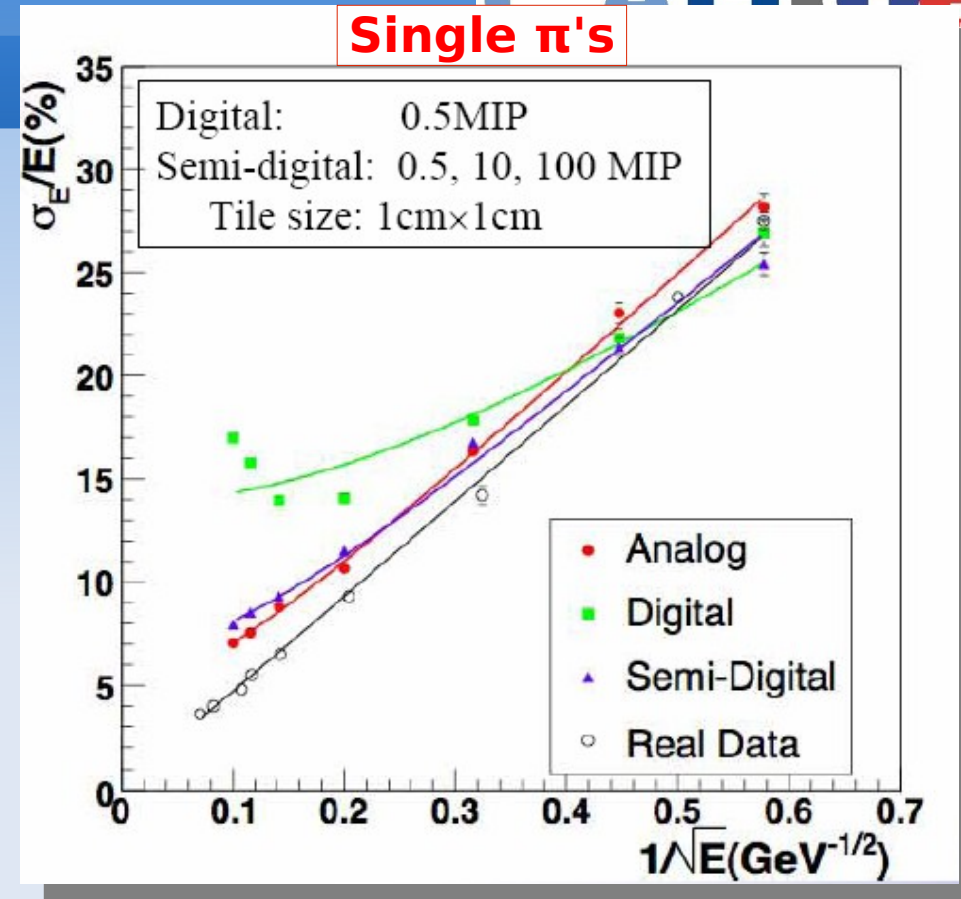
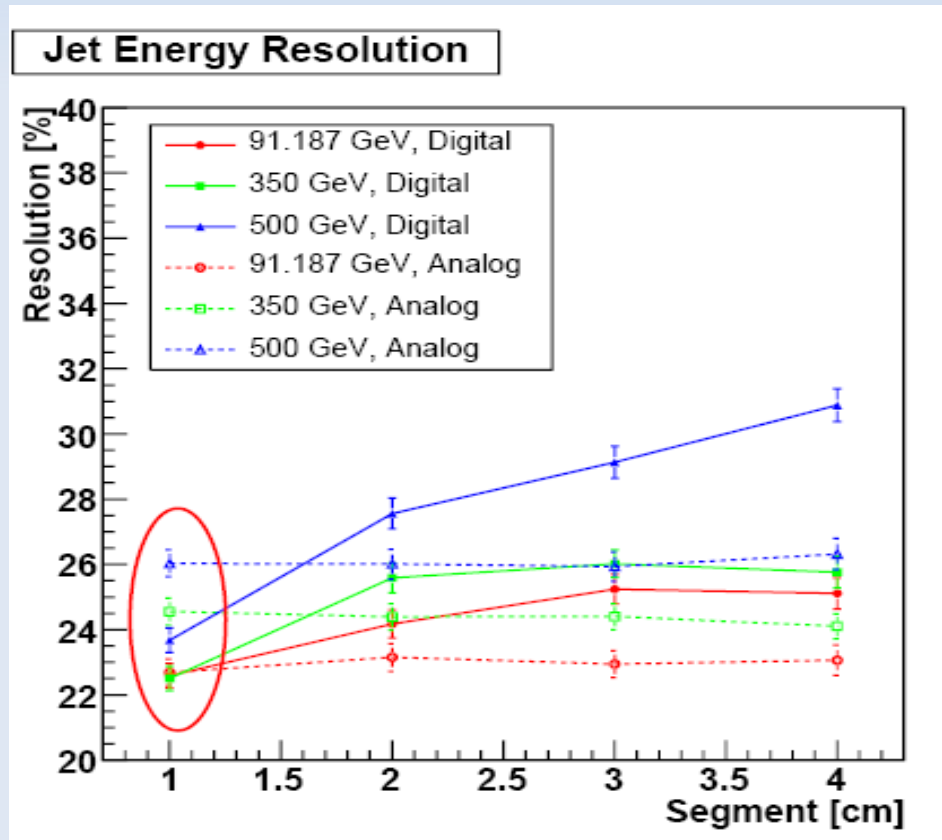
- 1 or 2 bits of information per cell
 - ▶ Finer granularity $\rightarrow 1 \times 1 \text{ cm}^2 \times 48 \text{ planes}$
 - ◆ Ideal for a **PFA** approach
 - ▶ Cheaper, simpler, more robust detectors
 - ◆ GRPC, MGRPC, μ MEGAS, GEM's
- Gaseous detectors
 - ▶ insensitivity to neutrons
 - ◆ narrower showers (99% of hits in $70 \times 70 \text{ cm}^2$ for 100 GeV π)
 - ◆ suppression of big fluctuations
- Recovery of information
 - ▶ counting
 - ◆ improvement: 3 thresholds
 - ▶ topology
 - ◆ clustering



See note LC-DET-2004-029

Resolution studies

- GLD HCAL study by KEK Group
 - ▶ 3 thresholds (0.5, 10, 100 MIP's)
 - ▶ 1×1 cm² **scintillator tiles**
- 1 bit better @ low E



- $e^+e^- \rightarrow qq$ (uds)
 - ▶ $\sqrt{s} = 91, 350, 500$ GeV
- Assuming Perfect PFA
 - ▶ Improved jet resolution

H MATSUNAGA

Pramana J. Phys., Vol. 69,
No. 6, December 2007

■ Performance studies

- ▶ MIP efficiency
- ▶ Hit multiplicity
- ▶ Ease of calibration (30 M cells $\Rightarrow$ 30 M elect. channels)
- ▶ Recovery time (RPC)
- ▶ Discharge rate (GEM, μ Megas)
- ▶ Behaviour in hadronic shower (detector & electronics)
- ▶ Operation in high magnetic field

$\Rightarrow$ Uniformity / detector / cell

■ Technological challenges

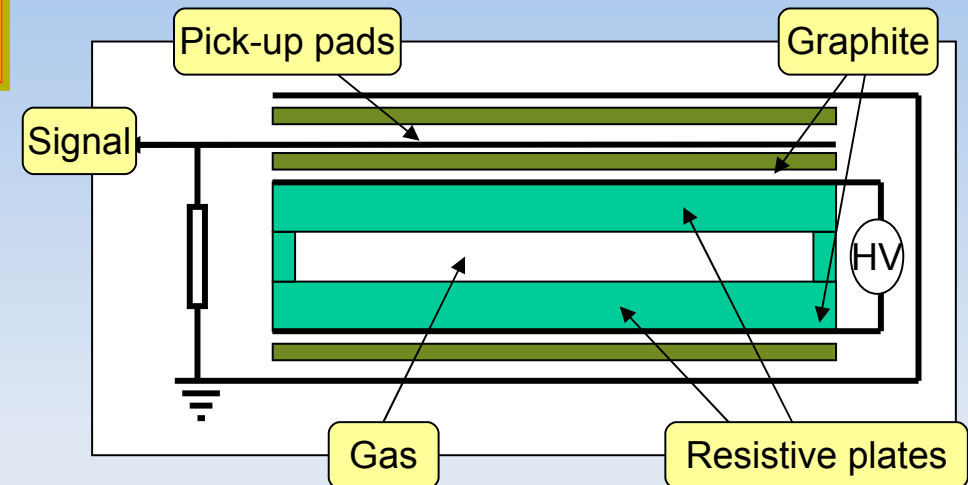
- ▶ Large surfaces
- ▶ Thickness
- ▶ Low cost and industrial process
- ▶ Aging: no performances degradation

RPC Gaseous detector prototypes

■ GRPC (*IHEP+IPNL*)

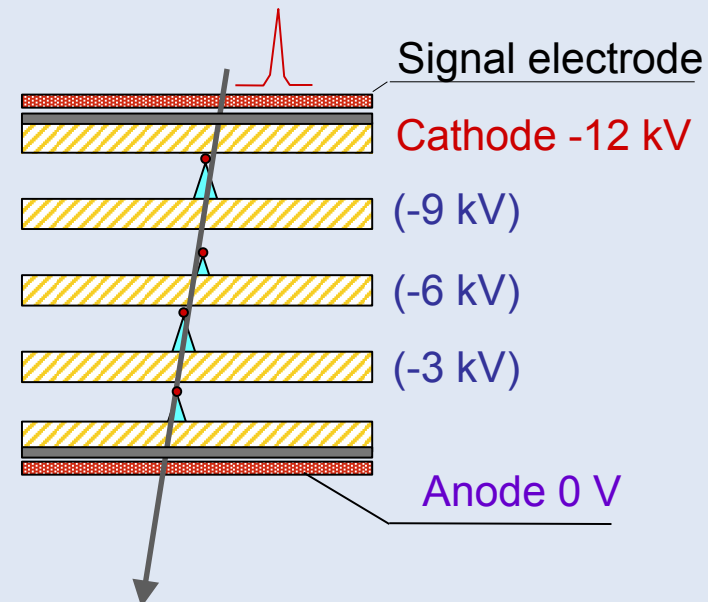
- ▶ simple, robust,
rate ≤ 100 Hz/cm²
- ◆ 1.2 mm gaz gap
- ◆ 400 μ m glass plate
- ◆ Graphite/Licron/Statguard resistive cover
- ◆ ~ 7.4 kV

TFE	93%
Isobutene	5%
SF6	2%



■ Multi-gap RPC (*INFN Bologna-CERN*)

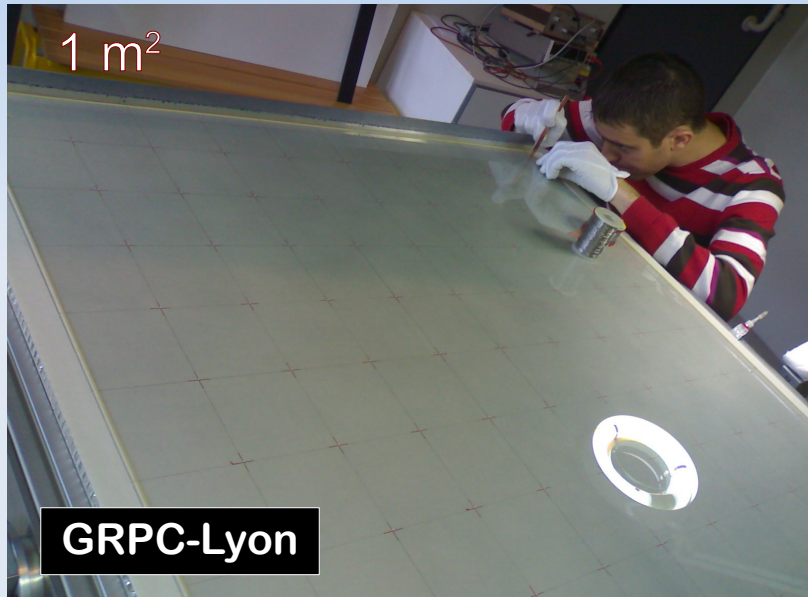
- ▶ Higher rates & efficiency
- ▶ Idem Alice ToF system
- ◆ 4 x 250 μ m gaz gaps
- ◆ 400 μ m inner glass plates
- ◆ 550 μ m ext. glass plates
- ◆ ~ 10 — 12 kV



Small & large prototypes

■ GRPC:

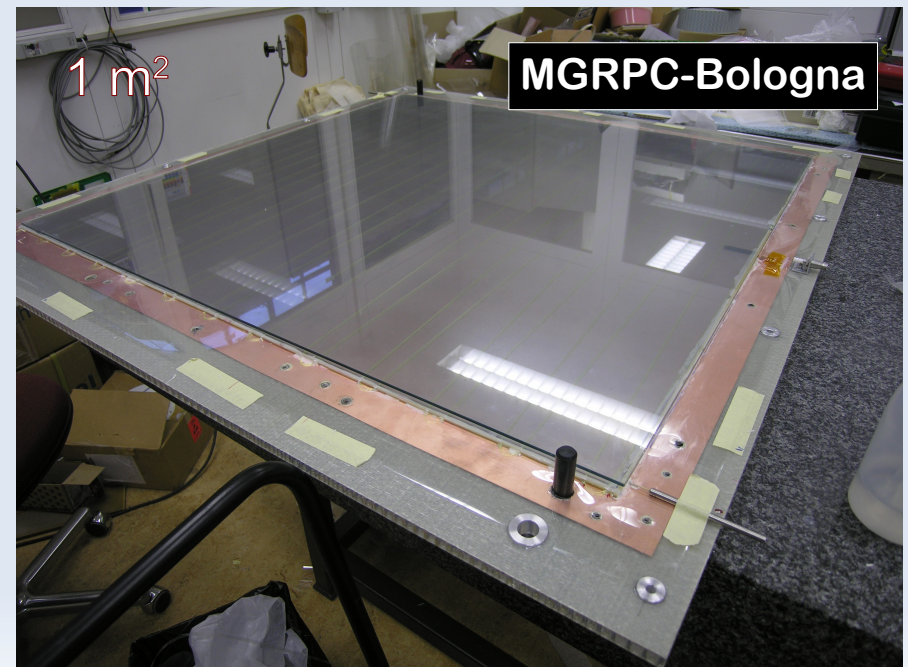
- ▶ 8×8 , 32×8 , 50×32 , 100×32 , 100×100
1 cm²-pad : already produced and tested.



■ MGRPC

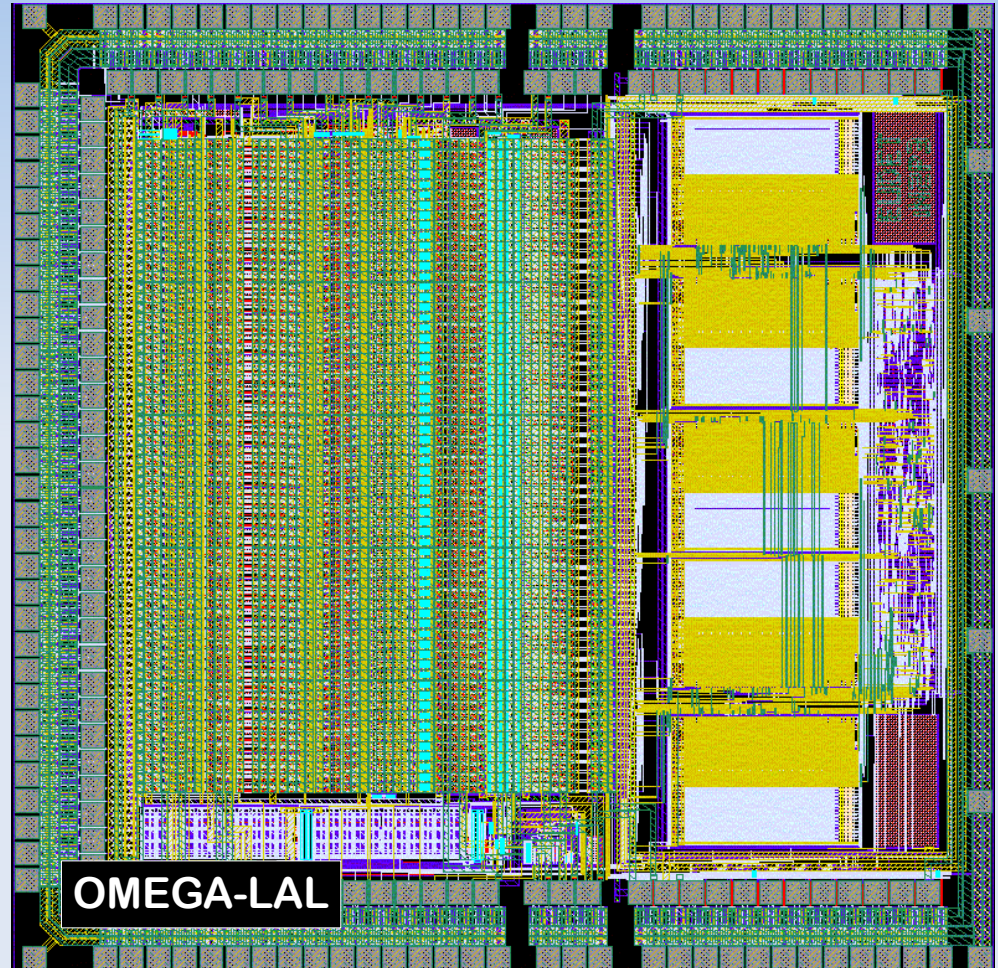
- ▶ 32×8 , produced & tested
- ▶ 100×100 under development

improve on gas distribution system, spacers and resistive painting, dead zones



HarDROC (Hadronic Rpc Detector Read Out Chip)

- AMS SiGe 0.35 μ m, 16 mm²
- 64 channels
- Digital/analogue output
- 2 independant thresholds
- low consumption
 - ▶ < 10 μ W/ch
 - ▶ Power pulsing
- Digital memory
 - ▶ 128 events
 - ▶ ASIC ID (8b), BC ID (24b), hits
- Large gain range (6bits)
 - ▶ Channel wise
- X-talks < 2%
- Threshold > 10 fC



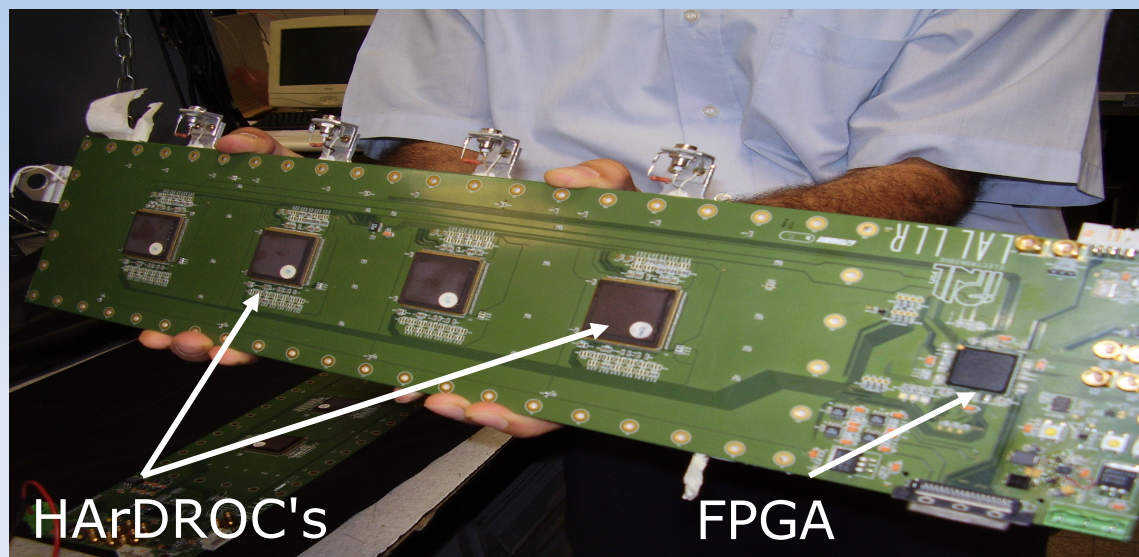
*** DIRAC: Another ASIC developed in IPNL/LAPP aims at a threshold of 3 fC**

- First batch (460 chips) produced and being tested
 - ▶ Will be used for the m^2
- Correction of the minor bugs of HR1
 - ▶ Mask, memory pointer (dummy frame)
 - ▶ Shift registers improvment (configuration loading)
 - ▶ Bypass on critical signals
- Improvement on Power Pulsing
 - ▶ Now also digital part $\Rightarrow$ consumption $\leq 10\mu\text{W}/\text{chan}$
- Dynamic range extension
 - ▶ Gain correction: 8 bits instead of 6
- 3 shapers and 3 threshold (3 indep^t DAC) coded on 2 bits
 - ▶ 10 fC, 100fC, 1pC (for μMEGAS)
 - ▶ 100 fC, 1pC, 10pC (for GRPCs)

Mini DHCAL project

Aim: Validate the new electronics/acquisition scheme for the DHCAL (GRPC/ μ MEGAS)

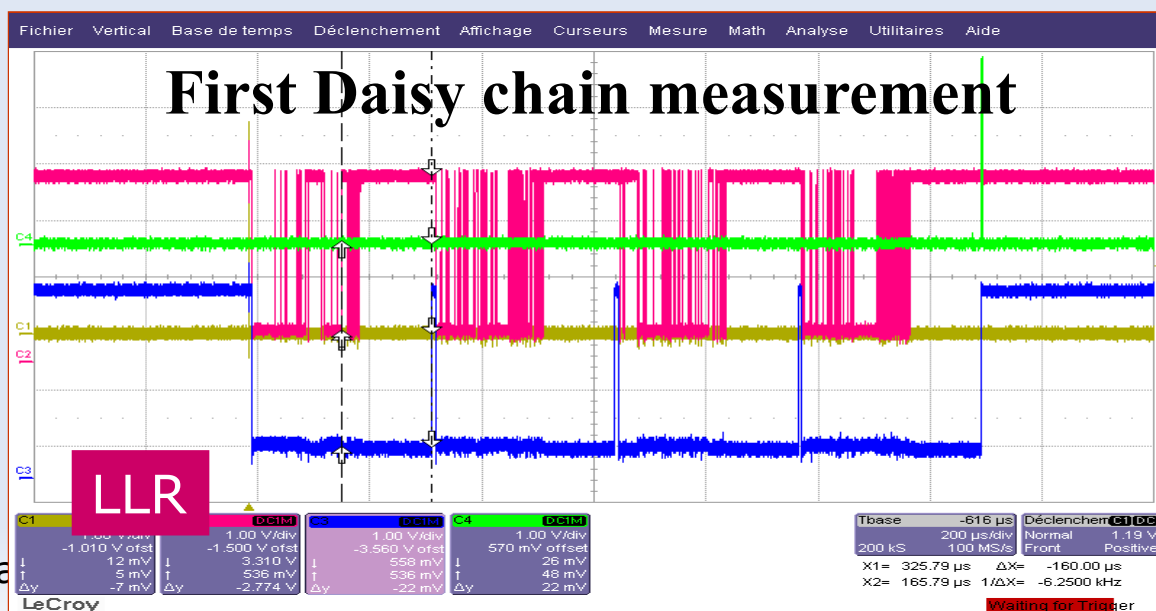
- **8-layer**, **800 μ** thick PCB buried and blind vias x-talk <0.3 %
- **4** hardroc chips
- Readout **FPGA** $\rightarrow$ **USB**
- **8x32** pads detector



Acquisition modes : different modes are allowed:

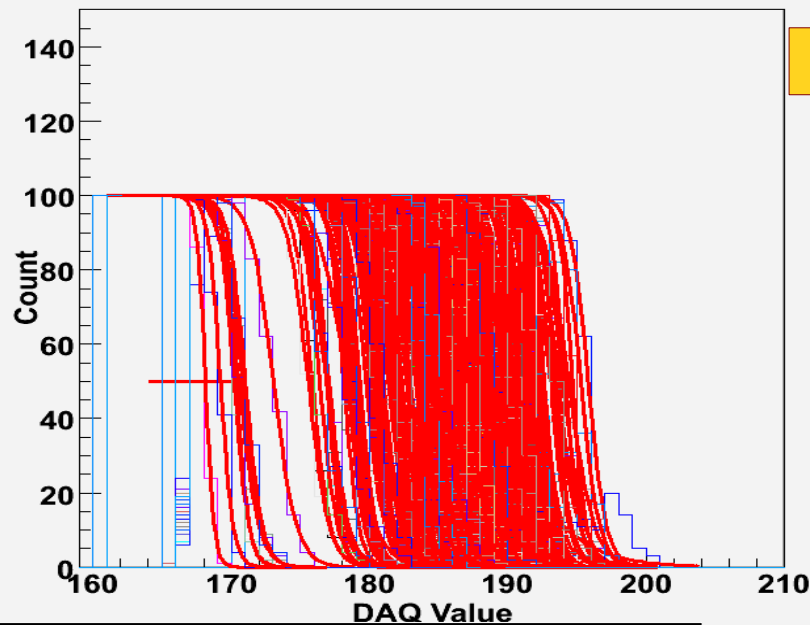
- a) Train (ILC mode)
- b) External trigger :
cosmic rays & test beam

Data output:
digital and **analogue**



Gain correction

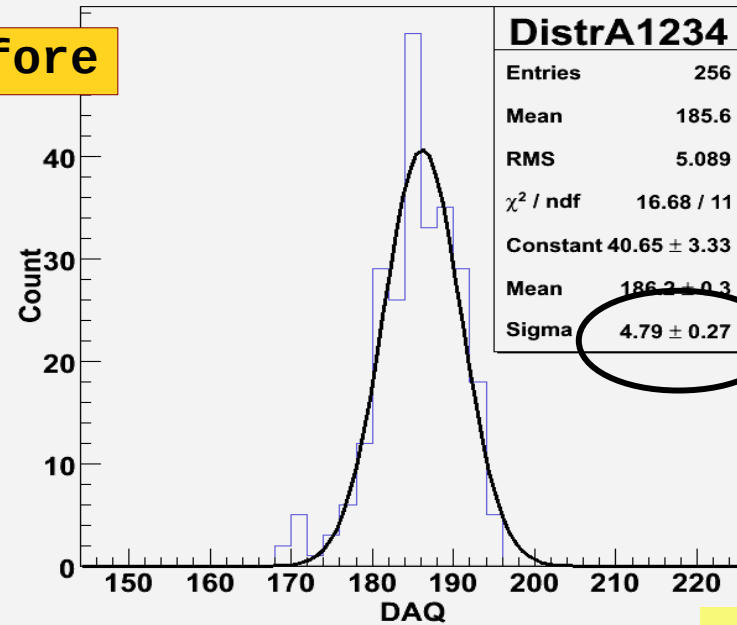
ASIC 1, 2, 3, et 4 Avant Corrections



before

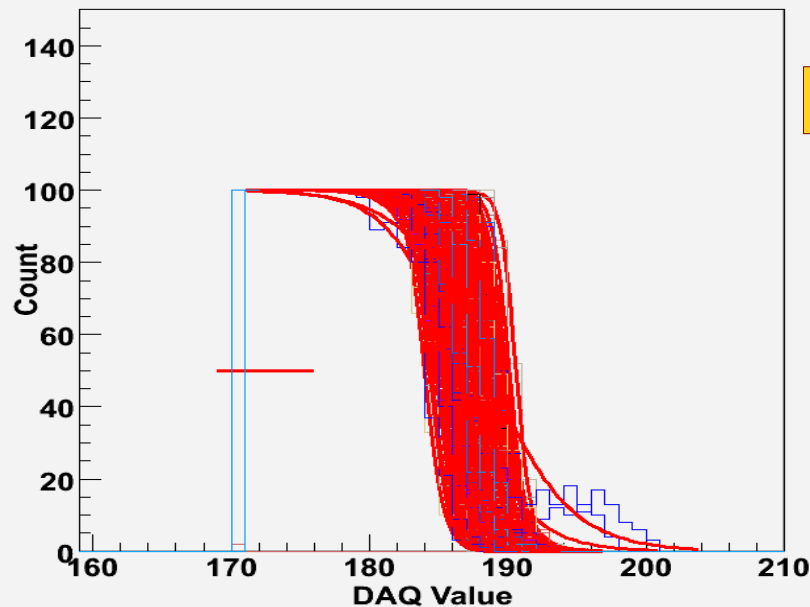
Injected charge = 100 fc

ASIC 1 2 3 et 4 Distribution des SCurves.

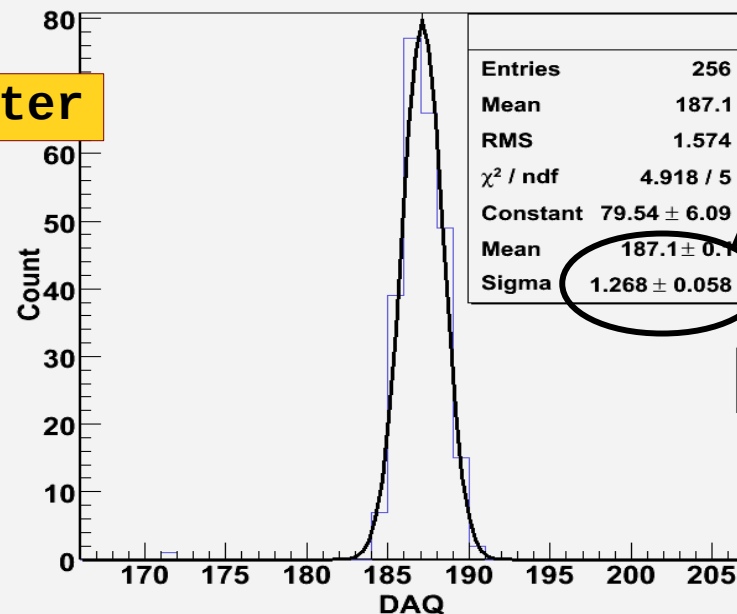


Reduction:4

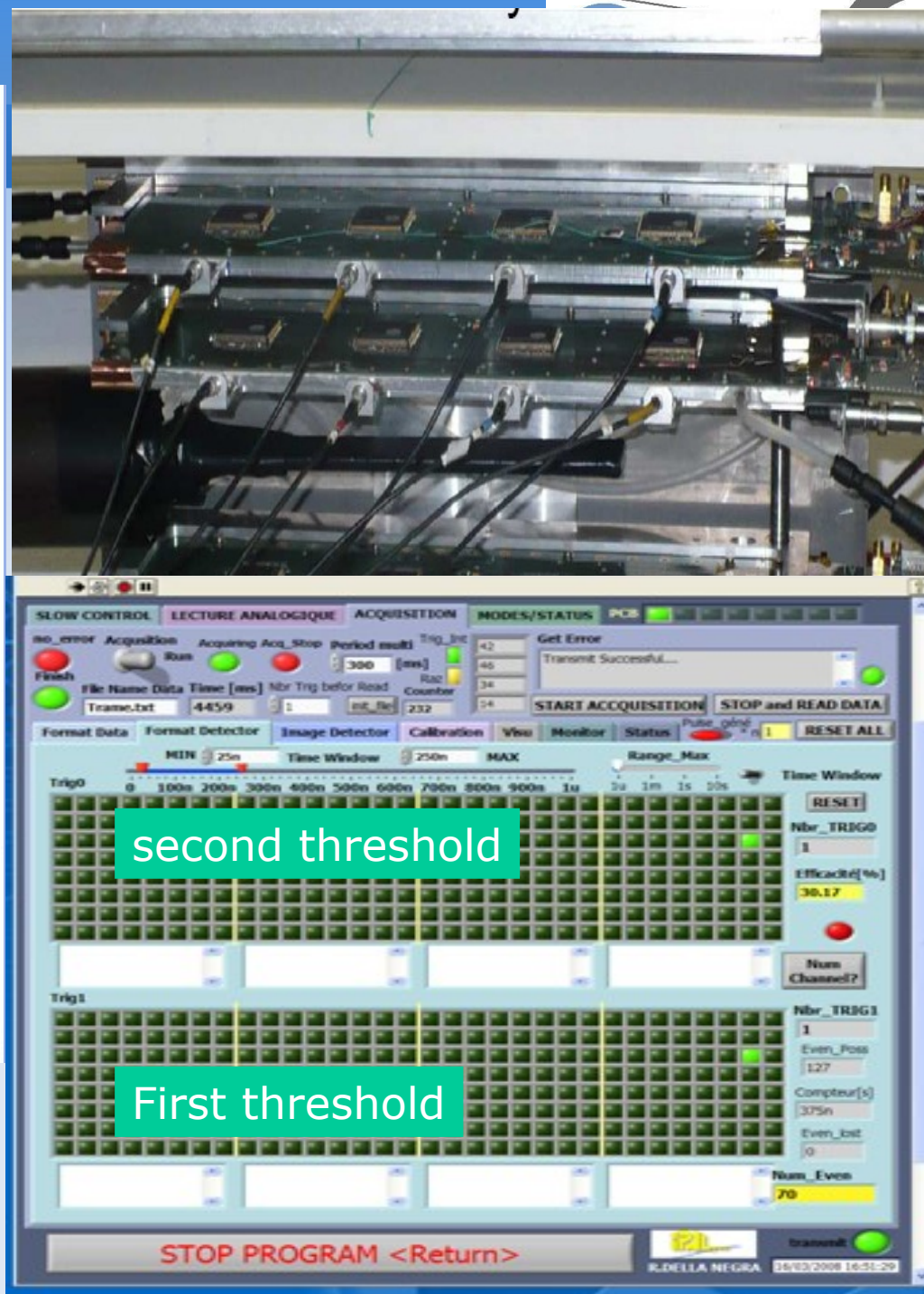
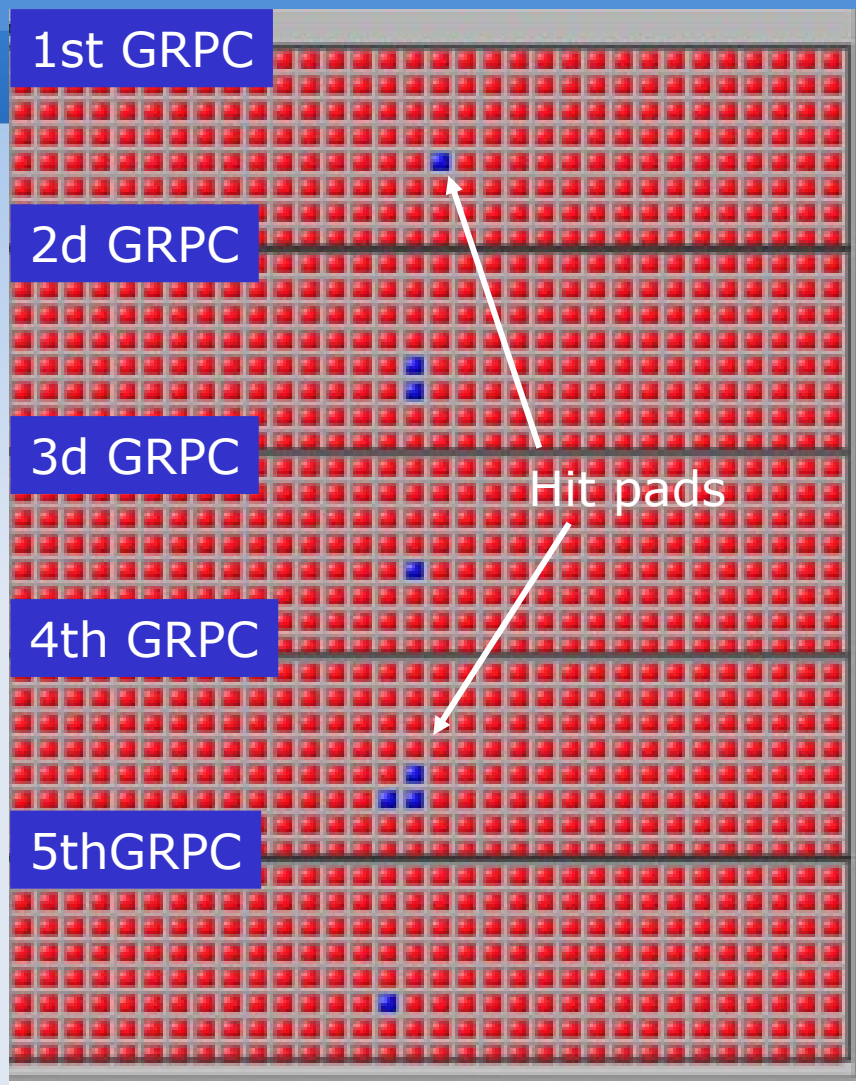
ASIC 1, 2, 3, et 4 Distribution des SCurves Corrigees.



after



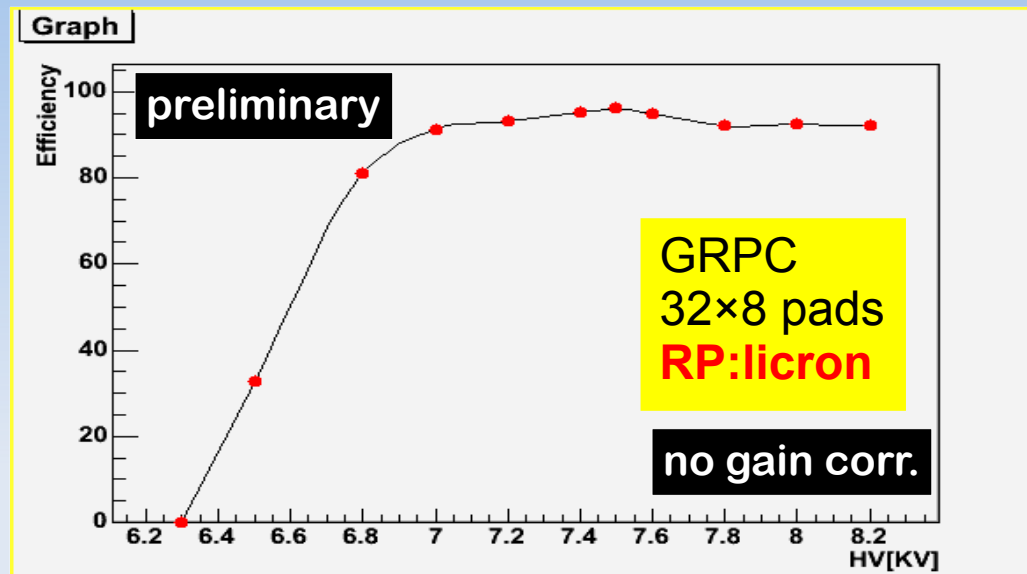
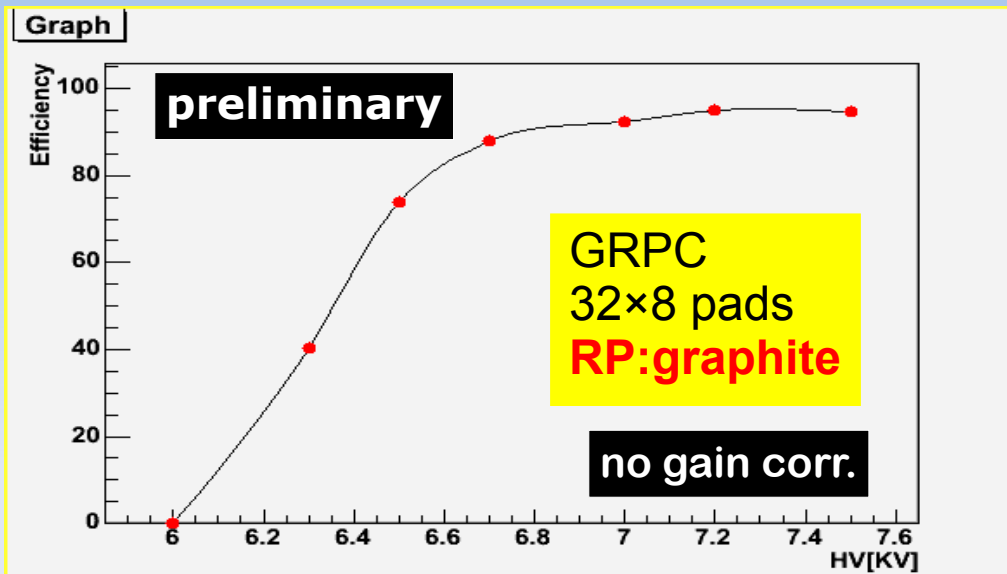
$\approx 2.5 \text{ fc}$



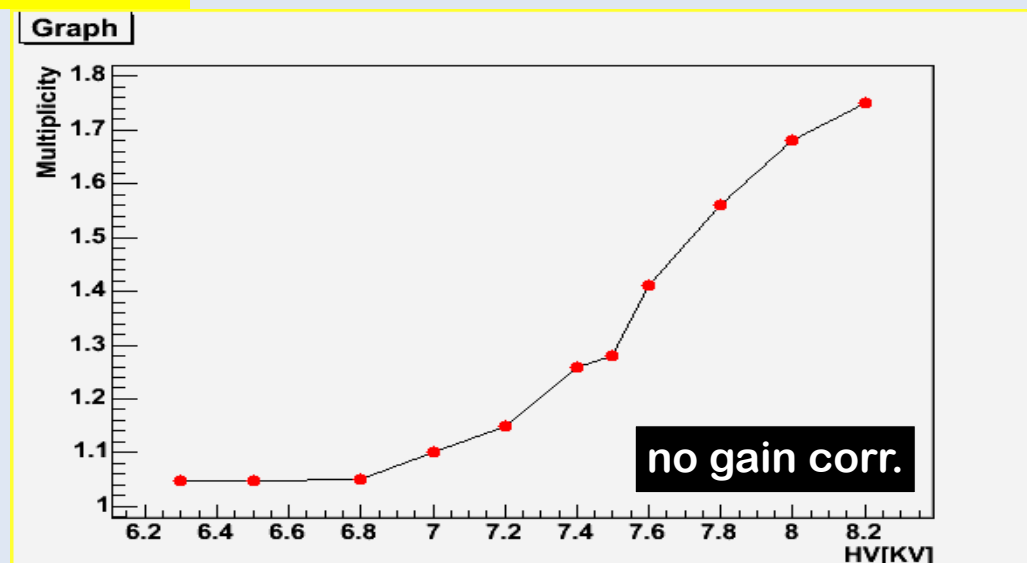
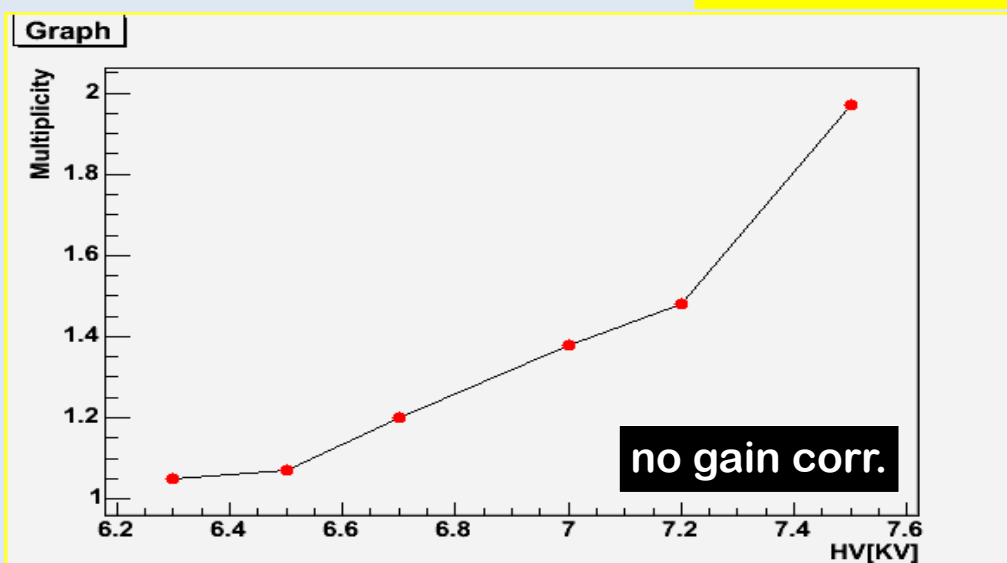
Example of a recorded mip
5-GRPC cosmic rays test bench
Thr. $\sim 100\text{fC}$

GRPC Efficiency & Multiplicity

TFE 93%
Isobutene 5%
SF6 2%



Threshold ≈ 100 fc

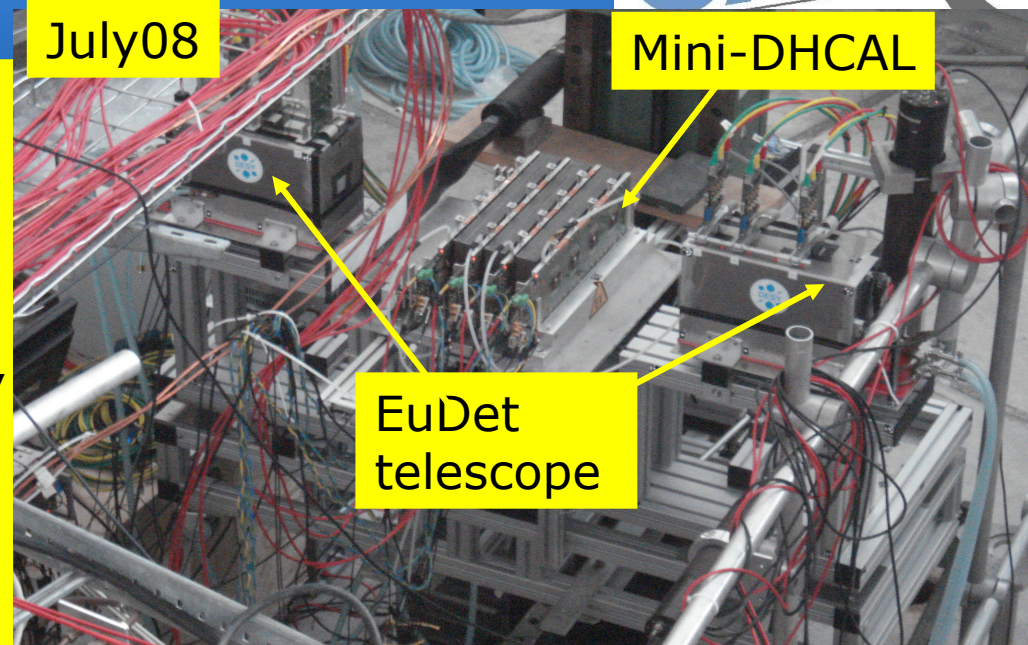


GRPC Mini-DHCAL test at CERN

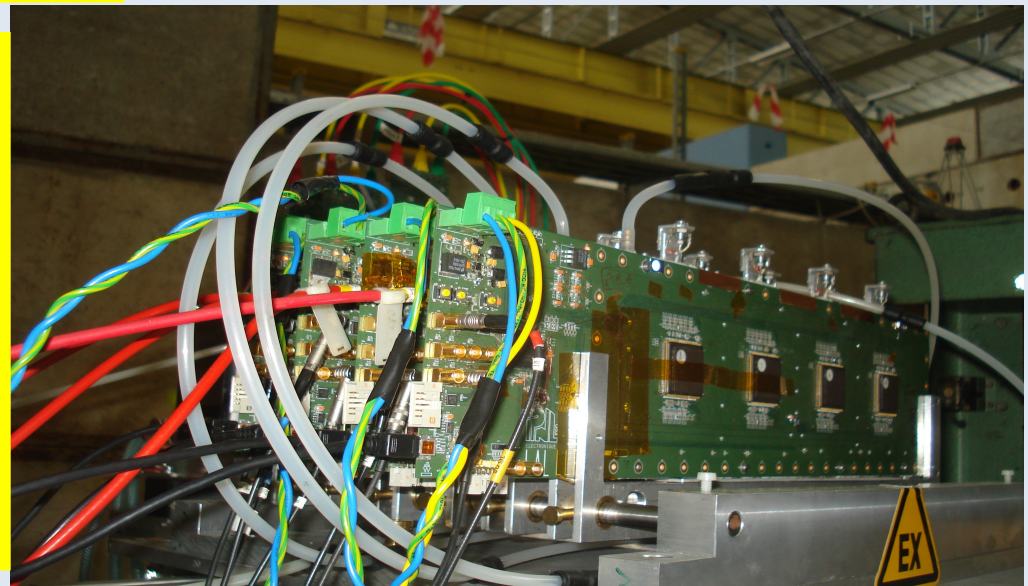


Aim:

- Validate the whole electronics readout system in beam conditions
- Study the GRPC behavior vs (HV, thresholds, angle, position, rate)
- Study the first phase of the hadronic shower (pion energy 1-12 GeV)



- About 400 k evts were collected (DAQ rate : 20 Hz) and being analyzed
- The readout system as the GRPCs performed very well: stability and efficiency



Beam test periods

PS: Mostly π (3-12 GeV) + few μ , very few e^-

PS T10 17—24 july with the EUDET telescope: ~260k trig evts

- With EUDET Pixel Telescope: 7×7 mm² active sensors
- **Angle & position** scans
- Other data: trigger large scintillators (10×40 cm²)

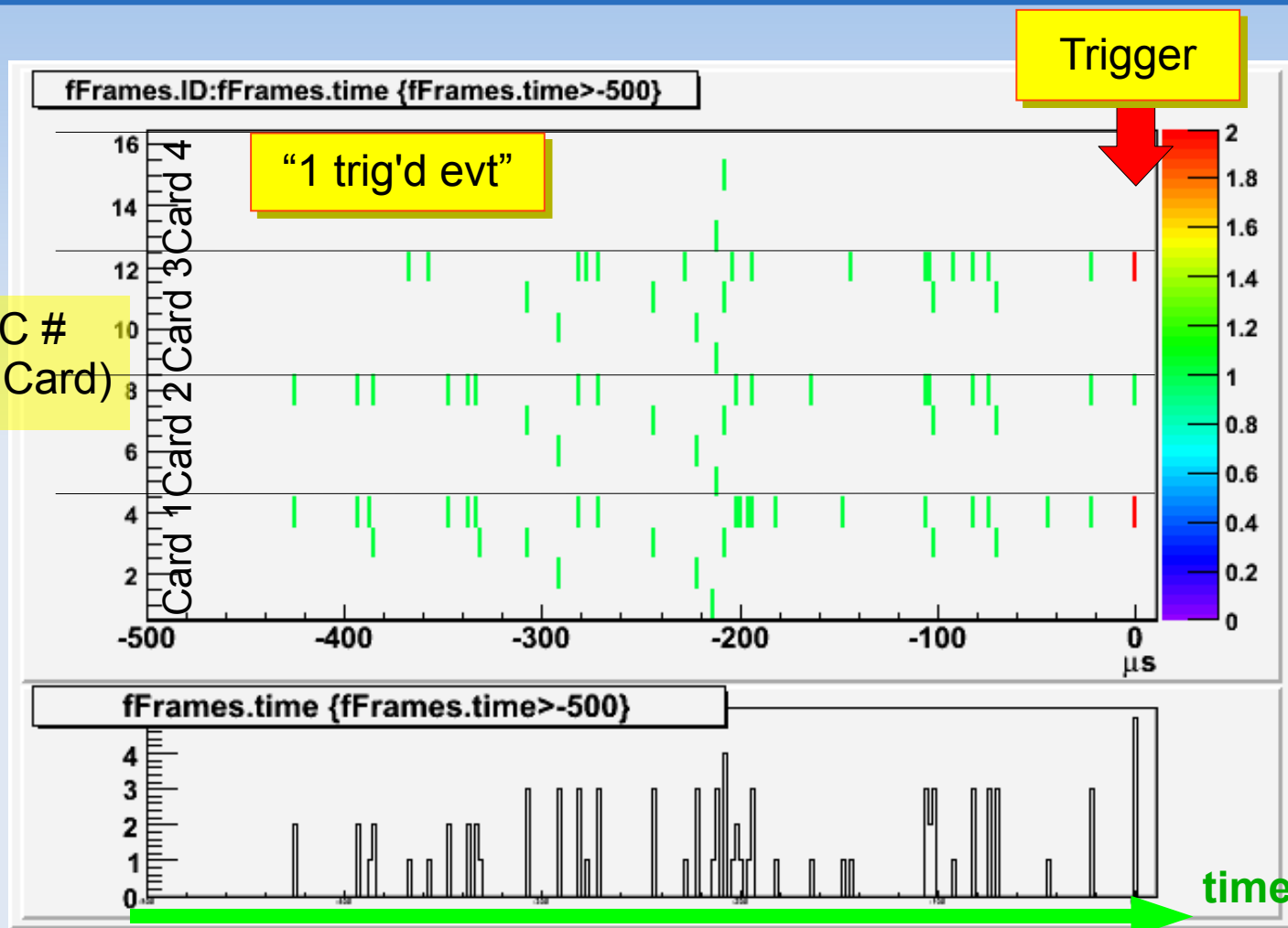
PS T9: 28/07 — 04/08 ~80k trig evts

- Complement Pion data with 2 λ of W, **angular** scan
- Analogue readout of 1 chamber
- Test of a wide RPC: 100×35 cm² (readout with 4 PCB $\Rightarrow$ $\sim 32 \times 32$ cm²)

PS T9: 07/11 — 12/08 ~65k trig evts

- Shared test with μ Megas ($\neq$ set-up)
- Complement test: **HV** scan, **thr.** Scan, **CO2** (as repl. of Isobutane), **Beam intensity** scan
- **Tentative:** m² + 24 HR1 PCB + new DAQ elec & soft (DIF)

Timing: single event + auto-trig

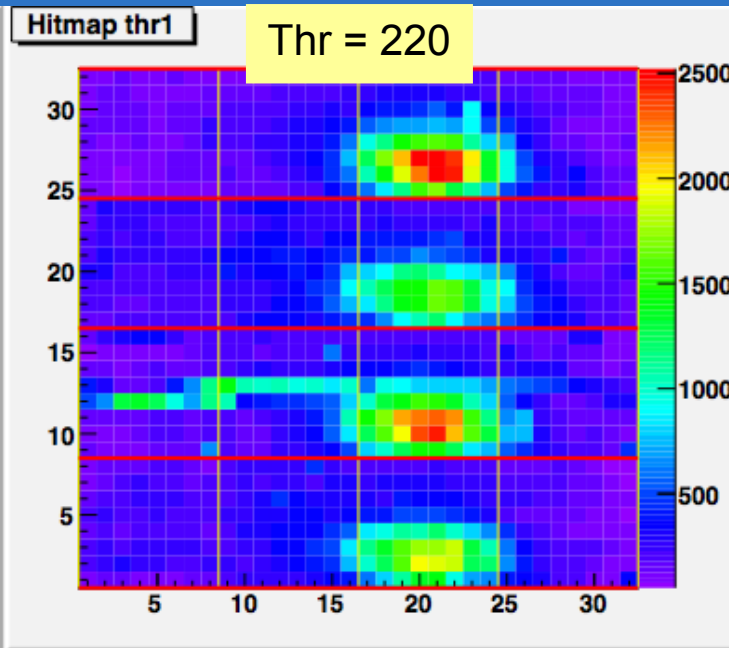
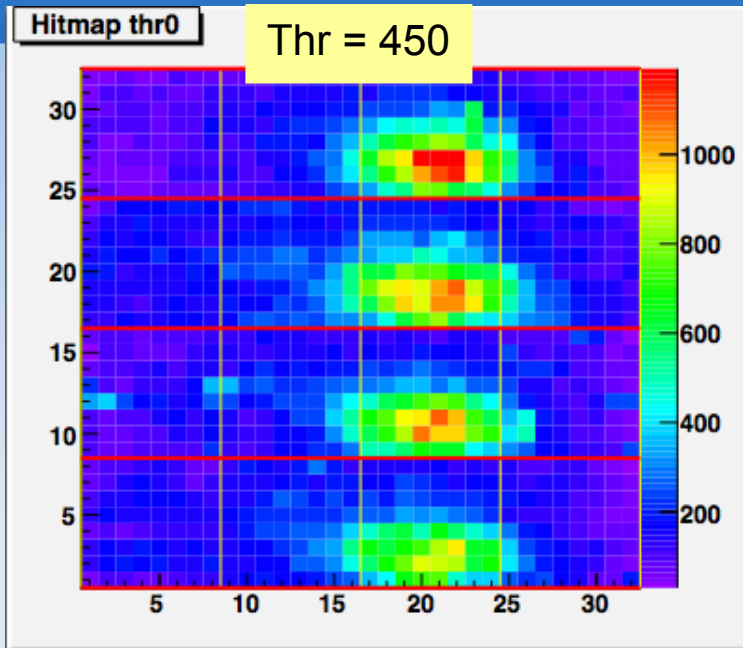


Many More stat
Available with
proper time
reconstruction

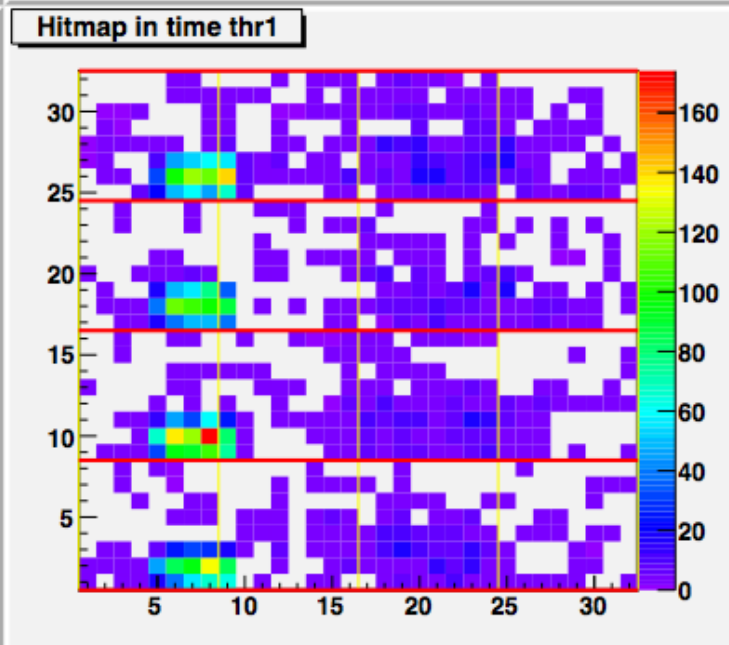
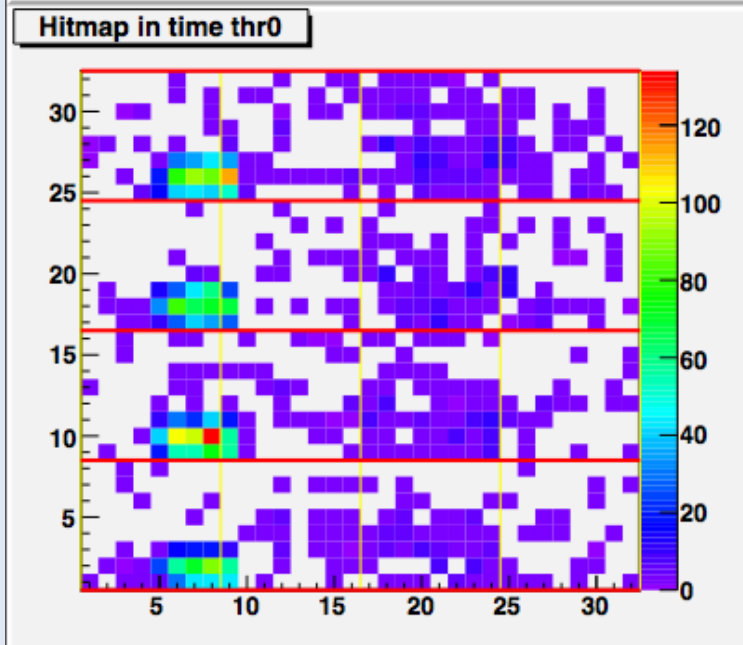
Expt'd: 830

- CERN PS: **400 ms** spills every 48 or 33s (day/night cycles).
- Running mode: **single event with auto trig**
+ BUSY logic & automatic RAMFULL recovery ($\Rightarrow$ BUSY signal)

First displays

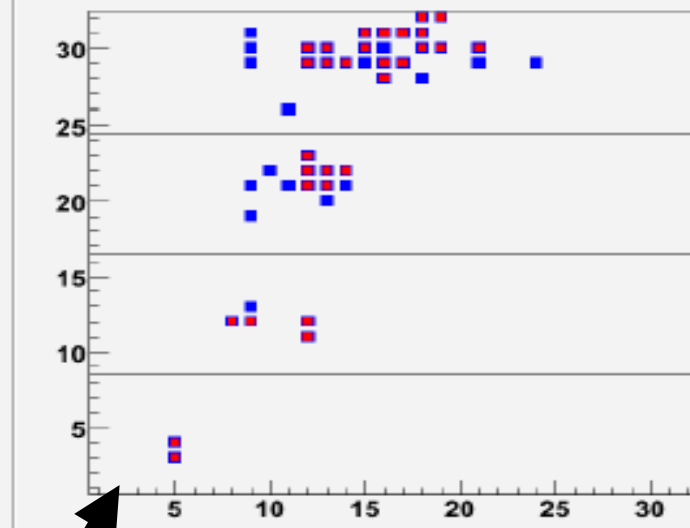
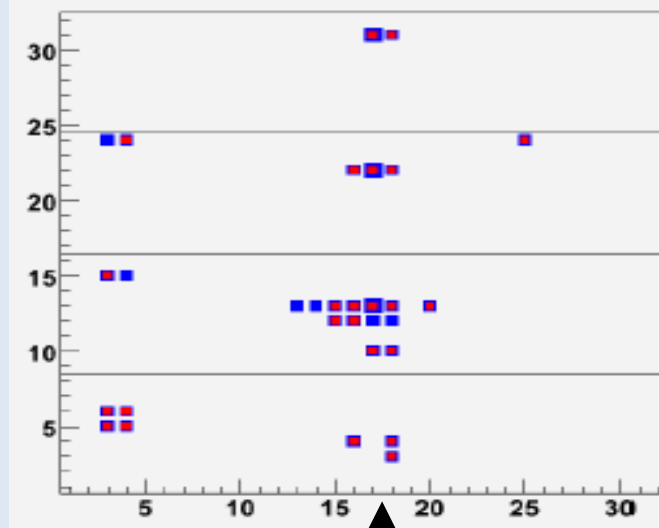
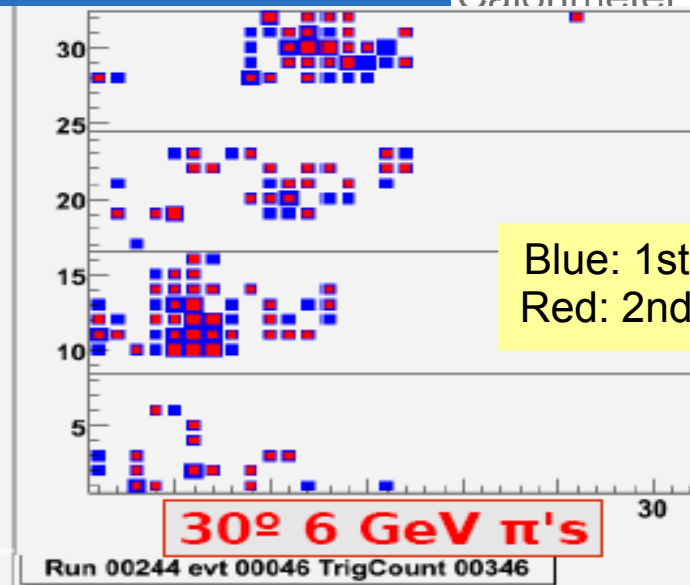
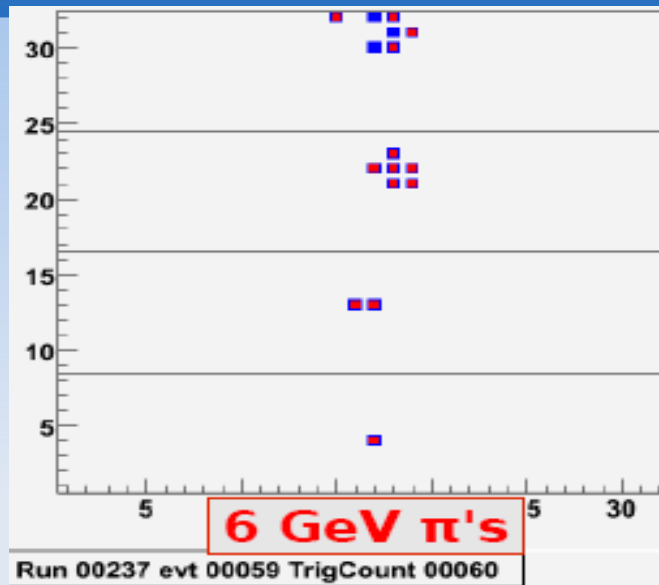


All Events



**in time
With ext.
trigger**

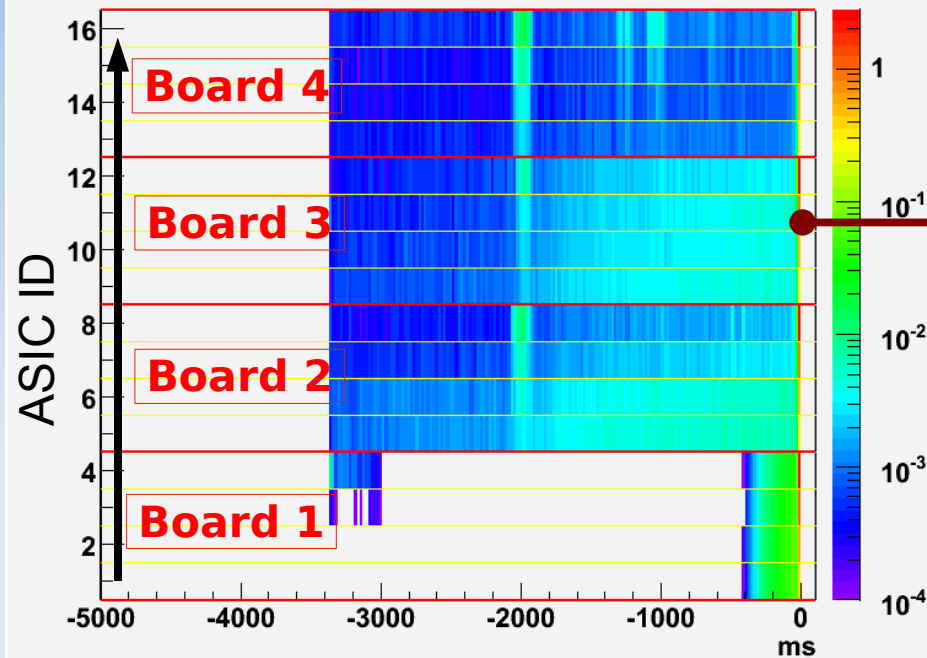
GRPC Mini-DHCAL test at CERN



Beam(pions)

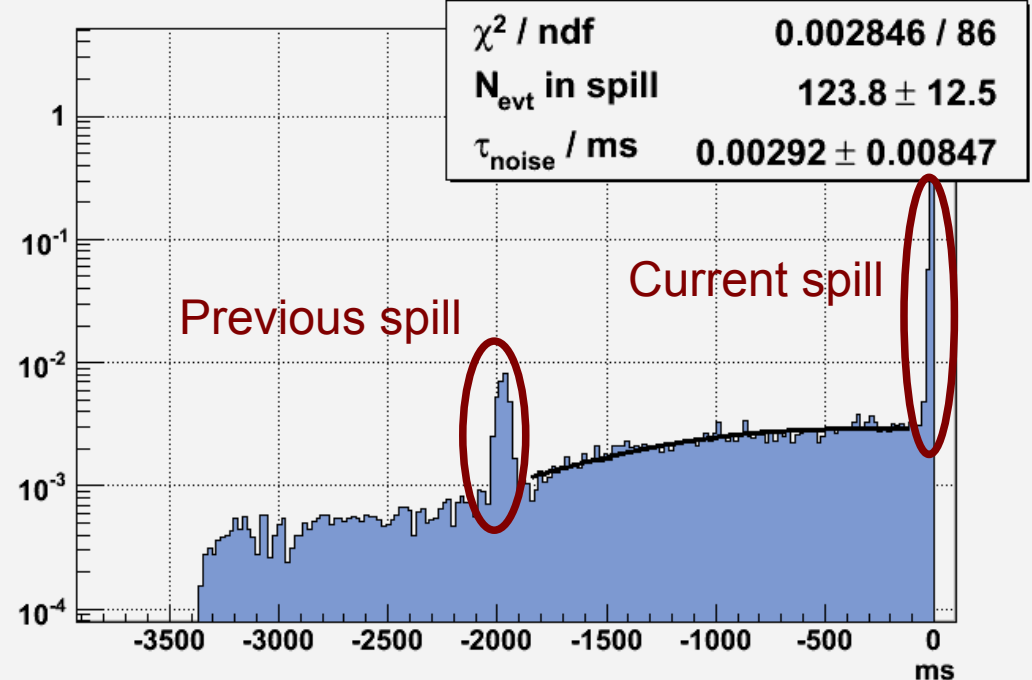
Noise & ROC study

Asic vs Time



Run00101
Hit rates for each triggered event

Event time distrib ASIC 12

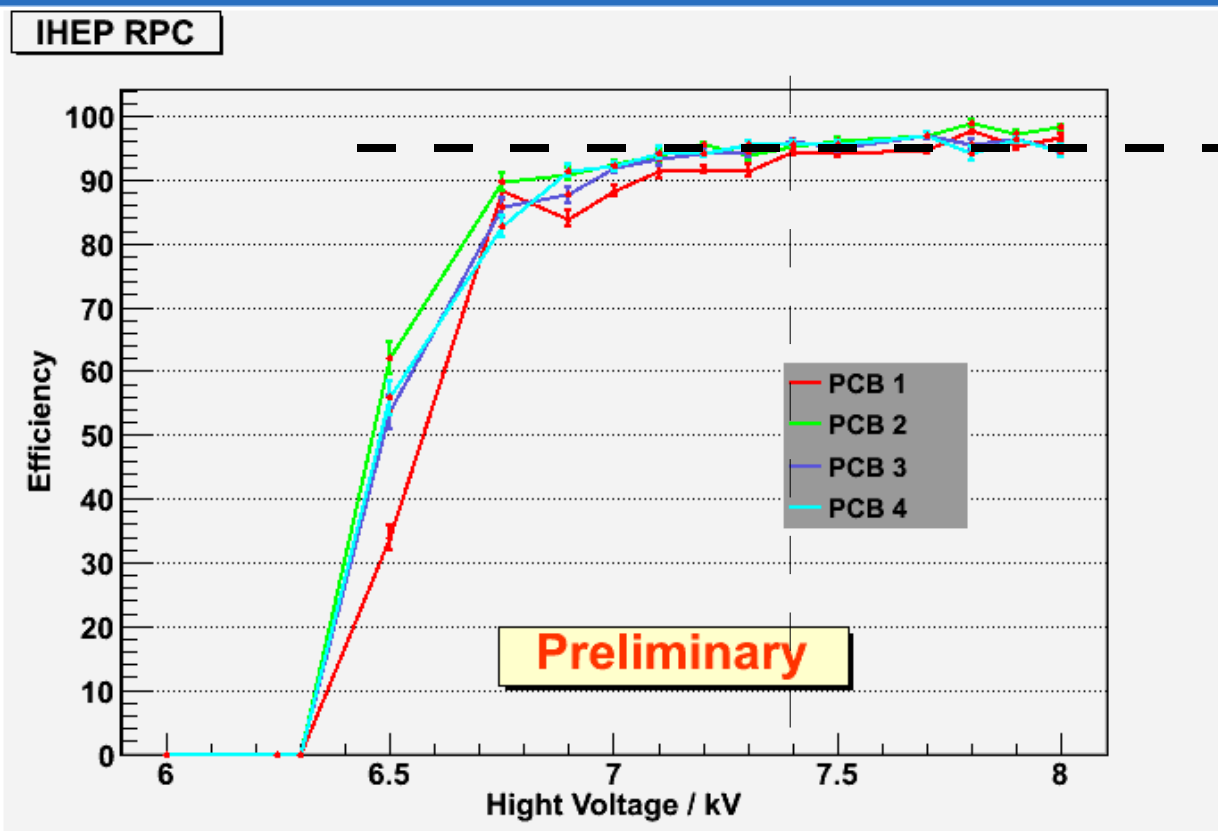


Shape:

- flat noise+event rate τ
- modified by RAMFull (Loss of memory)
- probability at $-t$ =
 - $(1 - P(\text{avail. mem}, t \times \tau))$
 - $\text{avail. mem} = 128 \text{ evts} - N_{\text{evt}} \text{ in spill}$

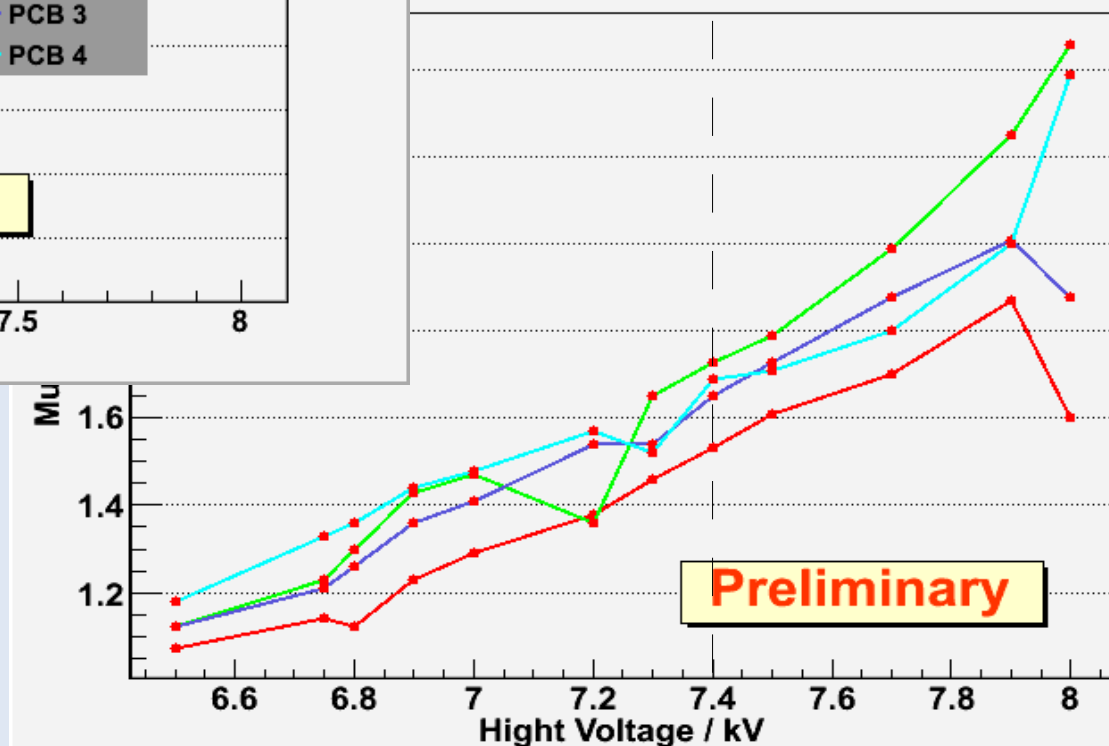
$$P(a, x) = \frac{1}{\Gamma(a)} \int_0^x t^{a-1} e^{-t} dt$$

IHEP GRPC: Efficiency & multiplicity

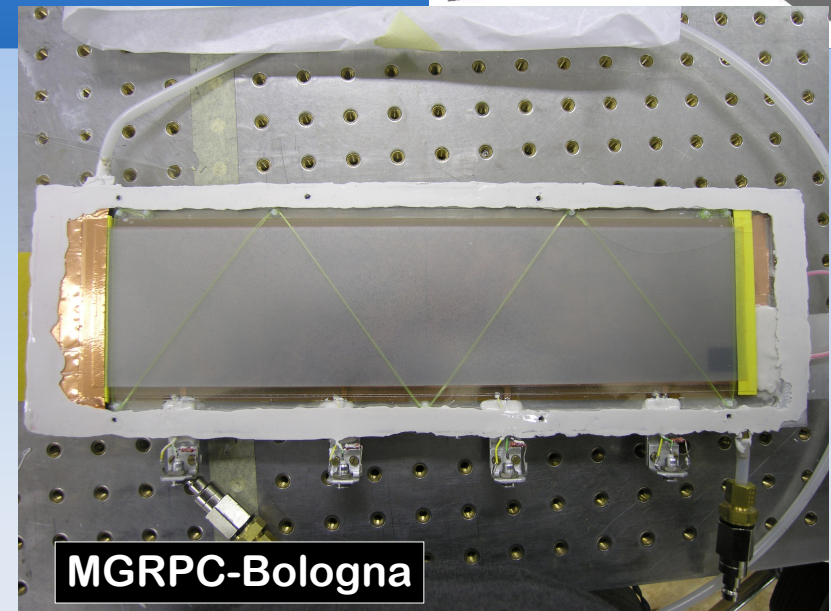
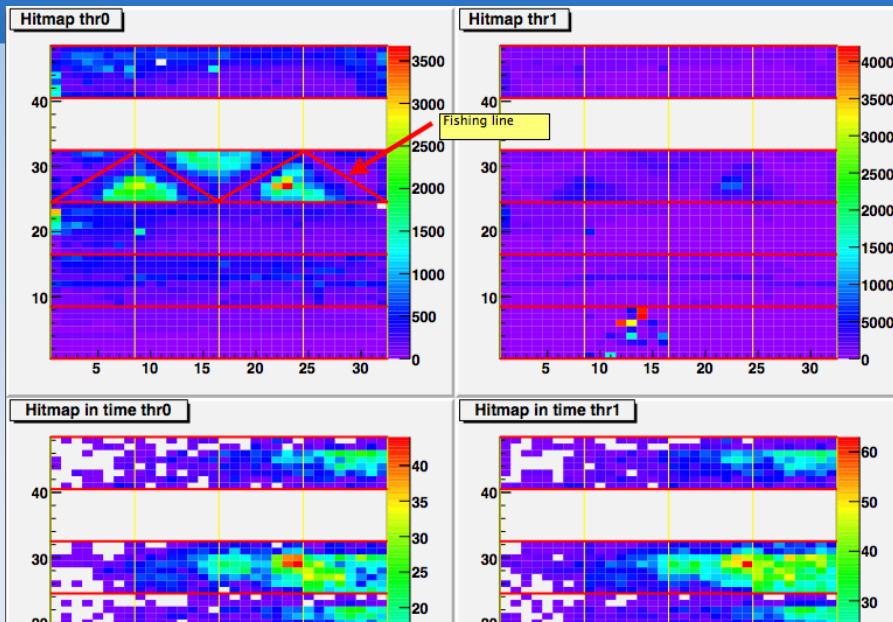


Working point: 7.4 kV
95% efficiency
1.6 pad/track

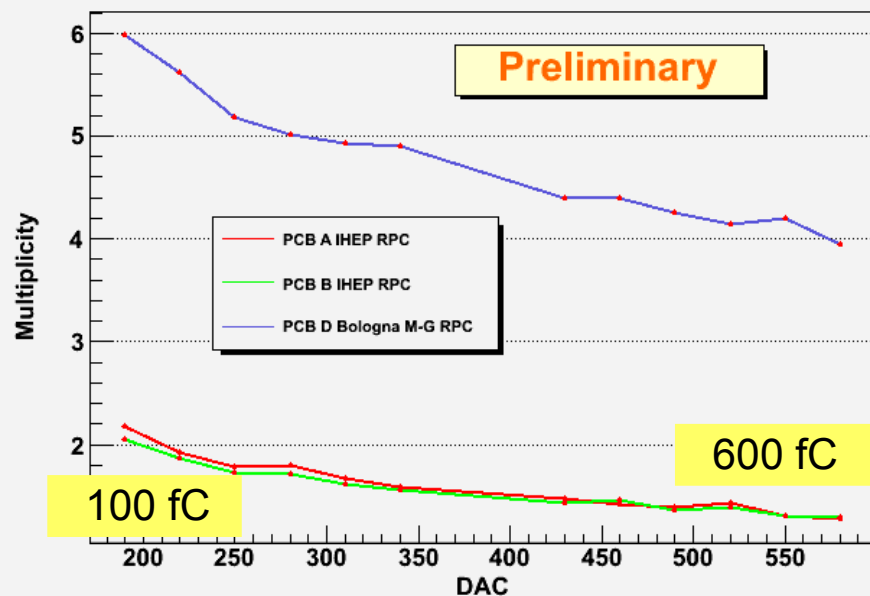
- Track reconstruction
- Threshold @100fC



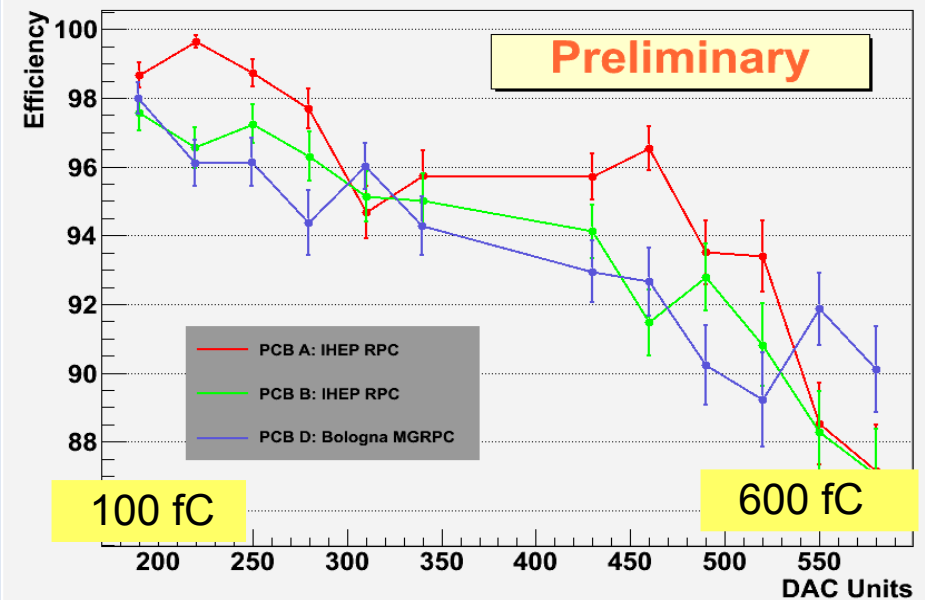
RPC vs. Multi-Gap RPCs



RPC & MGRPC



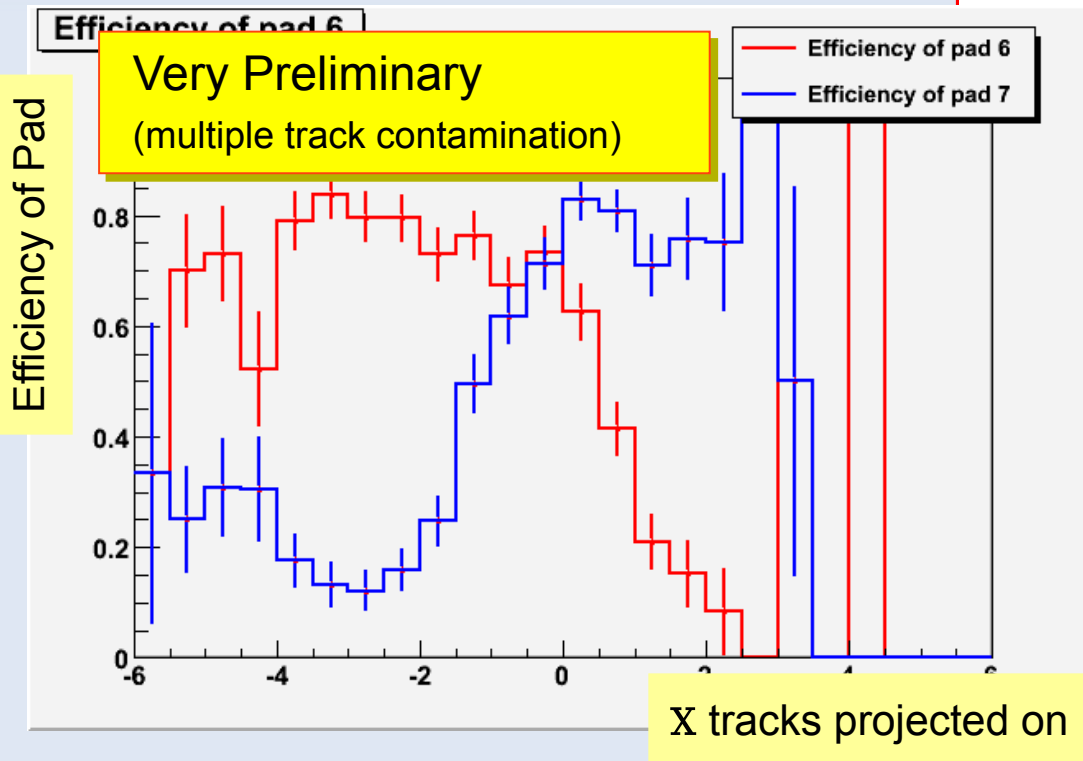
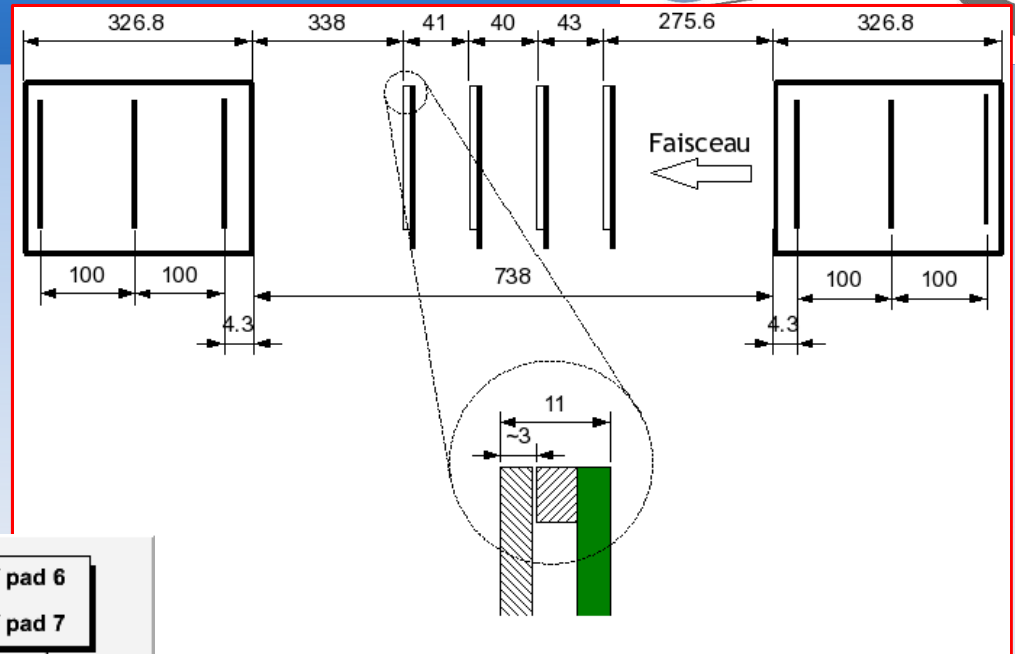
RPC & MGRPC Efficiency vs Thr.



Data with EUDET pixel telescope



- 2 independent DAQ's
 - Shift of 1 evt
- small surface: $7 \times 7 \text{ mm}^2$
- Track precision: $\leq 5 \mu\text{m}$



Clean-up (multiple tracks, multiple hits) and multiple runs analysis on going....

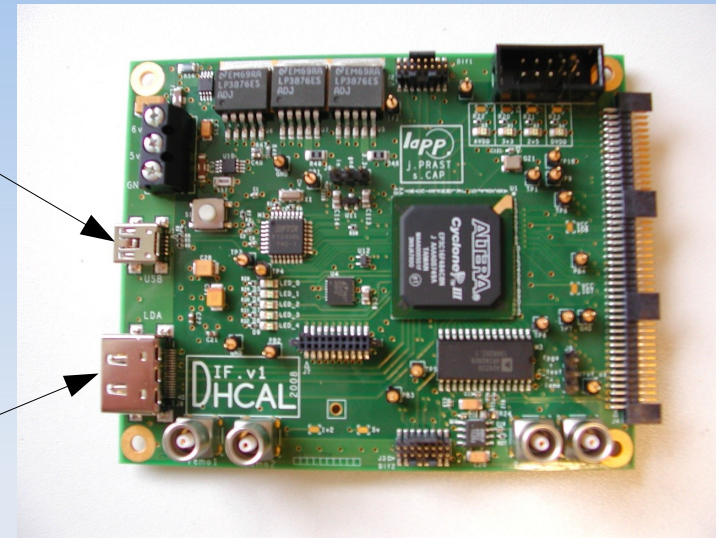
The 1 m² project

DIF

- 10-layer board (6 for signals) designed and prototype produced
- FirmWare & SoftWare operationnal and tested in beam (with 4 HR μ Megas card)

USB

HDMI

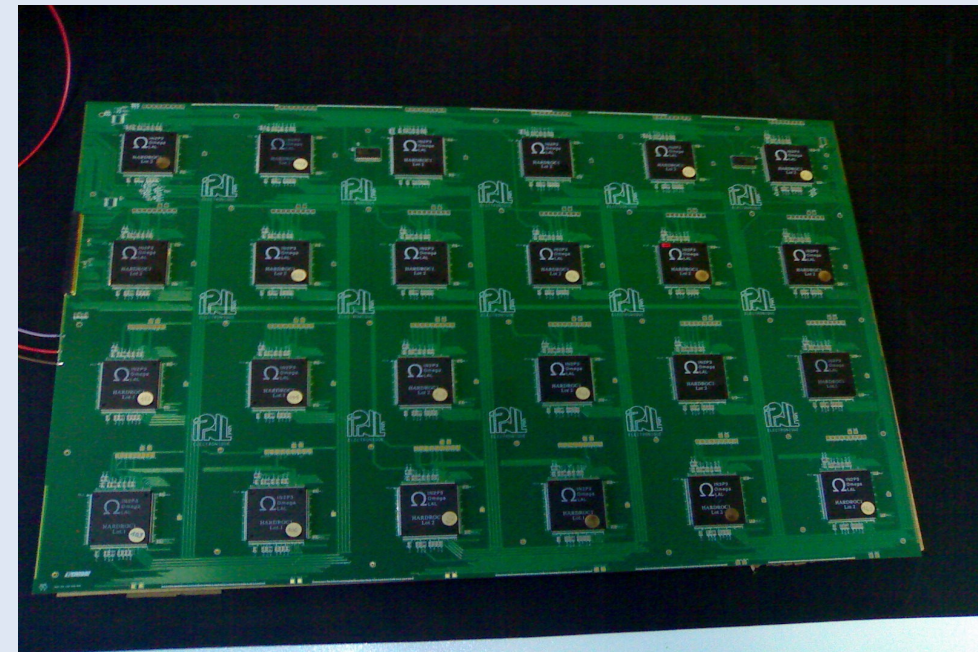


ASU

- 8-layer board designed and produced
- 500×33.3×1.2 mm³
- Connections between adjacent PCB foreseen
- ASICs were tested and plugged

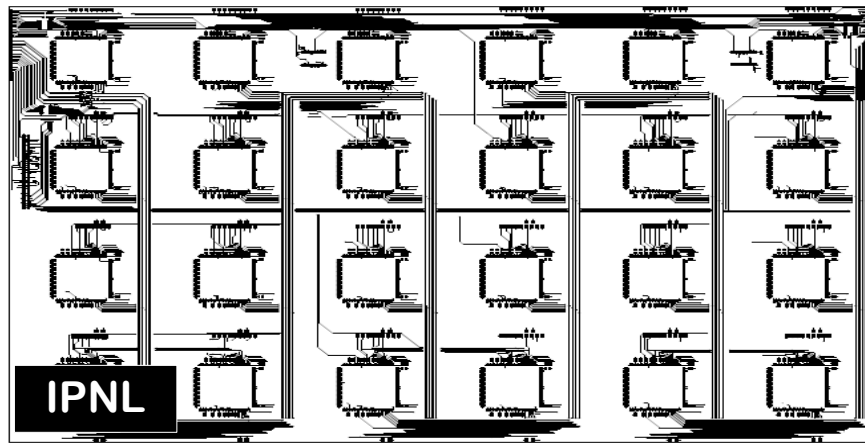
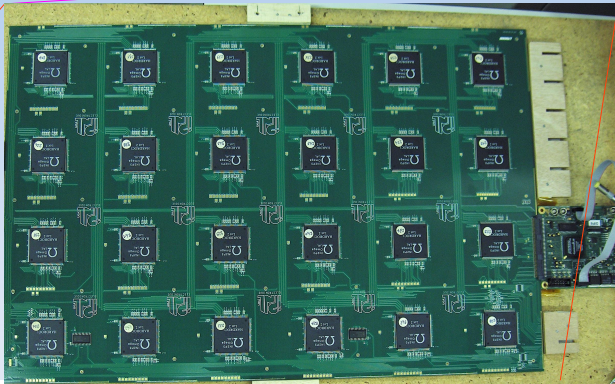
Software

Acquisition software
based on US/XDAQ developed

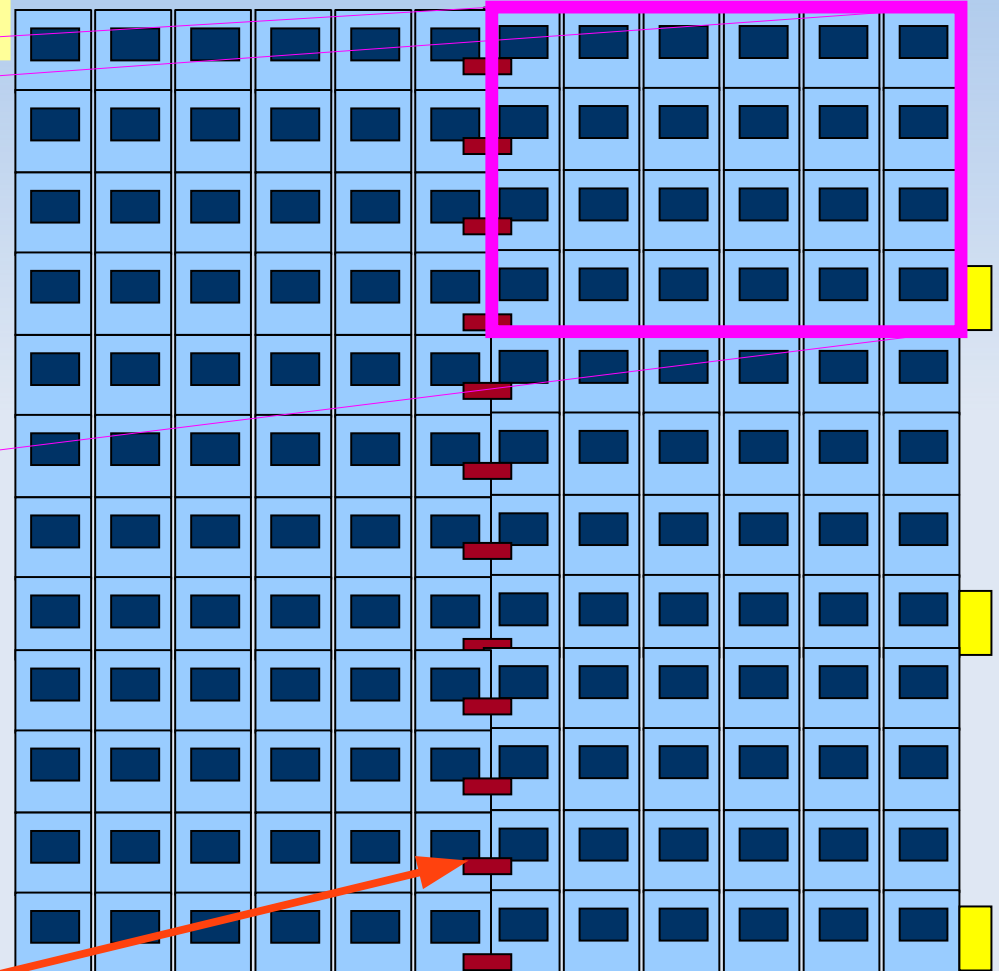


Next steps: m² ASIC support Units

1 ASU → 6×4 chips



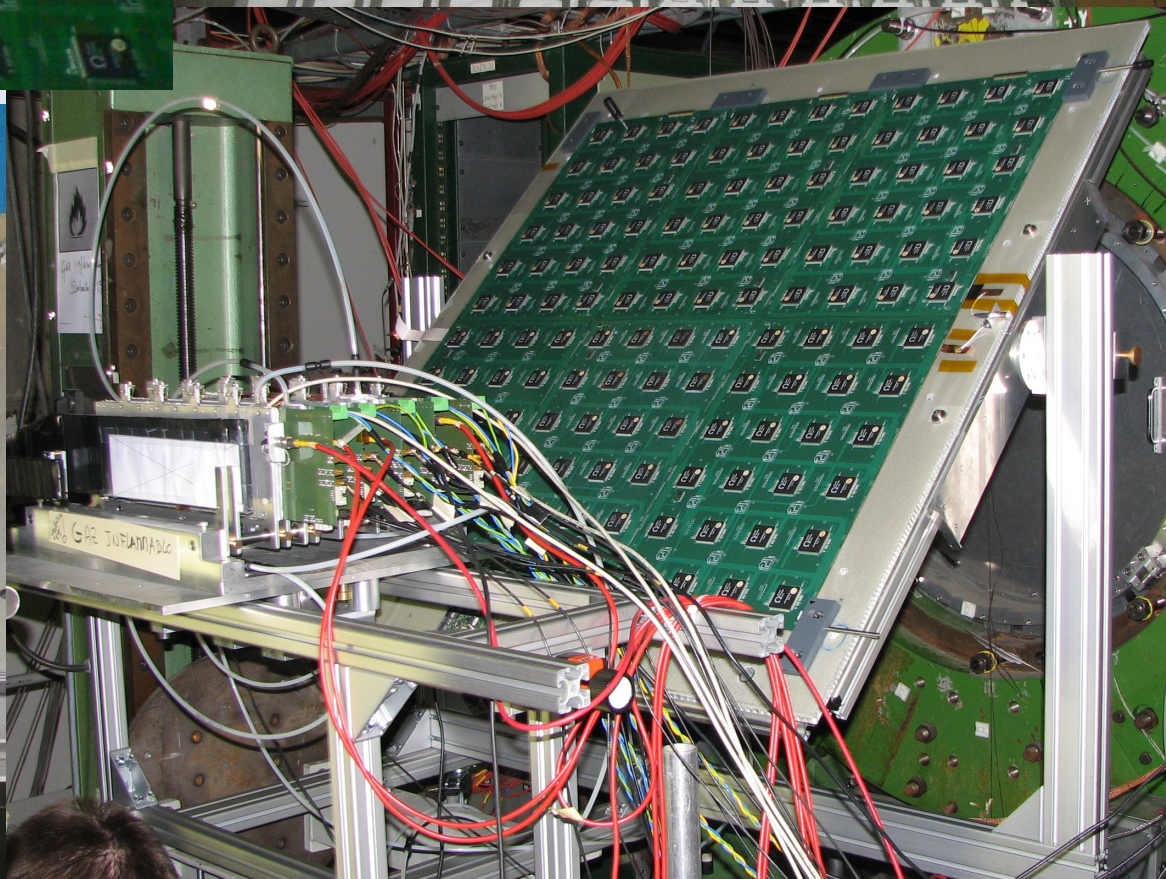
pcb-connector



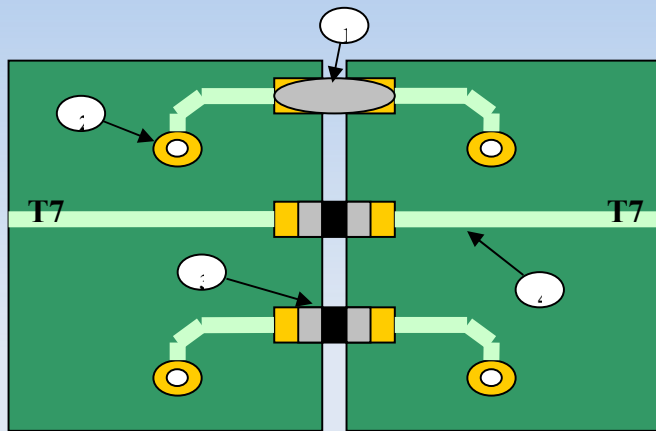
ASU hosting 24 HARDROC chips produced and being tested



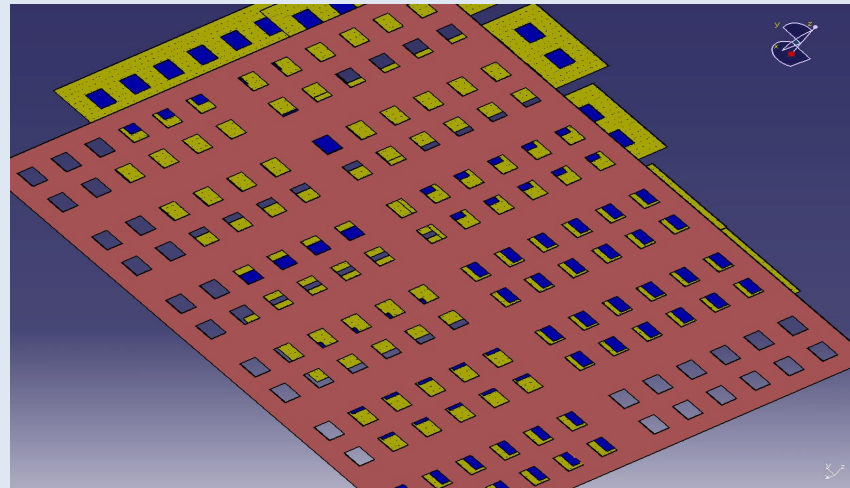
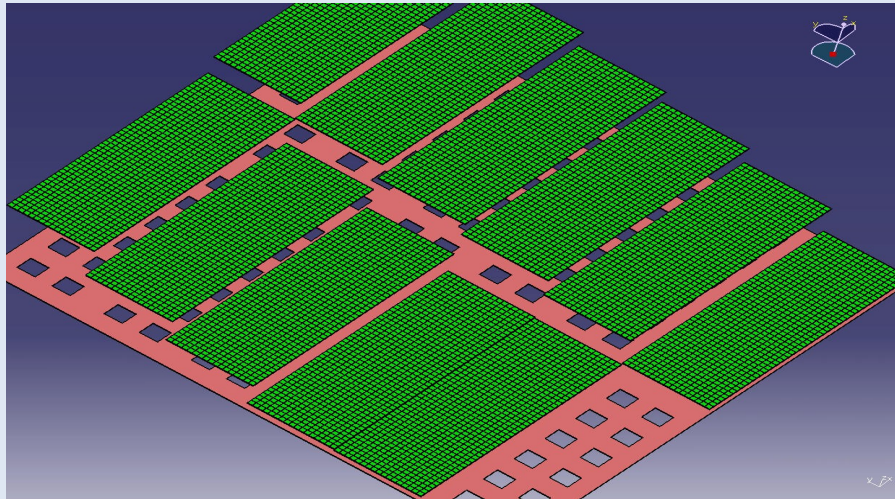
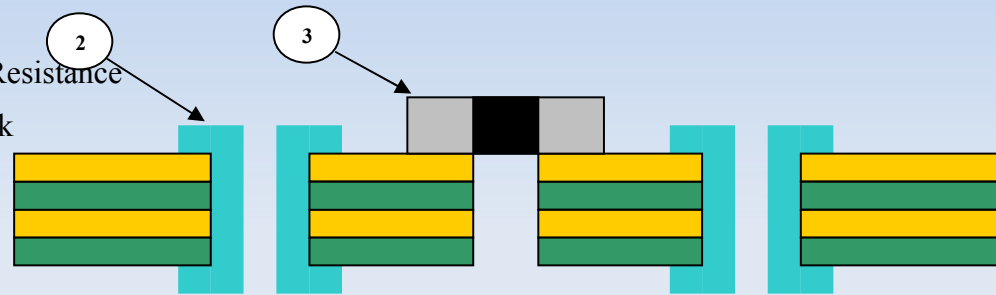
Support is being realized
CIEMAT



Connection between the different ASU is under study: signal transmission+ mechanics (IPNL+CIEMAT)



- 1 Weld
- 2 Via
- 3 0 Ω Resistance
- 4 Track



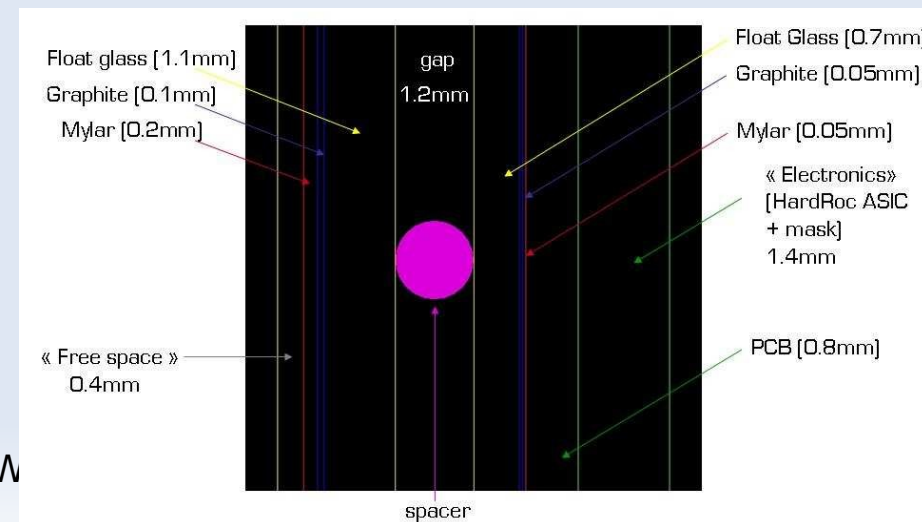
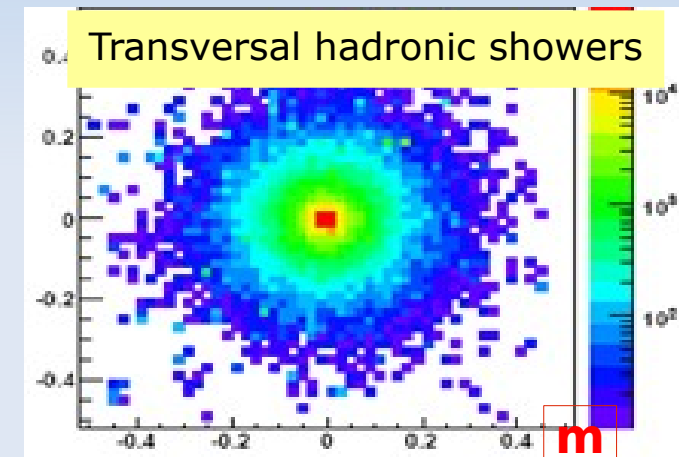
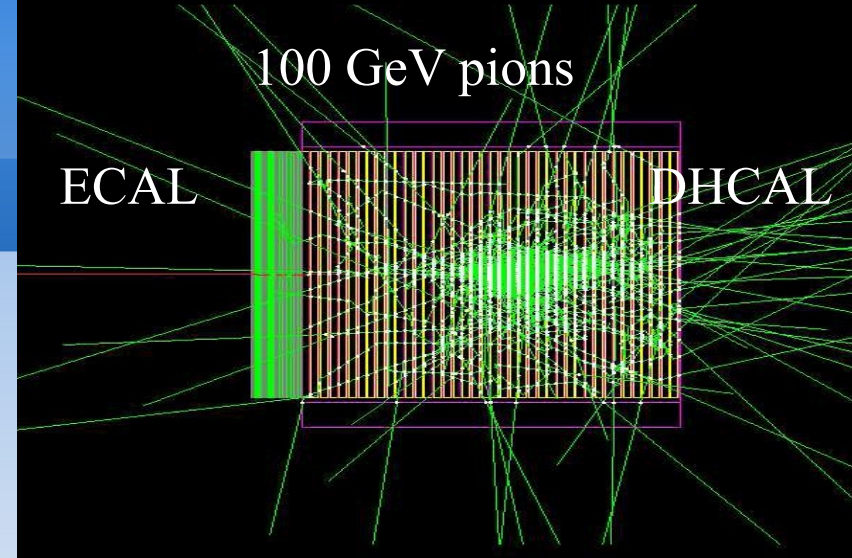
The 1 m³ project

Aims:

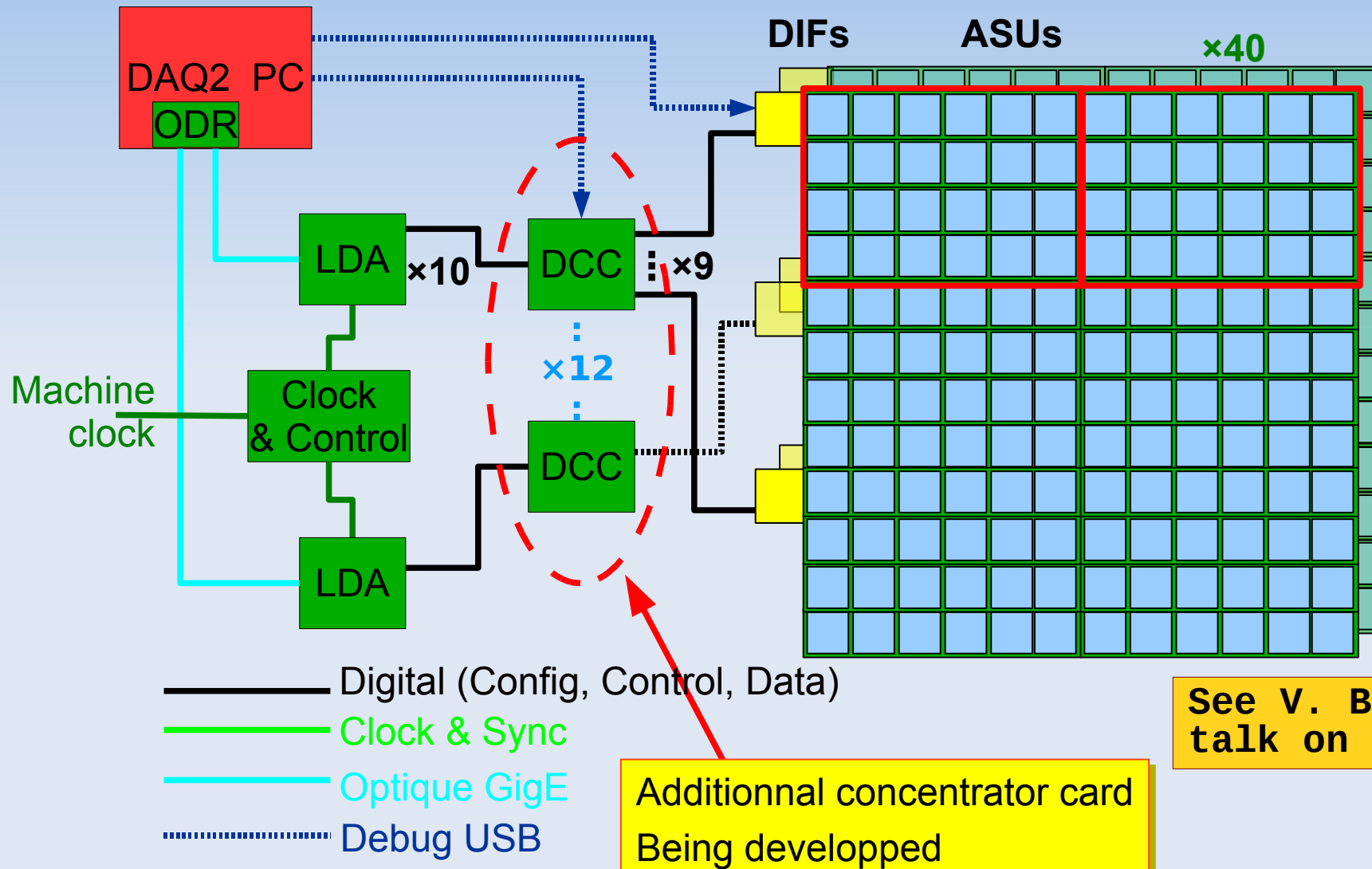
- Demonstrate the Digital SDGHCAL concept
- Learn as much as possible how to build a DHCAL for ILC (technological prototype)
- Study hadronic showers extensively

Implementation:

- ▶ 40 GRPC/μMegs interleaved with
- ▶ 40 stainless steel absorbers (2cm thick)
⇒ $4.5 \lambda_{\text{had.}}$
- Design optimization is on going using
- GEANT4 with **full cell details**



M³: First use of EUDET DAQ2

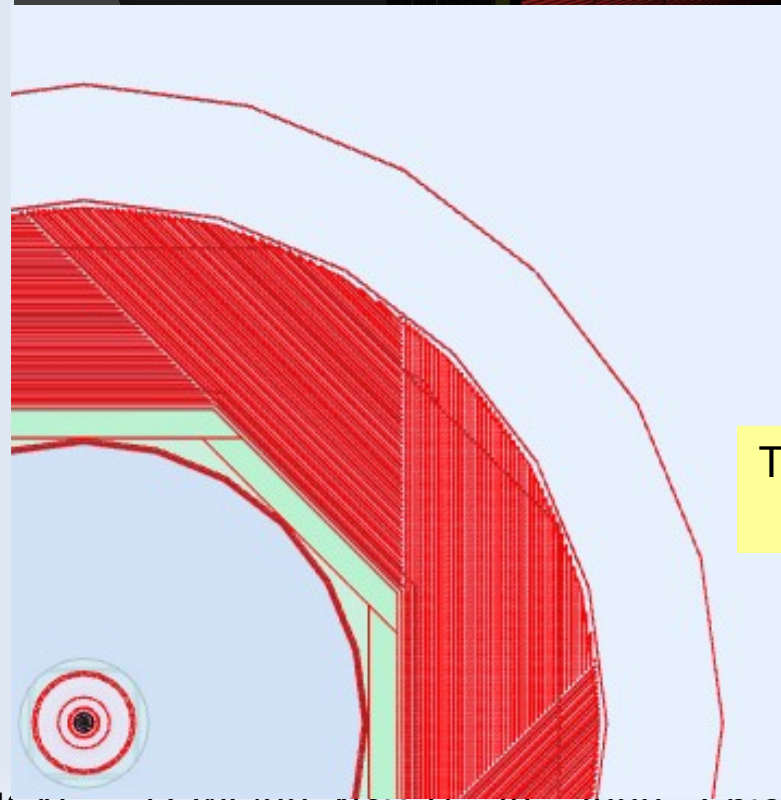
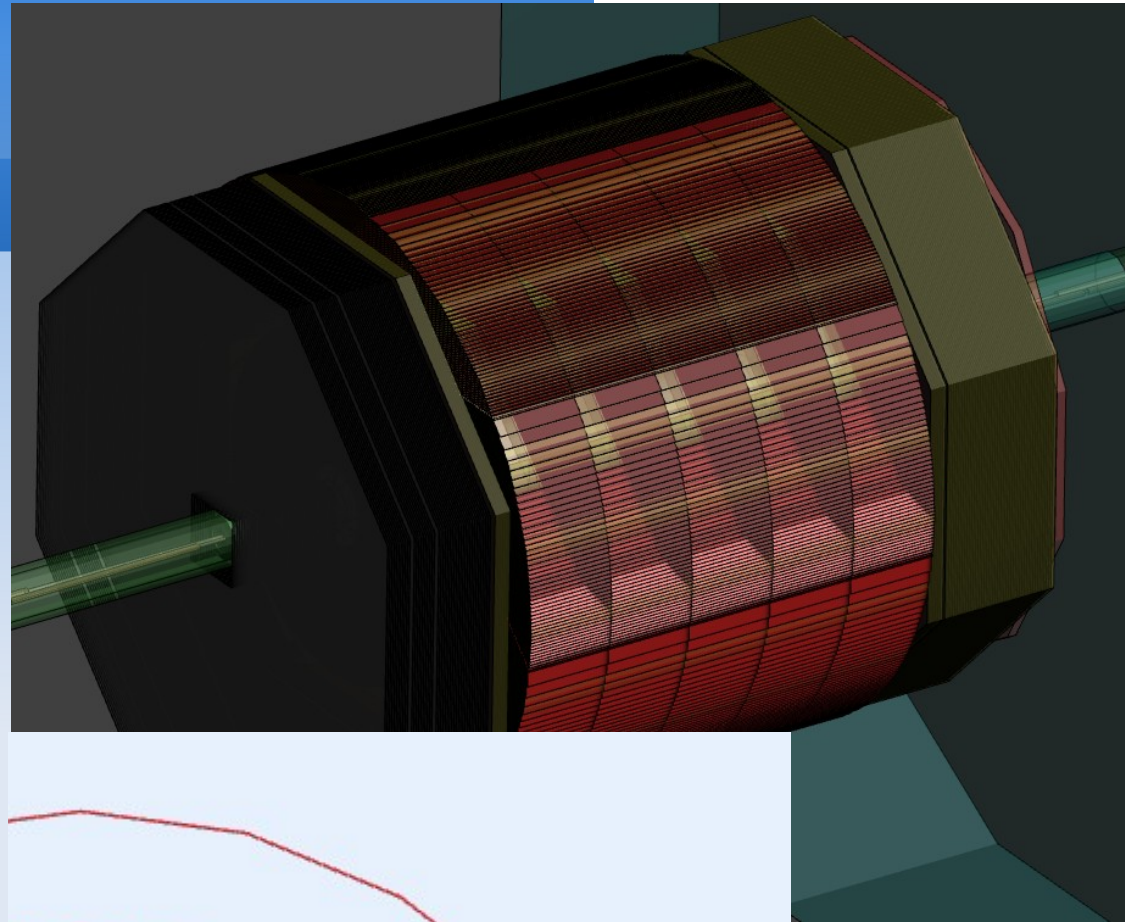


See V. Bartsch
talk on EUDET DAQ

Reminder: 40x100x100 cells = 400k channels!!!

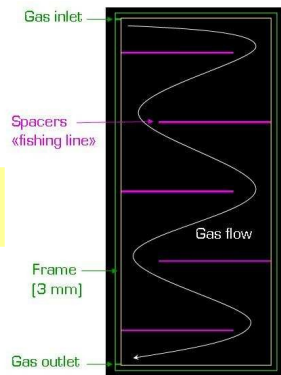
ILD integration

- Geometry in ILD simulation
 - ▶ 5 wheels + endcaps
 - ▶ 8 Modules/wheel
 - ▶ 48 layers/module
- Electronics, gaz and cooling on the periphery
 - ▶ Jointive barrel & endcaps
- Rigid mechanical structure



Tranverse cut

Gaz flow study

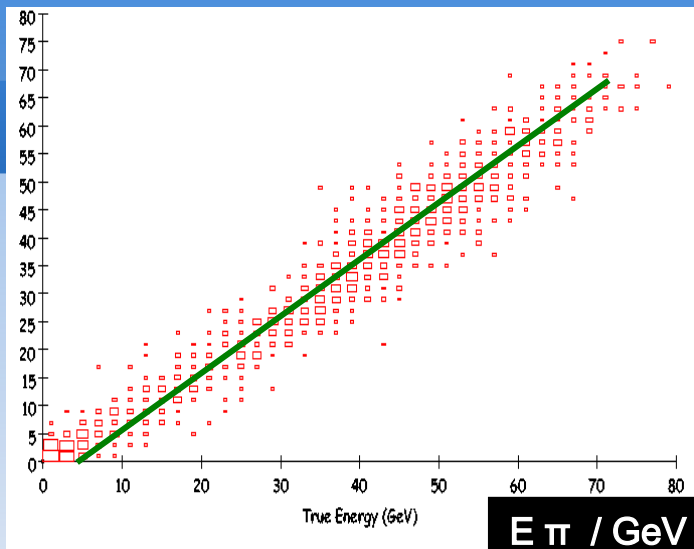


Conclusions & perspectives



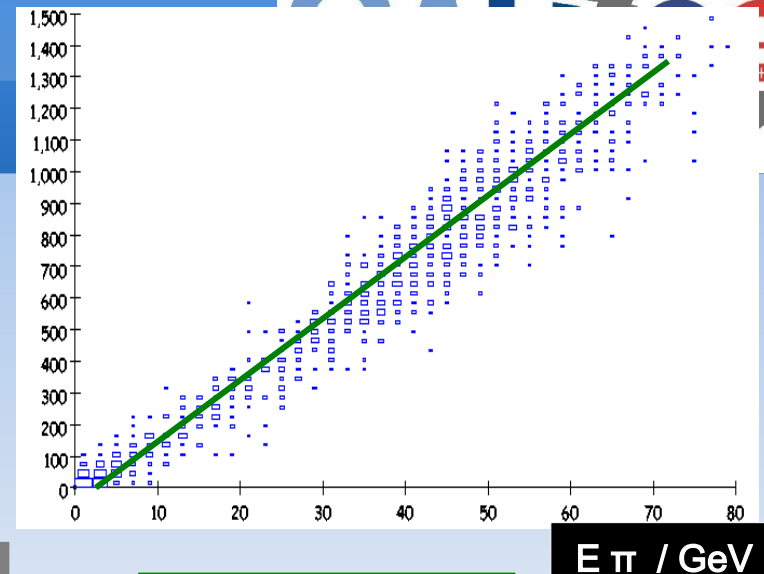
- A Semi-Digital Gaz Hadronic Calorimeter with embedded readout is a very promising candidate for future linear colliders experiments
- A mini SDGHCaI based on first generation readout with GRPC was successfully tested in laboratory and in test beam at CERN
 - ▶ the first results are arriving
- Active development on RPC's and MGRPC
- 1 m² project is ongoing
 - ▶ first equipped 1m² GRPC plan is expected before the end of 2008.
- A technological prototype "1 m³" is funded and expected in 2009-2010

Edep



Analog

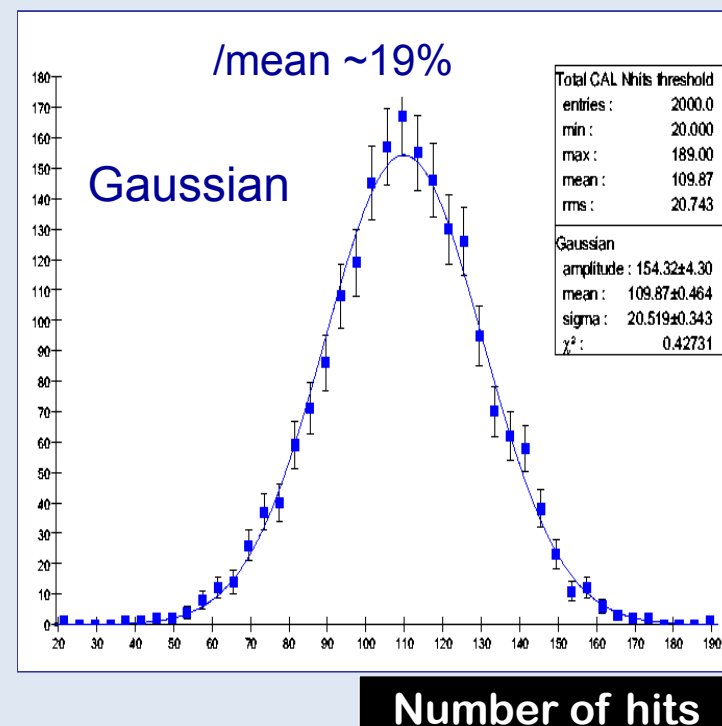
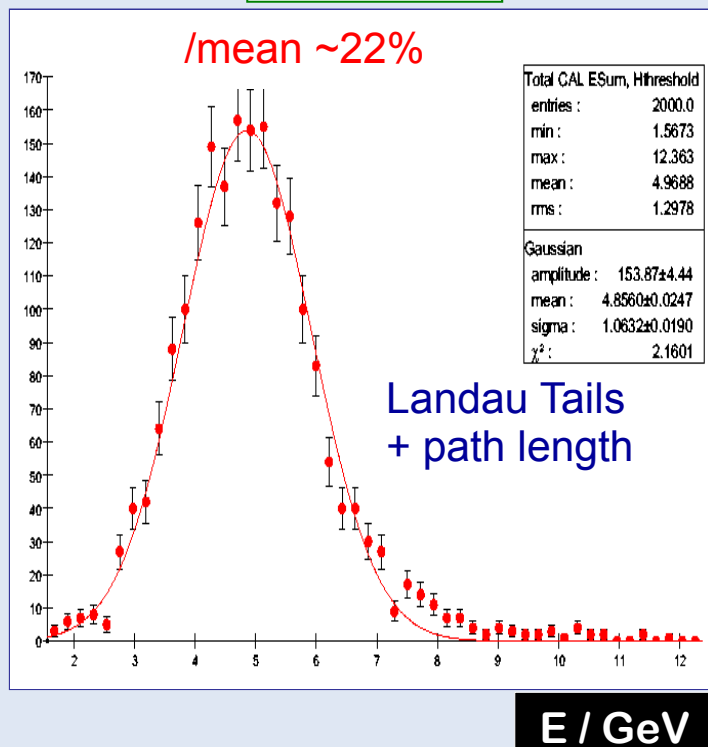
N hits



Digital-1bit

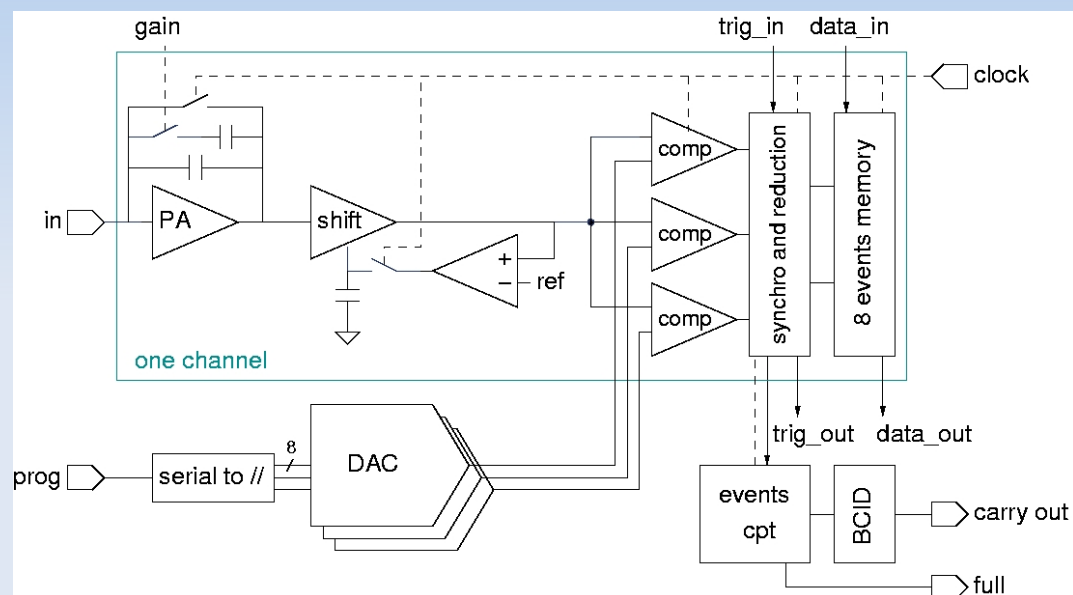
Simulation
Calice

$0^+ 5 \text{ GeV}$



DIRAC ASIC

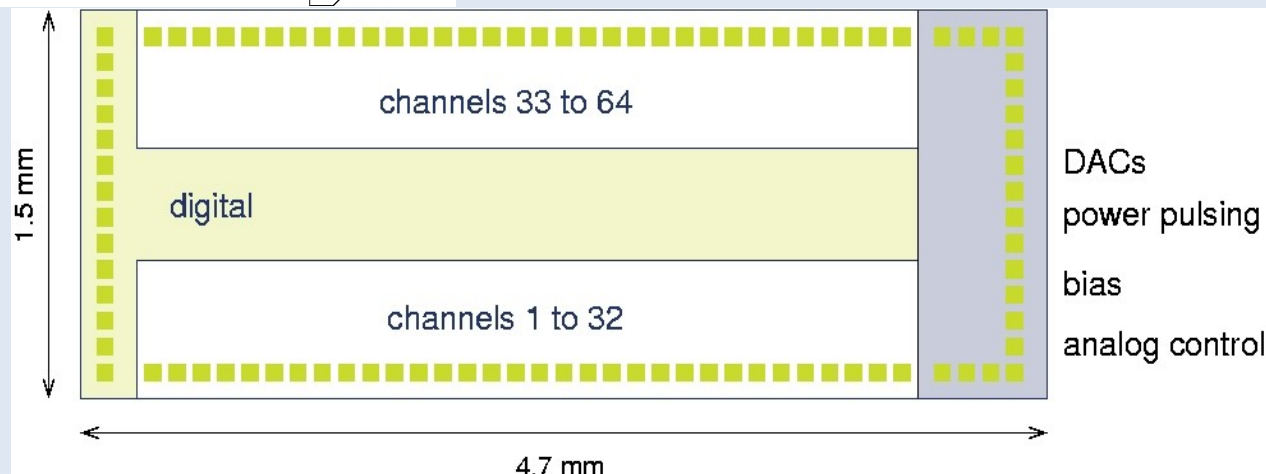
A new chip with a low threshold for μ MEGAS
is under development @IPNL



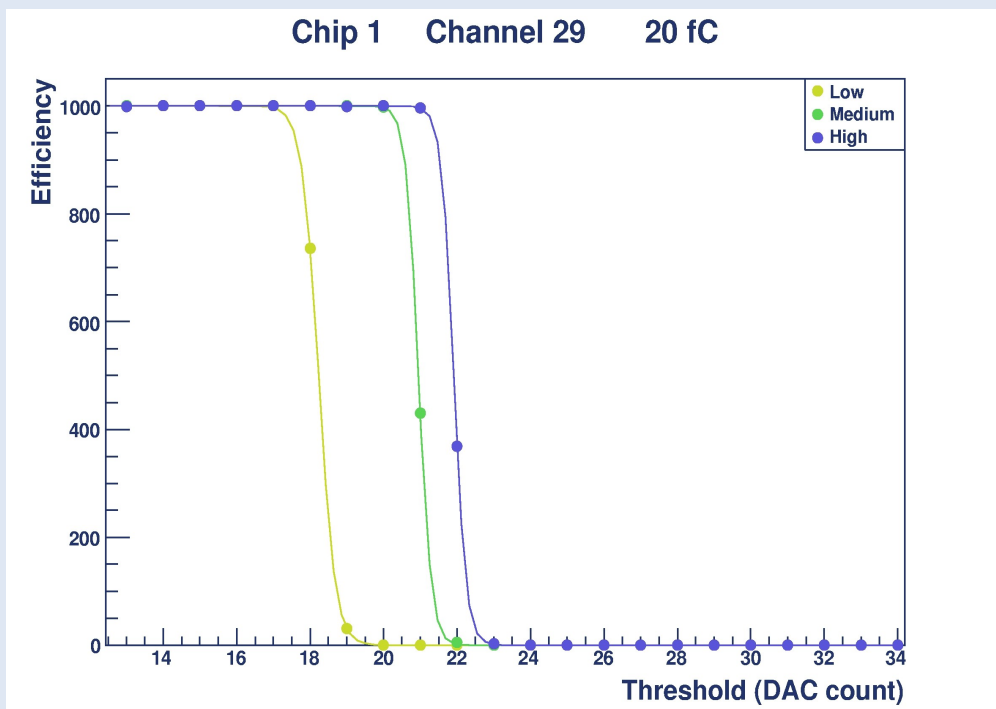
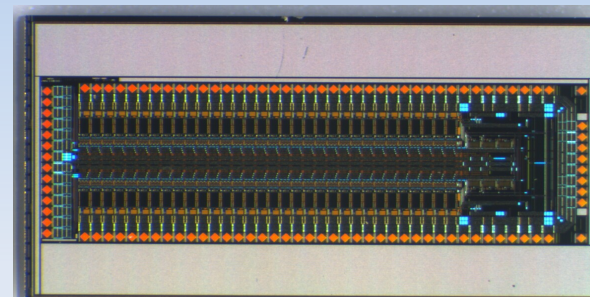
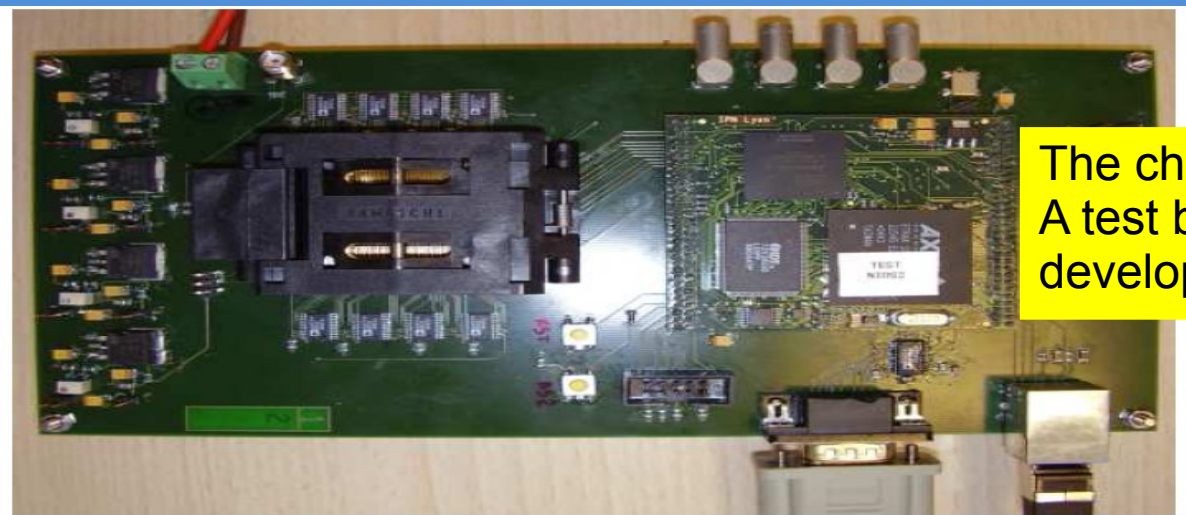
3 DACs (8 bits each)
BCID = 12 bits
memory depth= 8 evts

64-ch chip
CMOS tech
power pulsed

Simple geometry



The chip was designed and produced. A test board using OPERA DAQ developed @IPNL was used.



First results:
Mode μ MEGAS
0.8 fc/DAQ
Resolution < 2.5 fc

Tests and improvement are going on

HARDROC: Power pulsing

