# R&D status of FPCCD VTX

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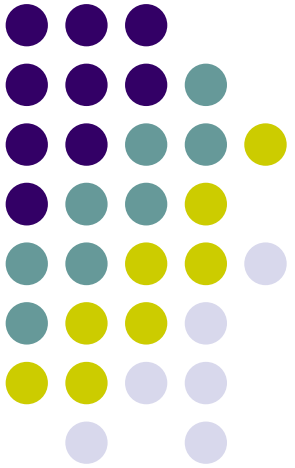
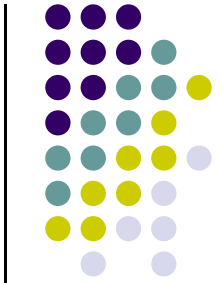


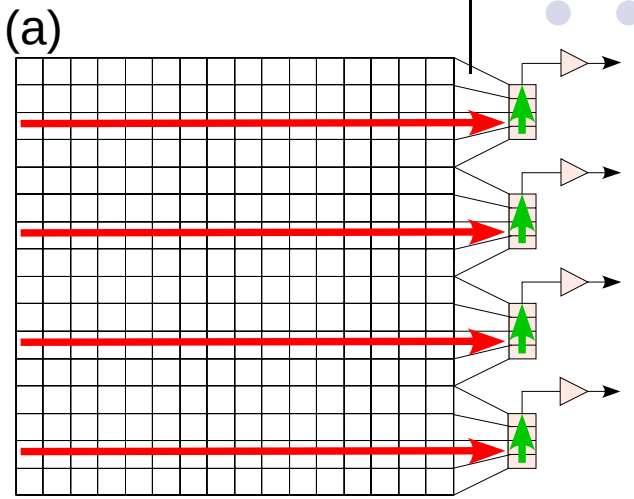
# FPCCD concept

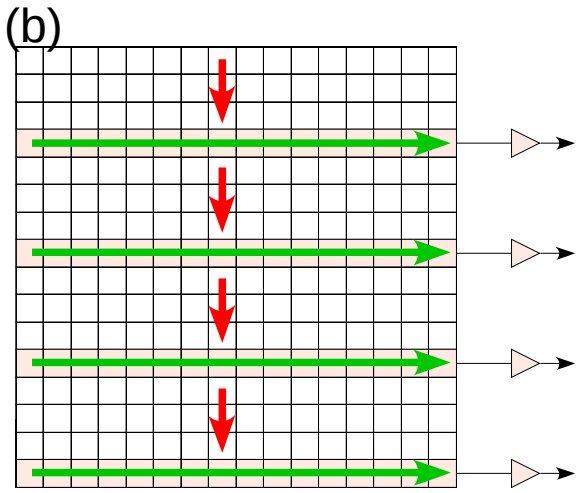


- Accumulate hit signals for one train (2625 BX) and read out between trains (200ms) → Completely free from EMI
- Fine pixel of ~5μm (x20 more pixels than “standard” pixels) to keep low pixel occupancy
  - Spatial resolution of ~1.5μm even with digital readout
  - Excellent two-track separation capability
- Fully depleted epitaxial layer to minimize the number of hit pixels due to charge spread by diffusion
- Two layers in proximity make a doublet (super layer) to minimize the wrong-tracking probability due to multiple scattering
- Three doublets (6 CCD layers) make the detector
- Tracking capability with single layer using hit cluster shape can help background rejection
- Multi-port readout with moderate (~10MHz) speed (Very fast readout (>50MHz) not necessary)
- Simple structure → Large area
- No heat source in the image area

# Design optimized for CTE

- Two options for multi-port readout
  - (a) is adopted for SLD VTX
  - (b) is more advantageous from the viewpoint of radiation tolerance (CTE: charge transfer efficiency)



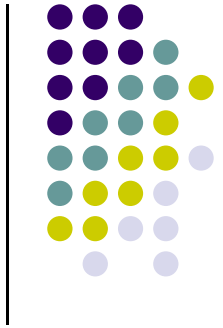




Charge transfer inefficiency (CTI) due to traps caused by radiation damage becomes smaller if $1/f_{clock} << \tau_c$, where $\tau_c$ is electron capture time constant (~300ns for 0.42eV level)

➔ $CTI_V > CTI_H$ (H-clock>10MHz, V-clock<1MHz)

➔ The number of V-shift should be small

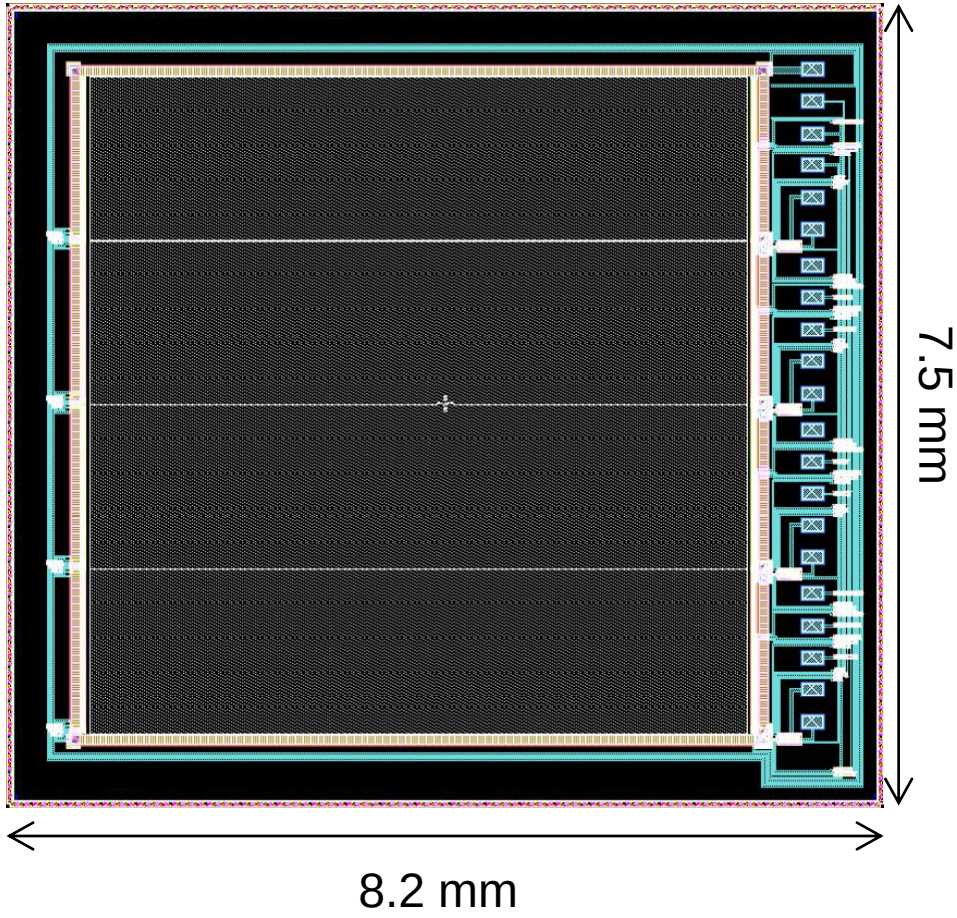
# R&D for FPCCD sensor



- Challenges of FPCCD
  1. Small pixel size ~5 μm
  2. Readout speed > 10 MHz
  3. Noise < 50 electrons (preferably <30 electrons)
  4. Power consumption < 10 mW/ch
  5. Horizontal register (same size as pixel) in the image area
  6. Wafer thickness ~50 μm
  7. Multi-channel low power readout ASIC ➔ Takubo's talk
- Prototype sensor in FY2007
  - Tackle issues 2, 3, 4, and 5

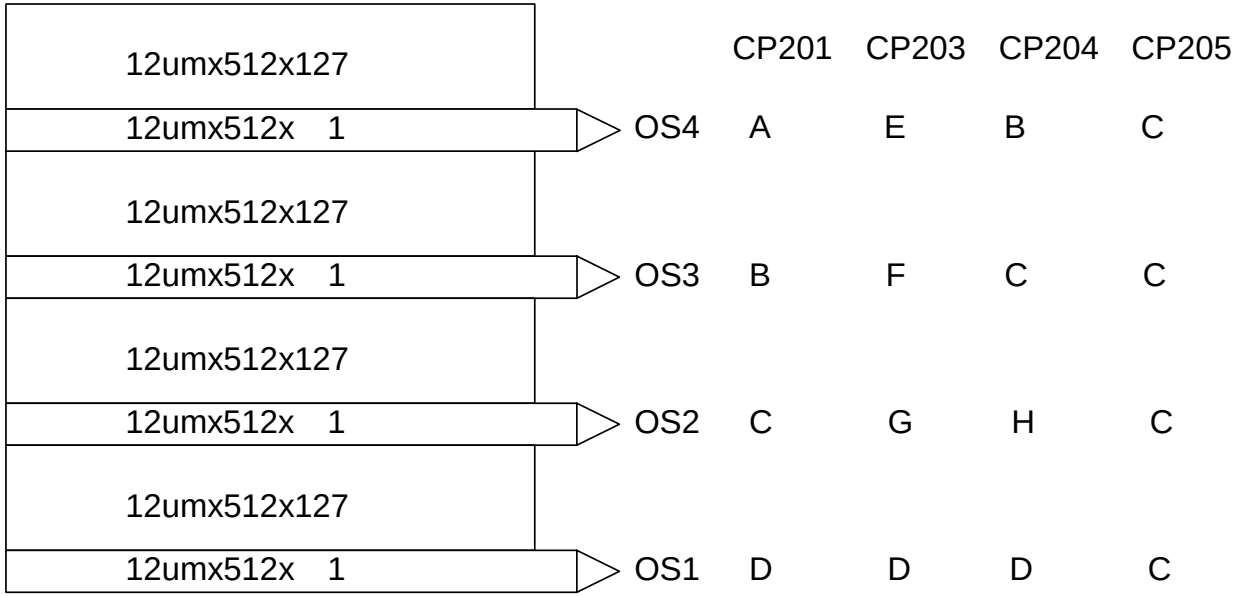
# Prototype of FPCCD

- 12μm pixel size
- 512x512 pixels
- 6.1mm$^2$ image area
- 4ch /chip
- 128(V)x512(H) pixels for each channel
- Several different designs of output amp
- Chips have been made by HPK



# Types of Prototype

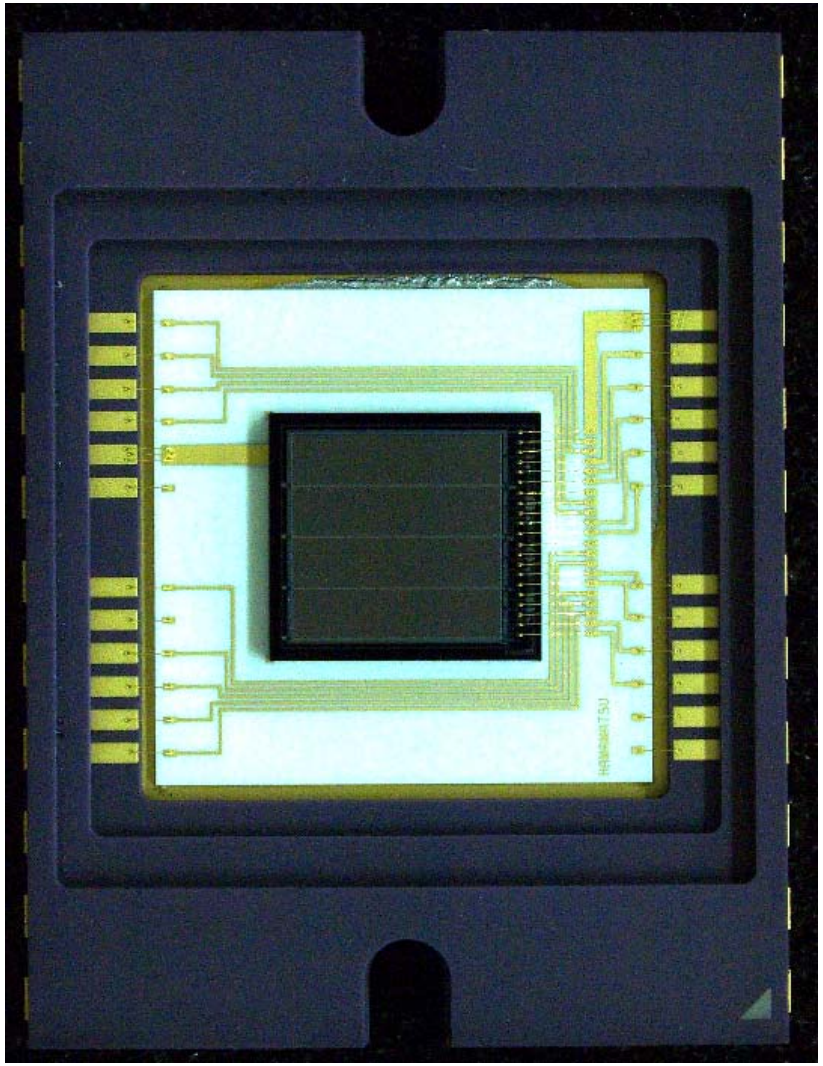
- Output amp: type A – H

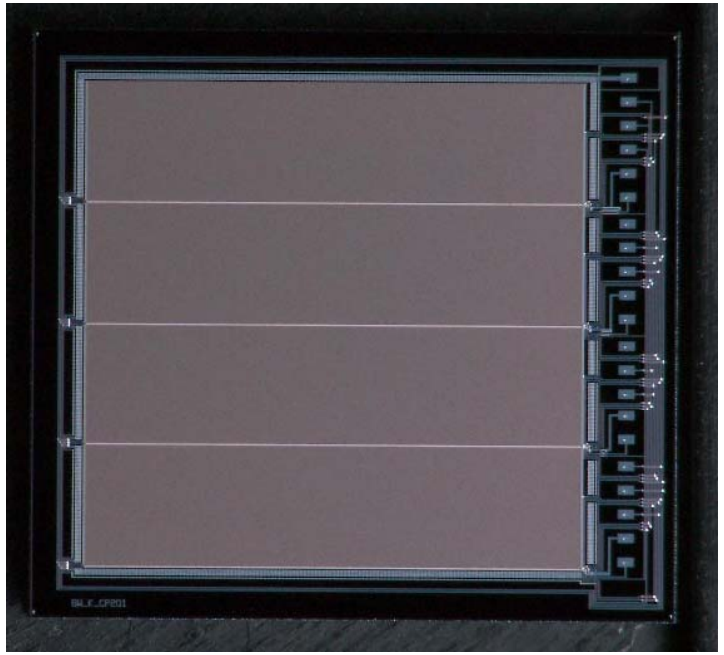



| | CP201 | CP203 | CP204 | CP205 |
|---|---|---|---|---|
| OS4 | A | E | B | C |
| OS3 | B | F | C | C |
| OS2 | C | G | H | C |
| OS1 | D | D | D | C |

- Process / Device type
  - Wafer: epitaxial layer 24 / 15 μm
  - Gate $SiO_2$ for output Tr: standard (all) / thin (CP204, 205)
  - Device type: package / bare chip

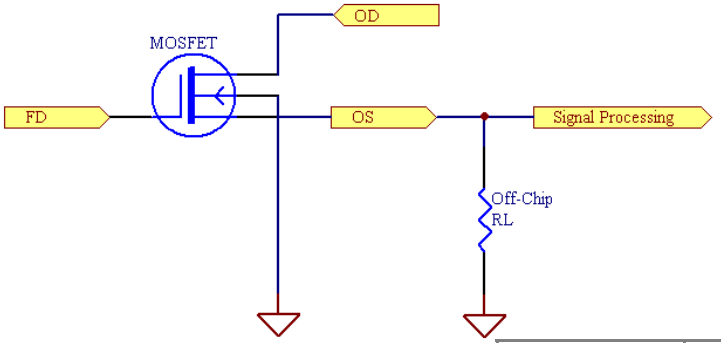
# Packaged and bare chip



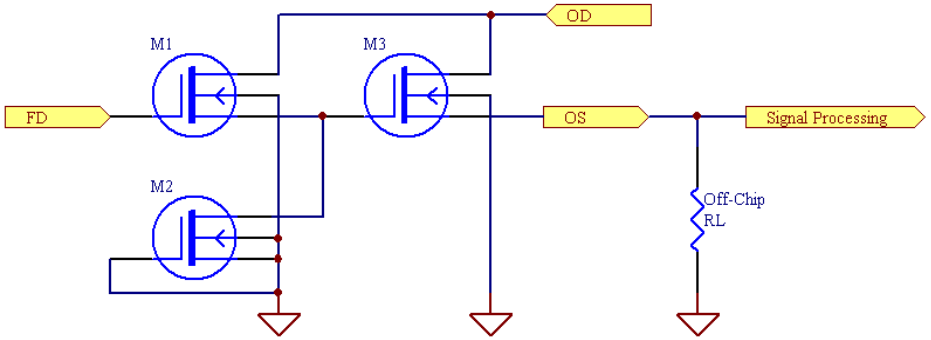


# Output amp

- Type D




- Others




| Type | M1 | M2 | M3 |
|---|---|---|---|
| A | M1-Type1 | M2-Type1 | M3-Type1 |
| B | | | M3-Type2 |
| C | | | M3-Type3 |
| E | | M2-Type2 | M3-Type2 |
| F | | | M3-Type3 |
| G | | | M3-Type4 |
| H | | M2-Type1 | M3-Type4 |
| Remark | | Type1 > Type2<br>at drain current | Type1 > Type2 > Type3 > Type4<br>at drain current |

# Characteristics of Prototype

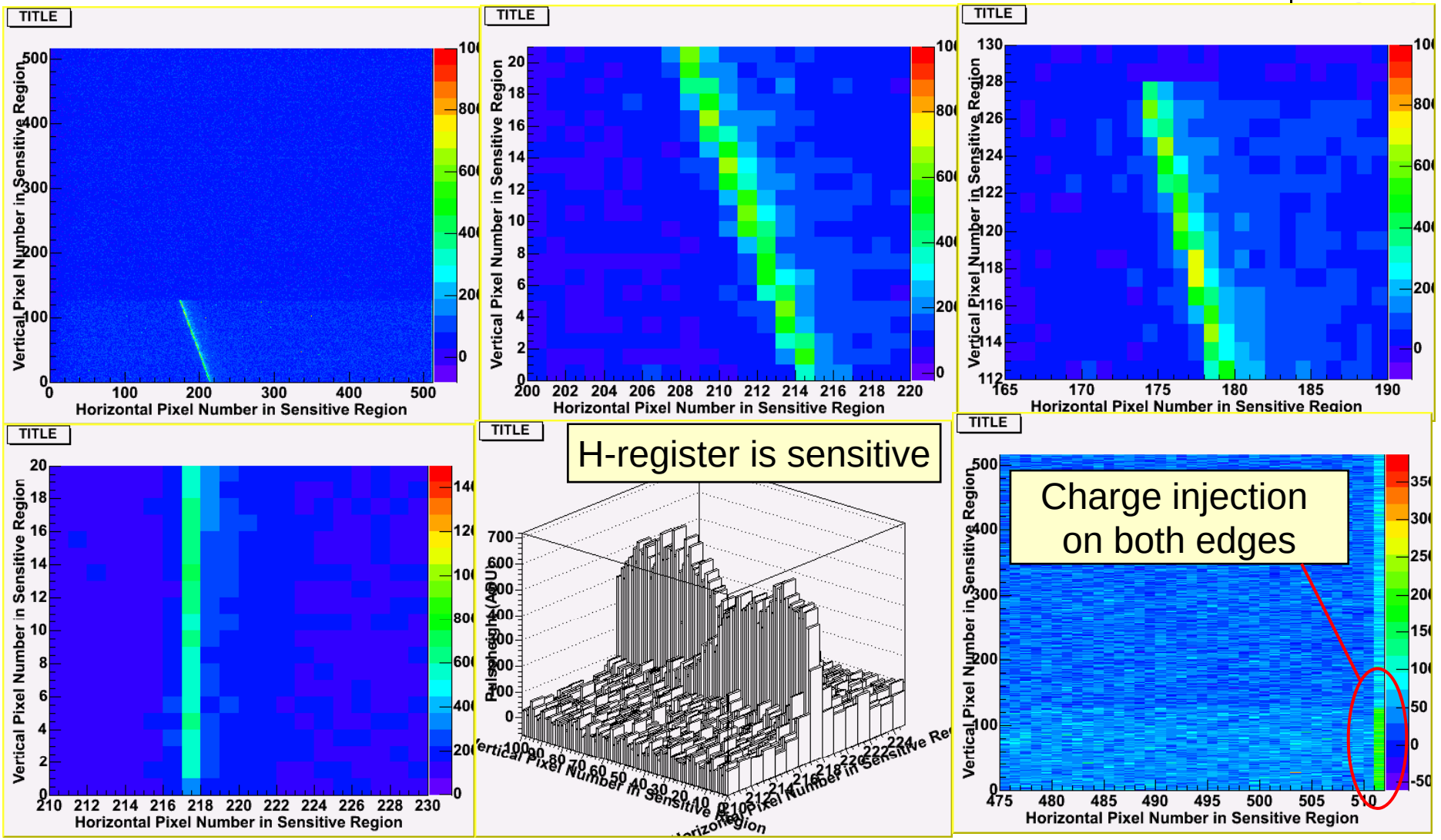
- Preliminary results given by HPK

| Device type | Package | | Bare chip | |
|---|---|---|---|---|
| Epi thickness (μm) | 15 | 24 | 15 | 24 |
| V-register gate capacitance (pF) | 1600 | 550 | 1600 | 550 |
| H-register gate capacitance (pF) | 40 | 40 | 40 | 40 |
| Output source capacitance (pF) | <4 | <4 | <2 | <2 |

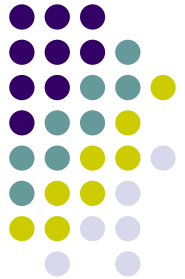
| Amp type | | A | B | C | E | F | G |
|---|---|---|---|---|---|---|---|
| Output gain (μV/e) | Epi:15 μm | 5.4 | 5.3 | 5.2 | 6.9 | 6.2 | 5.6 |
| | Epi:24 μm | 5.8 | 5.3 | 5.0 | 6.6 | 5.9 | 5.4 |
| Id (mA) | Epi:15 μm | 1.57 | 1.55 | 1.50 | 1.28 | 1.22 | 1.14 |
| | Epi:24 μm | 1.48 | 1.44 | 1.38 | 1.15 | 1.09 | 0.99 |

$V_{OD}$=10V, $R_L$=10kΩ, 10MHz, RT

# Test with line-focused LASER

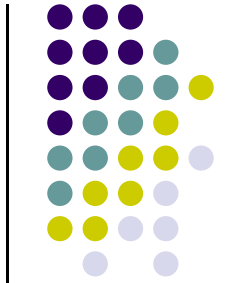


# Plan for FY2008 prototype



- Same pixel (12μm) and chip size
- Larger full-well capacity
- No charge injection
- Double Al layers to reduce R of H-register

# Summary and outlook



- The first prototype FPCCDs have been made by HPK
  - Pixel size: 12μm
  - H-register same size as pixels
  - 4ch/chip
  - Several types of output circuit
  - Two different epitaxial layer thickness (15 / 24 μm)
  - Two different gate oxide thickness for output transistors
- Detailed study on the prototype FPCCDs has started
  - H-register is sensitive
  - Charge injection is seen on both edges of the chip
- Improved prototype is planned in FY2008