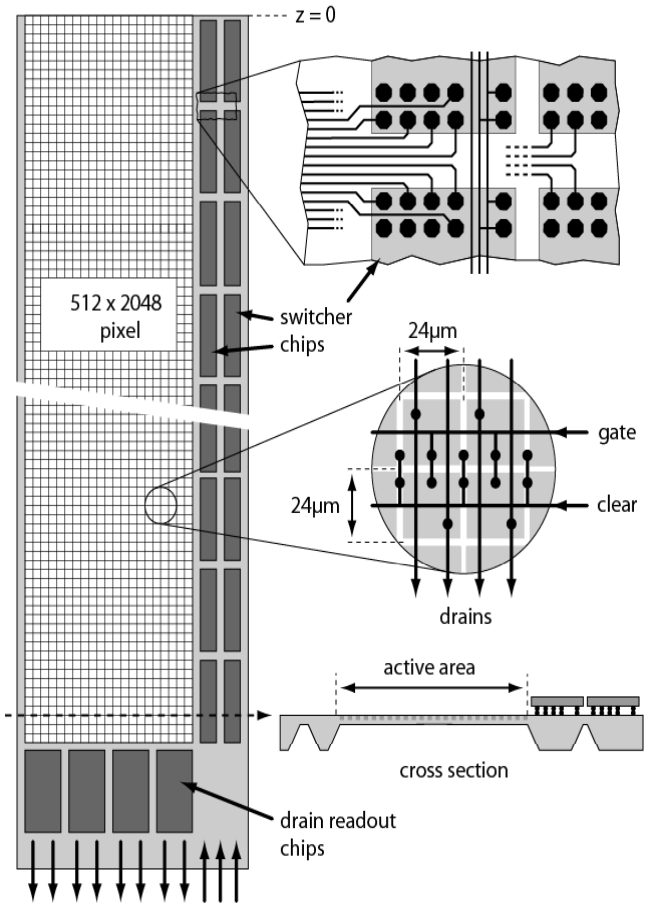
DEPFET Active Pixel Sensors
- Status and Plans -

Ladislav Andricek for the DEPFET Collaboration (www.depfet.org)

In Summary: Achievements and Status



DEPFETs for the ILC VXD

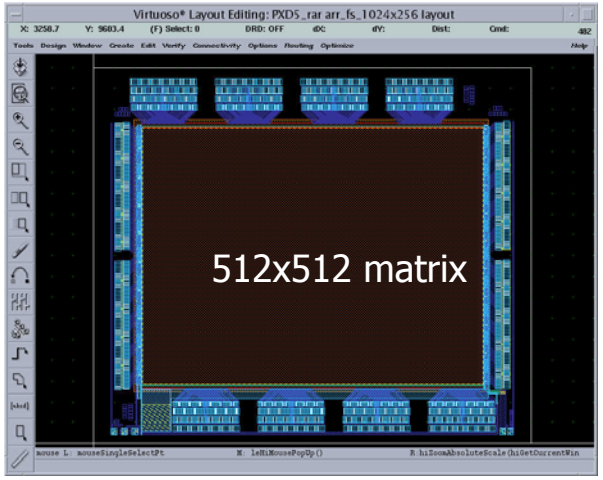
- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ many test beams @ CERN and Desy:
  - ✓ S/N≈140 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. with 24 µm pixels: 1.3 µm @ 450 µm ←→ goal ≈ 3..4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm), design goal 0.11 % X_0
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2

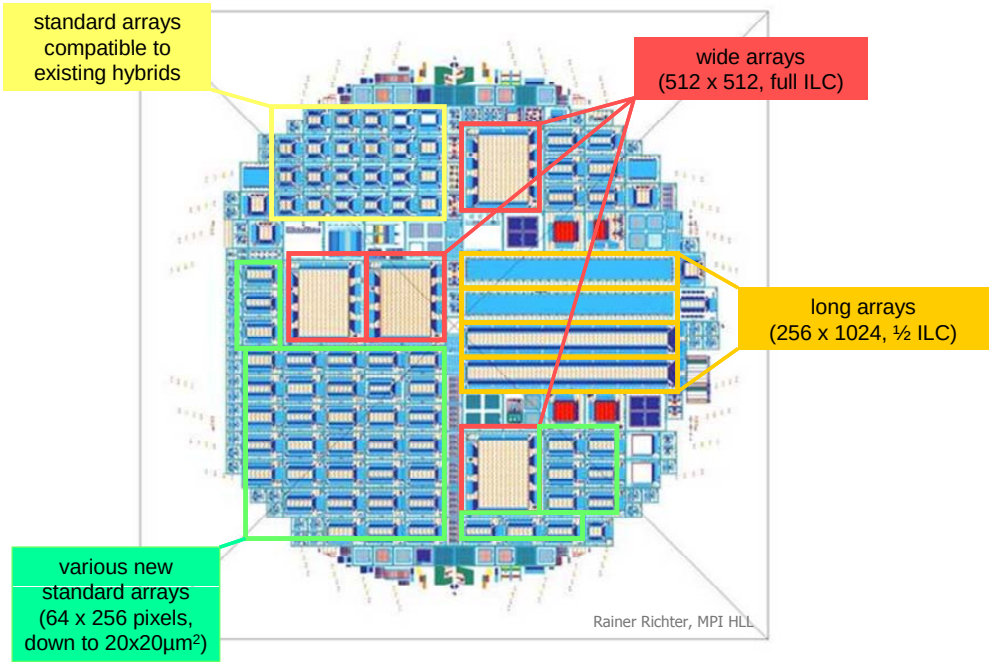
In this talk:

- Some new features of the latest DEPFET production
- Update on thinning/ladder R&D
- Next Steps

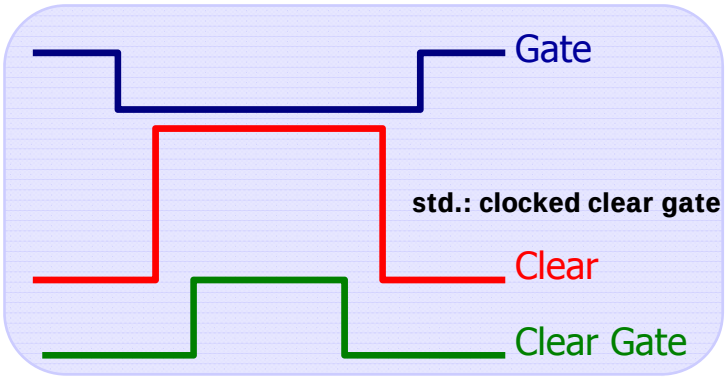
The latest DEPFET Generation 'PXD5'

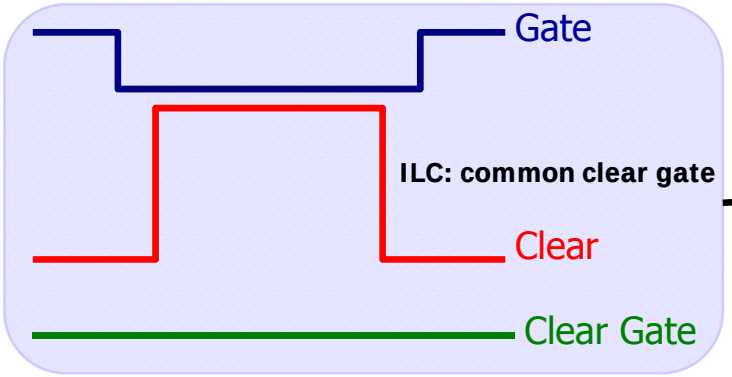
- Mostly use 'baseline' linear DEPFET geometry
- Build **larger matrices**
  - Long matrices (full ILC drain length)
  - Wide matrices (full Load for Switcher Gate / Clear chips)
- Try new DEPFET variants:
  - -: reduce **clear voltages**
  - -: Very **small** pixels (20µm x 20µm)
  - -: Capacitively Coupled Common Clear Gate
  - -: Increase internal **amplification** (g_q)

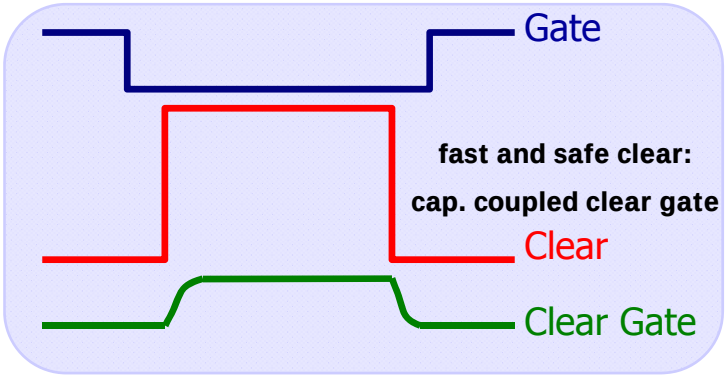


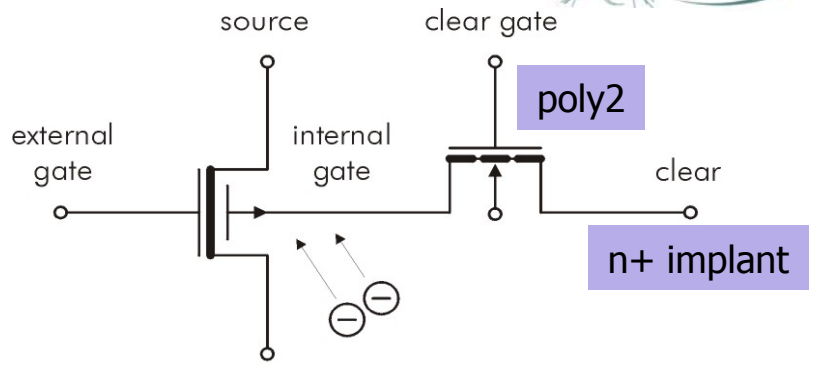


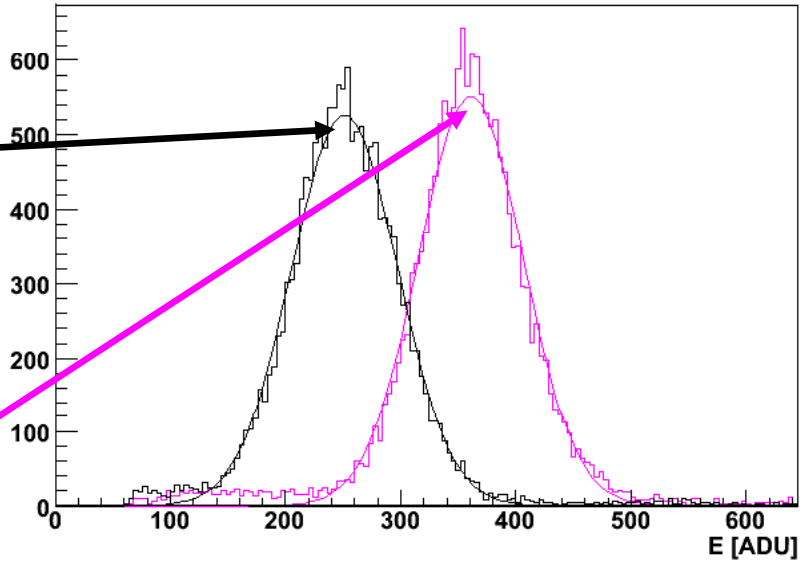
Capacitively Coupled Common Clear Gate









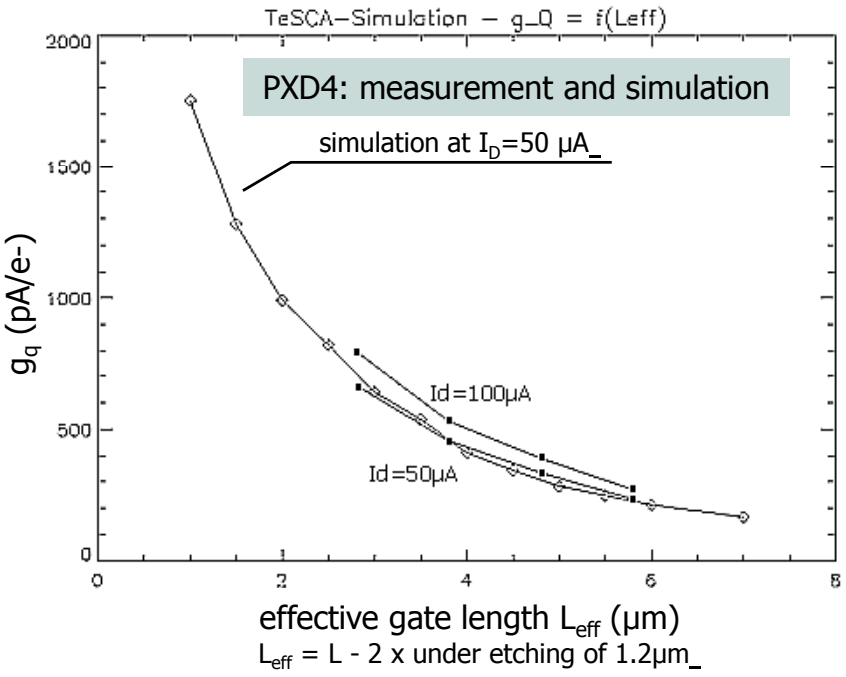


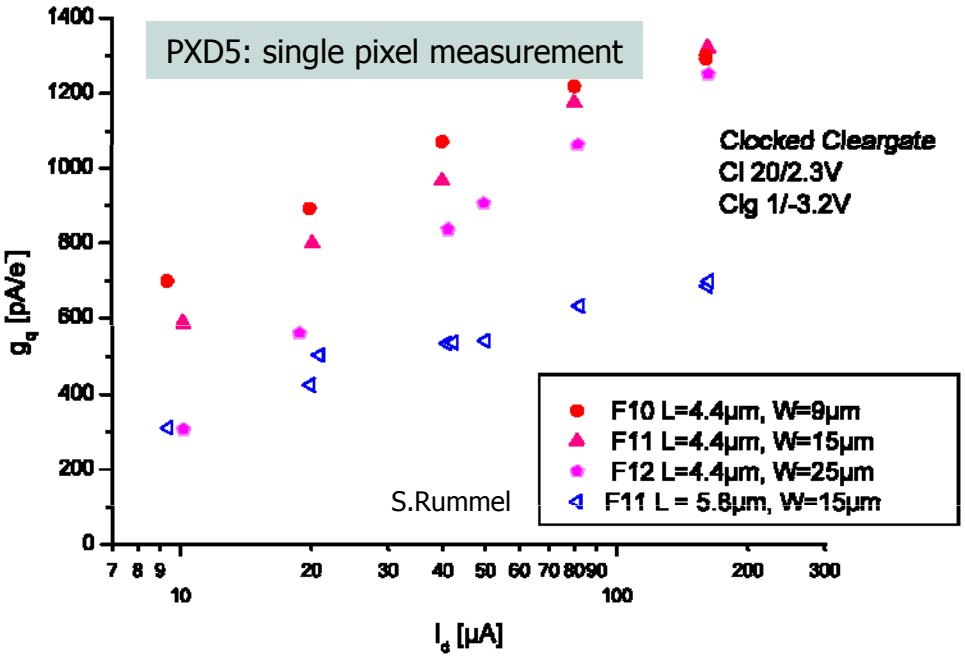
^{109}Cd spectrum (22keV, 6000 e$^-$)

taken with 128x64 matrix

Internal amplification g_q

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)



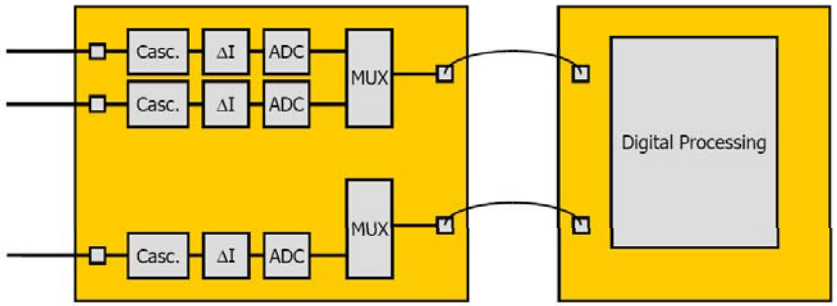


As long as noise is dominated by r/o chip → S/N linear with g_q

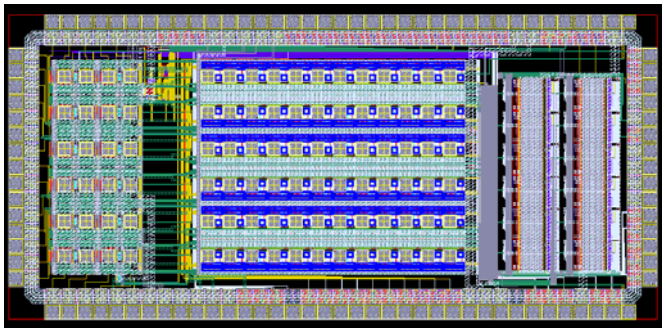
PXD4 has L=6µm, some matrices in PXD5 have now L=4µm → expect factor 2 better S/N

A new r/o chip - DCD

DCD: **D**rain **C**urrent **D**igitizer



Test chip DCD2: 6X12 channels



(Uni Heidelberg)

-: improved input cascode (regulated) and current memory cells

-: integrated 8bit current based ADC per channel, 12.5 MHz sampling rate but needs 600MHz Clock

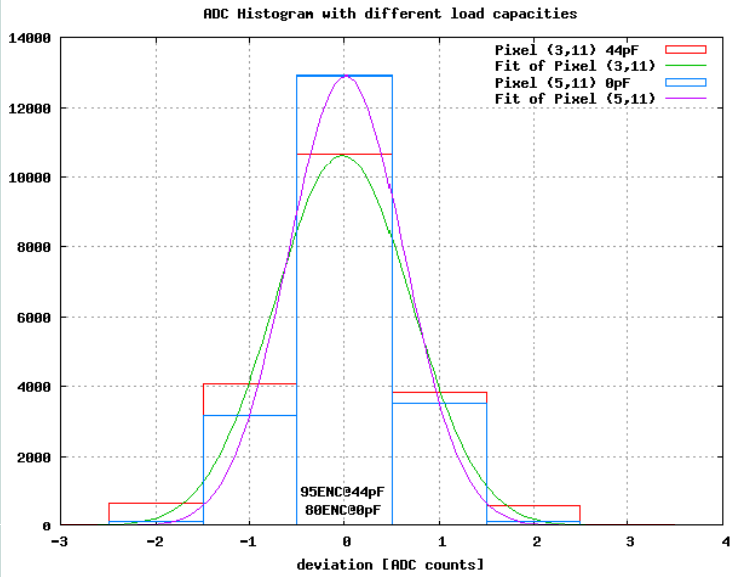
-: designed for 40 pF load at the input (5cm Drain line), 12 µm r/o pitch

-: f/e noise: 34nA@40pF, 17nA@10pF, add 37nA for memory cells
→ **50nA@40pF** → at 40pF with g_q=500pA/e → **100 e- ENC in total**

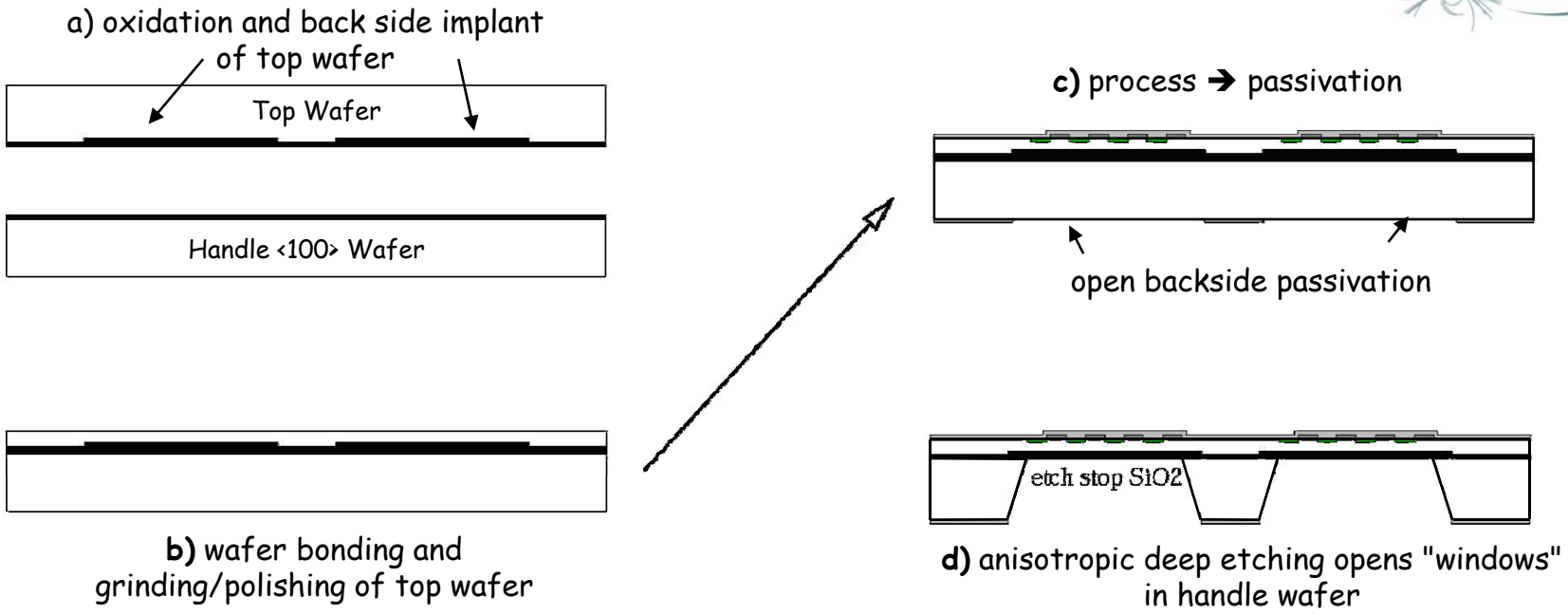
-: layout for bump bonding, rad. hard design

-: power consumption per channel 3.6 mW (measured)

-: digital hit processing done with 2nd digital chip (DHP)



Thinning Technology



Compatibility with the main production line tested

So far for ILC:

-: mechanical samples

-: test structures (diodes) on SOI wafers

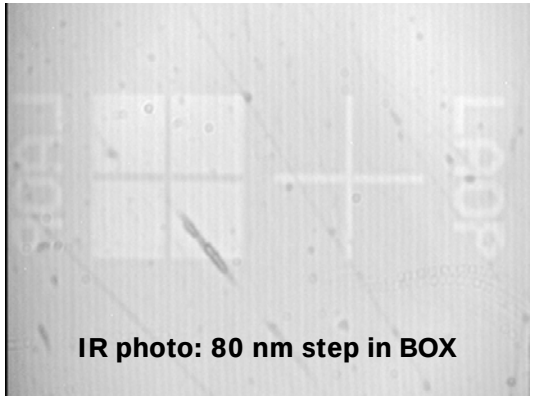
Presented the first time about 6 years ago, this technique found now its way into other projects:

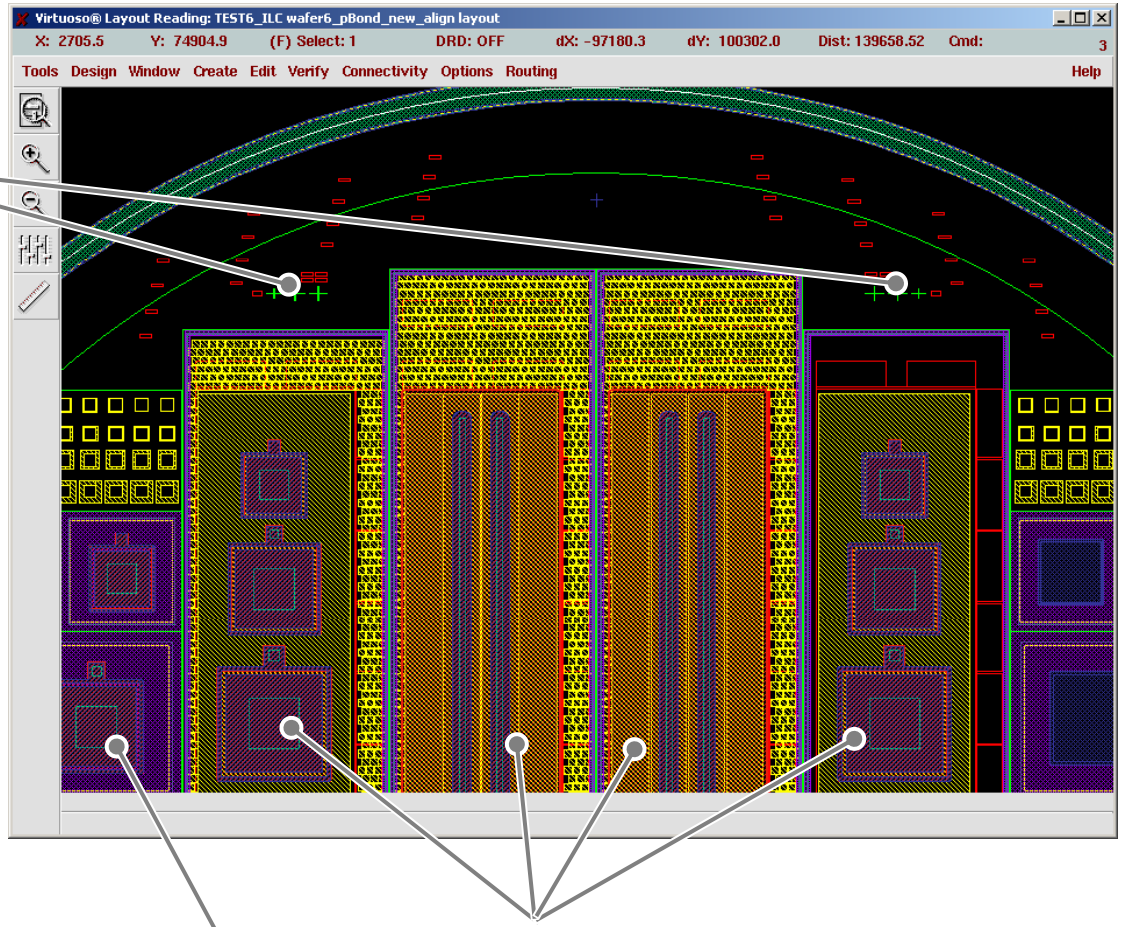
-: production of thin (75 and 150 µm) ATLAS pixel sensors for sLHC

-: first production of Geiger-mode APDs on 70 µm top layer

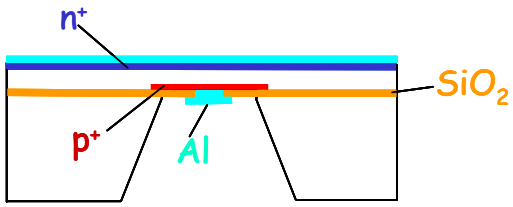
Large area diodes

Alignment marks in BOX to find the partial p-implant after bonding





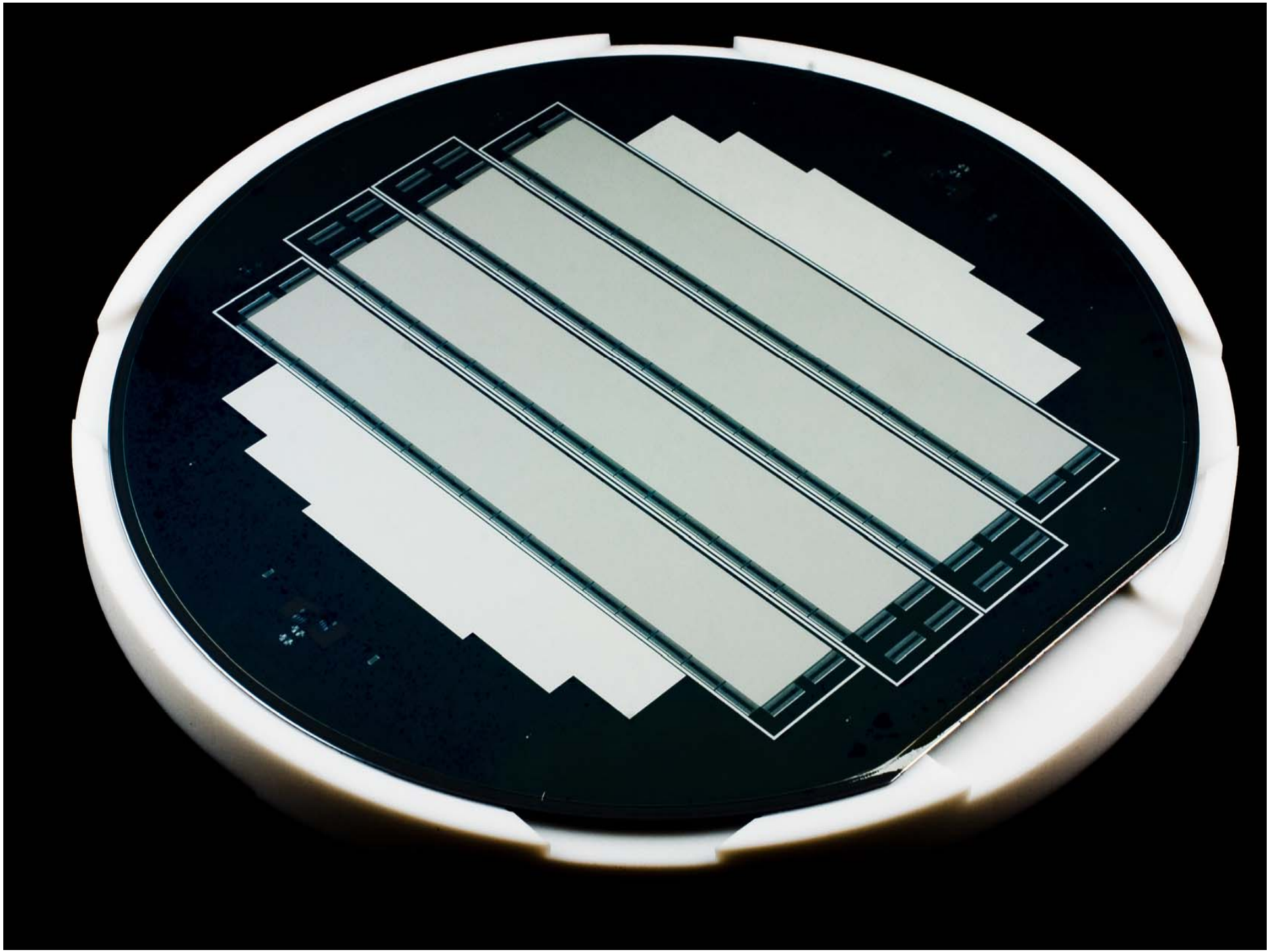
Implants like DEPFET config.

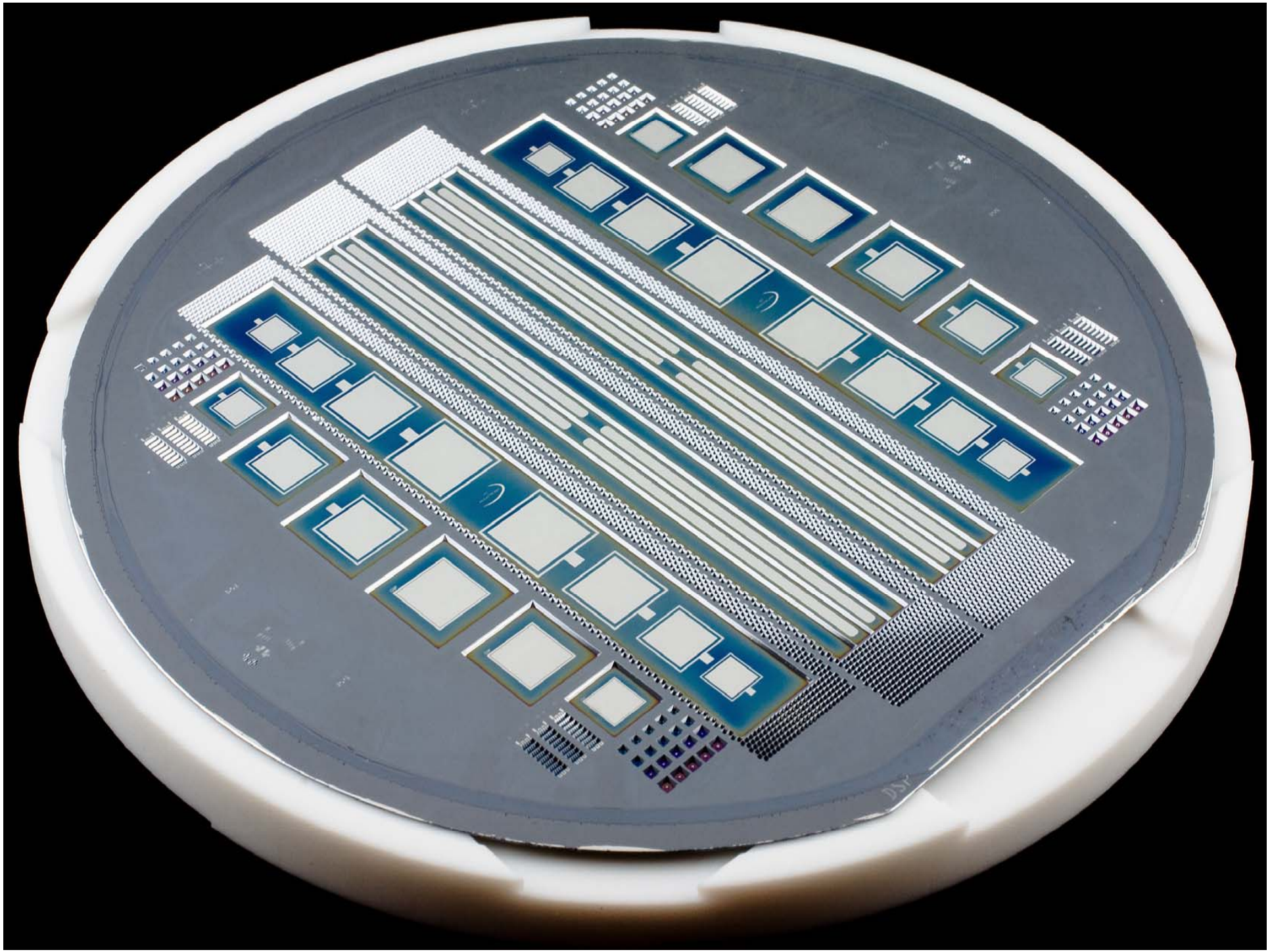


unstructured n+ on top
structured p+ in bond region

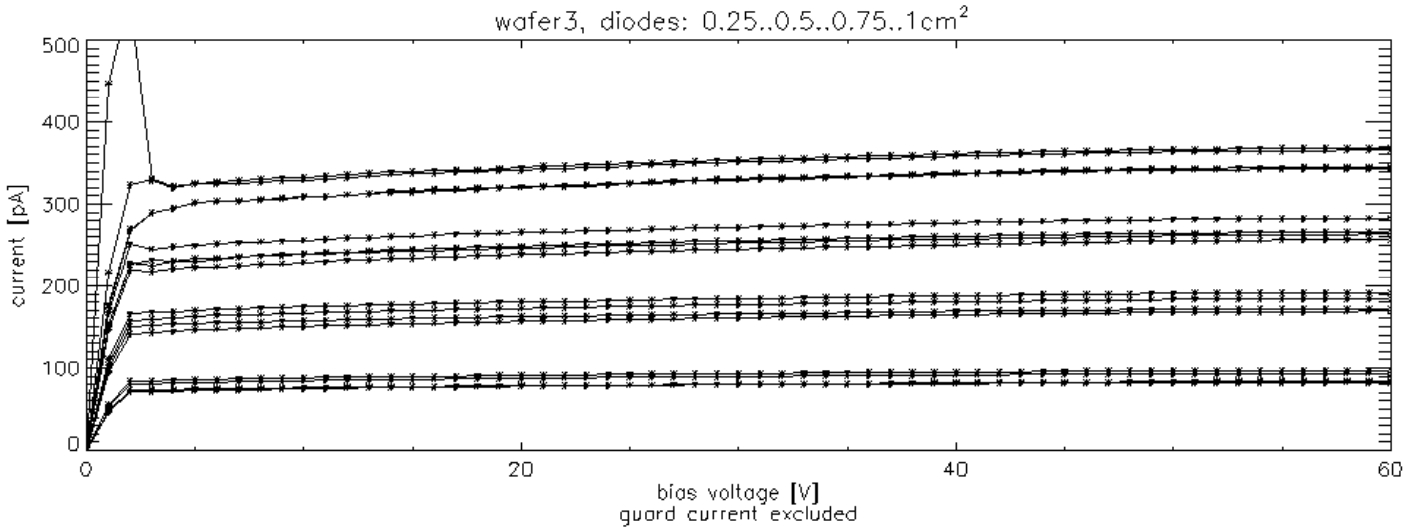
Diodes with various areas

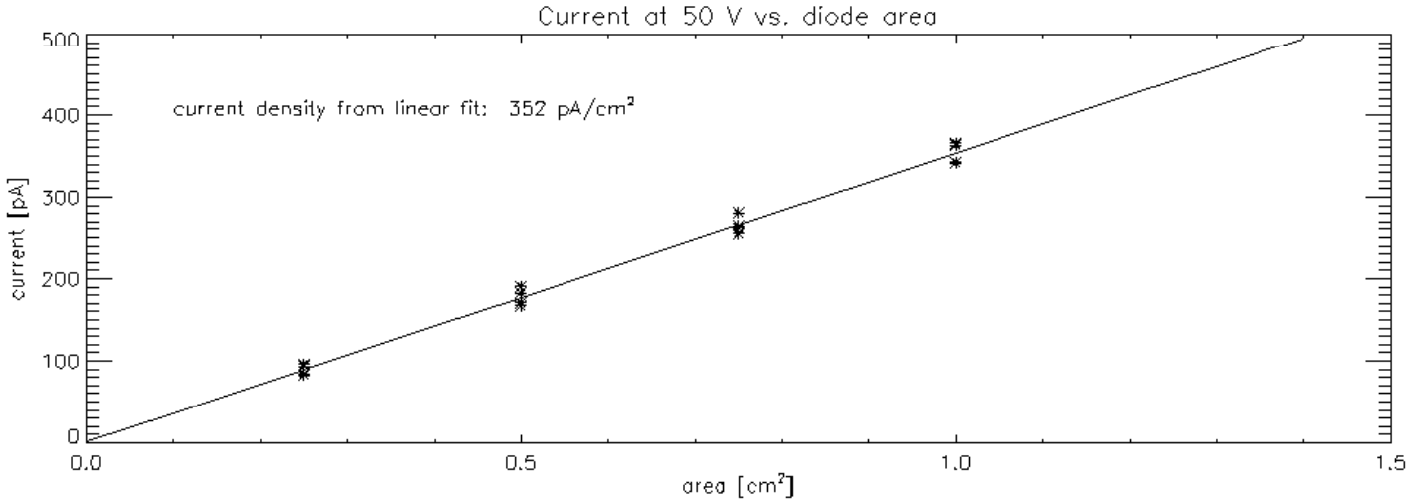
4 "full size" 1st layer ILC ladders 100x13 mm², 1 and 3 mm frame along the long side





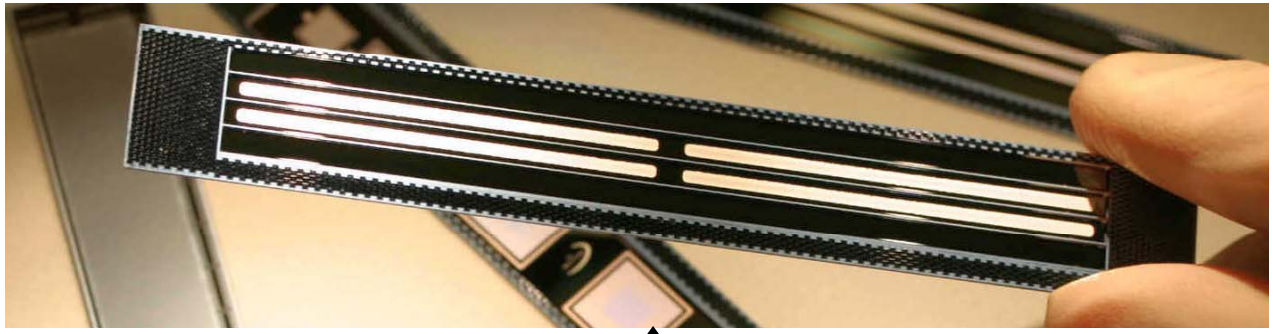
Large area diodes - characteristics



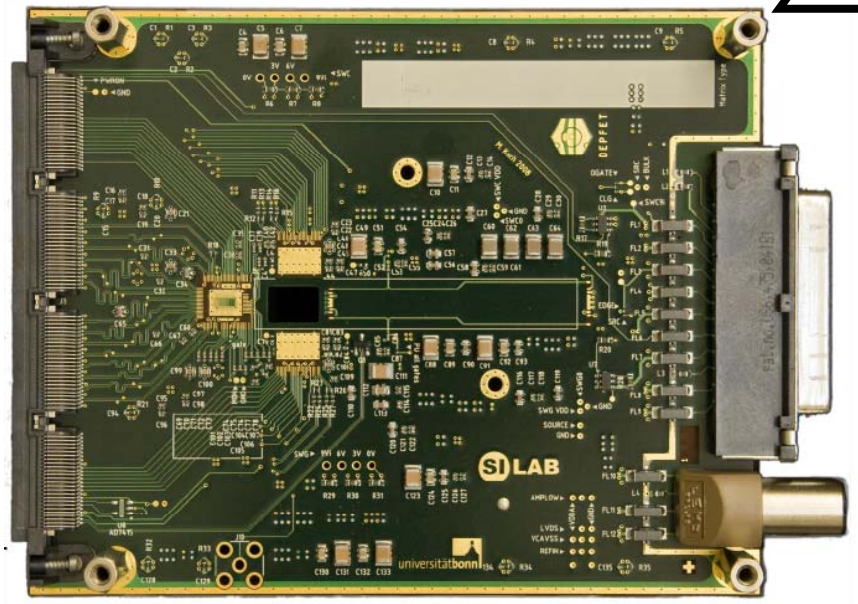


- Sensor + DCD + DHP → MultiChipModule (Ladder)

DEPFET Ladder



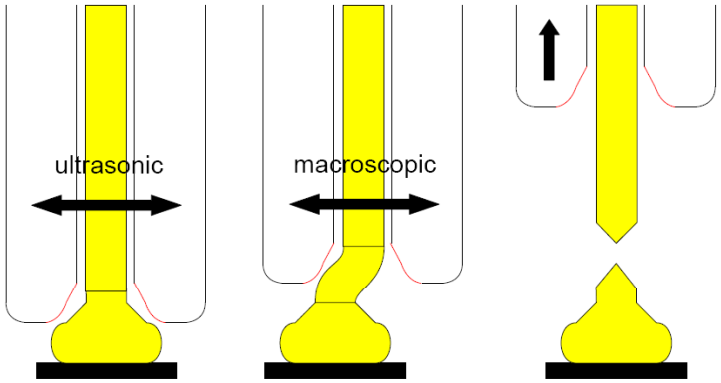
New DCD Hybrid (10 layers!!)

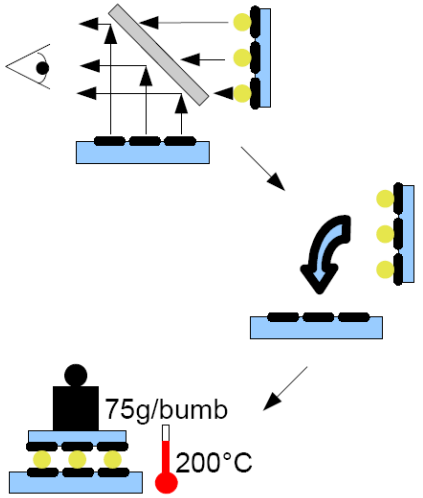


+

DCD full speed r/o system

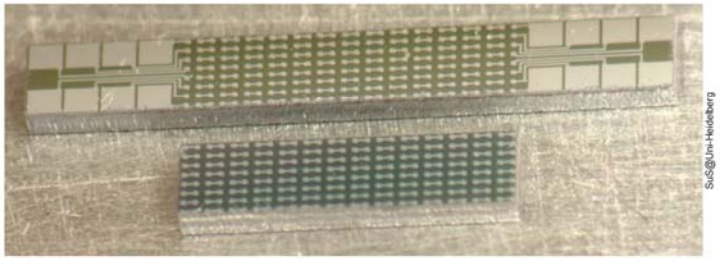
Baseline: Gold Stud Bump Bonding



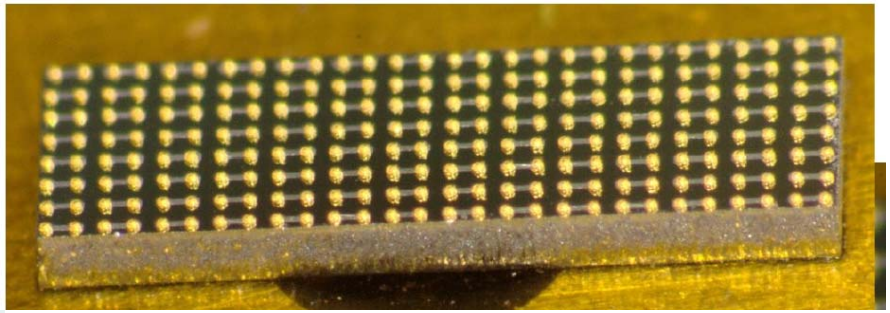


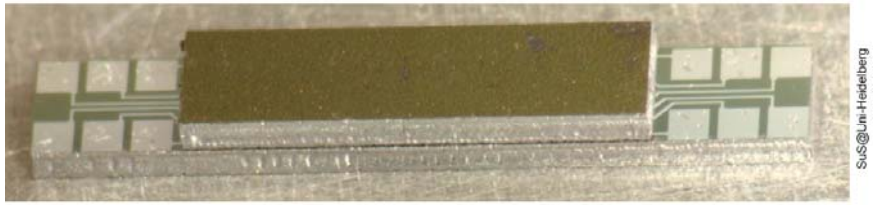
- Capillary presses ball onto Al-bondpad and forms bump
- Ultrasonic to get Au-Al interconnection
- Weakening of wire for break point near the bump
- Pull up capillary, clamp and rip off wire to get tail for next flame-off

21.03.2006 Christian Kreidl LS Schaltungstechnik & Simulation Uni-Mannheim, Germany

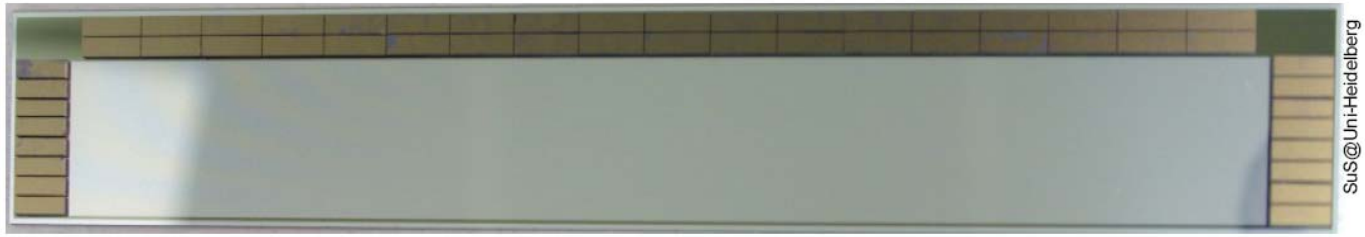


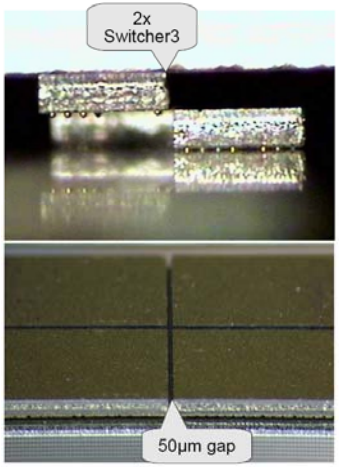
DCD dummy chip and substrate
224 pads



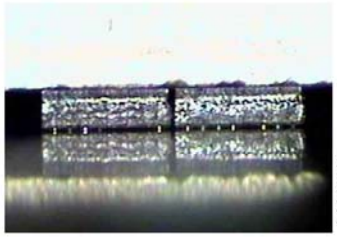


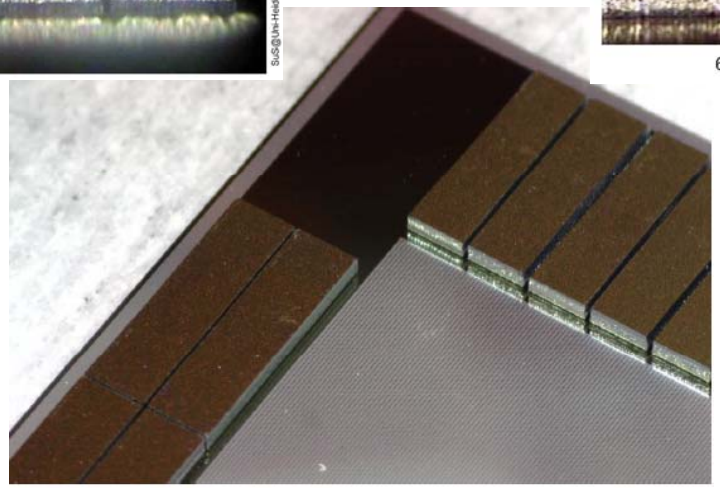
Baseline: Gold Stud Bump Bonding



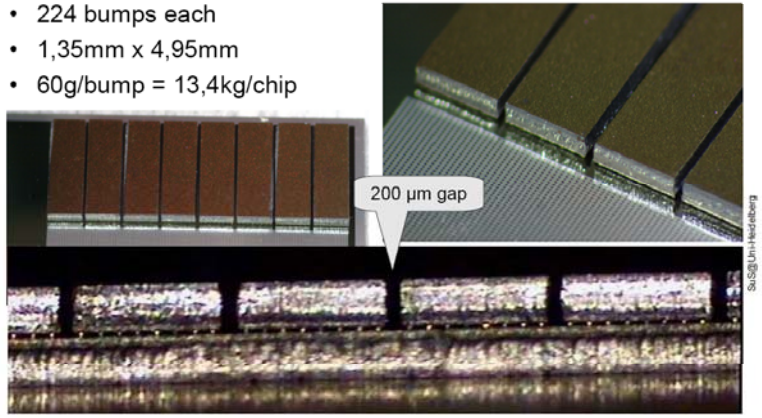


- 36 Switcher3 successfully flipped
- 164 bumps each
- 60g/bump = 9,8kg/chip
- 1,4mm x 5,8mm





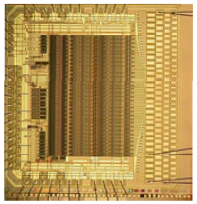
- 16 DCD successfully flipped
- 224 bumps each
- 1,35mm x 4,95mm
- 60g/bump = 13,4kg/chip



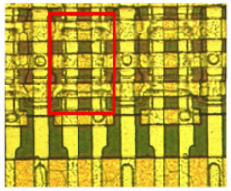
6 of 8 DCDs on the short balcony of one end of the ILC module

The next steps....

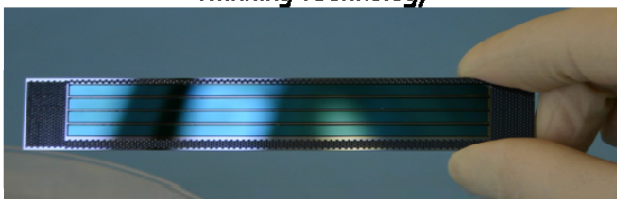
✓ steering chips Switcher



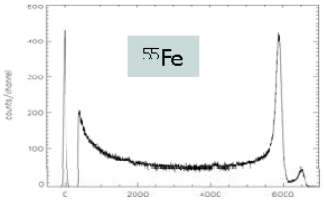
✓ sensor development

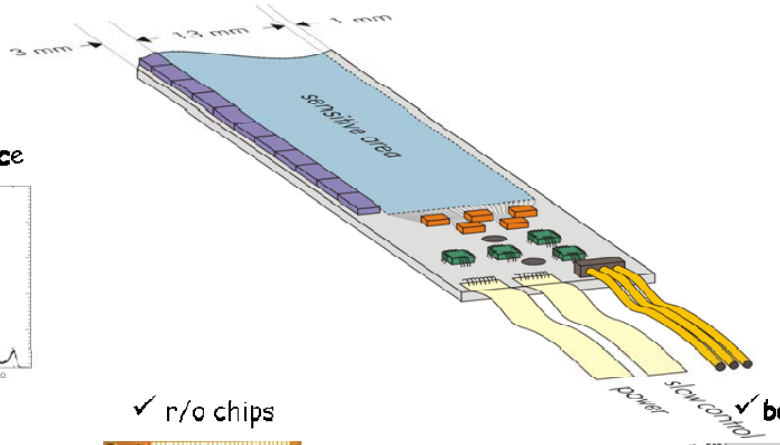


✓ thinning technology

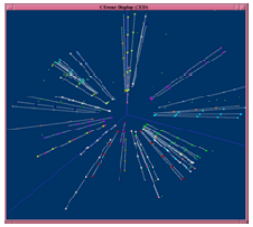


✓ radiation tolerance

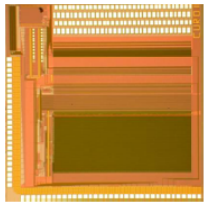




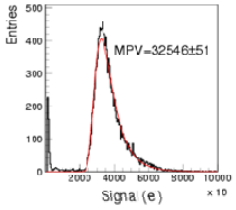
✓ Simulation



✓ r/o chips



✓ beam test



See DEPFET Backup Document at www.depfet.org

Many years of R&D for the ILC VXD (see review fall 2007)

→The DEPFET is ready to be used in precision vertex detectors

Super-B Factory at KEK

(Masa Yamauchi, Spring 2008)

mpi halbleiterlabor

KEKB Upgrade Plan : Super-B Factory at KEK

- *Asymmetric energy e^+e^- collider at E_{CM}=m(ϒ(4S)) to be realized by upgrading the existing KEKB collider.*

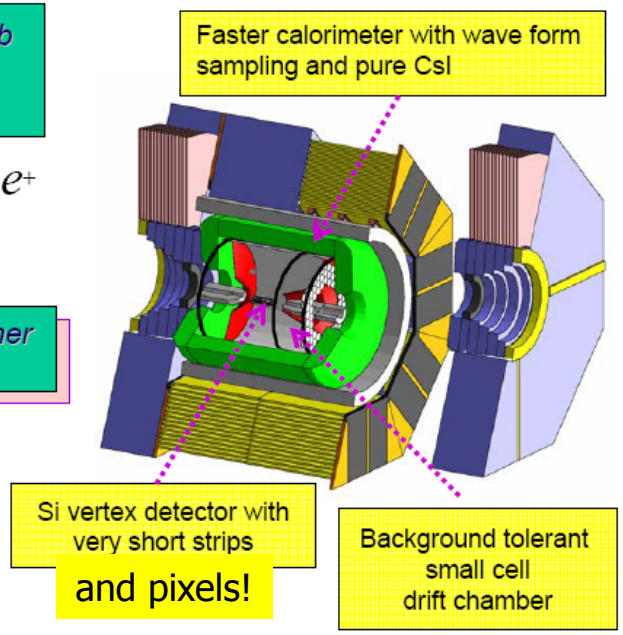
~2012

- *Initial target:* *10 × higher luminosity* ≅ $2\times10^{35}/cm^2/sec$
  → 2×10^9 *BB and* $\tau^+\tau^-$ *per yr.*

~202X

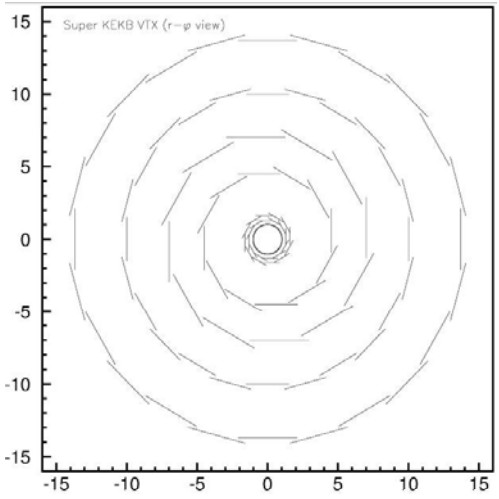
- *Final goal:* $L=8\times10^{35}/cm^2/sec$ *and* $\int L\,dt = 50\ ab^{-1}$

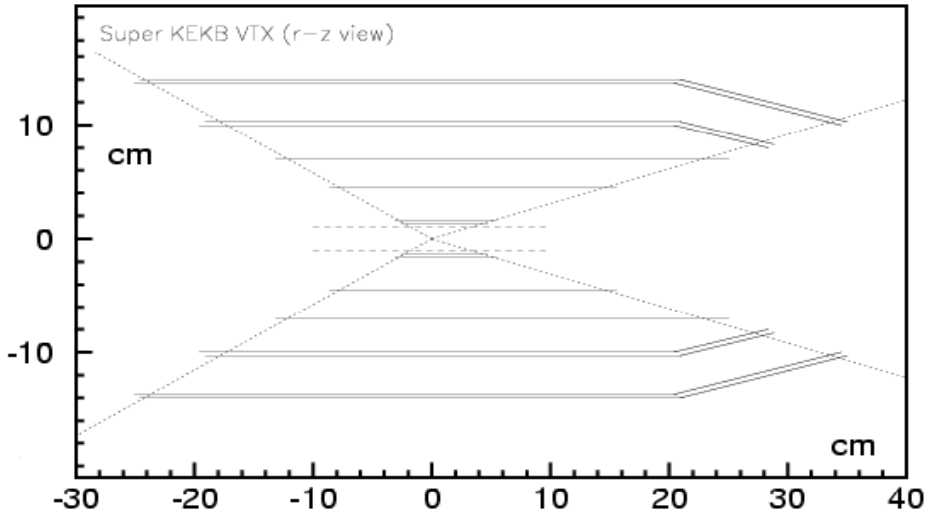
Belle with improved rate immunity

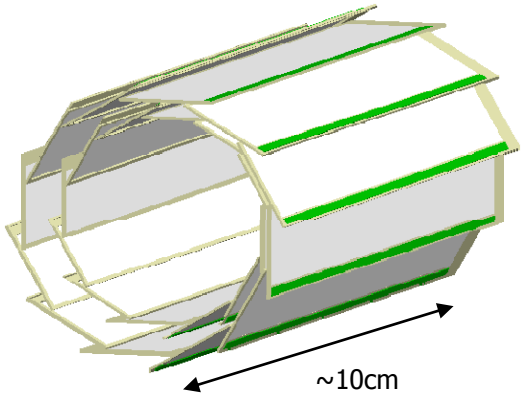


The Vertex Detector at SuperBelle (LoI Layout)

-: 2 thin pixel layers at 1.3 cm and 1.6 cm (subject to optimization)
-: 4 layers with double sided Si-strip detectors
-: Angular coverage 17°<θ < 150°, slanted at the end







From ILC to superKEKB → Pixel Size

Super KEKB is more challenging than ILC

	ILC	super KEKB
Occupancy	0.1..0.2 hits/μm^2/sec	0.4 hits/μm^2/sec (initial)
Radiation	<100 kRad/year	> 1 Mrad/year
Duty Factor	1/200	~1

ILC needs excellent IP resolution over a large momentum range:

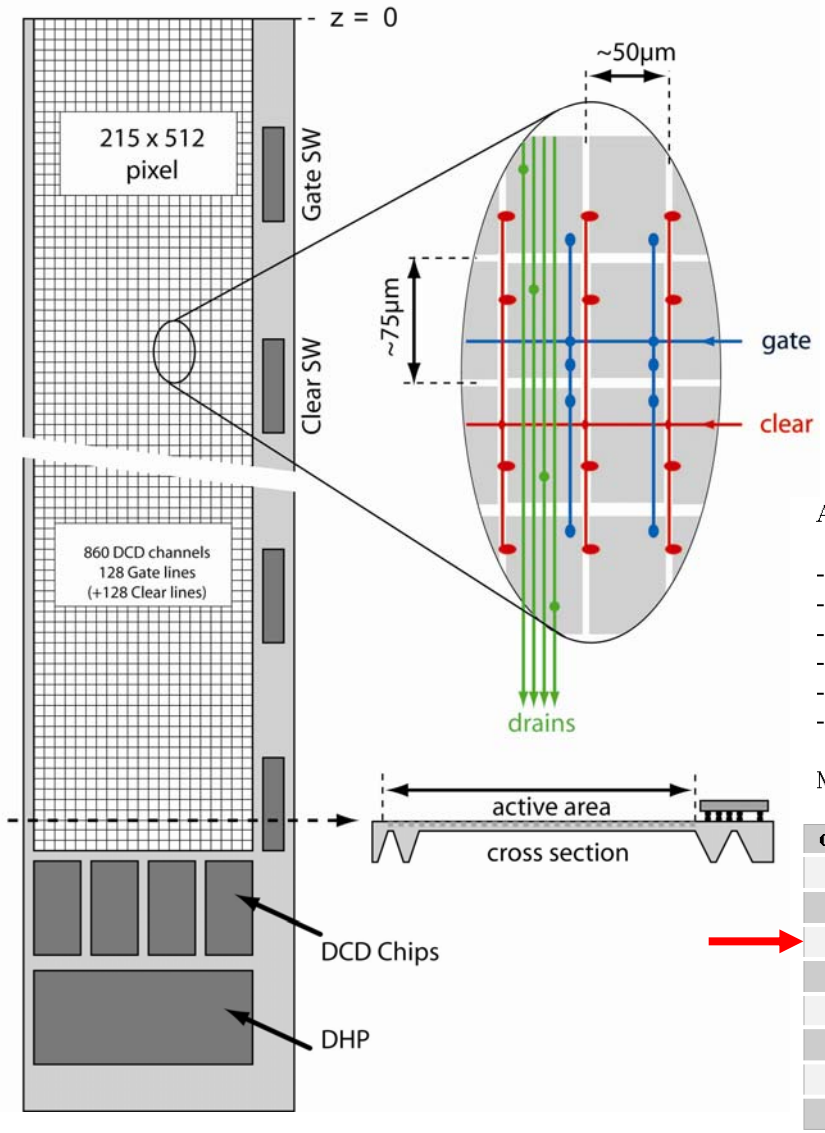
-: Low material → thin ladders down to the very forward region
-: Good single point resolution (σ = 3..5 μm) → small pixels (24μm)

superKEKB is dominated by low momentum tracks (< 1GeV/c):

-: Low material!!!
-: but IP resolution always dominated by MS error (beampipe & 0.14%X_0 Si →~ 9 μm at 1 GeV/c

→ Modest intrinsic resolution of σ ~ 10 μm sufficient: pixels could be larger

ILC VXD → SuperBelle PXD



Some important numbers for the baseline layout:

four-fold read out : frame rate 100 kHz, 80ns/row

sensitive region : 1.15x7.25 cm^2 (L1), 1.15x9.26 cm^2 (L2)

material budget : 0.15% X_0 (incl. frame, chips, bumps)

power/module : DEPFETs ~ 0.5 W

Switcher ~ 0.2 W

DCD ~ 3 W on each ladder end

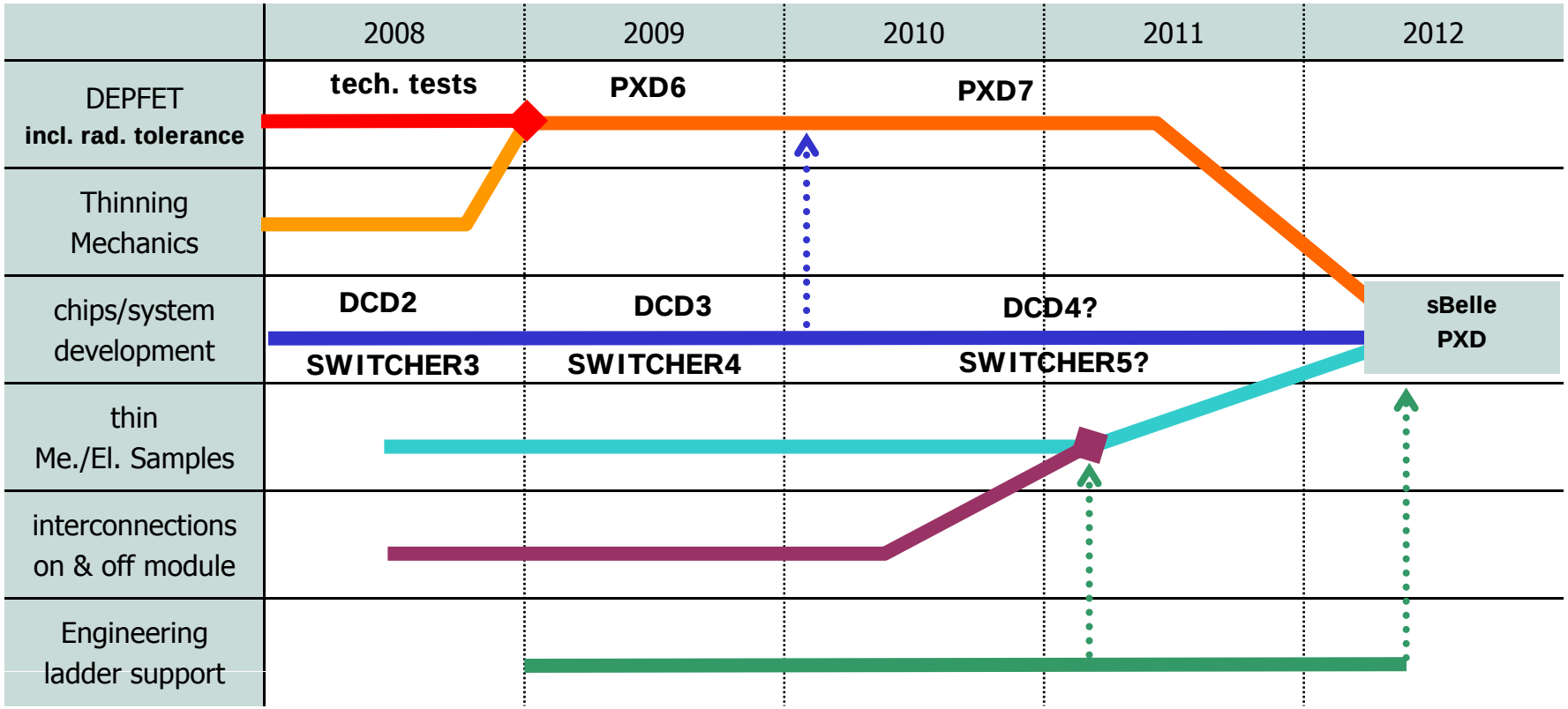
Assumptions:

-: sensitive area of the first layer ladder: 1.15x7.25 cm^2
-: support frame: 0.1+0.2 cm
-: Switcher-Sensor Interconnect: Gold stud bumps, one bump/side, Φ=48 µm
-: Switcher dimensions: 0.14x0.2 cm^2
-: Number of Switchers: 16 (16x2 channels per chip – gate and clear)
-: Material reduction by frame etching: 1/3

Material is averaged over sensitive area!

option	Sens. Thickness (µm)	Sw. Thickness (µm)	Frame thickness	%X_0
1	50	500	450	0.17
2	50	500	300	0.14
3	50	200	450	0.15
4	50	200	300	0.12
5	75	500	450	0.2
6	75	500	300	0.17
7	75	200	450	0.18
8	75	200	300	0.15

....towards sBelle ladders



- ✓ ASIC production: UMC, AMS, IBM, TSMC.... use the best available process
- ✓ DEPFET prototyping and series production of the sensors at the MPI Halbleiterlabor

Summary

-: Tests of the latest DEPFET production are in full swing. We are looking forward to see the new features like capacitive coupling of the clear gate and shorter gate lengths in next year's test beam!

-: The DEPFET is ready to be used as a high precision vertex detector at SuperBelle. This Project will certainly boost the R&D for ILC DEPFETs. The next production (PXD6) will start January 2009 → the first **thin DEPFETs** for SuperBelle **and ILC**!