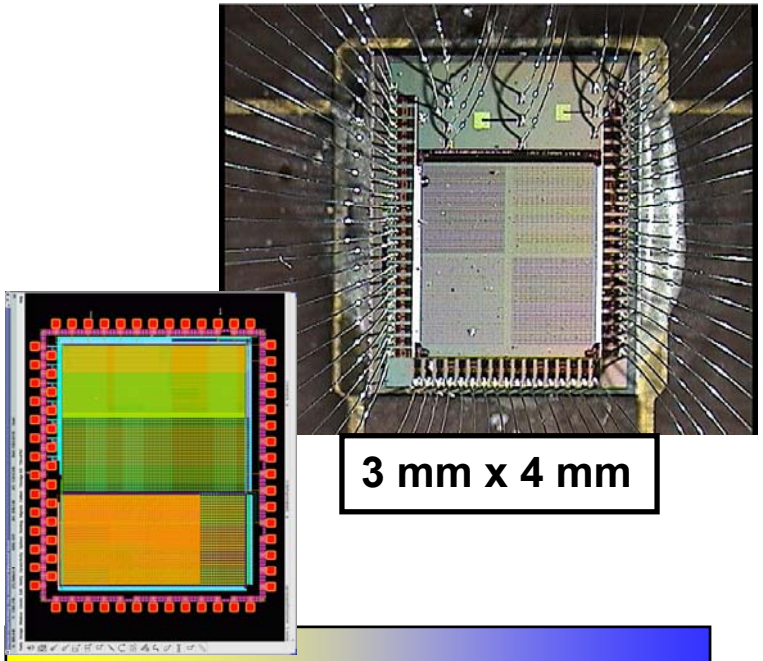
Mimoroma2 MAPS chip: all NMOS on pixel sparsification architecture (LCWS08, November 2008)

Eleuterio Spiriti (INFN RomaTre)

1. **Our (RomeTre group) experience on MAPS**
   - **Mimoroma1 chip: brief description**
2. **The Mimoroma2 sensor**
   - **Main goals and constrains**
   - **Proposed ladder readout and Pixel architecture**
   - **Test set up**
   - **Mimoroma2 sensor radioactive sources test results**
   - **Mimoroma2 sensor simulation and threshold spread measurements**
3. **3D implementation of the proposed sparsified architecture**
   - **Tezzaron/Chartered 3D implementation, supported by the INFN P-ILC/VIPIX projects (FNAL-IN2P3-INFN collaboration)**
4. **Conclusions**

Our (short) experience on MAPS at RomeTre INFN group

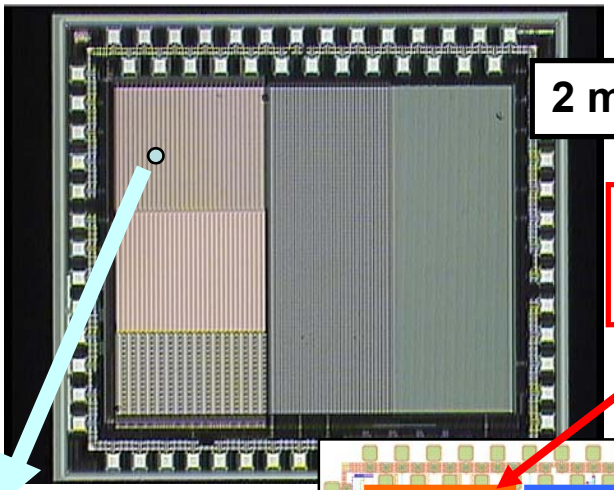
Chip mimoroma1
(TSMC 250nm technology)



3 mm x 4 mm

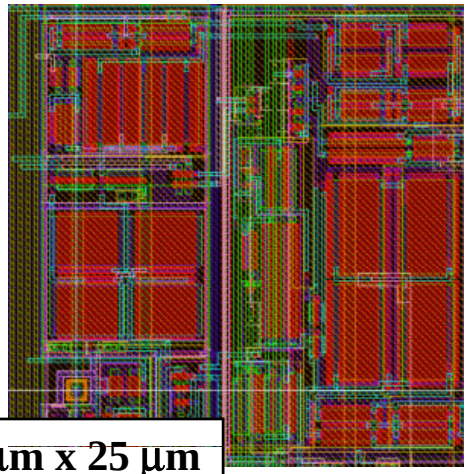
mimoroma1 chip
(first MAPS designed at
INFN RomaTre)

Chip mimoroma2
(STMicroelectronics 130nm technology)

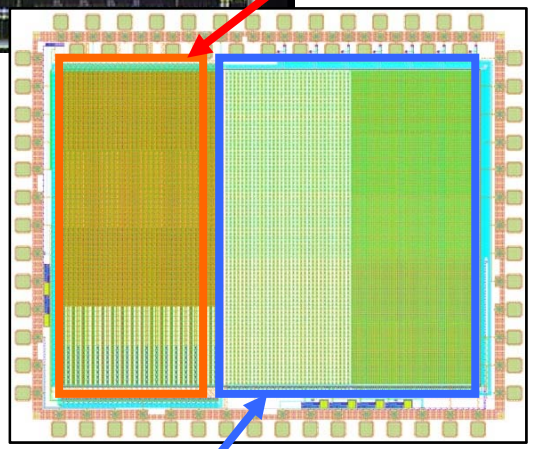


2 mm x 3 mm

Sparsified side



25 µm x 25 µm



Non sparsified side

Basic motivation for the proposed sparsified architecture

• Physics
• Machine background

MAPS are matching the requirements for an ILC vertex?
- Spatial resolution
- Efficiency
- Thickness
- Readout speed?

Occupancy = ~1%

Why reading all pixels?

sparsification (reading hitted pixel only)

One possible approach: end of column sparsification!

Mimoroma architecture (**possible?)** solution:
On pixel sparsification with analog signal readout using "standard" MAPS sensing diode (no deep NWELL)

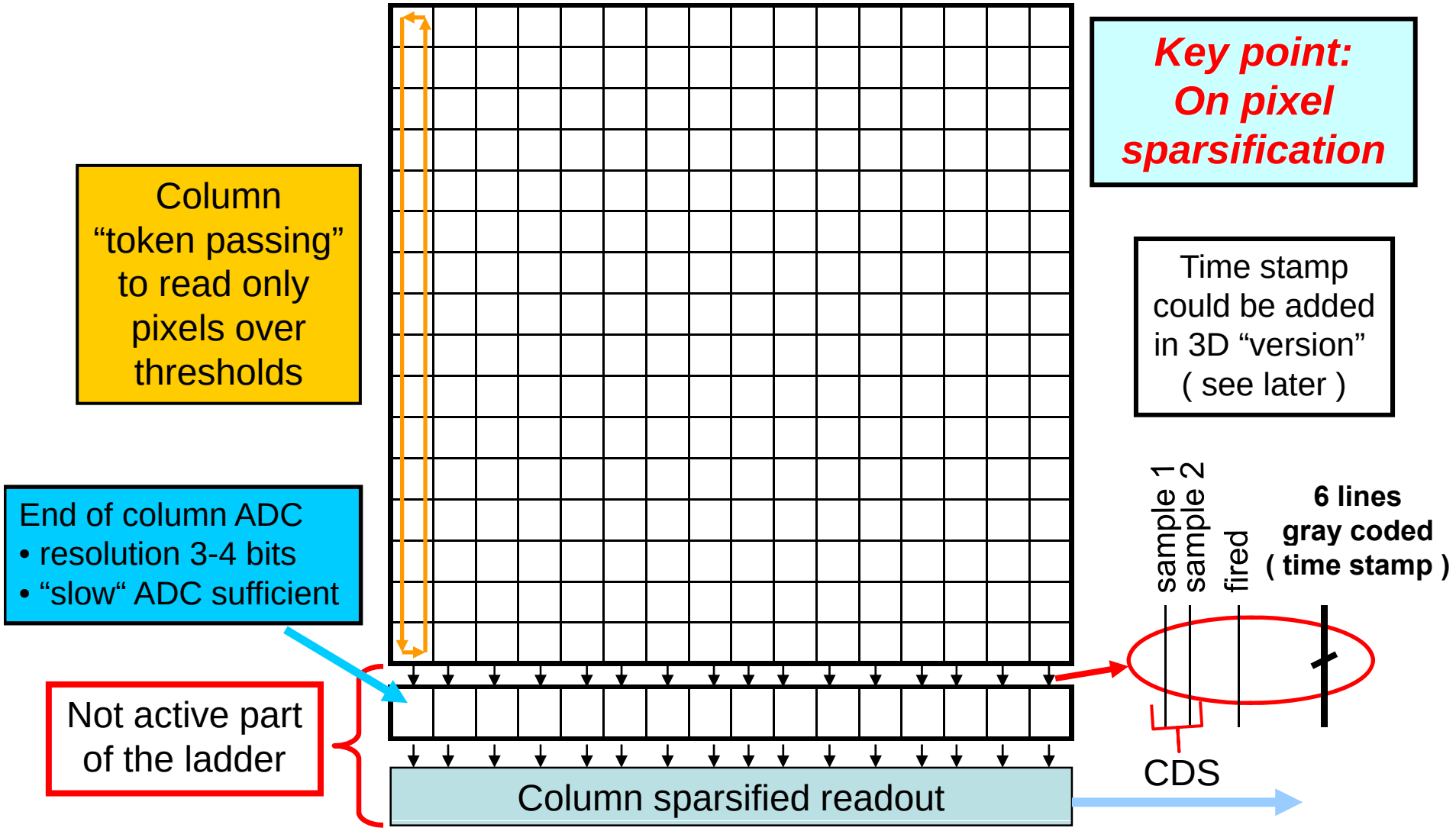
Main constrains:
- No competing NWELL
- limited available area

J. Mlynarczyk, E. Spiriti, A. Bulgheroni, "Design of a monolithic active pixel sensor in ST 0.13um technology," *Proceedings of the 10th ICATPP Conference*, World Scientific , pp. 999-1003, Oct. 2007.

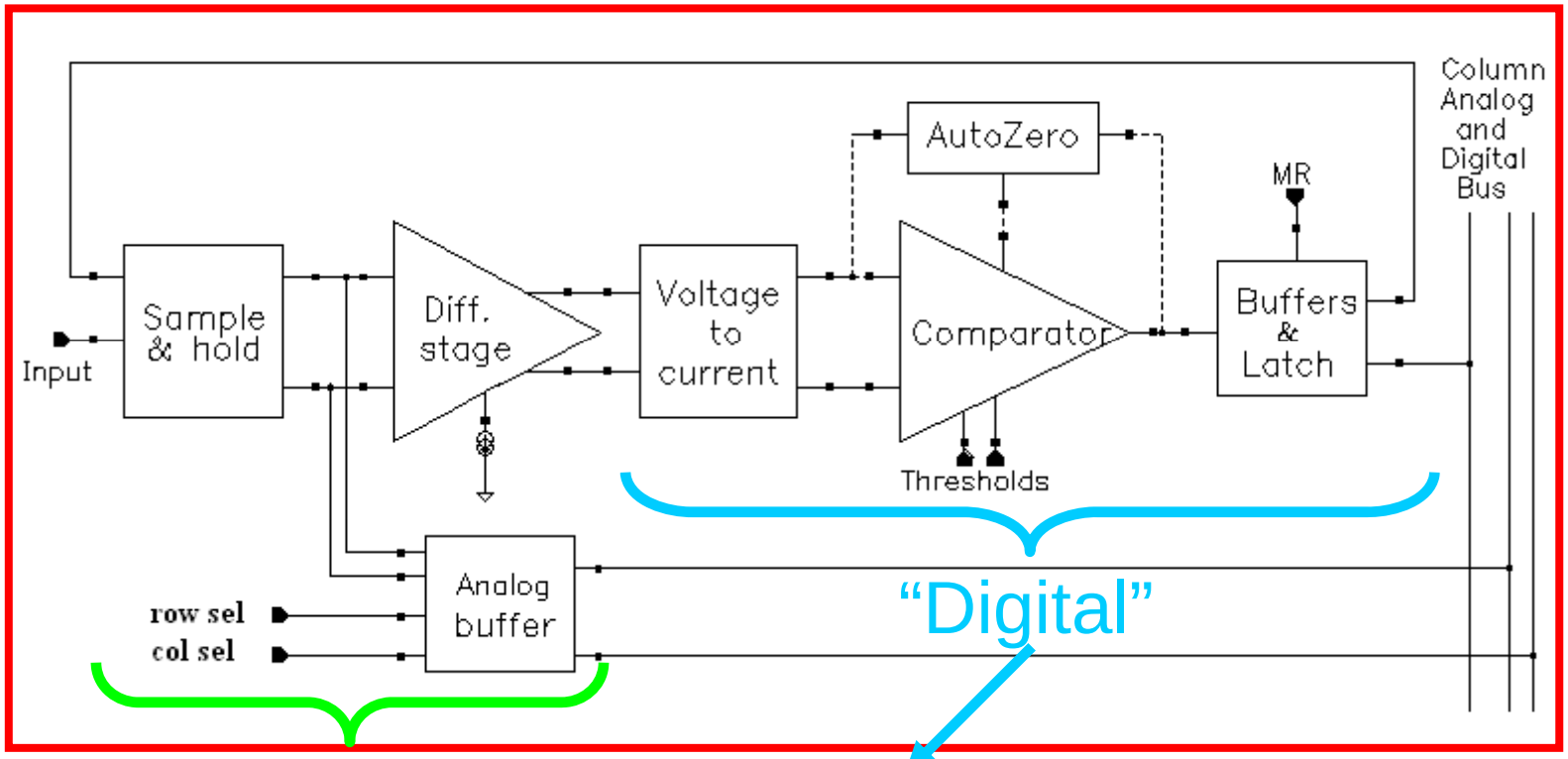
J. Mlynarczyk, E. Spiriti, "On pixel signal processing for MAPS sparsified readout implemented in CMOS VLSI technology," *Proceedings of the ICSES'08* (International Conference on Signals and Electronic Systems), Sep. 2008.

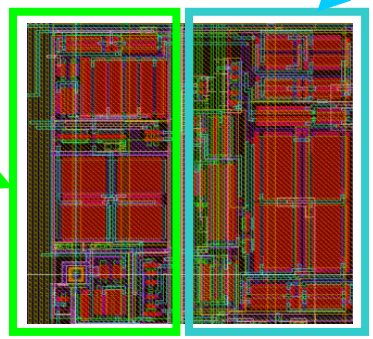
E. Spiriti, J. Mlynarczyk, "Results of an on Pixel sparsification architecture in a Maps test chip in STM 130nm technology," *Proceedings of the IEEE-NSS'08*, Oct. 2008.

Overall ladder possible readout architecture



Sparsified pixel architecture





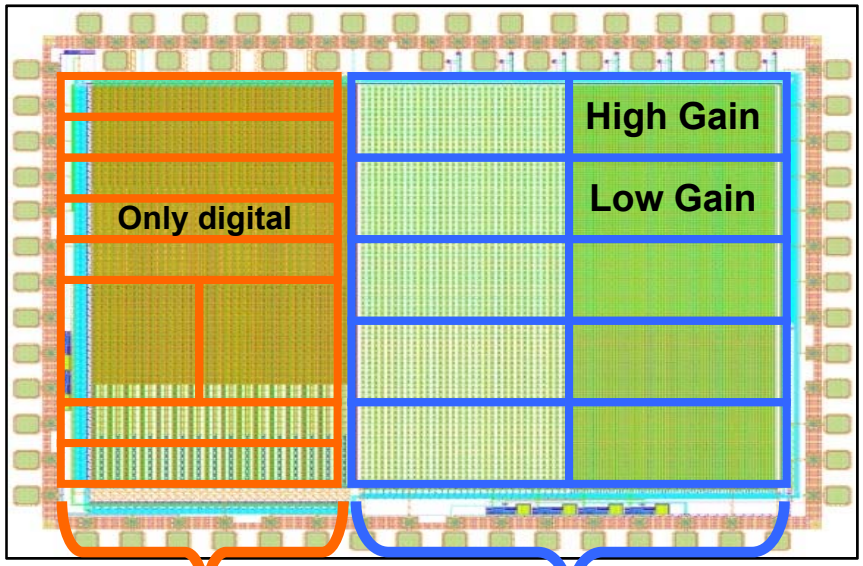
- **Only NMOS used in the Pixel**
- **Pixel area 25 µm x 25 µm**

Mimoroma2 chip: main goals and constrains

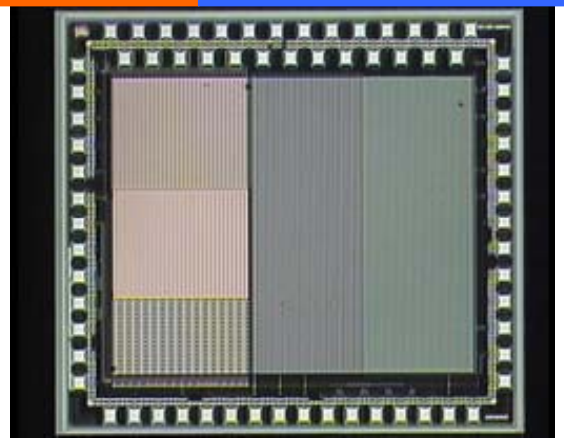
- Characterization of the signal (epitaxial thickness and quality) level provided by the STM 0.13 μm technology
- Implementation of an on-pixel sparsification architecture test structures (different sub-blocks)

1. **Only NMOS transistors: no competing n-wells**
2. **Small available area (pitch 20-25 μm)**
3. **Common threshold for all pixels in a chip**
4. **Threshold voltage and curren mismatch in submicron CMOS**
5. **Noise:**
   - ❑ **Temporal noise**
   - ❑ **White and 1/f noise**
   - ❑ **Charge injection**
   - ❑ **Digital to analog cross-talk**

Mimoroma2 chip layout



8 sparsified | 10 non sparsified



Different parameters for the non sparsified part of the chip

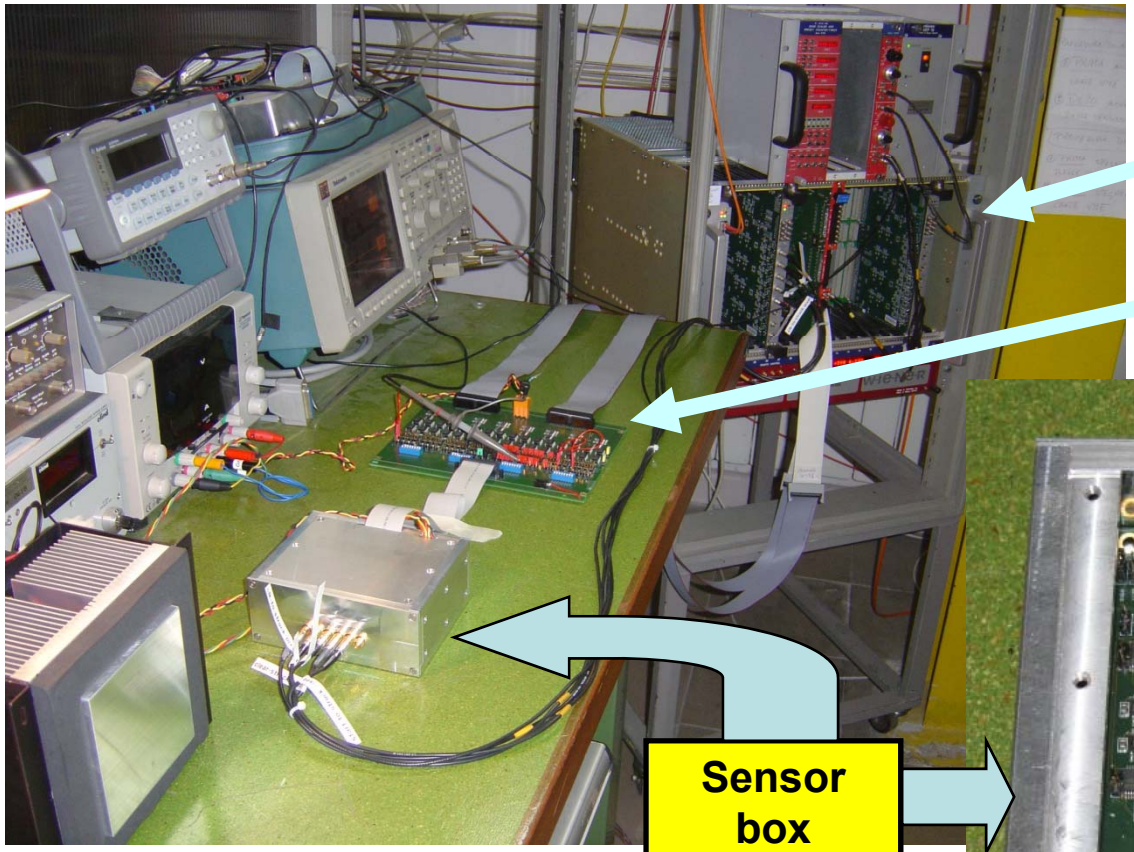
- ✓ **Five 32x16 pixels arrays with 20x20 µm size**
- ✓ **Five 64x32 pixels arrays with 10x10 µm size**

Parameter	Value 1	Value 2
Pixel structure	3T	SB
Pitch	20 µm	10 µm
Diode dimension	1 µm x 1 µm	1.5 µm x 1.5 µm
SF transistor size	Small gain	Large gain
Power supply	2.5 V	1.2 V

8 sparsified pixel subarray

two 8x32 pixel arrays (1.2V,2.5V) only analog part
two 16x16 pixel arrays (1.2V,2.5V) without autozero
two 8x32 pixel arrays (1.2V,2.5V) only digital part
one 8x32 pixel arrays only digital part with autozero
one 8x32 pixel arrays complete pixel with autozero

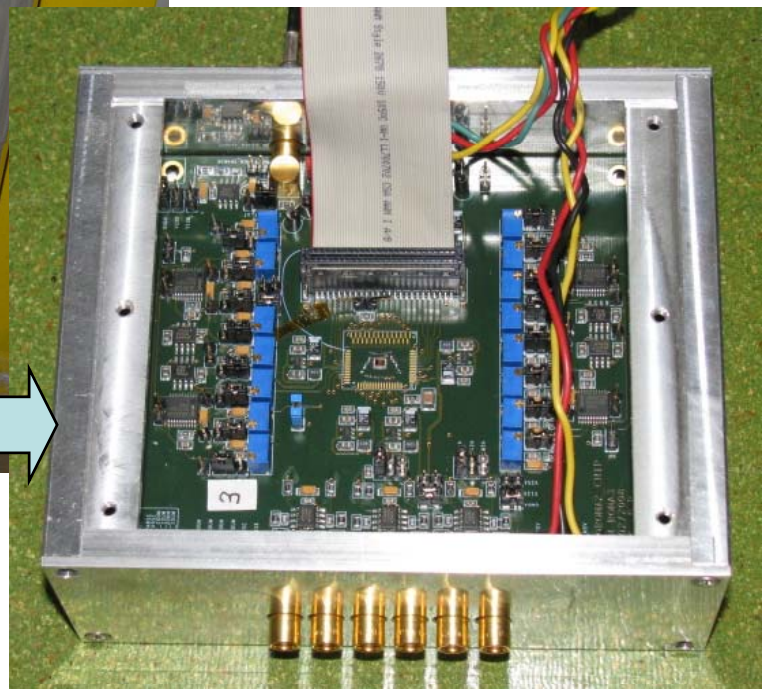
Mimoroma2 laboratory test set-up



VME DAQ crate

Digital signal adapter card

Sensor box

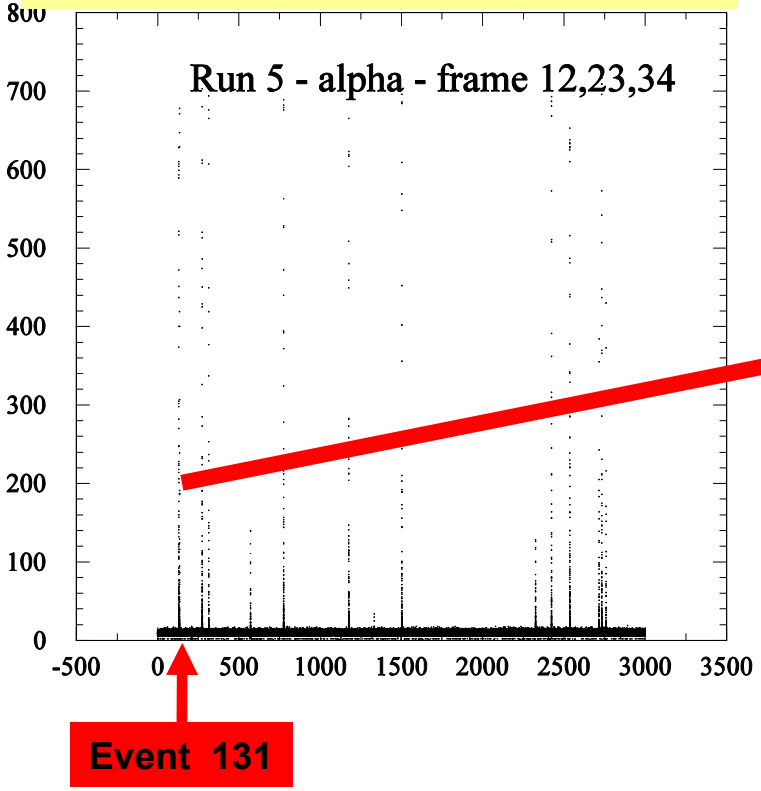


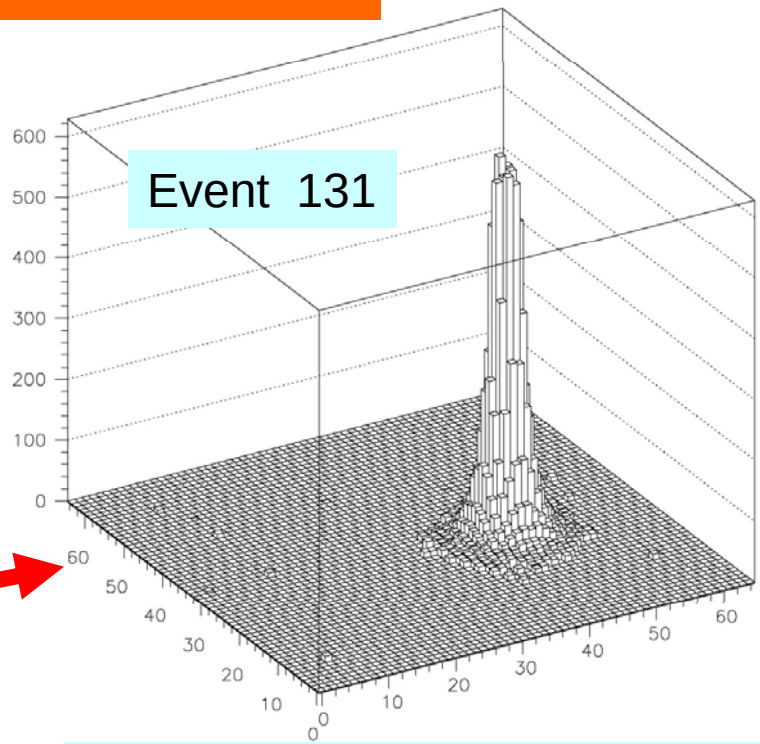
- SIS (Struck Innovative Systeme) SIS3300 8 Channel 100 MHz 12-bit ADC: to acquire the seven (six analog plus one digital) output signals
- V1495 General Purpose VME Board (CAEN): internal FPGA produce the 32 needed digital control signals.

Non sparsified pixel arrays alpha radioactive source measurements

To check the overall system correctness!

Number of pixels over threshold per event number





Alpha particle cluster on the two (32x64 pixels each) high/low gain non sparsified 10um pitch arrays.

Non sparsified pixel arrays CCE (Charge Collection Efficiency) measurements

^{90}Sr ➡ Maximum @ 24 pixels sum

MIP ➡ Maximum @ 13 pixels sum

Qualitative results for test beam!!!

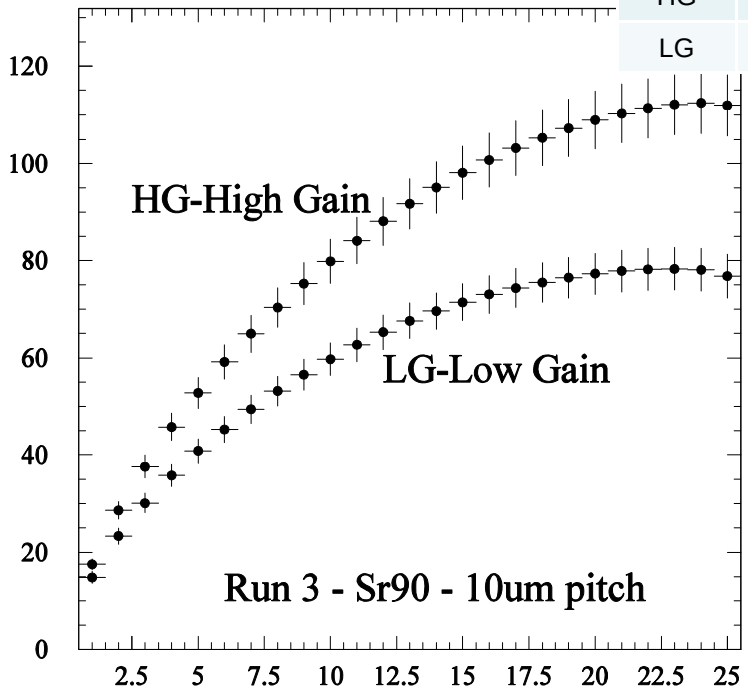
Based on a preliminary run (accelerator fault).

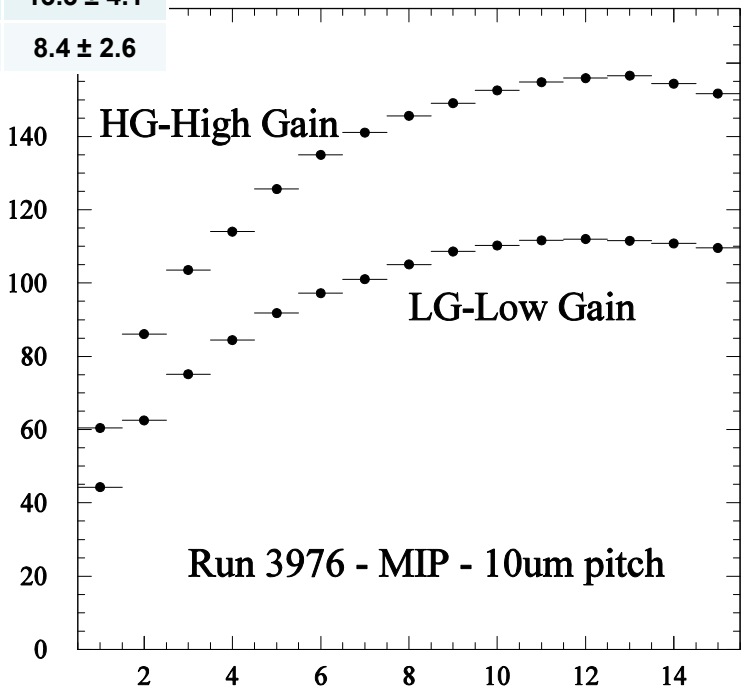
- noise ~ ten times the lab one
- missing synchronization with the telescope

Test beam data: 120GeV pions at the Cern beam, line H6B on the EUDET telescope.

^{90}Sr (beta source) lab test

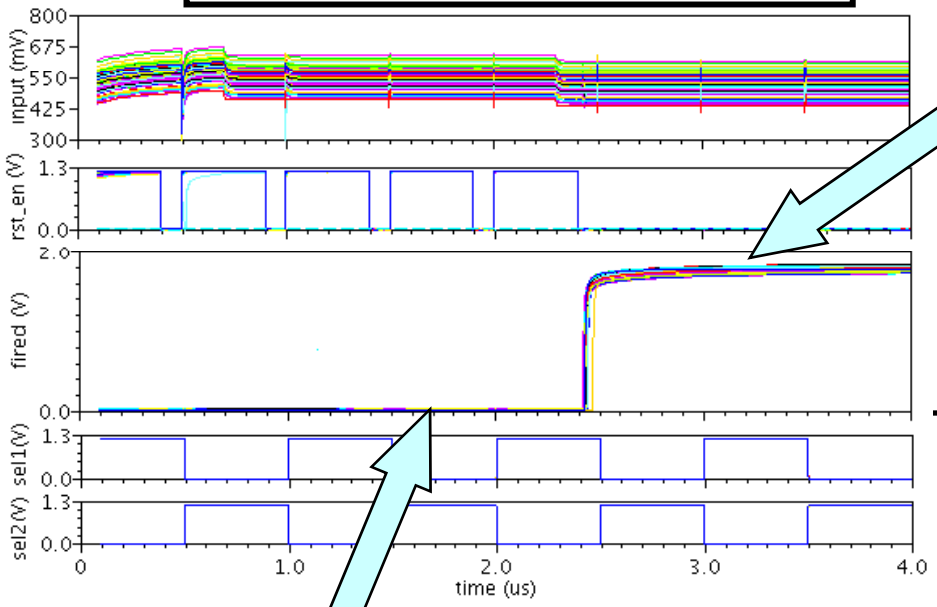
Noise	^{90}Sr	MIP
HG	1.5 ± 0.2	13.3 ± 4.1
LG	1.3 ± 0.5	8.4 ± 2.6





Simulation of the sparsified pixel

Montecarlo simulation (100 runs)
process and mismatch included



Digital output HIGH on all pixel:

Simulation → $\Delta V_{in} = 67mV$

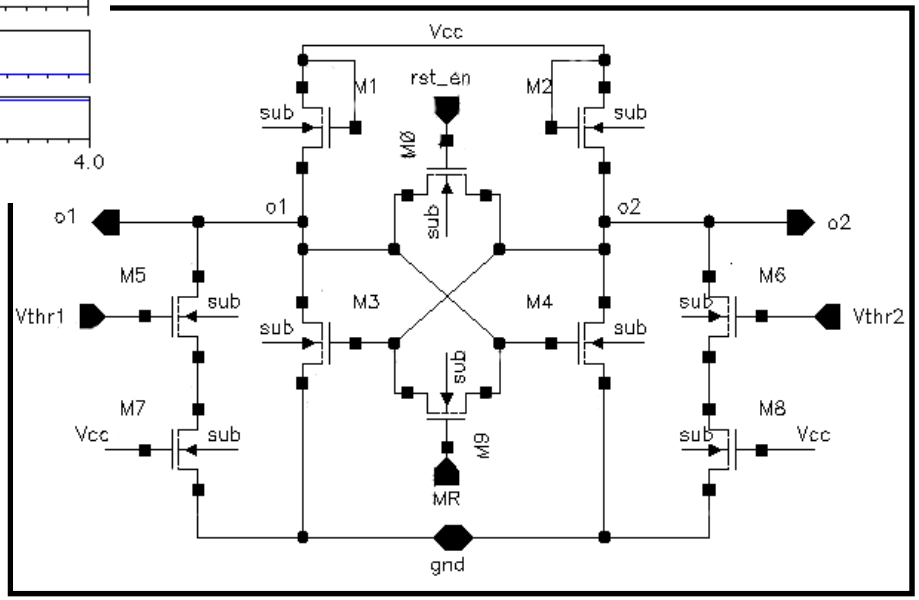
Measurements → $\Delta V_{in} = 47mV$

Digital output LOW on all pixel:

Simulation → $\Delta V_{thr} = 95mV$

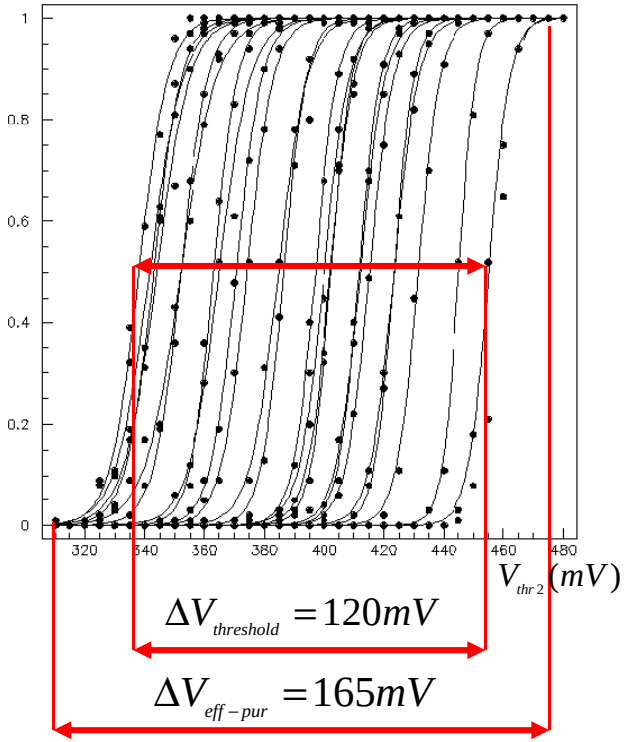
Measurements → $\Delta V_{thr} = 75mV$

The discriminator: the core of the digital part of the sparsified pixel



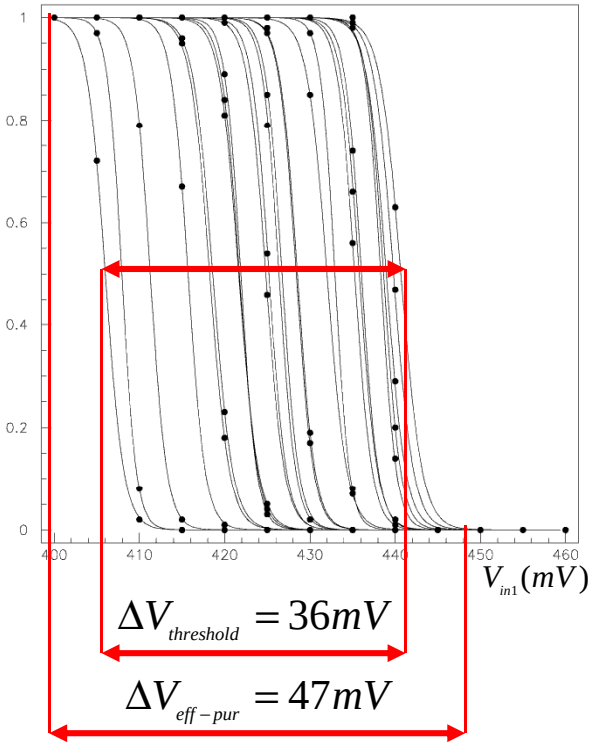
Sparsified pixel digital part threshold dispersion measurements

Threshold scan



Test on 5x5 pixels array. Submatrix only digital.

Input scan



all pixels LOW → $V_{thr2} = 475mV$

all pixels HIGH → $V_{thr2} = 310mV$

$V_{thr1} = 400mV$

$V_{in2} = V_{in2} = 400mV$

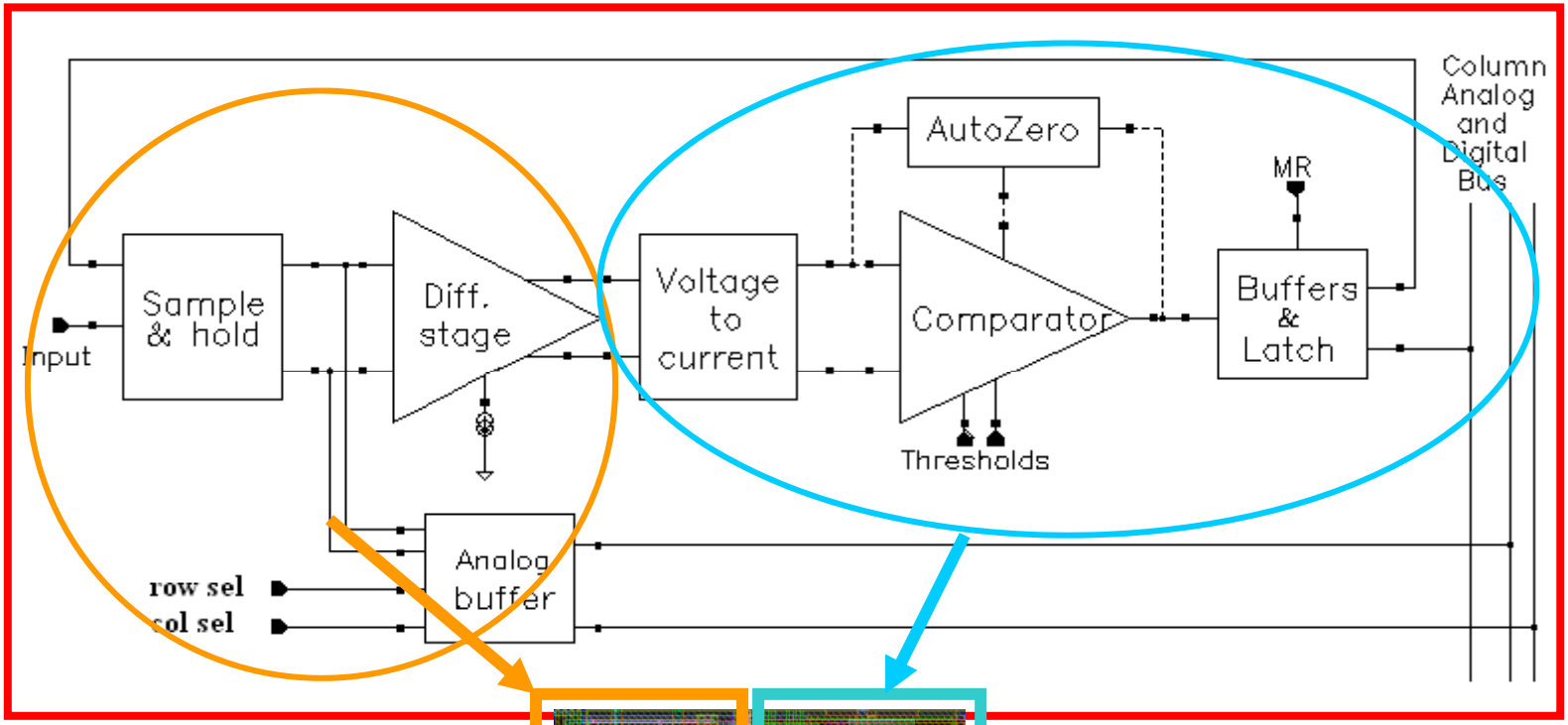
all pixels LOW → $V_{in1} = 400mV$

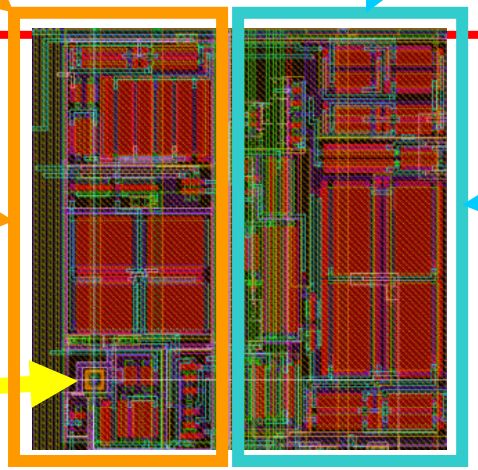
all pixels HIGH → $V_{in1} = 447mV$

$V_{in2} = 400mV$

$V_{thr1} = 400mV, V_{thr2} = 475mV$

Proposed 3D implementation of the sparsified architecture





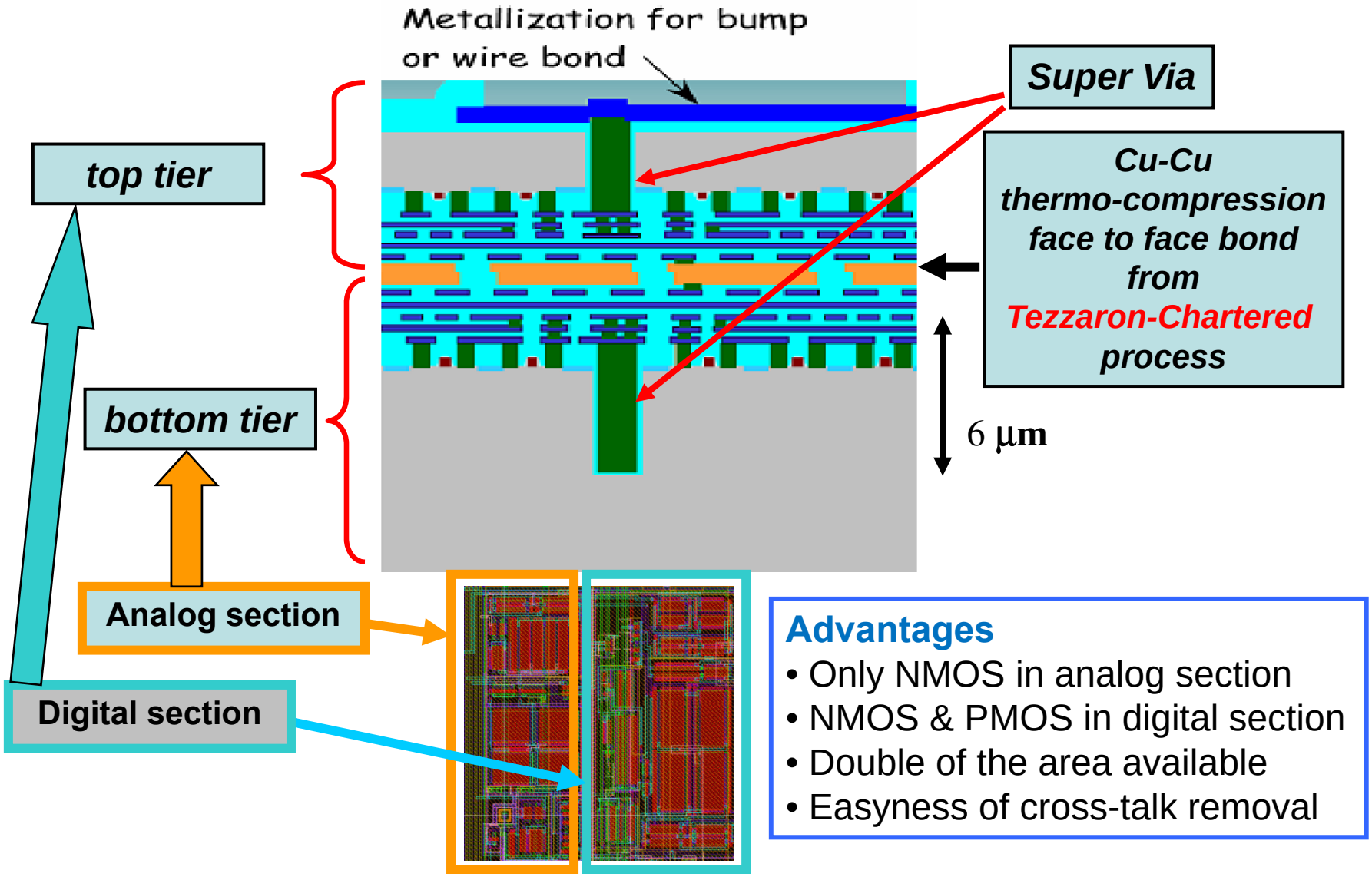
Analog section

Digital section

Sensing diode

Size 25 μm x 25 μm
~ 70 transistors

Proposed 3D implementation of the sparsified architecture



Advantages

- Only NMOS in analog section
- NMOS & PMOS in digital section
- Double of the area available
- Easyness of cross-talk removal

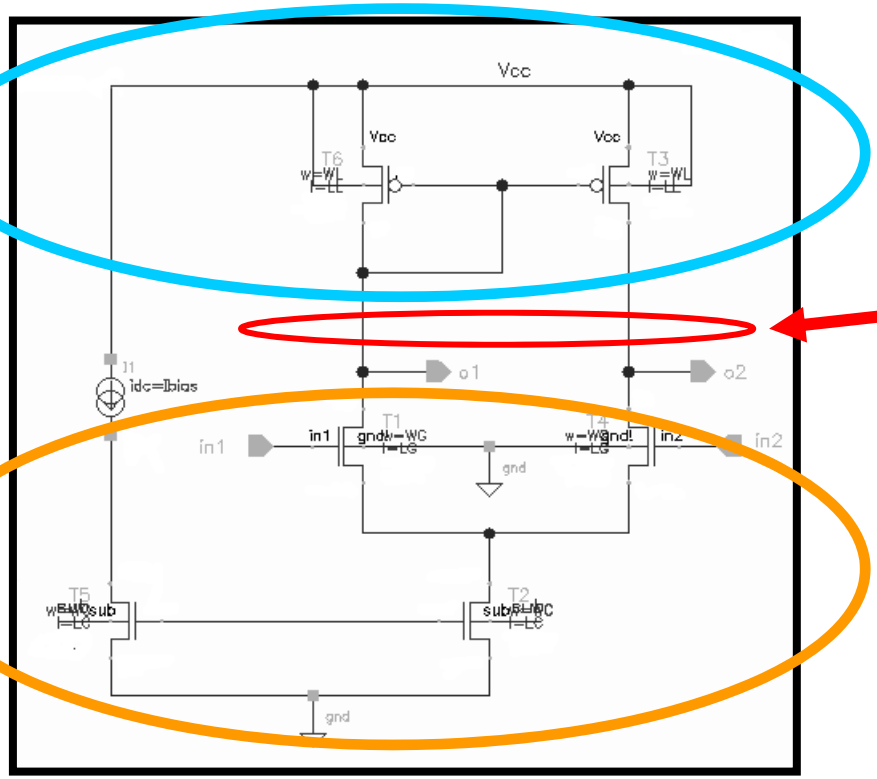
Proposed 3D implementation of the sparsified architecture

A differential stage is used to supply the signals from the sample & hold to the discriminator and the following digital circuitry.

How to possibly split it in a 3D version!

top tier

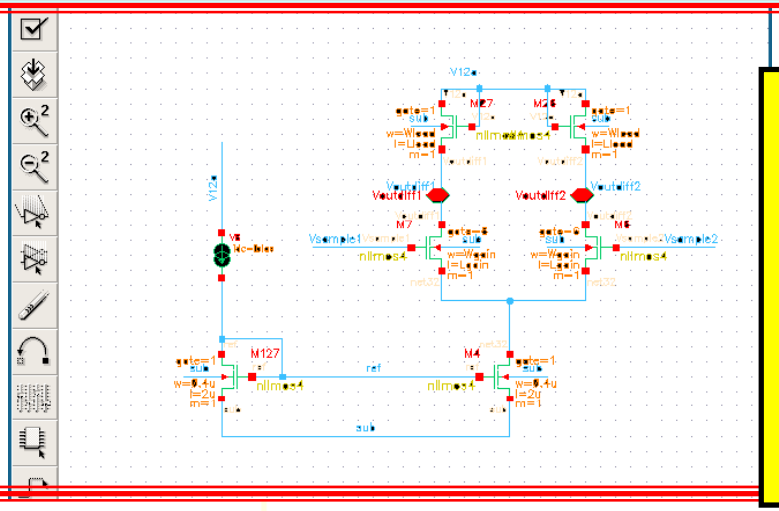
bottom tier



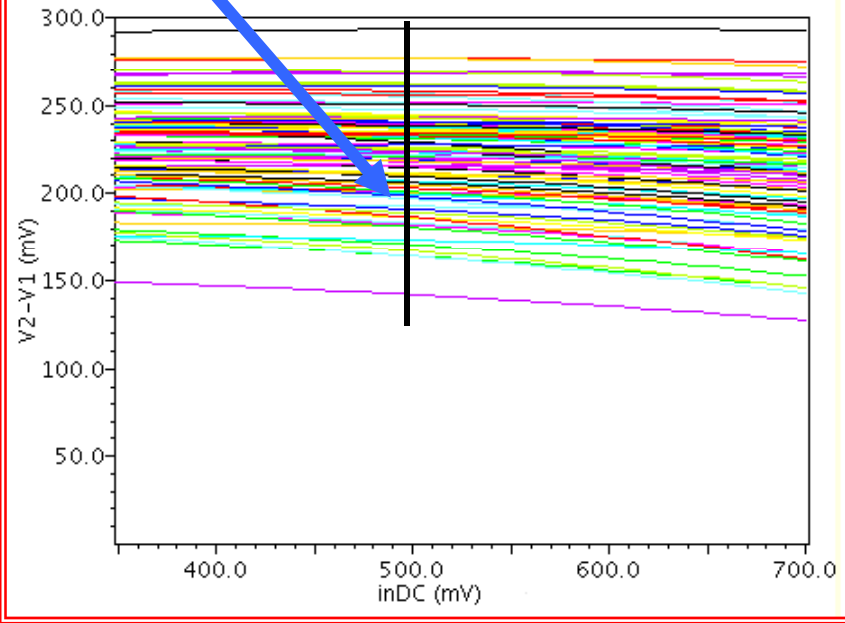
tier1 to tier2 border (2 current signals)

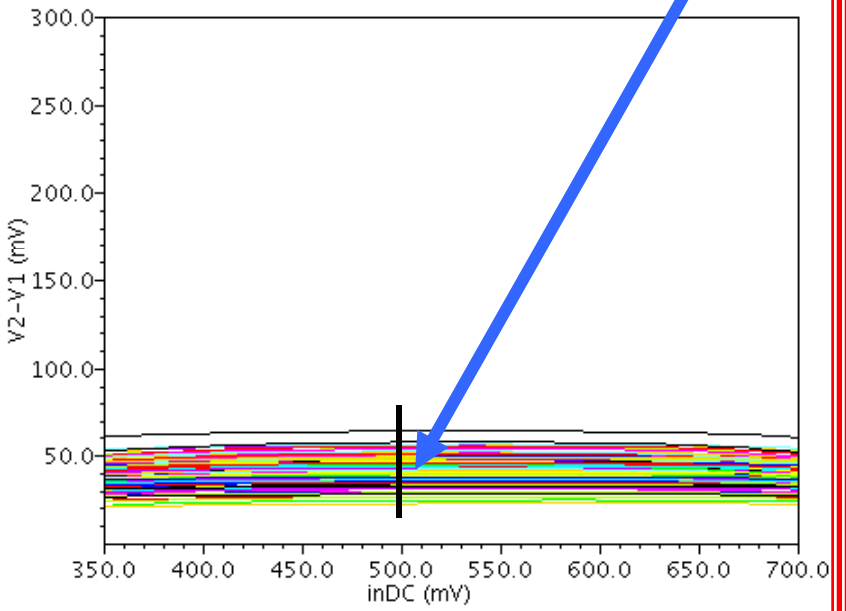
Proposed 3D implementation of the sparsified architecture

Differential stage mismatch spread PMOS & NMOS IBM 8WL 130nm Average=219.6mV RMS=33.4mV Ratio=6.57 (Vin_diff=10mV)



Differential stage mismatch spread only NMOS STM 130nm Average=38.0mV RMS=9.1mV Ratio=4.16 (Vin_diff=10mV)





Conclusions

- **Mimoroma1** was a **tremendously useful exercise** in MAPS design and testing.
- **Key point** to use MAPS to built vertex detectors in new accelerators experiments could be **on-pixel sparsification**.
- First results of the **Mimoroma2 on-pixel signal processing architecture are promising** **(even more than expected).**
- The **autozero correction technique** could be of great help for **threshold spread reduction.**
- 3D solution could **strongly improve the performances**.
- Most of the tests still to be done (second test beam planned).