ILC Instrumentation R&D at SCIPP

ILCWS '08

University of Illinois at Chicago

November 22 2008

Bruce Schumm

Santa Cruz Institute for Particle Physics

The SCIPP/UCSC SiLC/SiD GROUP (Harwdare R&D Participants)

Faculty/Senior	Collaborator	Undergrads
Vitaliy Fadeyev	Rich Partridge	Sean Crosby
Alex Grillo		Jerome Carman
Bruce Schumm		Jared Newmiller
		Ryan Stagg

Lead Engineer: Ned Spencer

Technical Staff: Max Wilder, Forest Martinez-McKinney

All participants are mostly working on other things (BaBar, ATLAS, biophysics…)

Students: undergrad physics and/or engineering majors at UCSC

Recent Areas of Inquiry

ILC-Specific

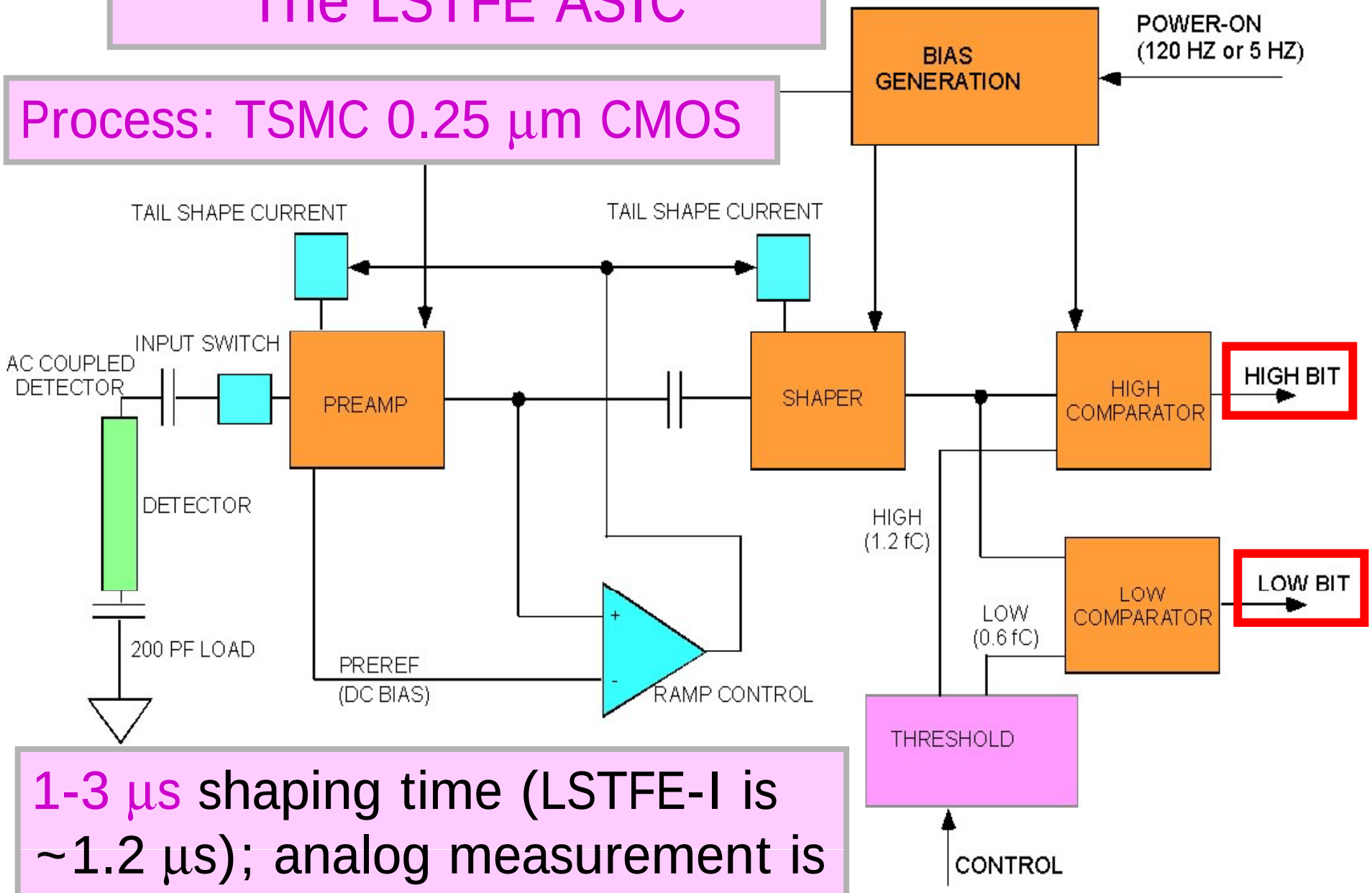
- LSTFE front-end chip development
- SiD sensor testing

Generic

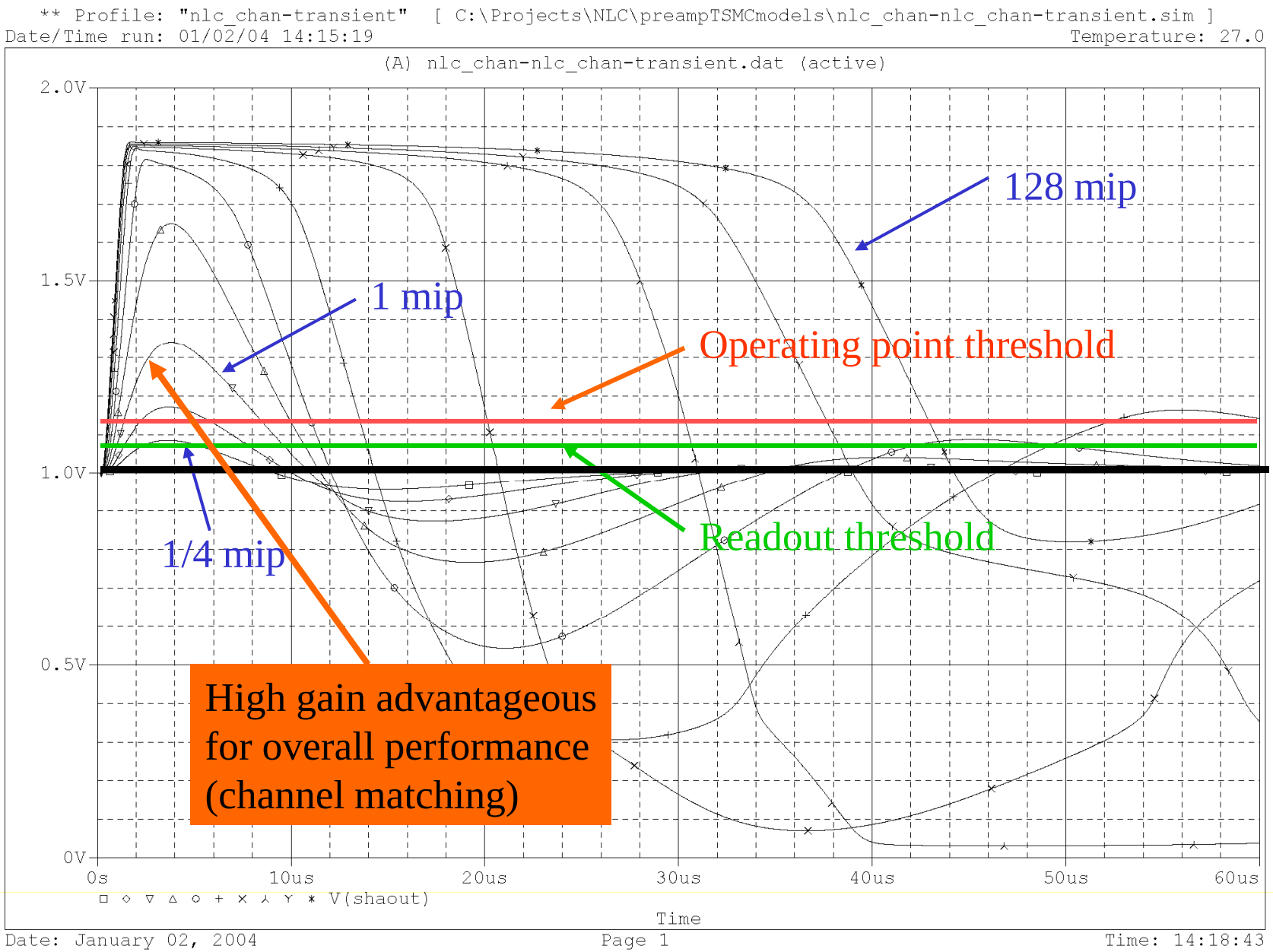
- Charge division and longitudinal resolution
- Noise sources in high-resolution limit

The LSTFE ASIC

Process: TSMC 0.25 μm CMOS



1-3 μs shaping time (LSTFE-I is ~1.2 μs); analog measurement is Time-Over-Threshold


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
V(shaout)
Time
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
High gain advantageous for overall performance (channel matching)
Date: January 02, 2004
Page 1
Time: 14:18:43

EQUIVALENT CAPACITANCE STUDY

Noise vs. Capacitance (at τ_{shape} = 1.2 μs)

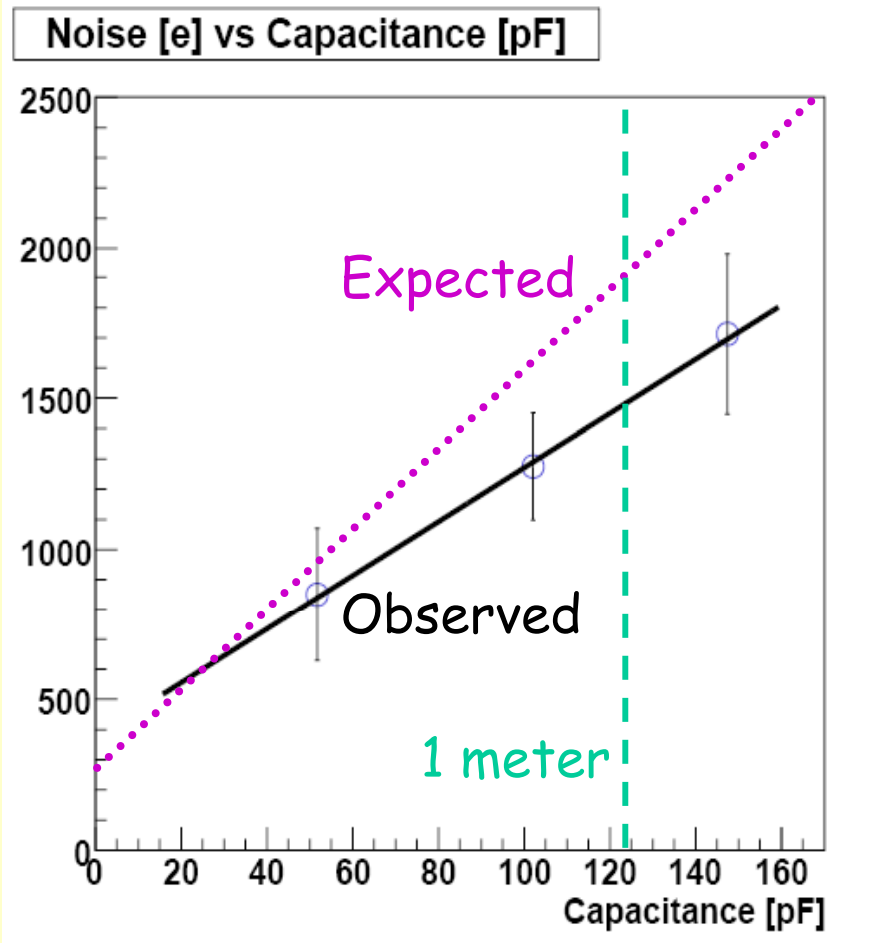
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with *C* in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



LSTFE-II Prototype

Additional “quiescent” feedback to improve power-cycling switch-on from 30 msec to 1 msec

Improved environmental isolation

Additional amplification stage to improve S/N, control of shaping time, and channel-to-channel matching

Improved control of return-to-baseline for < 4 mip signals (time-over-threshold resolution)

128 Channels (256 comparators) read out at 3 MHz, multiplexed onto 8 LVDS outputs

Testing underway by end of calendar year

SiD Sensor Testing

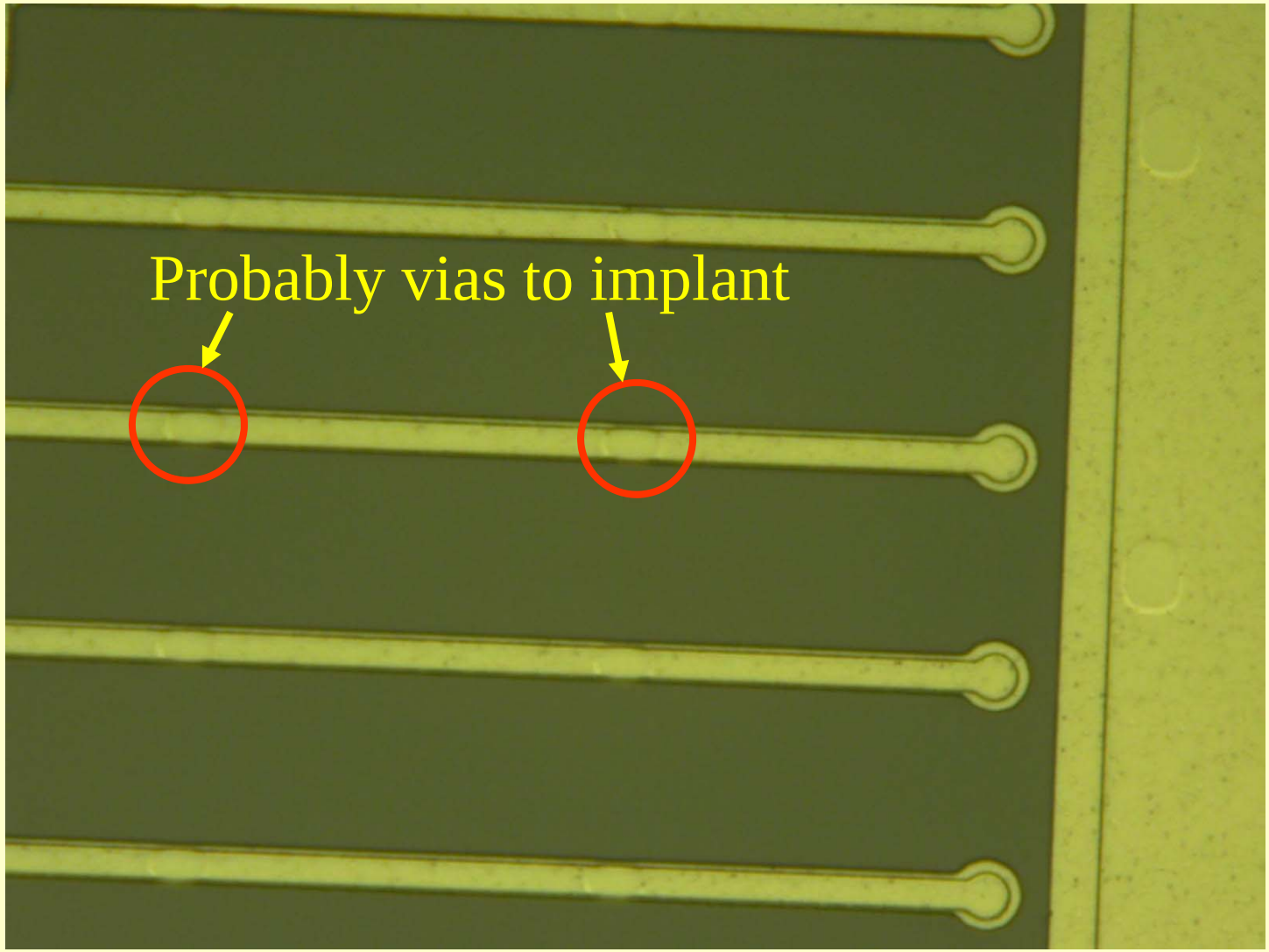
SiD 10cm x 10cm “tile” intended for “KPIX” kilo-channel bump-bond ASIC.

Resistance from strips as well as traces.

First look by SCIPP (Sean Crosby)

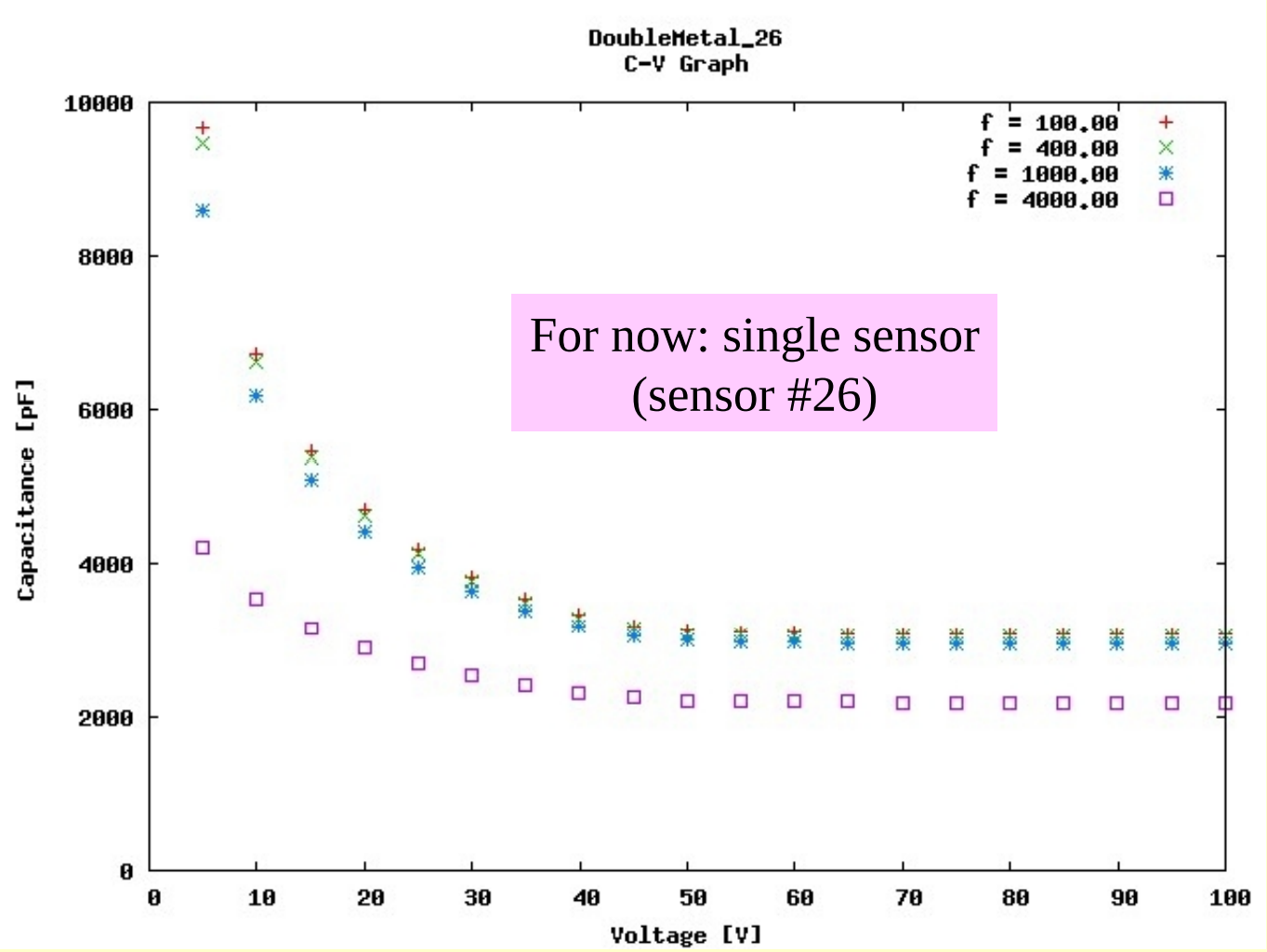
Also looked at “charge division” sensor; want to read out 600 kΩ implant at both ends; confirmed strip that shorts implant (268Ω) mistakenly added by manufacturer.
(Would like to savage one to measure implant resistance)

Magnification of SiD “Charge Division” Sensor

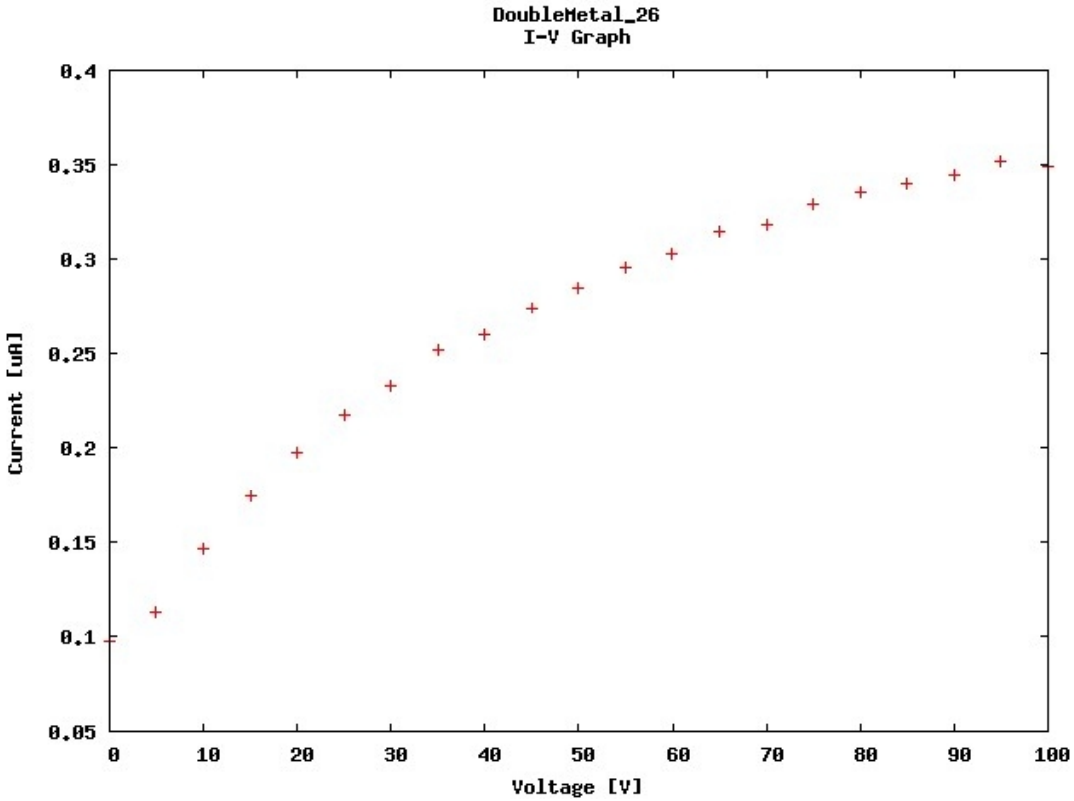


SiD Tiles: Biasing and Plane-to-Plane Capacitance

Sensors bias at ~50 V.
Capacitance shown is for all 1840 strips, but strips to backplane only



For now: single sensor
(sensor #26)



SiD Leakage Current (sensor #26): Average leakage for 1840 channels is about ~160 pA/channel

Measured strip and trace resistances for two sensors:

Sensor Number	Strip Res.	Typical Trace Res.
24	578	225
26	511	161

Looks a bit odd (just first blush still…)

Longitudinal Resolution via Charge Division

Proposed by Rich Partridge, based on seminal paper by Radeka:

V. Radeka "Signal, Noise and Resolution in Position-Sensitive Detectors", IEEE Trans. Nucl. Sci. 21, 51 (1974),

which in turn references earlier work with planar sensors from

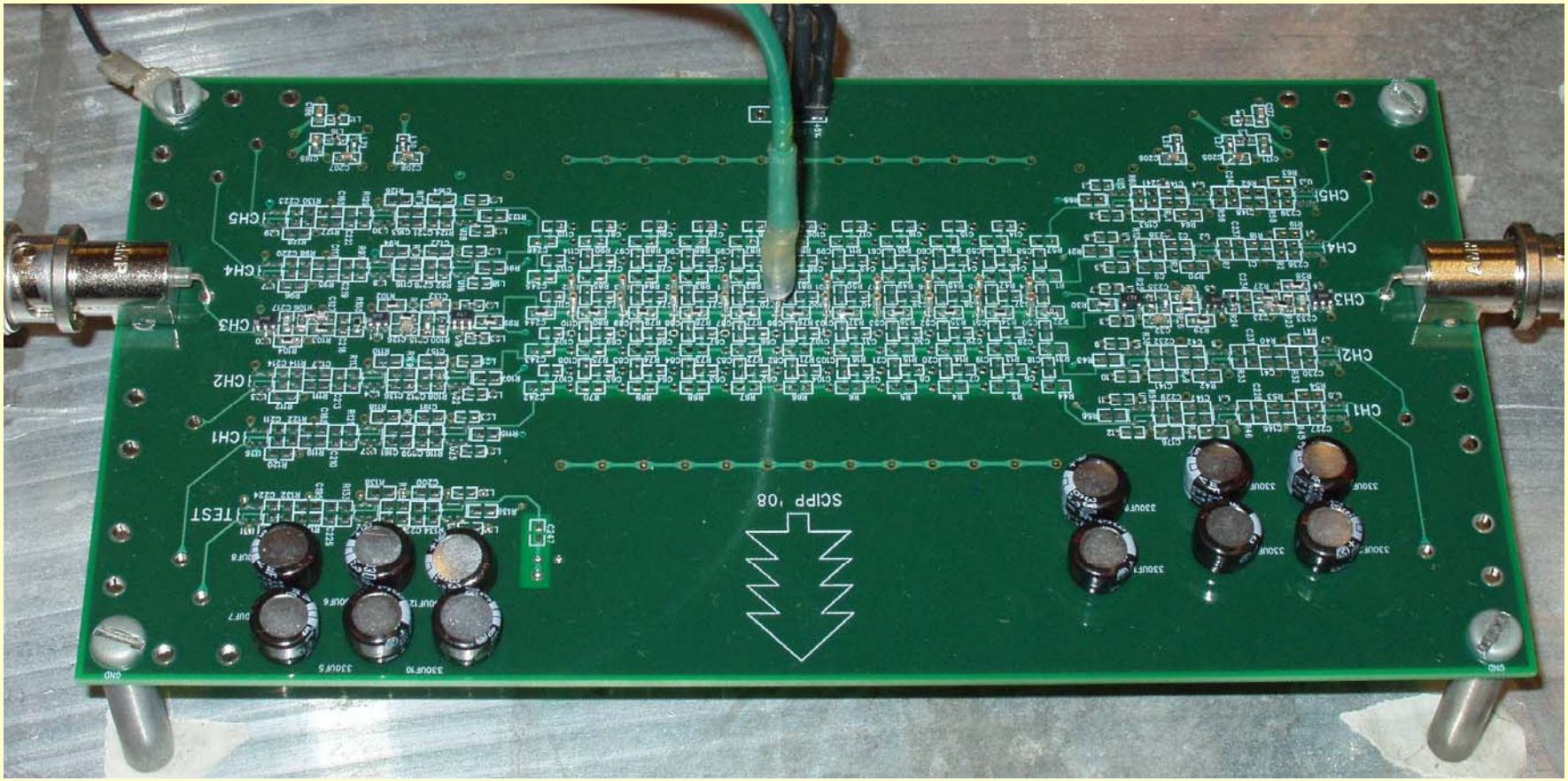
R.B. Owen and M.L. Awcock, IEEE Trans. Nucl. Sci. 15, 290 (1968)

Small ($16K) LCRD grant supports this work. Progress due to UCSC undergraduate physics major Jerome Carman

Basic idea: For resistive sensor, impedances dominated by sensor rather than amplifier input impedance → charge should divide proportional to point of deposition. So, forget about metal strip and read out implant (~100kΩ)

Charge Division Sensor Mock-Up

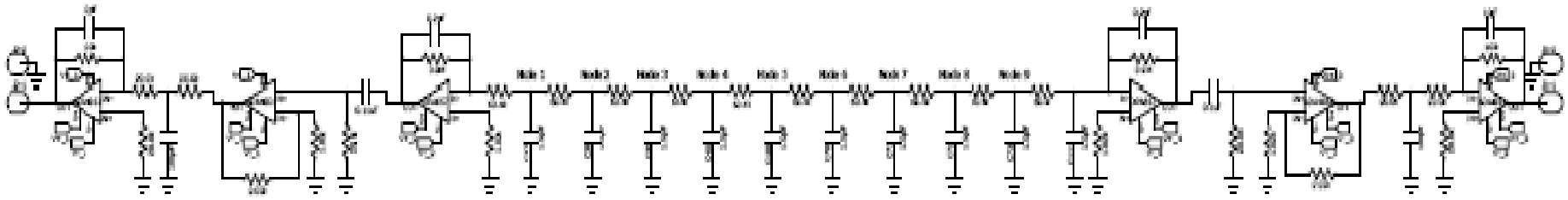
10-stage RC network PC board (Jerome Carman)



Charge Division Sensor Mock-Up

Model 600 kΩ resistive implant with 10-stage RC network

Read out at both left (“L”) and right (“R”) ends



Amplifiers:

First Stage: TI OPA657 Low-noise FET OpAmp

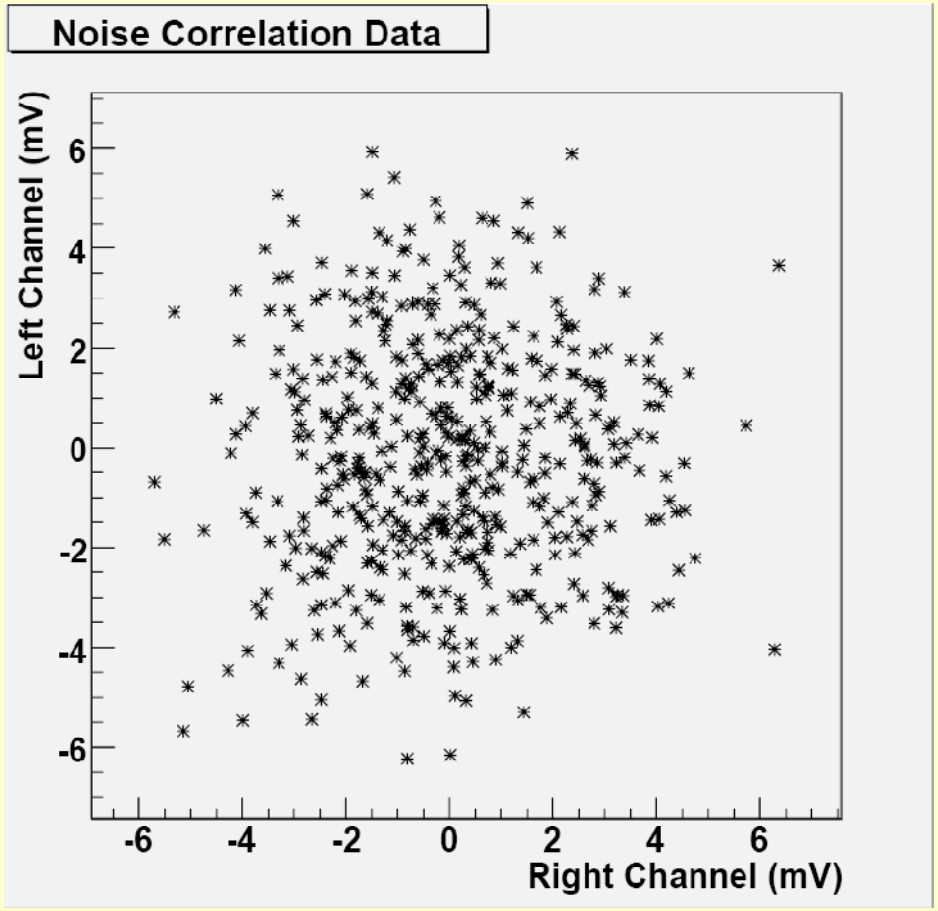
Later Stages: Analog Devices ADA4851 rail-to-rail video amp

Readout Noise Results

Try several configurations, looking at noise from RH amp

Nominal:	0.64 fC
Short RH amp input (163 Ω to ground):	0.26 fC
Disconnect LH amp; ground that end:	0.66 fC
Disconnect LH amp; float that end:	0.44 fC

Correlation Between Left and Right Readout



Naïve expectation:

Dominated by Johnson noise across resistive implant

➔Noise should be anticorrelated

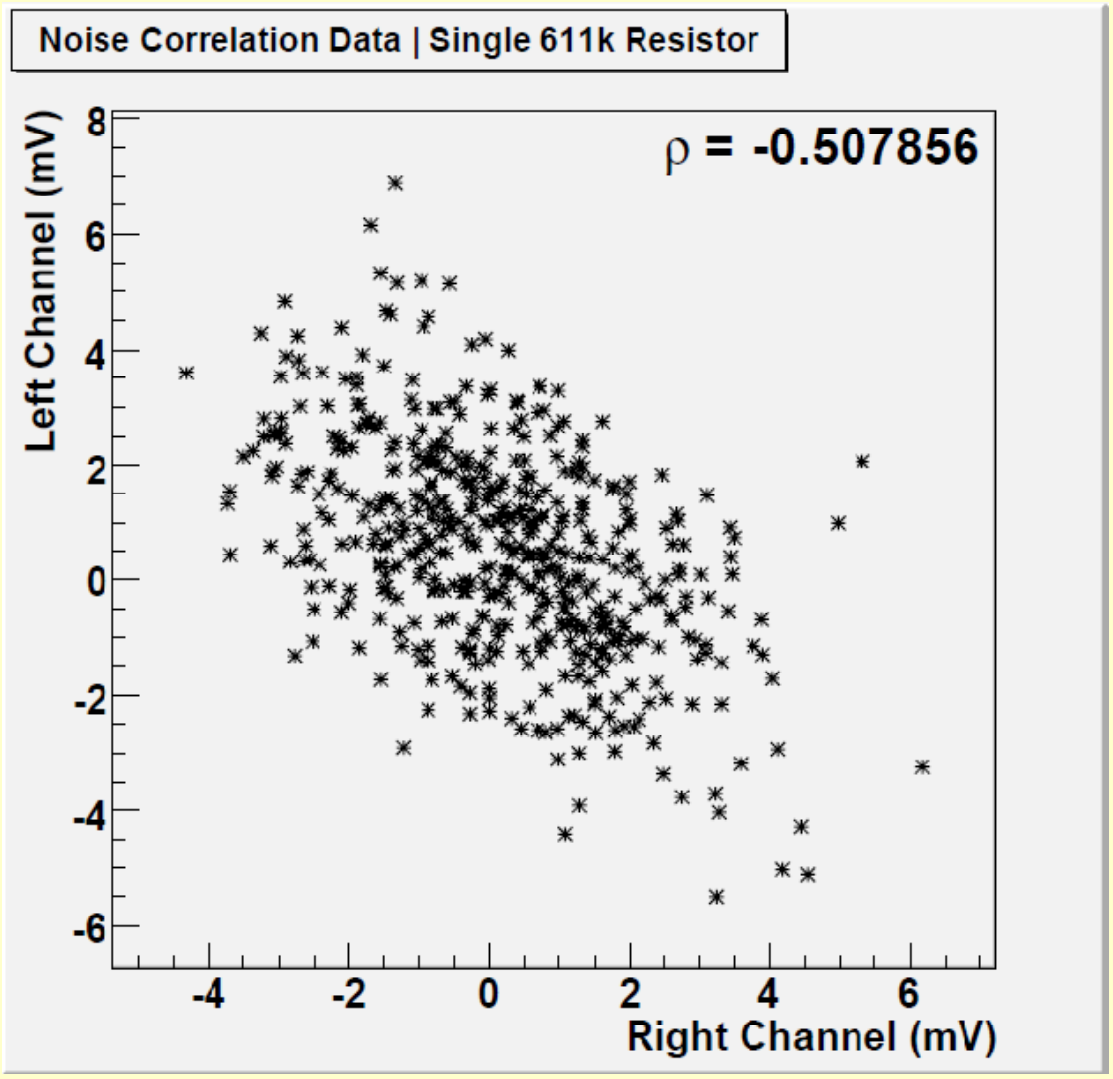
➔ Bad for position resolution

Result: Observed correlation (3%) consistent with 0.

Good news, but why?

Note: With LH amplifier disconnected, +20% correlation observed (?)

Correlation Between Left and Right Readout Cont'd

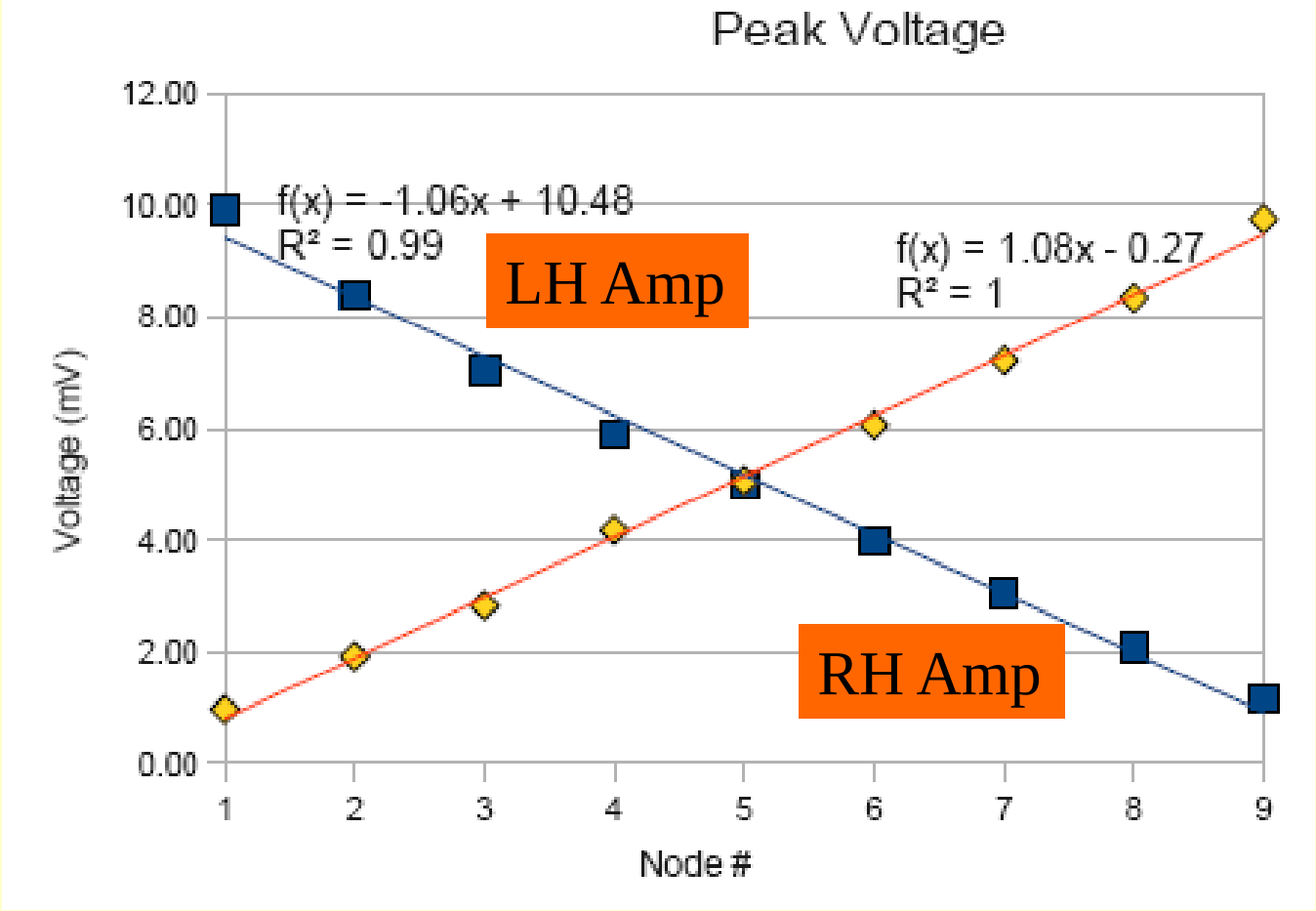


Replace network with single 600 kΩ resistor

➔Anticorrelation observed

Network effects appear to de-cohere Johnson noise currents?

Mean Amplifier Response vs. Injection Point



Linear, with very minor offsets (as you might expect with a 600 kΩ load)

Longitudinal Resolution Estimate

Trying to measure fractional distance *f* from right to left end of strip:

$$f = \frac{R - L}{R + L}$$

Rewrite:

$$f = \frac{1 - L/R}{1 + L/R} = \frac{1 - x}{1 + x}; \quad x \equiv L/R$$

Then,

$$\mathrm{d}f = -\frac{2}{(1+x)^2}\,\mathrm{d}x \quad \text{with} \quad \mathrm{d}x = x\left[\frac{\mathrm{d}L}{L} + \frac{\mathrm{d}R}{R}\right]$$

and d*L*, d*R* apparently uncorrelated.

Longitudinal Resolution Estimate: Conclusion

Depends upon location of hit (middle or near end of resistive implant) and the magnitude of the charge deposition.

Assume a 4 fC deposition in the middle of the strip (x=1):

$$\mathrm{d}f = -\frac{1}{2}\left[\frac{\mathrm{d}L}{L} \oplus \frac{\mathrm{d}R}{R}\right] = \frac{\sqrt{2}}{2}\left[\frac{0.64\ \mathrm{fC}}{2\ \mathrm{fC}}\right] = 0.23$$

However, note that $\frac{1}{\sqrt{12}} = 0.29$, so this is not much better.

➔ Optimize shaping time, implant resistivity, ?

➔ Goal of better than 0.1 (1cm for SiD sensors).

Readout Noise for Linear Collider Applications

Use of silicon strip sensors at the ILC tend towards different limits than for hadron collider or astrophysical applications:

- Long shaping time
- Resistive strips (narrow and/or long)

But must also achieve lowest possible noise to meet ILC resolution goals. How well do we understand Si strip readout noise?

Standard Form for Readout Noise (Spieler)

Parallel Resistance

Series Resistance

$$Q^2 = F_i \tau \left(2eI_d + \frac{4kT}{R_B} + i_{na}{}^2 \right) + \frac{F_v C^2}{\tau} \left(4kTR_s + e_{na}{}^2 \right) + 4F_v A_f C^2$$

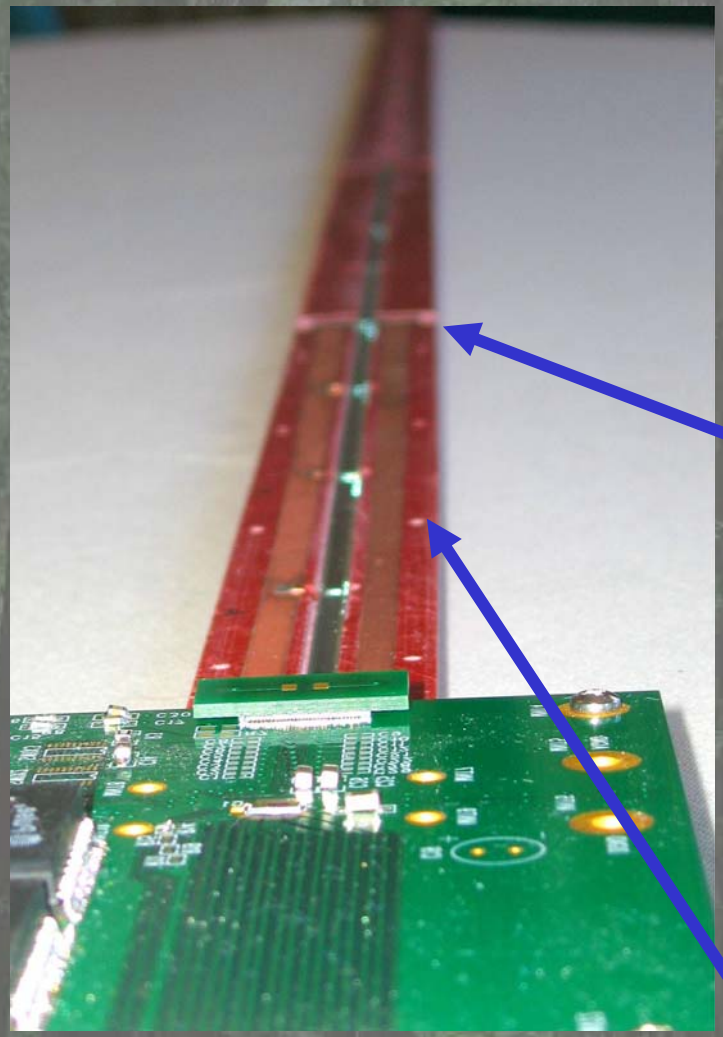
Amplifier Noise (parallel)

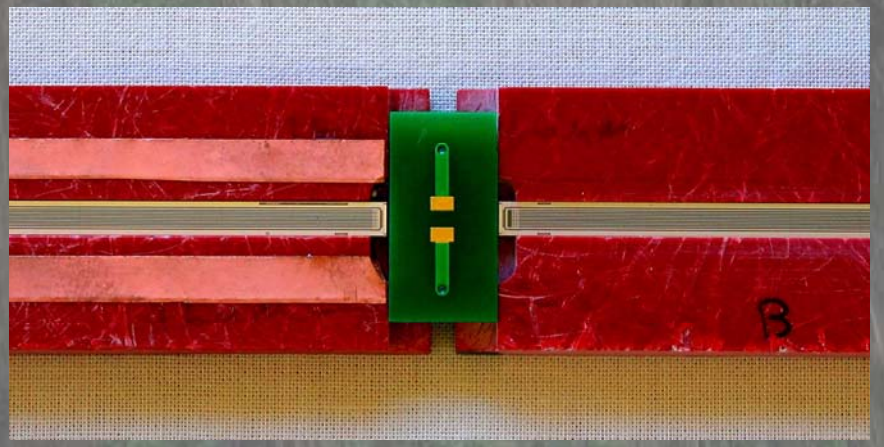
Amplifier Noise (series)

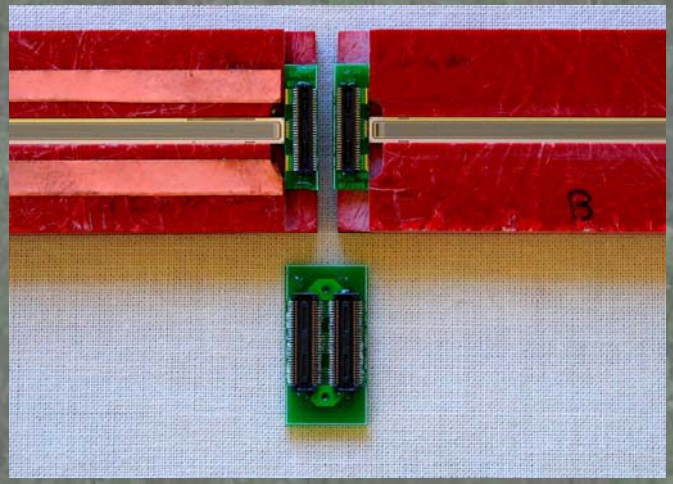
F_i and F_v are signal shape parameters that can be determined from average scope traces.

There is some circumstantial evidence that this may be an oversimplification, particularly for the case of series noise…

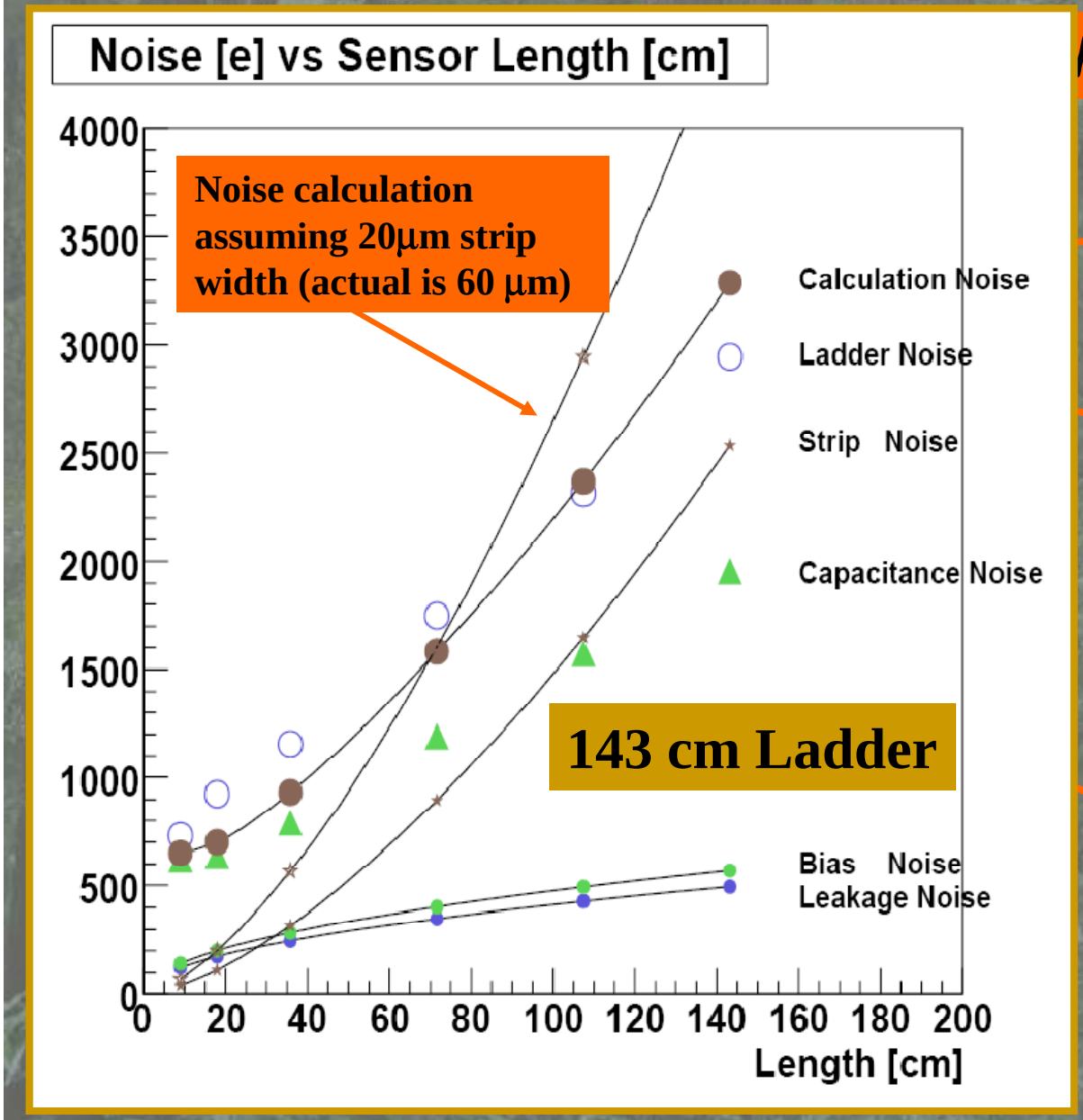
LONG LADDER CONSTRUCTION







Measured Noise vs. Sum of Estimated Contributions



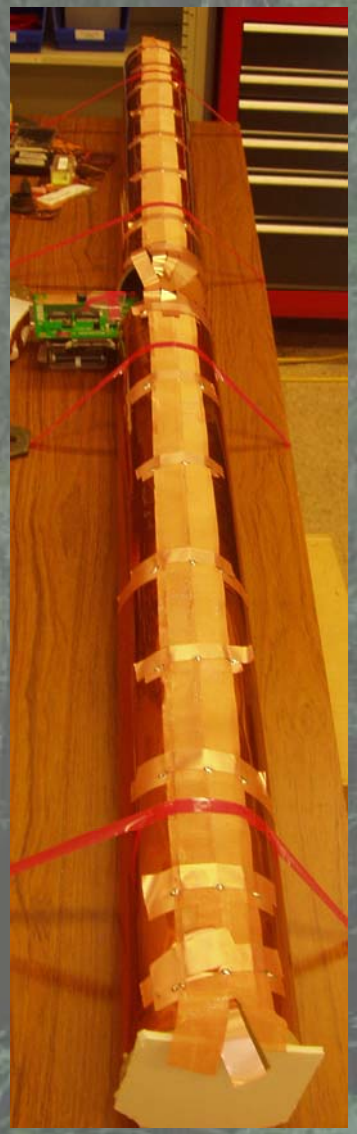
Measured noise

Sum of estimates

Projected Johnson noise for 20 μm strip (not part of estimate)

Estimated Johnson noise for actual 65 μm strip (part of estimate)

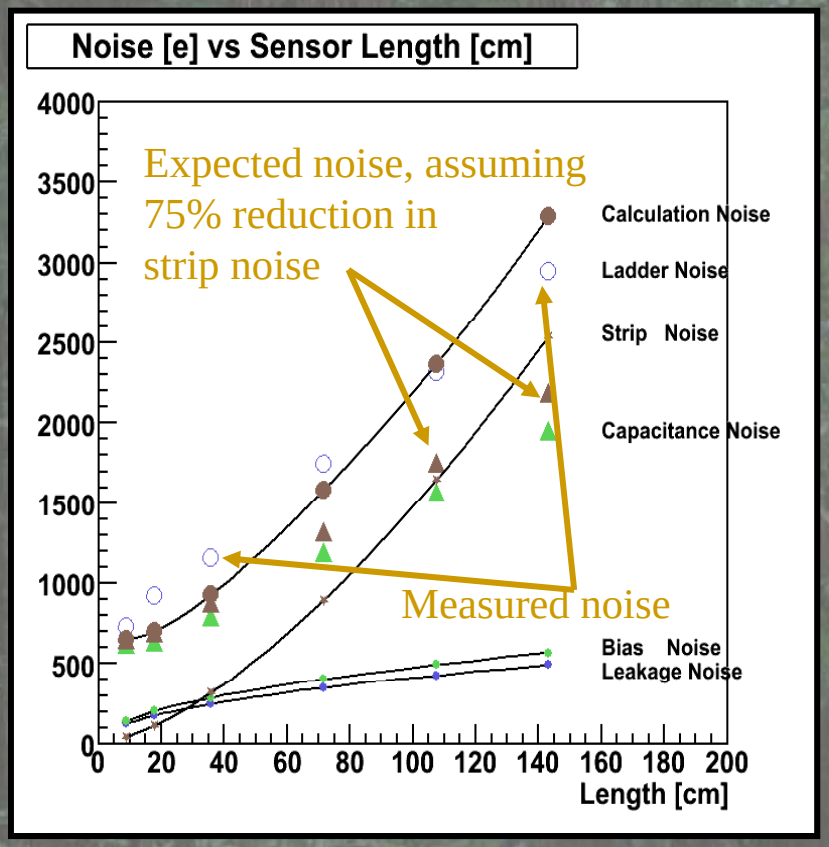
Strip Noise Idea: "Center Tapping" – half the capacitance, half the resistance?



Result: no significant change in measured noise

However, sensors have 237 μm pitch

➔ Currently characterizing CDF L00 sensors



CDF L00 Sensor “Snake”

CDF L00 strips: 310 Ohms per 7.75cm strip (~3x GLAST)

➔Long-ladder readout noise dominated by series noise (?)

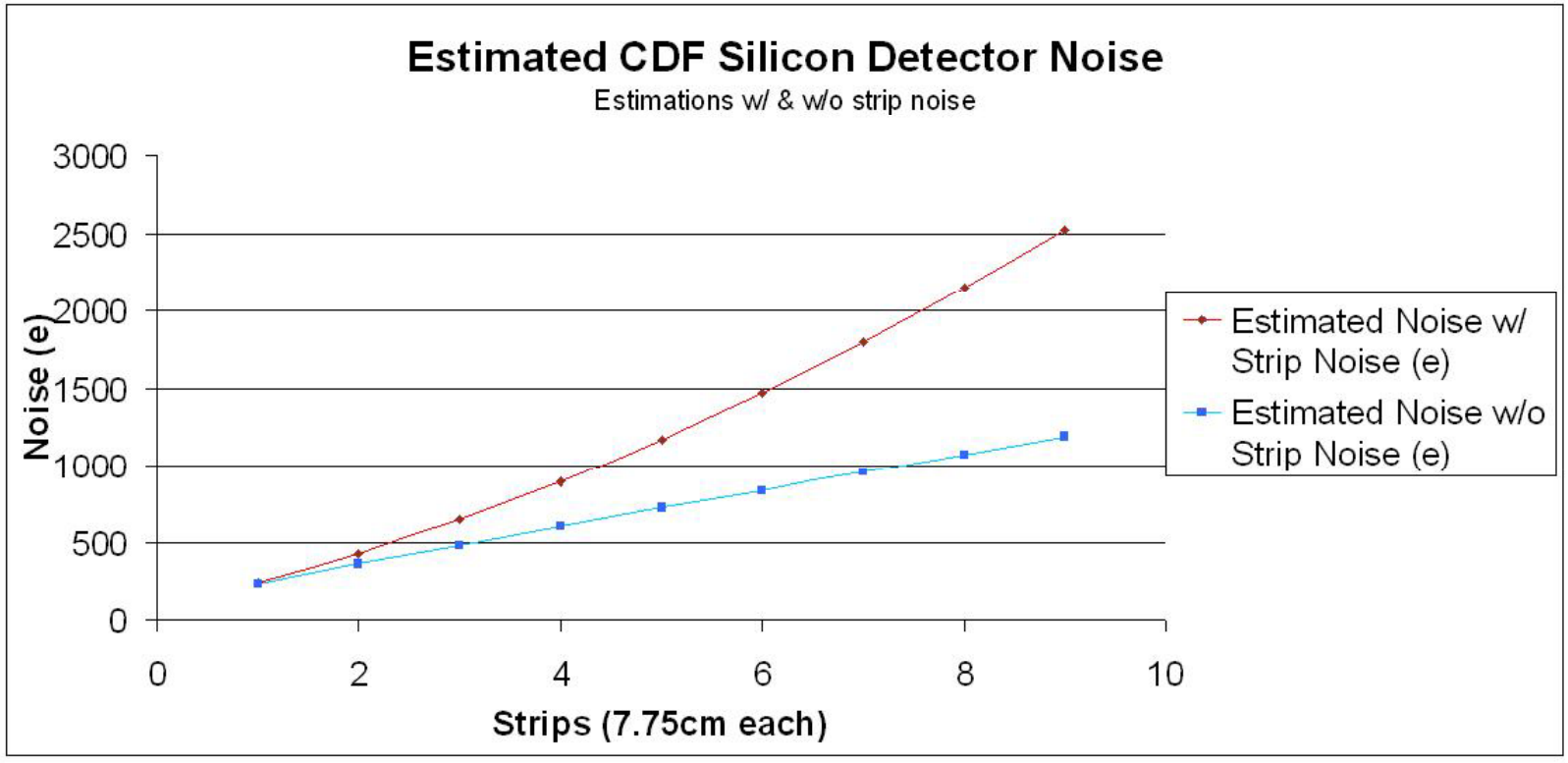
Construct ladder by bonding strips together in “snake” pattern (Sean Crosby)

At long shaping-time, bias resistors introduce dominant parallel noise contribution

➔Sever and replace with custom biasing structure (significant challenge…)

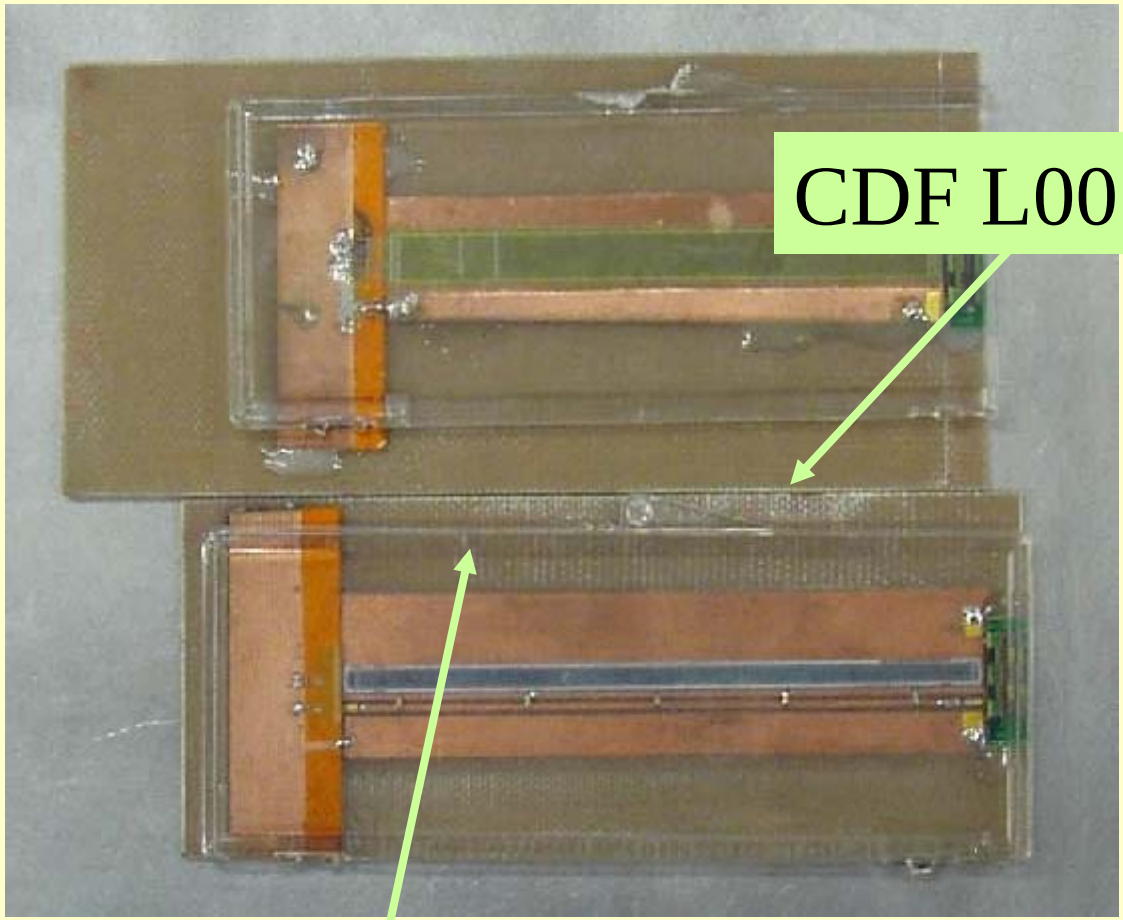
Thanks to Sean Crosby, UCSC undergraduate thesis student

Expected Noise for Custom-Biased L00 Ladder

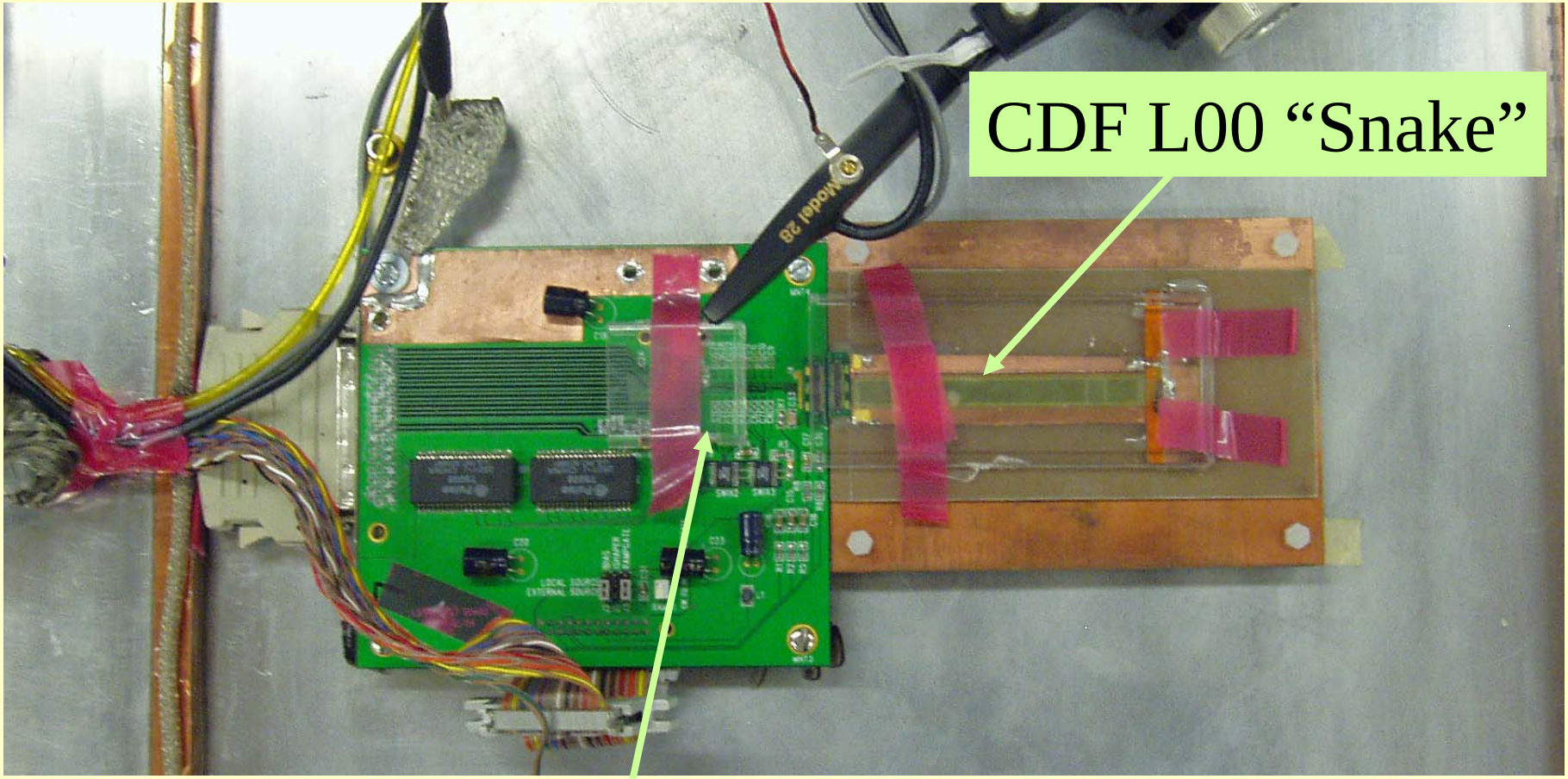


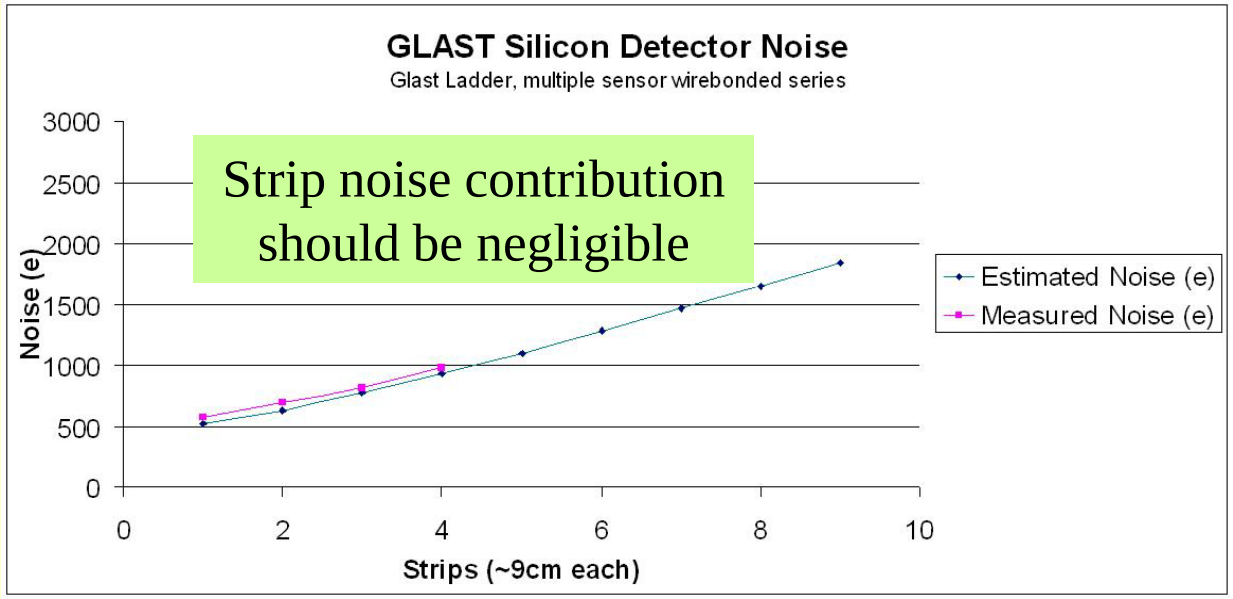
Spieler formula suggests that series noise should dominate for ladders of greater than 5 or so sensors.

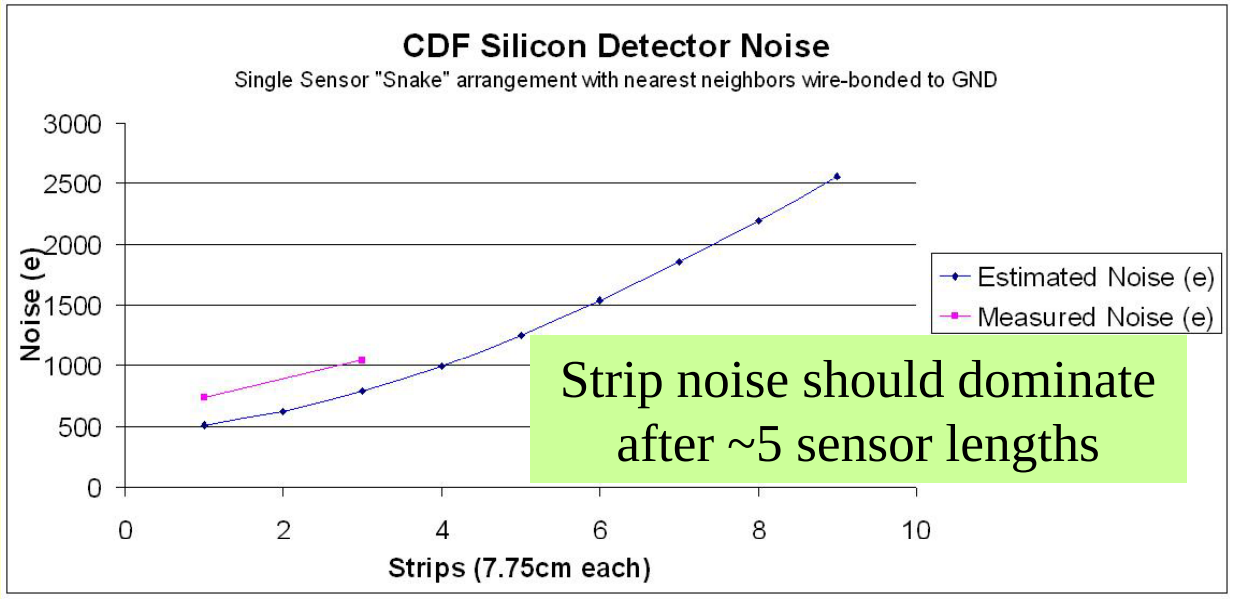
CDF L00 Sensor “Snake”



CDF L00 Sensor “Snake”







(After lengthy effort to eliminate non-fundamental noise sources)

What happens when we add more CDF modules?

Can we understand "extra" CDF noise by studying shaping-time dependence?

Conclusions

SiD sensor: first pass characterization looks fine (complex design!). “Charge Division” sensors shorted by strips.

LSTFE-2 awaits testing (soon!); design refined by studies of LSTFE-1

Charge division approach looks interesting; needs to be optimized and some questions explored (but what happens to S/N and transverse resolution?)

Effects of series noise being questioned; empirical study of readout noise contributions underway

Starting SPICE simulation of “snake” and charge-division setup to calibrate understanding (Ryan Stagg)