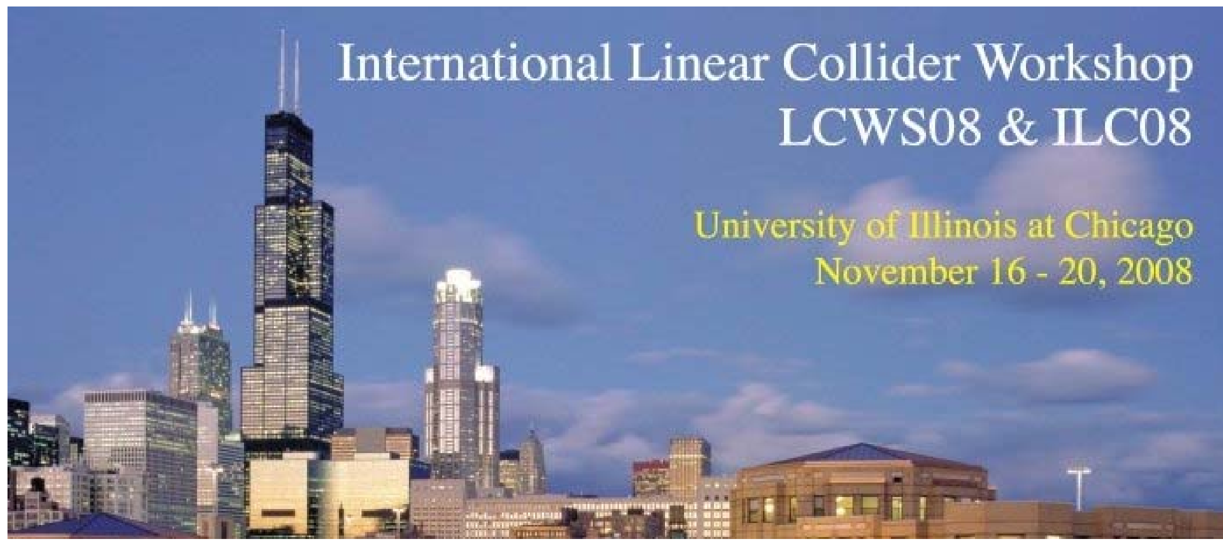
Front end electronics R&D for the CALICE/EUDET calorimeters



Rémi CORNAT

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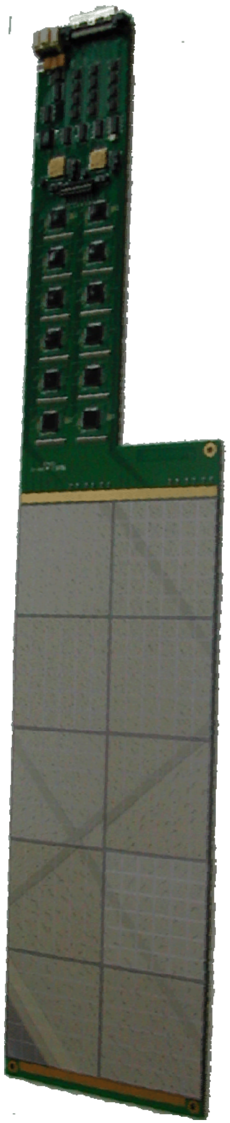
On Behalf of the **CALICE Collaboration**

Outline :
Detectors & constraints on electronics
Read-out chip
Technical studies

First prototypes of calorimeters in CALICE

SI-W ECAL SLAB



Proof of principle

- Imaging calorimeters
- Signal processing, sensors performance
- Noise, stability, uniformity

DHCAL slice test

AHCAL

FE Electronics outside the detectors
Poor digital layer within the FE chips
Power consumption not optimized
DAQ not integrated (when applicable)

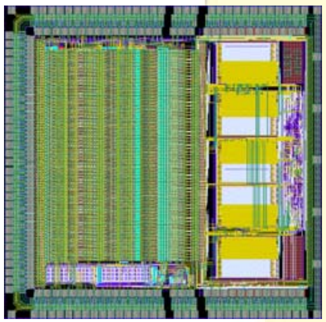
Next development steps

Step by step approach

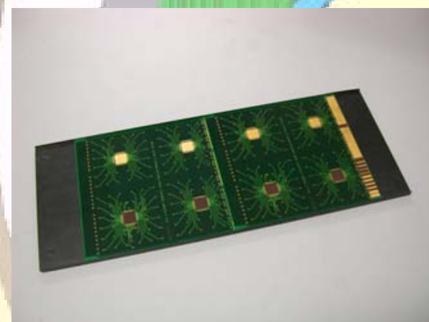
Physics performance → Technological feasibility → Module 0 → Production

Physics prototype → Technological demonstrator → Finalized design

A common scheme



Read-out chips
ROC series



Modular detector plane
Assembled from identical units : sensors + ROCs on PCBs

DIF (detector interface)
+specific adapter
(LV, buffers)

Clock & fast control
DAQ and online SW
See Valeria's talk

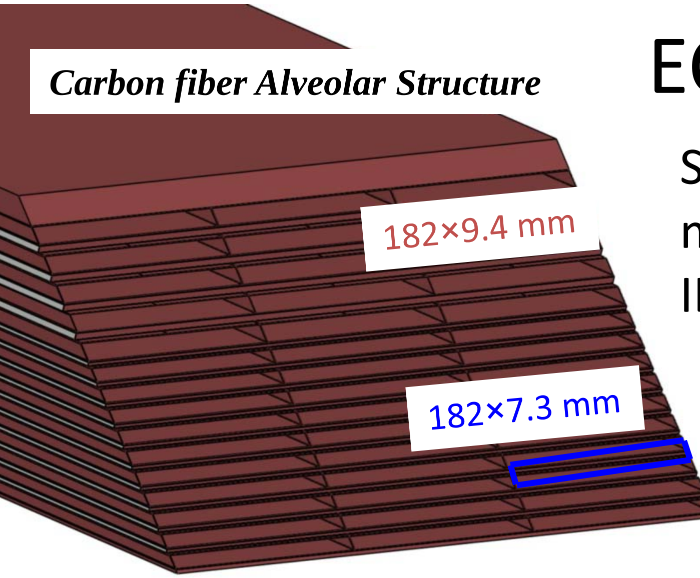
CALICE/EUDET demonstrator : ILD flavored technological prototype

Partly funded under the European Framework : EUDET contract

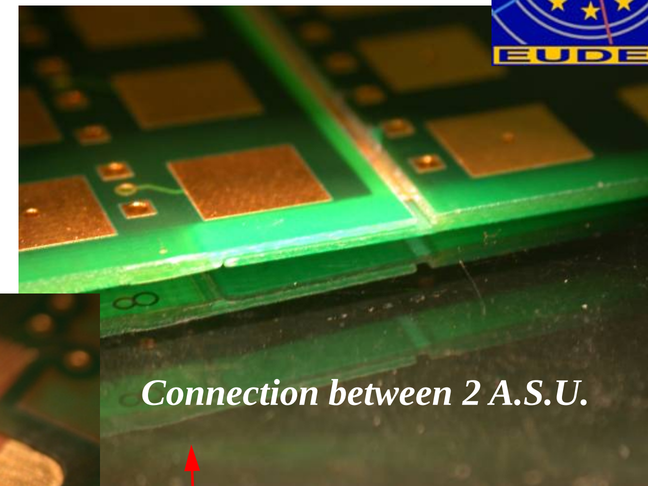
Designed with up to date constraints from ILD design

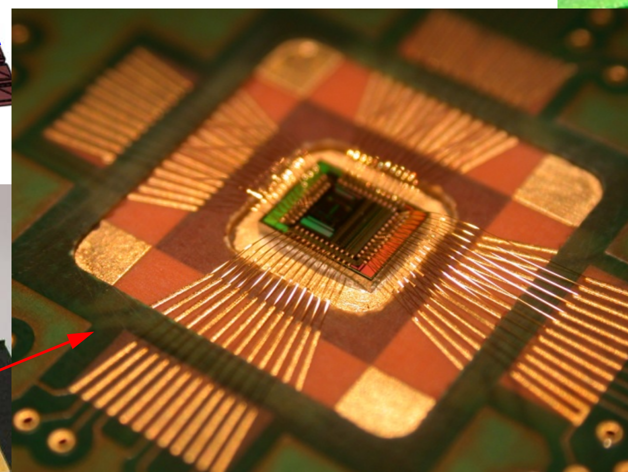
Not optimized for physics and data tacking on tests beams

ECAL detector slab

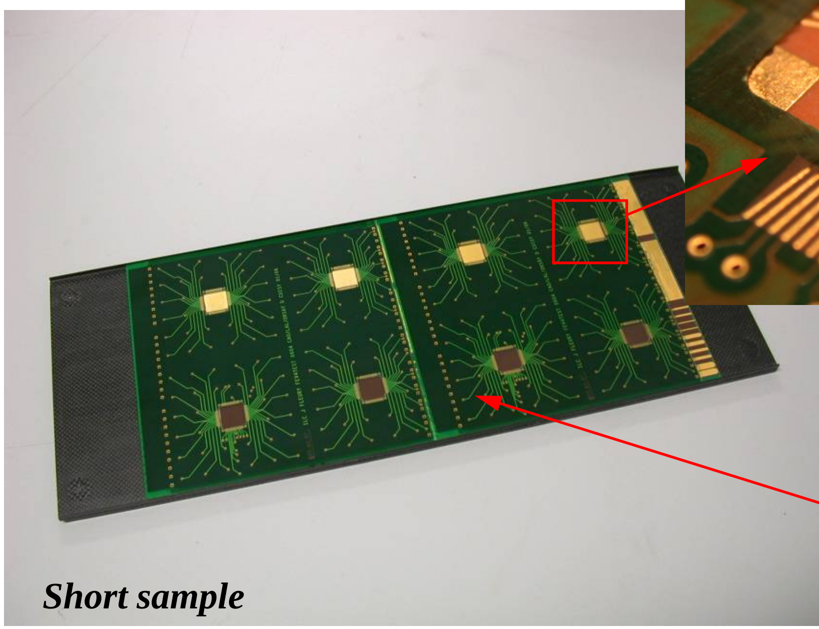


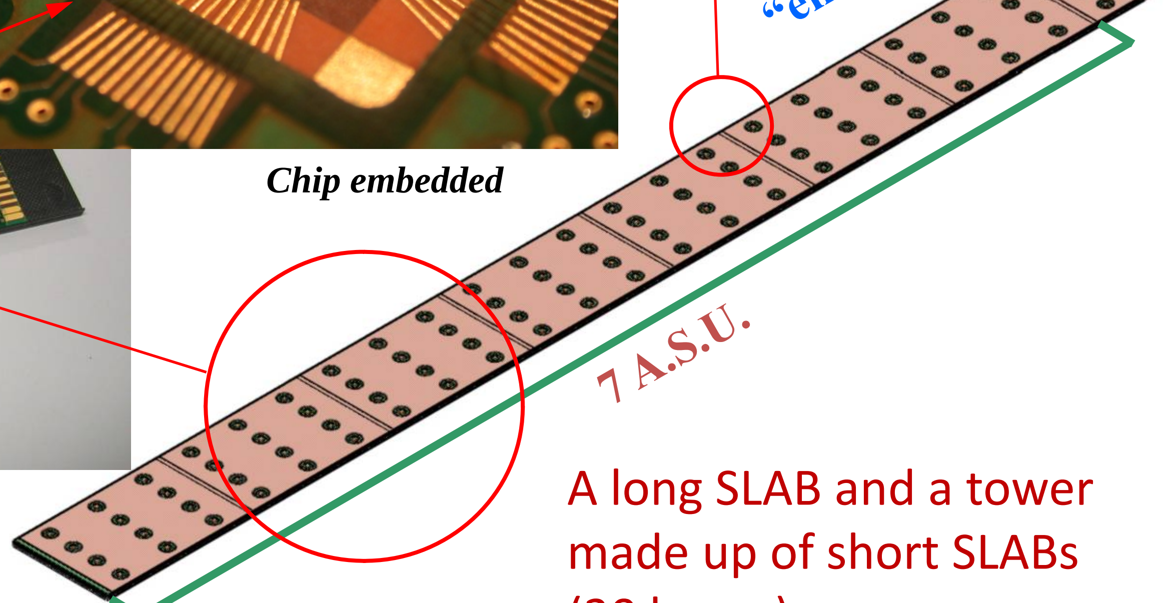
Slightly relaxed mechanical constraints : ILD + 0.4 mm





Chip embedded

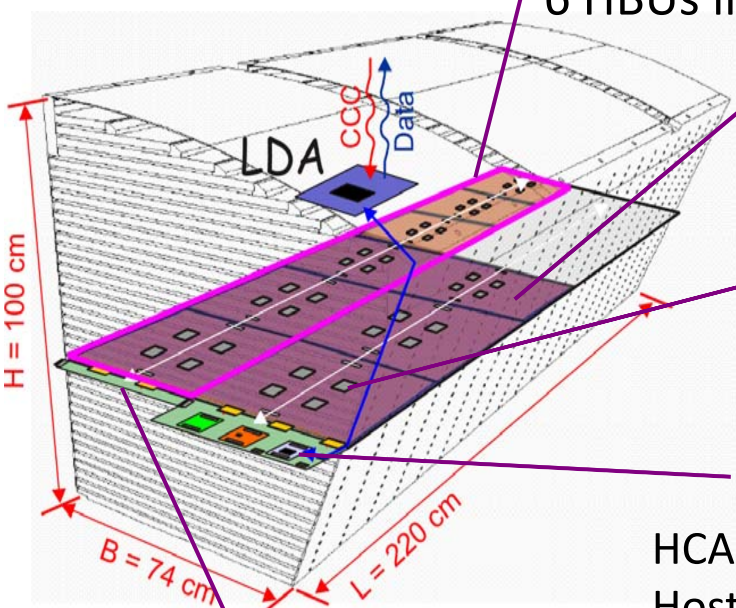




A long SLAB and a tower made up of short SLABs (30 layers)

AHCAL

A detection plan + a tower



AHCAL Slab

6 HBUs in a row

HBU

HCAL Base Unit

12 x 12 tiles

SPIROC

4 on a HBU

HEB

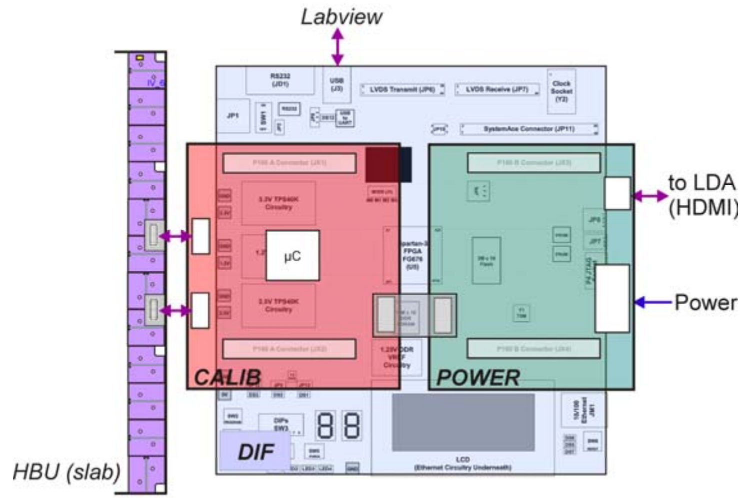
HCAL Endcap Board

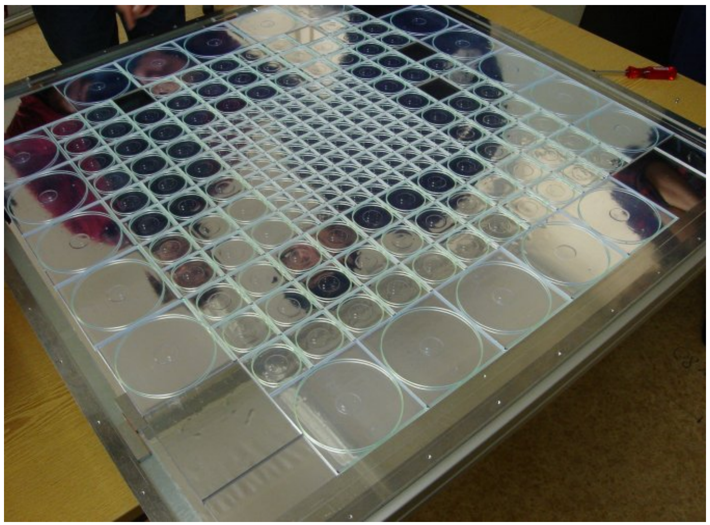
Hosts mezzanine modules:

DIF, **CALIB** and **POWER**

HLD

HCAL Layer Distributor



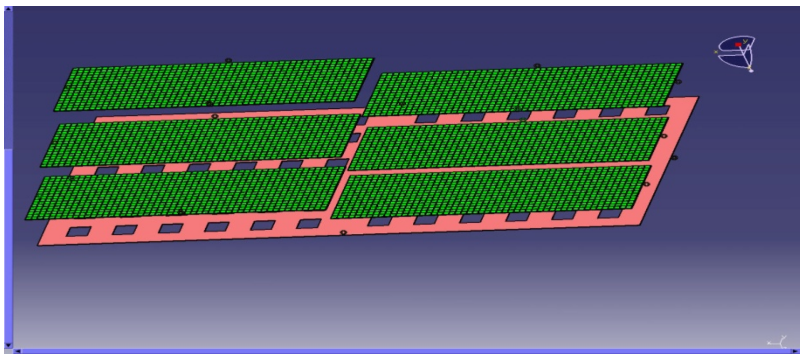


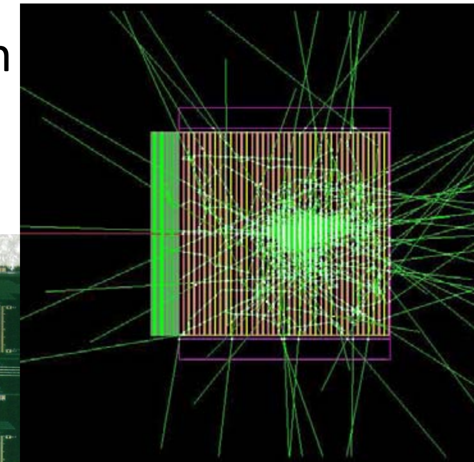
DHCAL

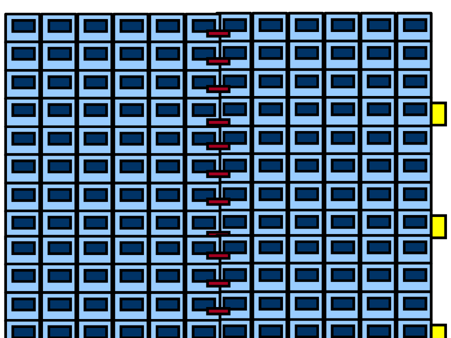
The goal is a cubic meter (40 layers)

A square meter is in preparation

+ large PSB design, coupling to GRPC to be proven

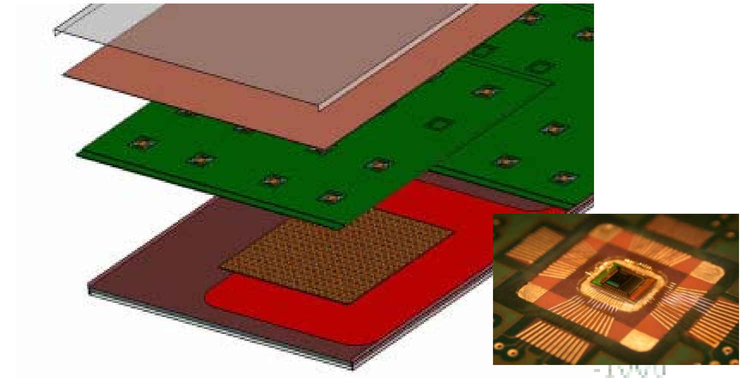


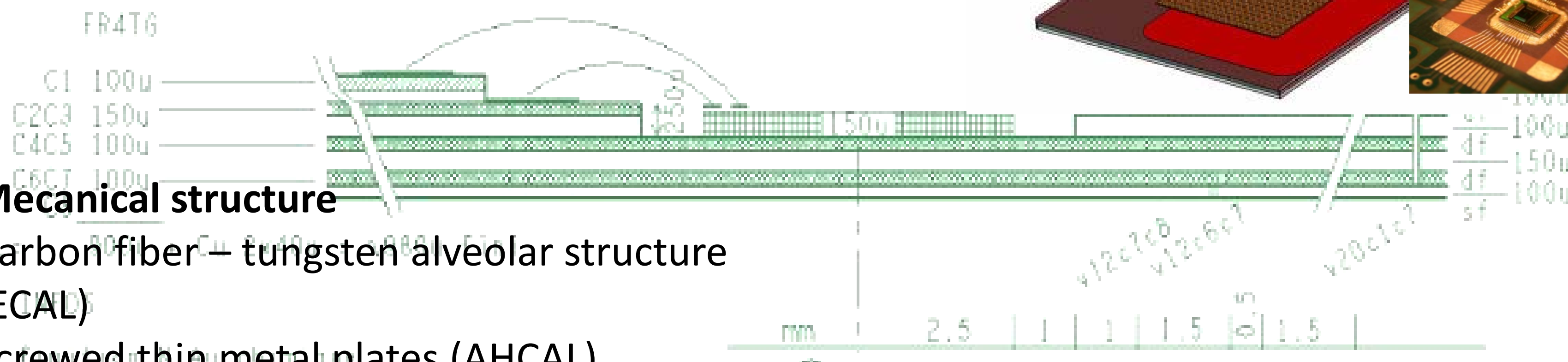




EUDET/CALICE module : challenge of Integration

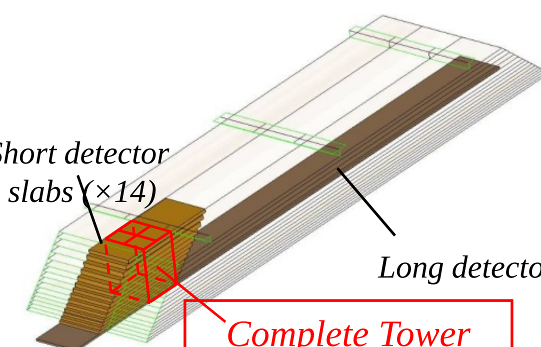
Integration of the electronics inside the detector
ECAL : chips bounded into a groove on a 800 µm thick PCB





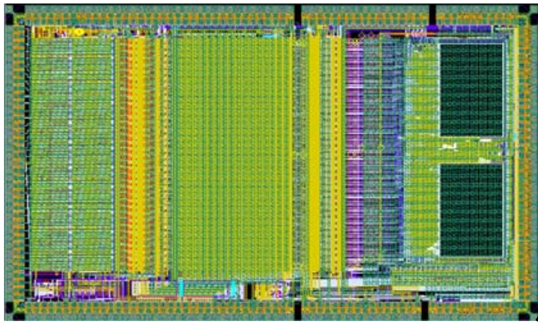
Mecanical structure
Carbon fiber – tungsten alveolar structure (ECAL)
Screwed thin metal plates (AHCAL)

New read-out chip : ROC family generation 2
ADC & digital memory
Power pulsing
Control and data on a serial bus

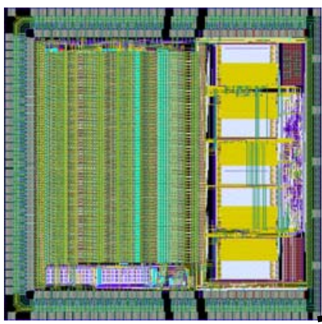


Generic and modular DAQ:
LVDS
G-Ethernet + Optical links

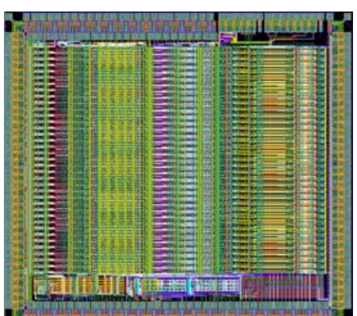
The front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. $32 mm^2$
June 07



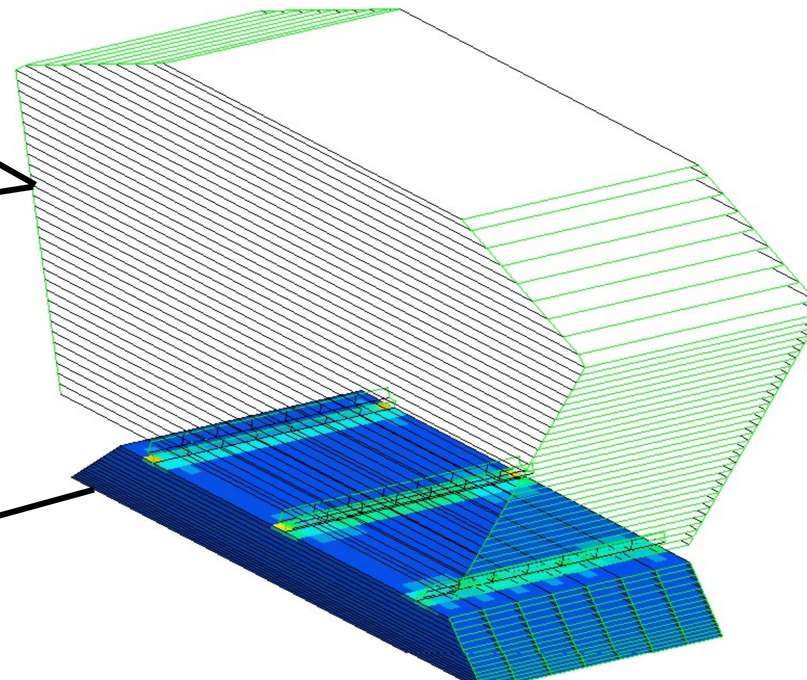
HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. $16 mm^2$
Sept 06

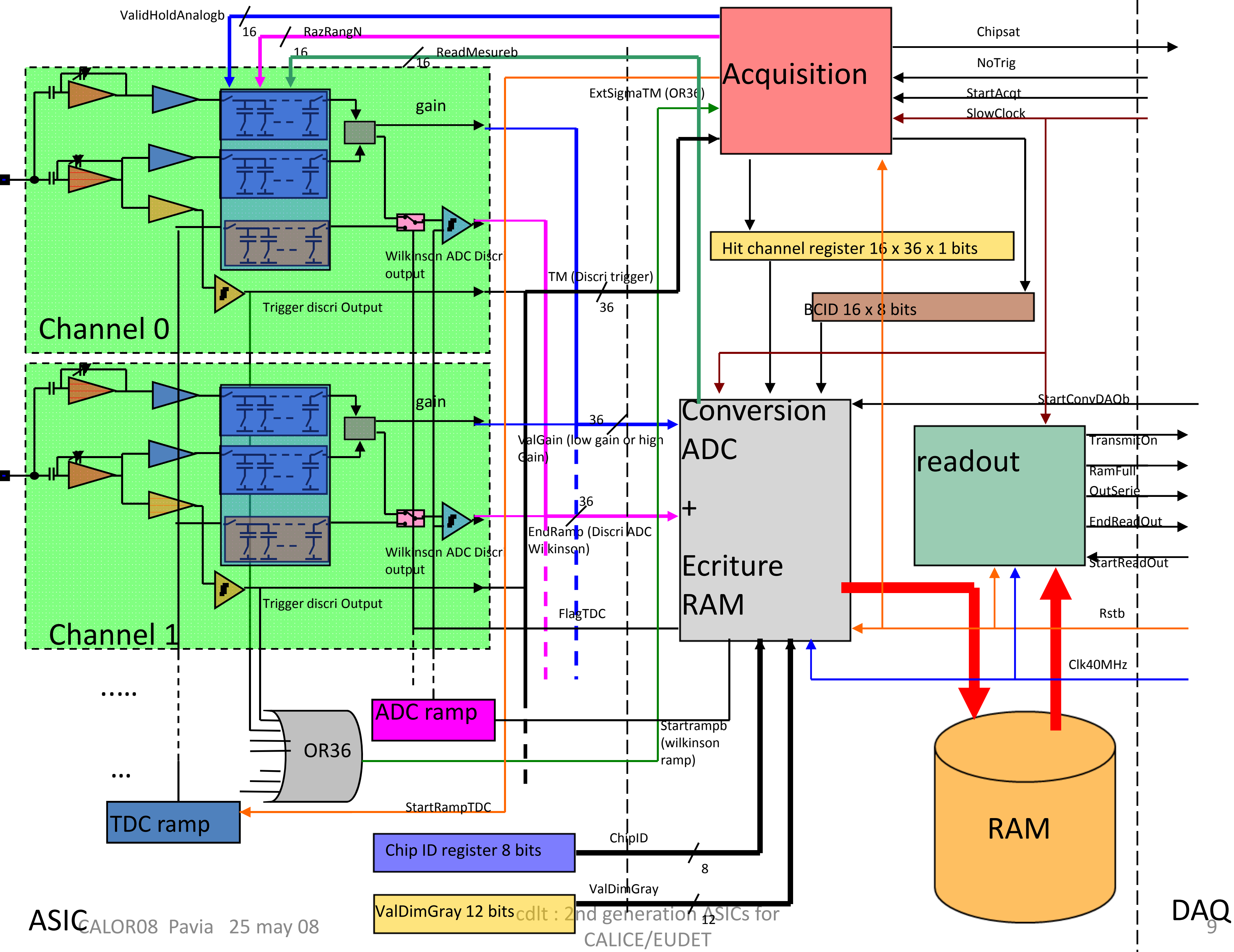


SKIROC
ECAL
(Si PIN diode)
36 ch. $20 mm^2$
Nov 06

“A front-end board in a chip”

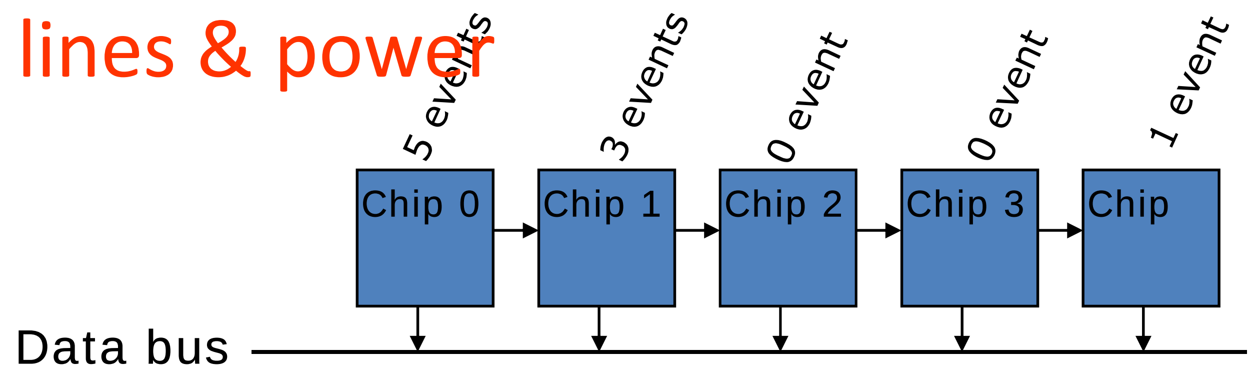
Common blocs, similar design
But flavored to a detector type

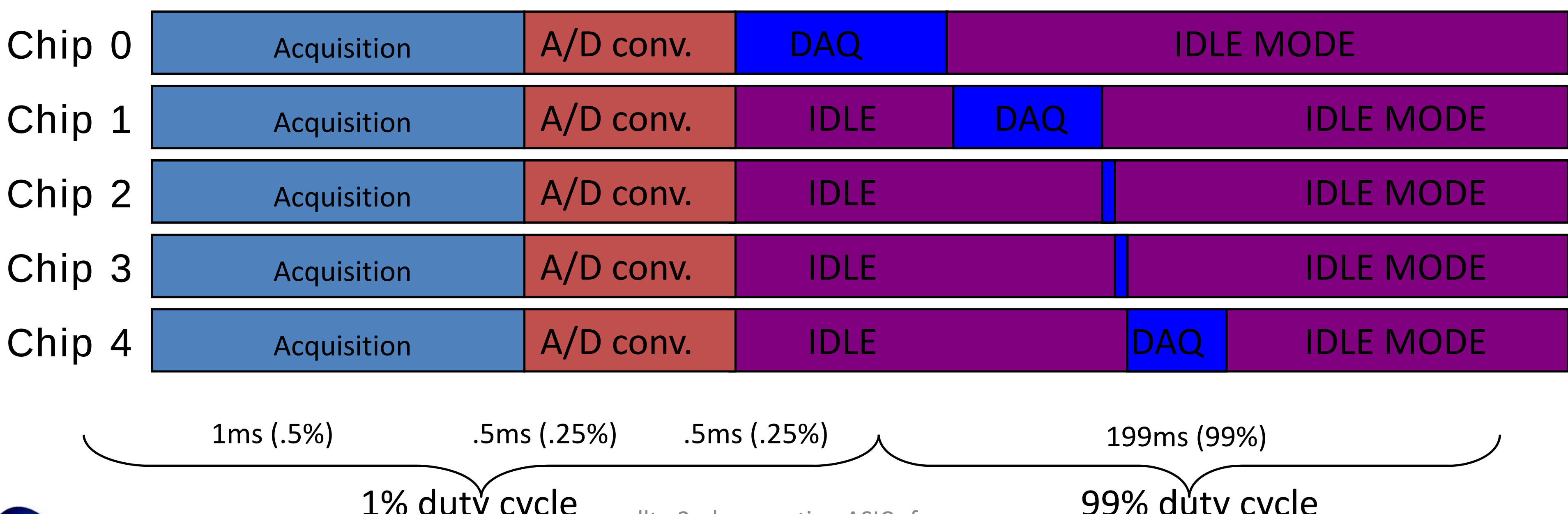



ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC Discr output
TM (Discri trigger)
36
Trigger discri Output
Channel 0
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
StartConvDAQb
36
Conversion ADC
+
Ecriture RAM
ValGain (low gain or high Gain)
36
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
EndRamp (Discri ADC Wilkinson)
Wilkinson ADC Discr output
Trigger discri Output
FlagTDC
Channel 1
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb (wilkinson ramp)
RAM
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
ASIC
DAQ

Read out : token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power





Front-end ASICs : V2, V3

Large dynamic range (15 bits)

Auto-trigger on ½ MIP

On chip zero suppress

Front-end embedded in detector

Production foreseen beg 2009

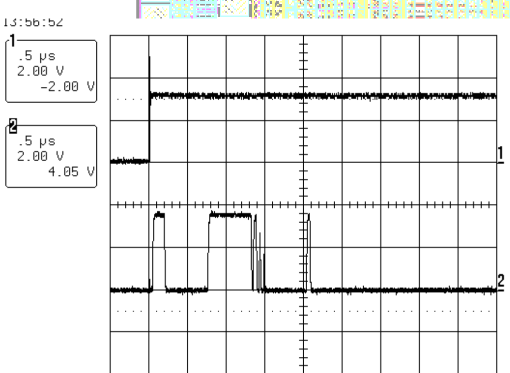
3rd generation chips still to come

Alternative ADC designs

All channels treated independantly

No external Components

Ultra-low power : (25µW/ch)



PWR ON: ILC like (1ms,199ms)

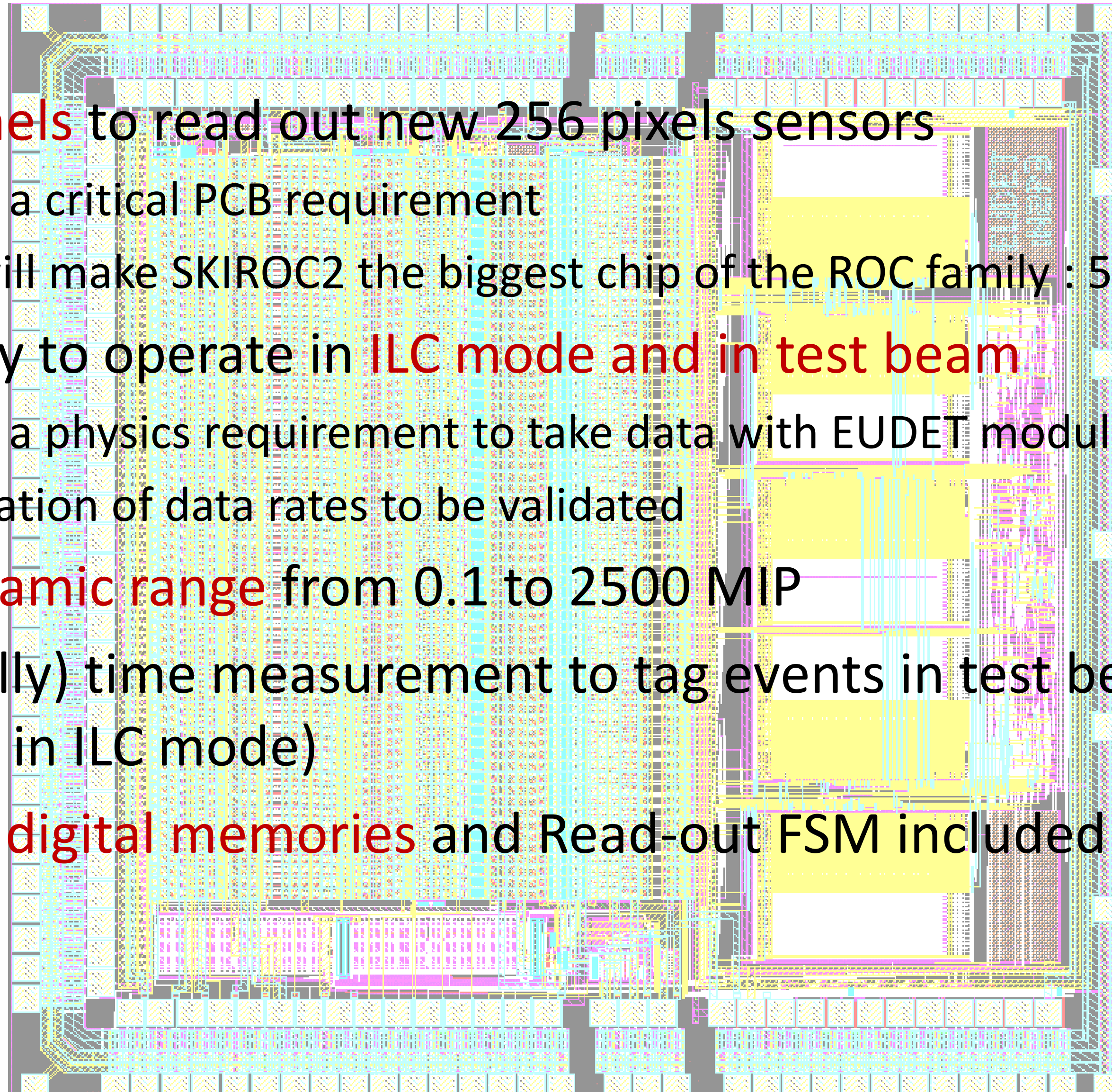
All decoupling capacitors removed :
difficult compromise between noise filtering and fast awake time

Awake time :

- Anaog part = 2 us
- DAC part = 25 us

0.5 % duty cycle achieved, now to be tested at system level

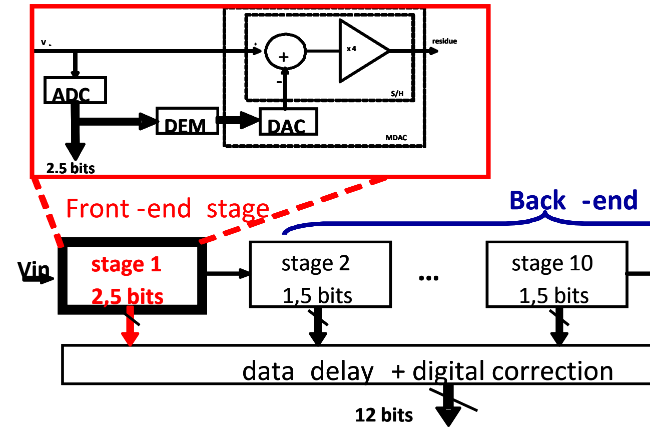
SKIROC exemple : Expectations for EUDET



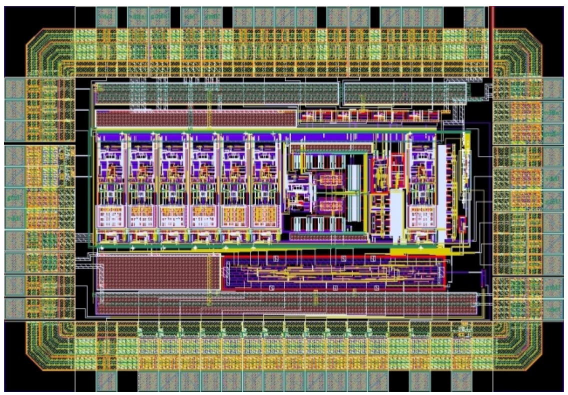
- 64 channels to read out new 256 pixels sensors
  - This is a critical PCB requirement
  - This will make SKIROC2 the biggest chip of the ROC family : 50-60 mm²
- Capability to operate in ILC mode and in test beam
  - This is a physics requirement to take data with EUDET module
  - Calculation of data rates to be validated
- High dynamic range from 0.1 to 2500 MIP
- (Eventually) time measurement to tag events in test beam (not useful in ILC mode)
- ADC and digital memories and Read-out FSM included

Front-end ASICs : ADCs

12b, good linearity, high density integration, low power
But “low” sampling frequency
=> pipe-line, cyclic architecture

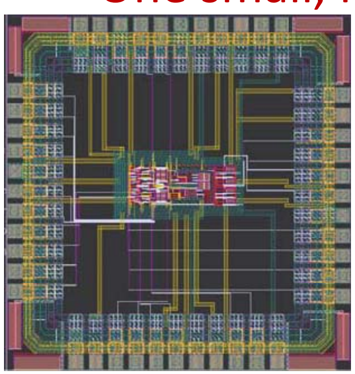


A single multiplexed ADC

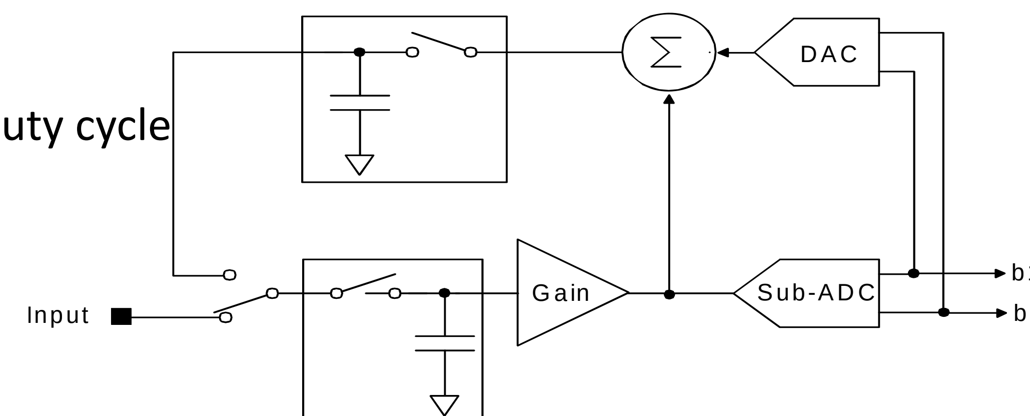


2 mm2
2 mW/ch @ 100% duty cycle
35 MHz

One small, low power ADC per channel

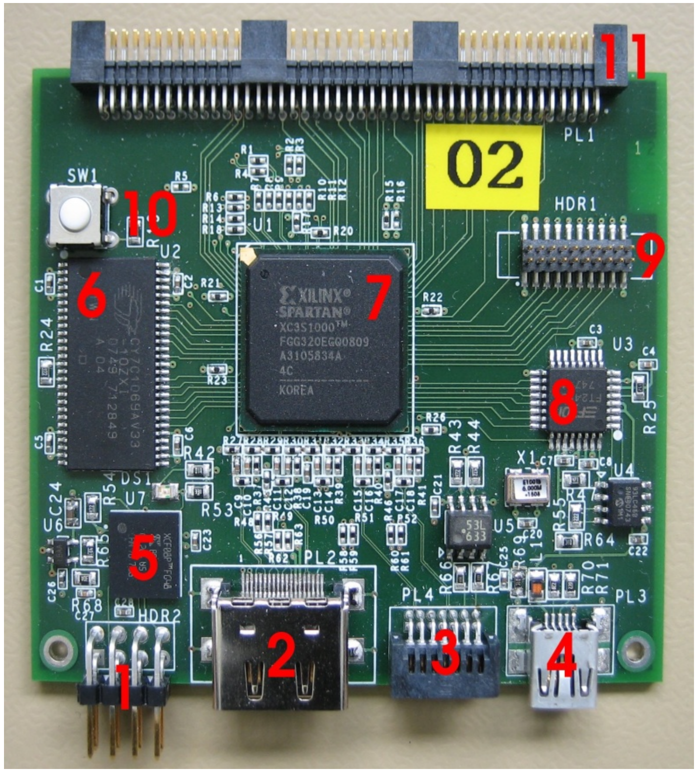


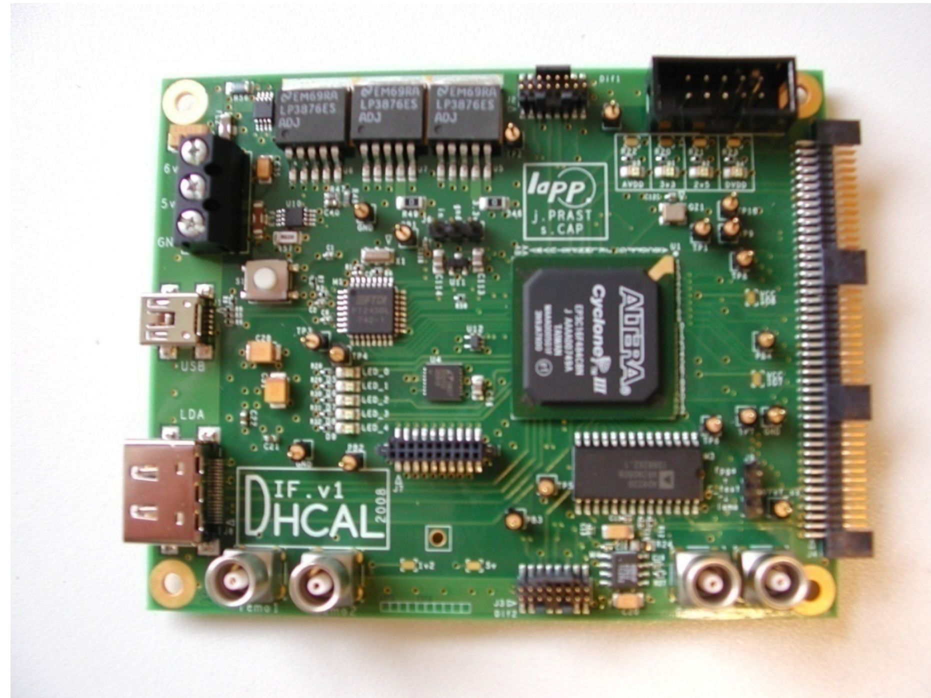
0.18 mm2
4 mW/ch @ 100% duty cycle
5 MHz
INL < 3 lsb
DNL < 1 lsb
Noise < 1 lsb



DIF

SLAB / PLAN controller, interface to DAQ

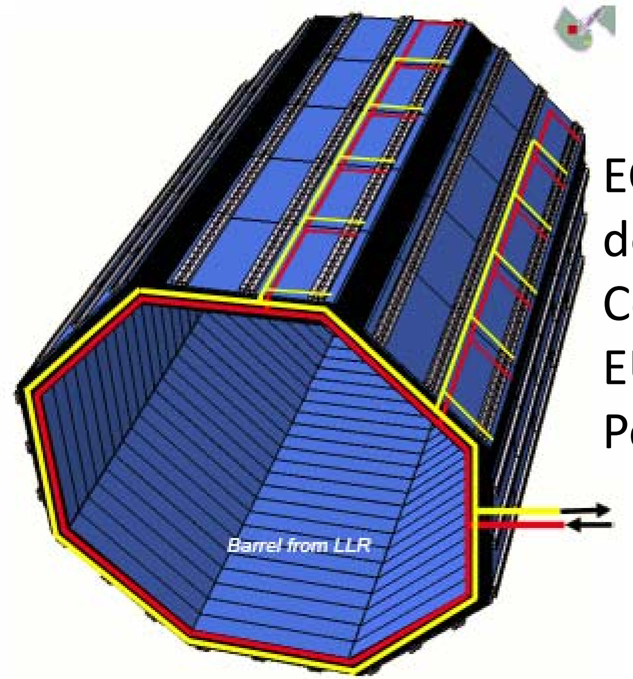




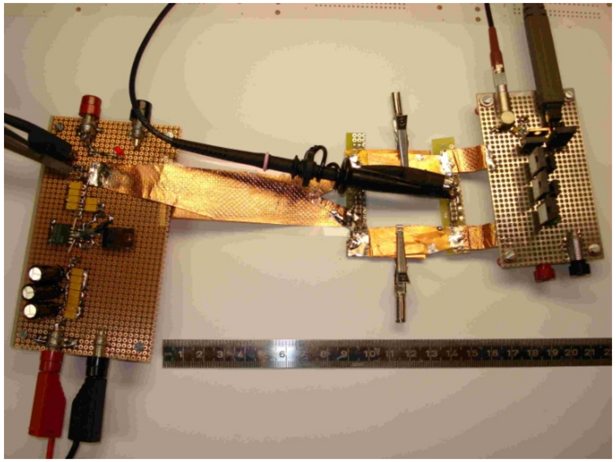
FPGA based, USB for debug, RAM, common connector

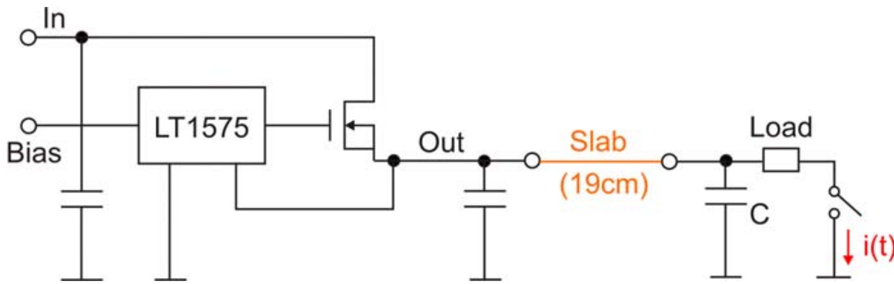
Would need more effort on integration: ECAL 7x3x0.7 cm3

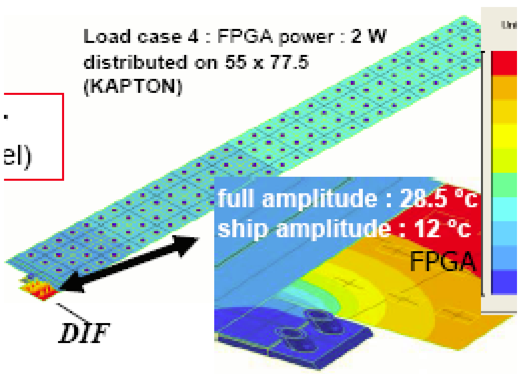
Power



ECAL : 2kW for the whole ILD detector
Constraints passed to the EUDET module
Power storage on DIF, ~10 mF

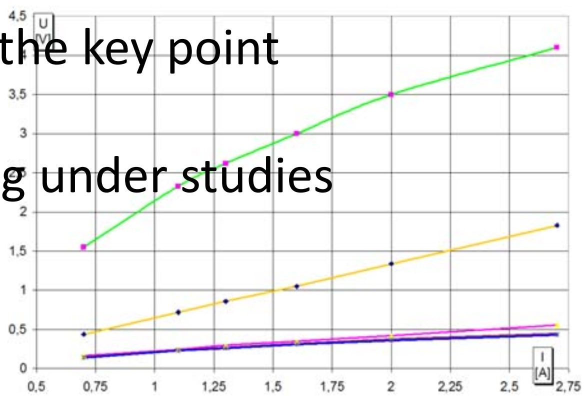




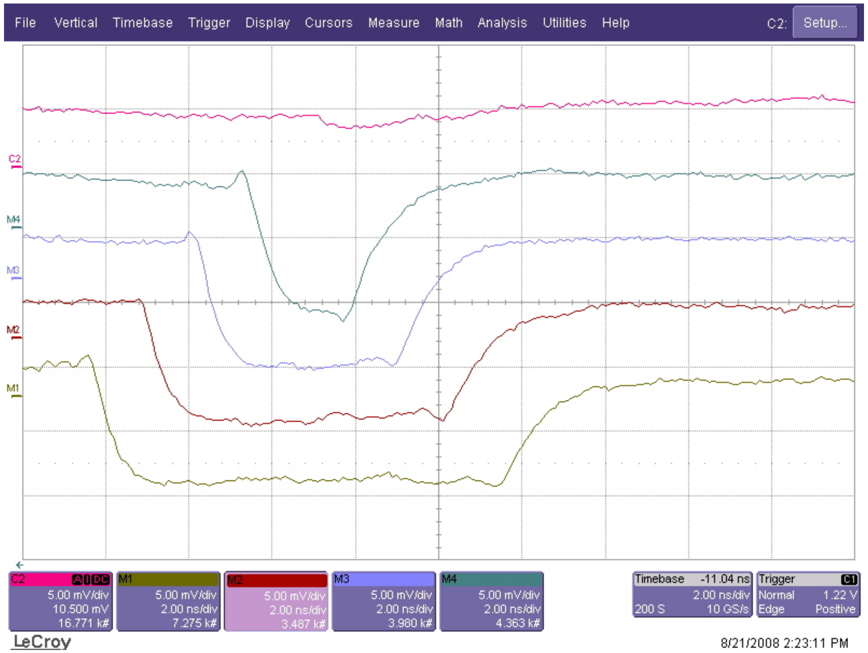


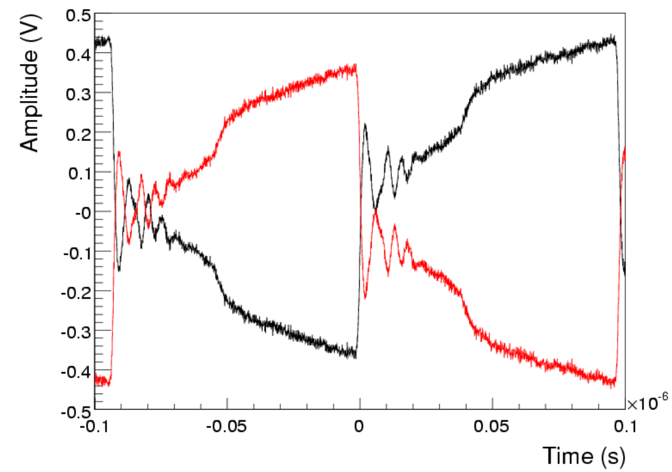
Low power but still heating…
Need thermal simulations

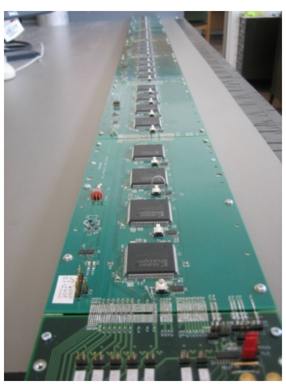
Power pulsing is the key point
1% duty cycle
ON/OFF switching under studies



Signal integrity



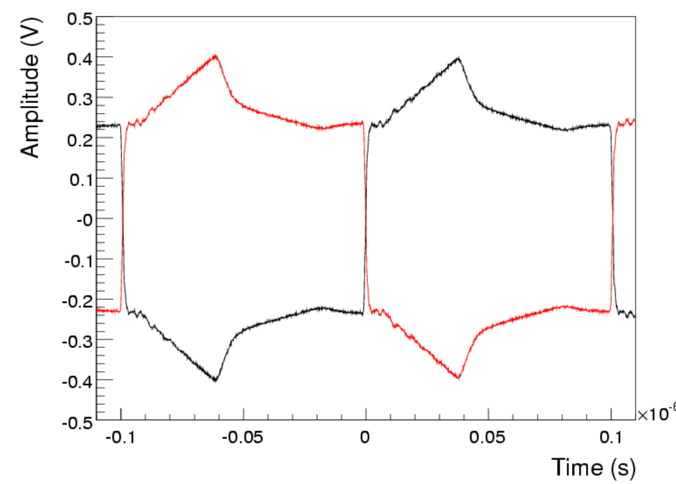




Long PCB traces

Signal integrity to be checked

Crosstalk, attenuation, jiiter



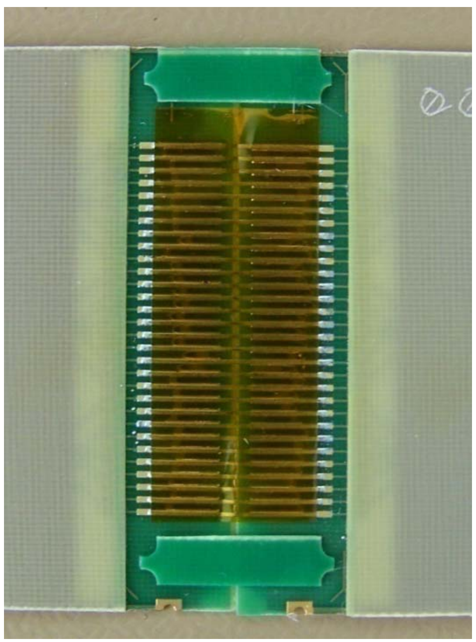
Interconnections

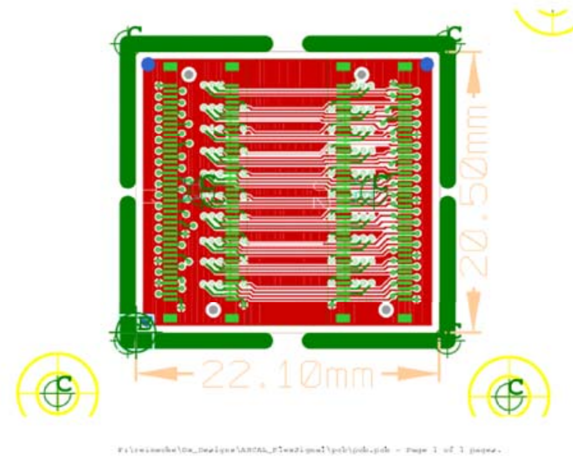
Minimized number of signal to route outside

But no room for connector

Limited thickness

→ flat Kapton “cables”





Reliability

Soldering technique vs contact resistance

Influence of heat on other components

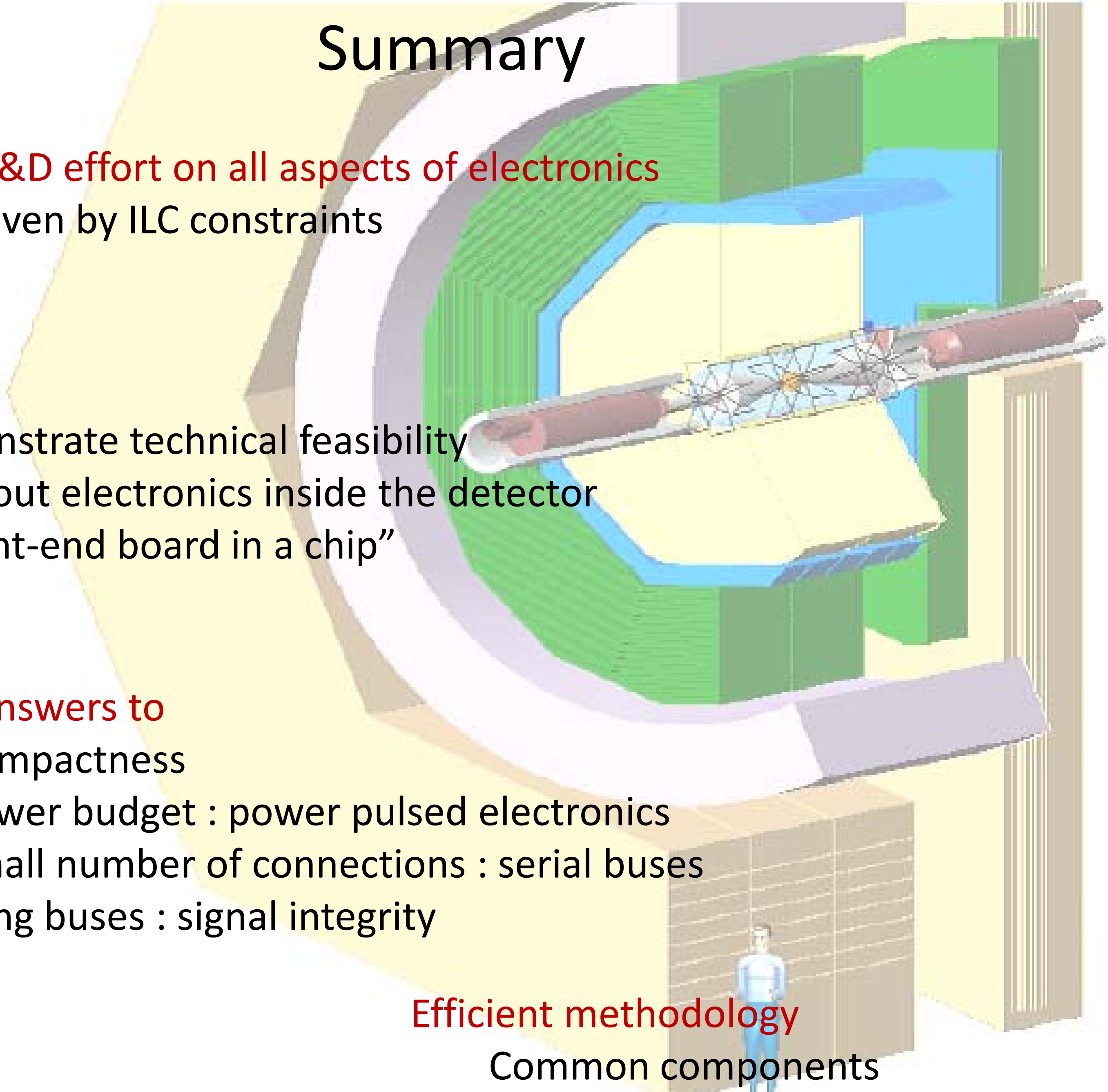
Failure rate

Behavior vs time

Time before failure

Capability to dismount for repair operations

Summary



Huge R&D effort on all aspects of electronics

- Driven by ILC constraints

Next step

- Demonstrate technical feasibility
- Read-out electronics inside the detector
- “A front-end board in a chip”

Bring answers to

- Compactness
- Power budget : power pulsed electronics
- Small number of connections : serial buses
- Long buses : signal integrity

Efficient methodology

- Common components
- Shared designs