Development of Pair Monitor

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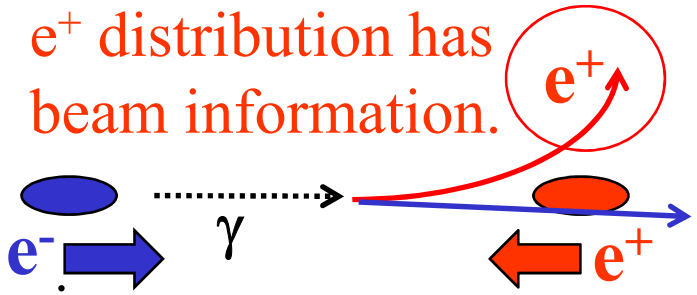
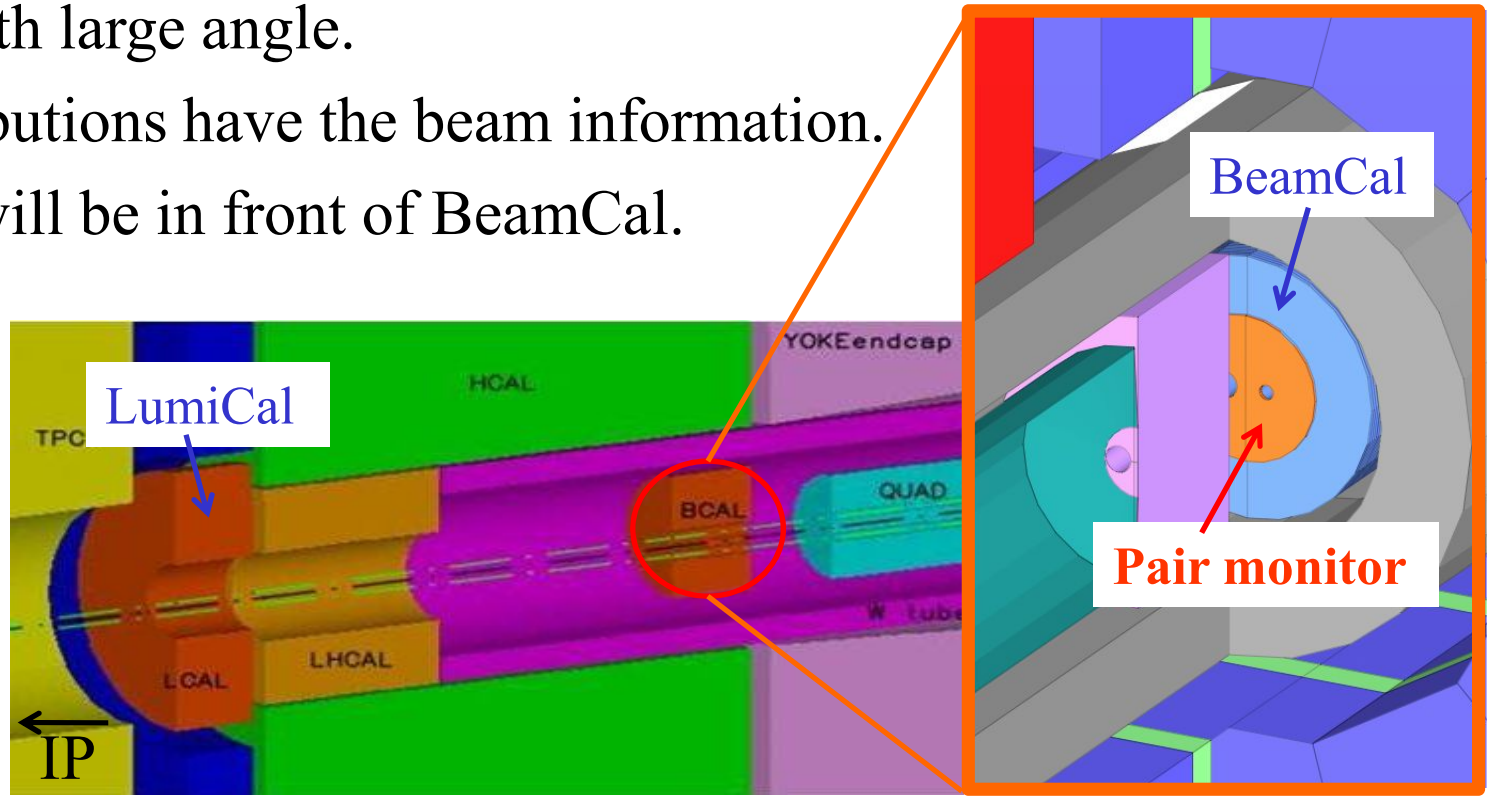
Pair monitor

Pair monitor

- Monitor of the beam profile at IP.
- The distributions of the pair B.G. is used.
  - The same charge with the oncoming beam is scattered with large angle.
  - The distributions have the beam information.
- The location will be in front of BeamCal.



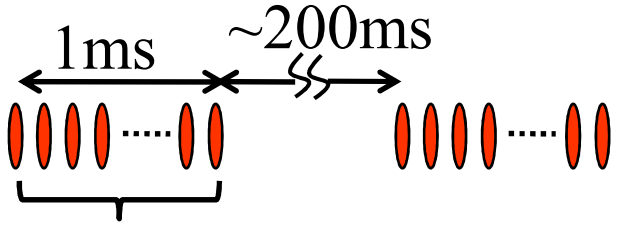


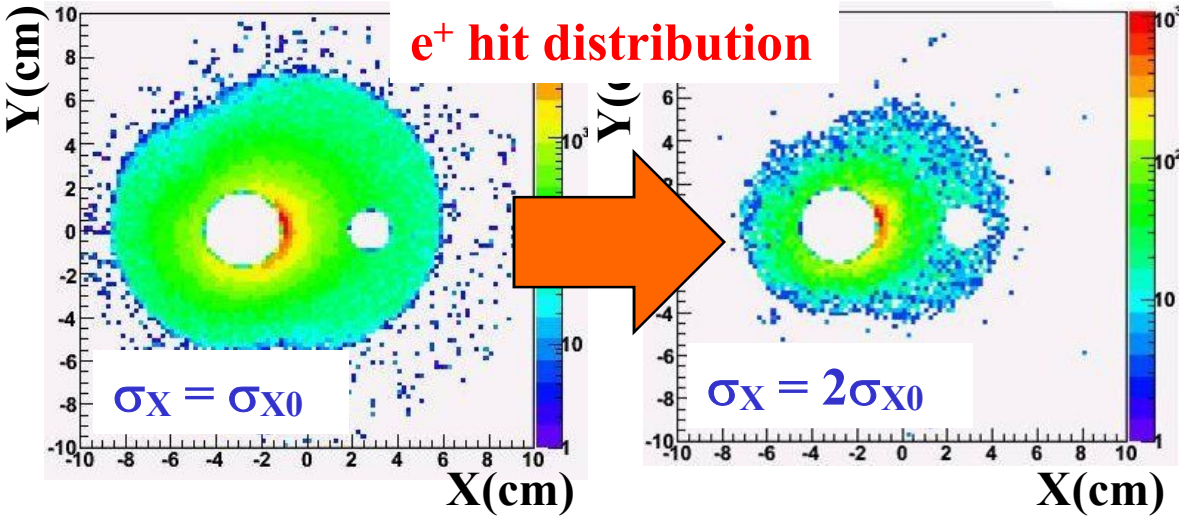
Requirement to pair monitor

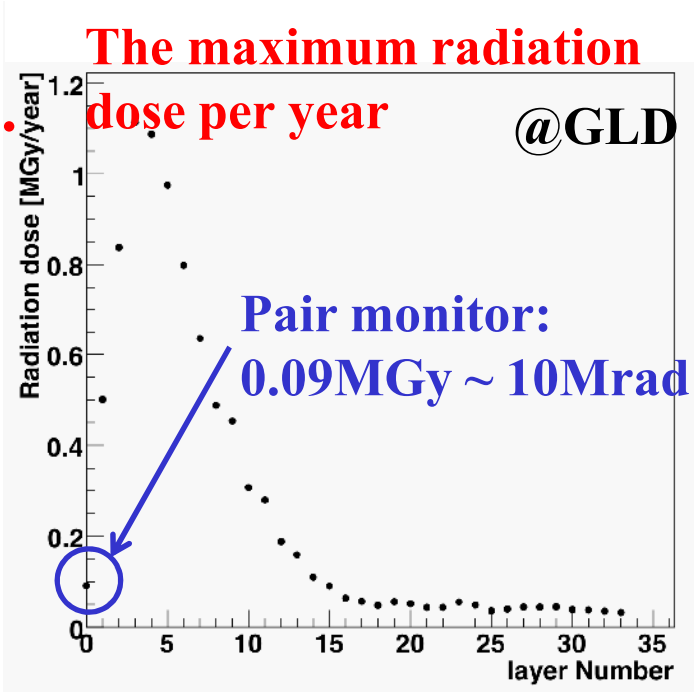
Requirement to pair monitor

- Pair monitor measures the hit distribution for train by train.
- The data should be readout within inter-train time (200ms).
- Radiation tolerance: >1Mrad/year

→ **Development of pair monitor was started.**





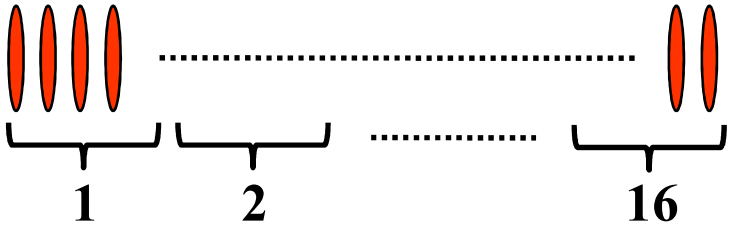


Development of readout ASIC

As the first step, readout ASIC was developed.

Design concept of readout ASIC

- The pair monitor measures the distributions of the pair-B.G. .
- Hit rate for one pixel : < one hit per 300ns (~4MHz)
- Measurement is done for16 timing parts in one train.
- Data is read within inter-train time (200ms).
- Si pixel detector is assumed as a detector.



The readout ASIC measures the hit count for each timing parts.

- Information of energy deposit in a detector is not necessary.

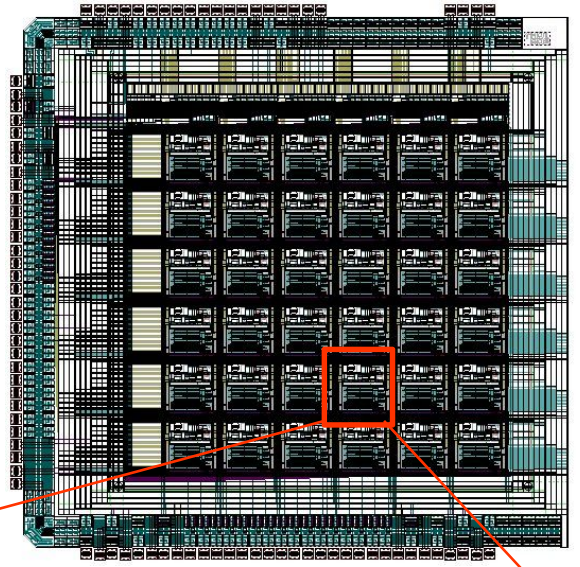
The prototype of the readout ASIC was designed to satisfy these concept.

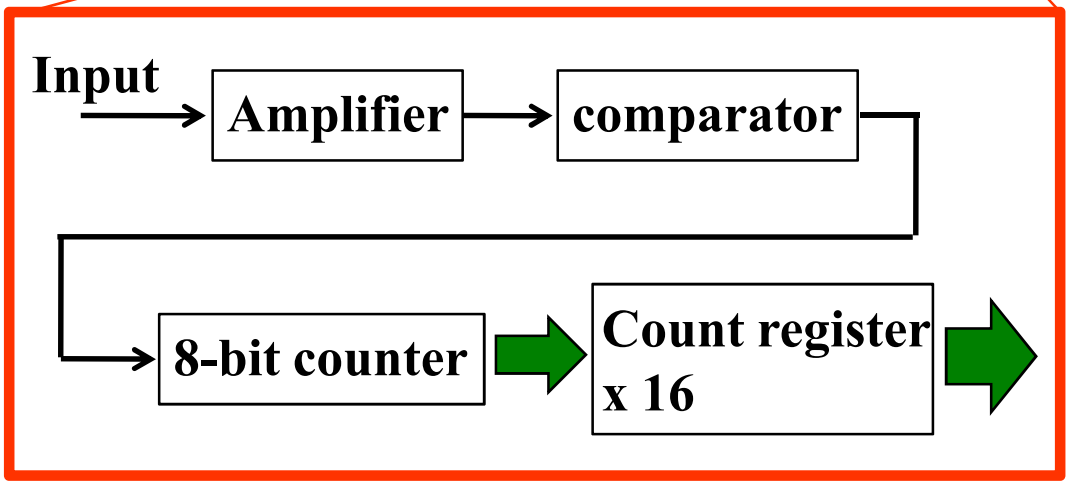
Design of readout ASIC

Design of readout pixels

- Amplifier
- Comparator
- 8-bit counter
  - A number of hits is counted.
- 16 count-registers
  - Hit counts in each timing parts are stored.

Layout of prototype ASIC





The prototype ASIC was developed.

History of ASIC production

History of ASIC production

- 2004 : Readout ASIC for JLC was developed.
  - The ASIC was confirmed to work as designed.
- 2006: The first readout ASIC was develped for ILC
  - The input lines of the operation signals were insulated.
- 2007: The 2nd prototype
  - The MIM (Metal Insulator Metal) capacitor was not implemented.
- 2008: The 3rd protoytpe was delivered in Oct, 2008.

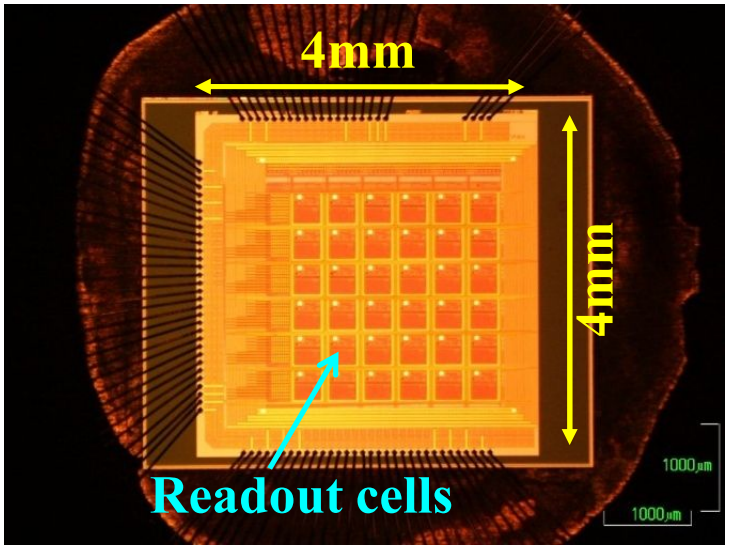
  → The response test was performed.

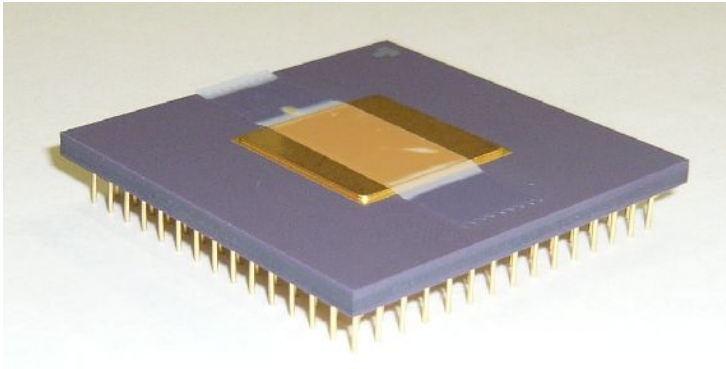
New readout ASIC

A new readout ASIC was developed in Oct., 2008.

Prototype ASIC

- Production process: 0.25 μm TSMC
- Chip size : 4 x 4 mm^2
- # of pixel : 36(= 6 x 6)
- Pixel size : 400 x 400 μm^2
- A sensor will be bump-bonded to the ASIC.
- The chip was covered by PGA144.



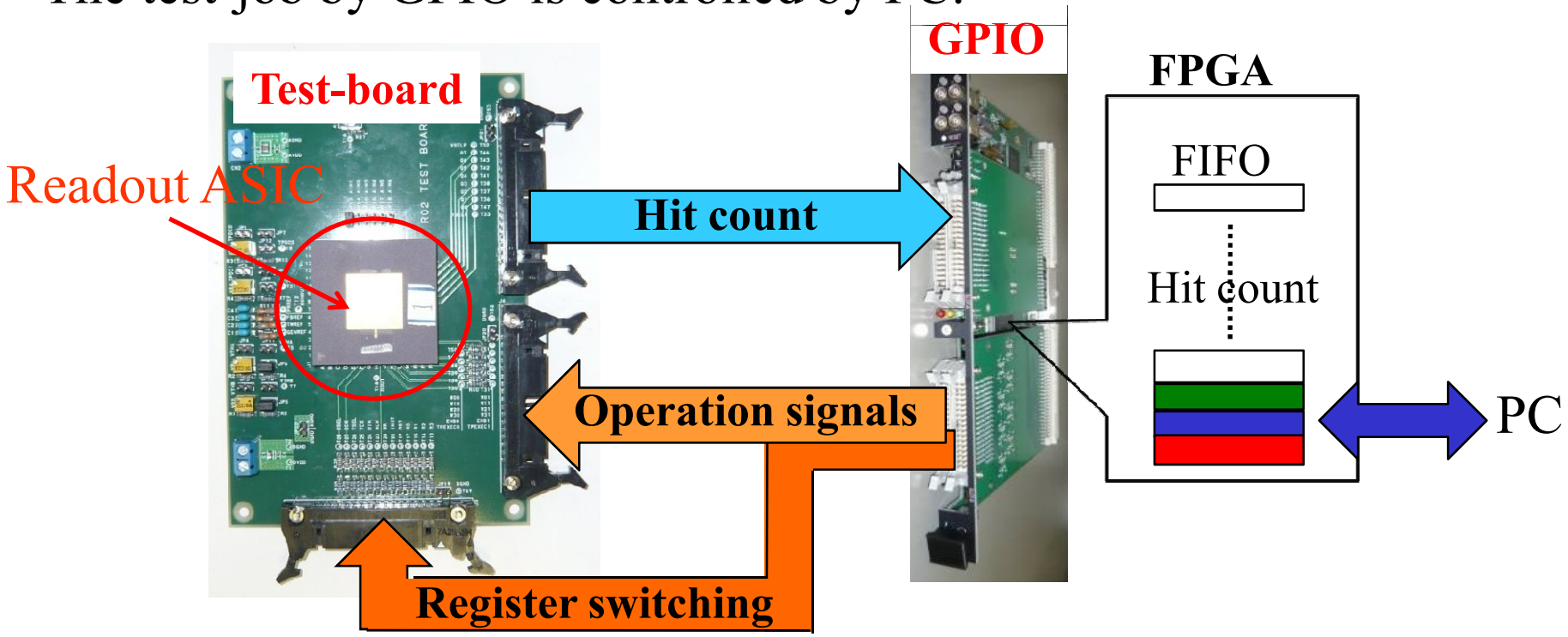


The response test was performed.

Readout system

Readout system

- VME-GPIO module was used for the operation and readout.
  - KEK-VME 6U module
  - Any logic can be realized with a FPGA.
- The test-job by GPIO is controlled by PC.

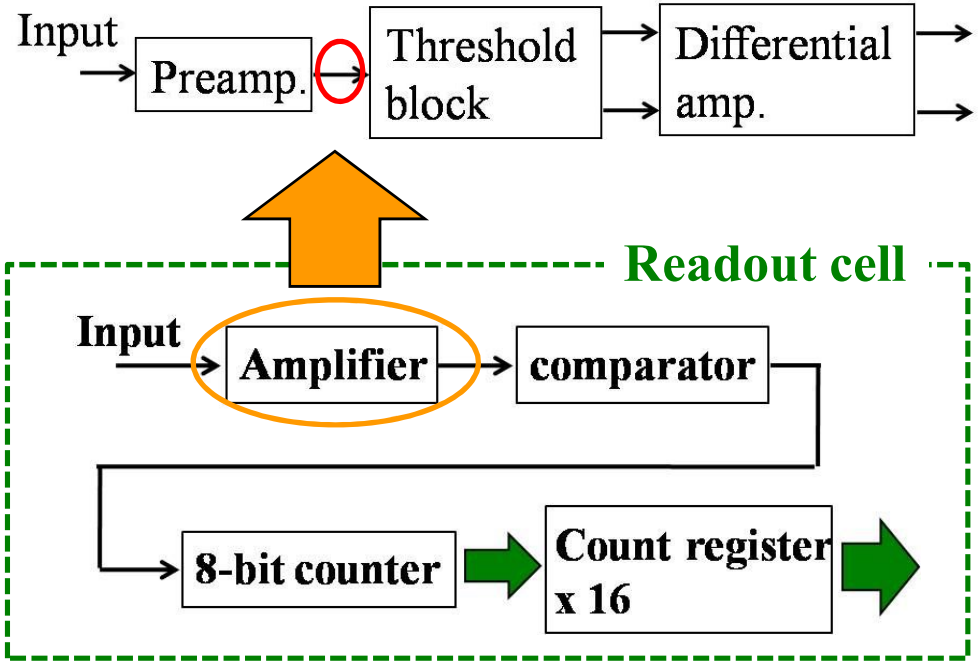


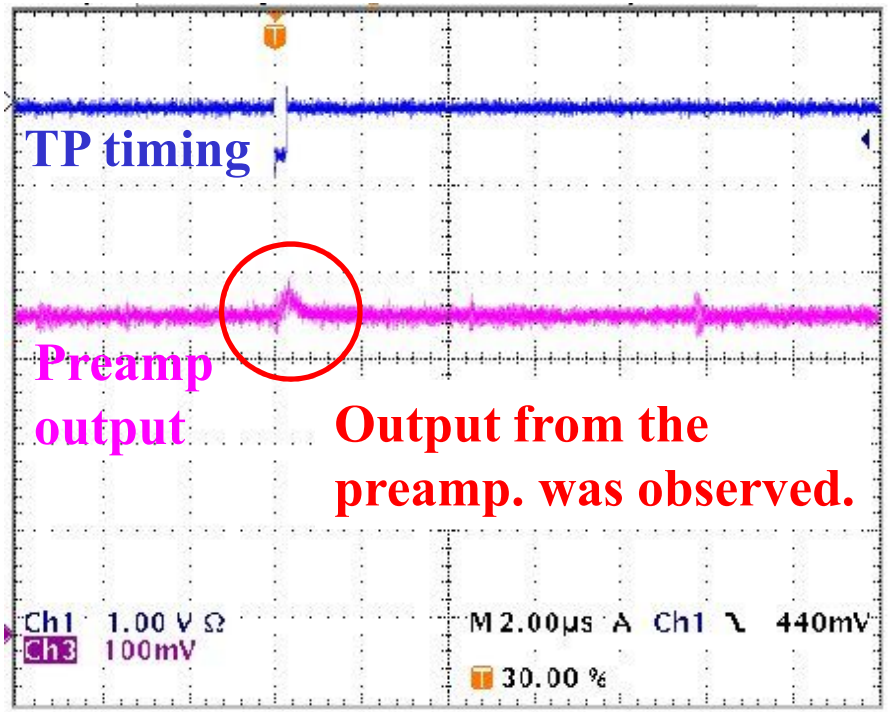
Response of pre-amplifier

The response of the amplifier block was checked.

- Amplifier block: preamplifier, threshold block, differential amplifier.
- The output from preamplifier was observed, inputting the test-pulse.

→ **The pre-amplifier works correctly**



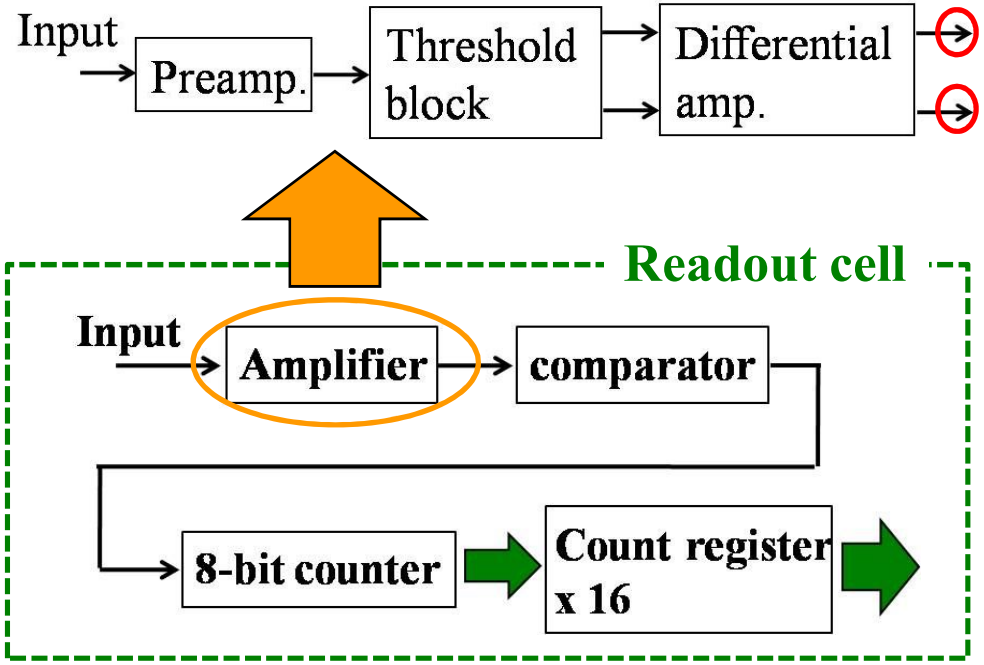


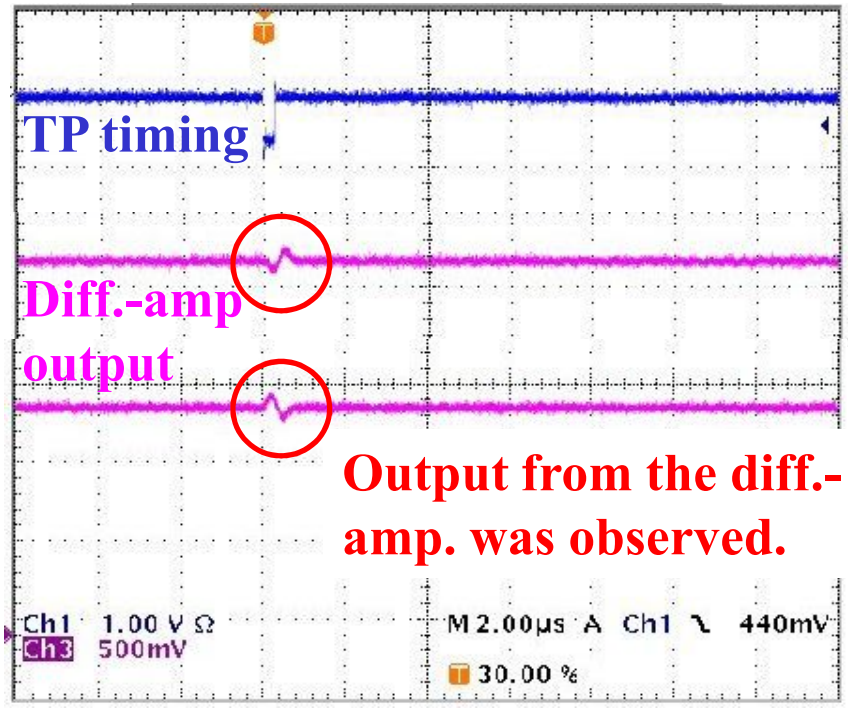
Response of differential-amplifier

The response of the differential amplifier was checked.

- In the previous ASIC, the MIM capacitor was not prepared at the threshold block.
- The output from the differential amplifier was observed.

→ **The differential amplifier works correctly.**





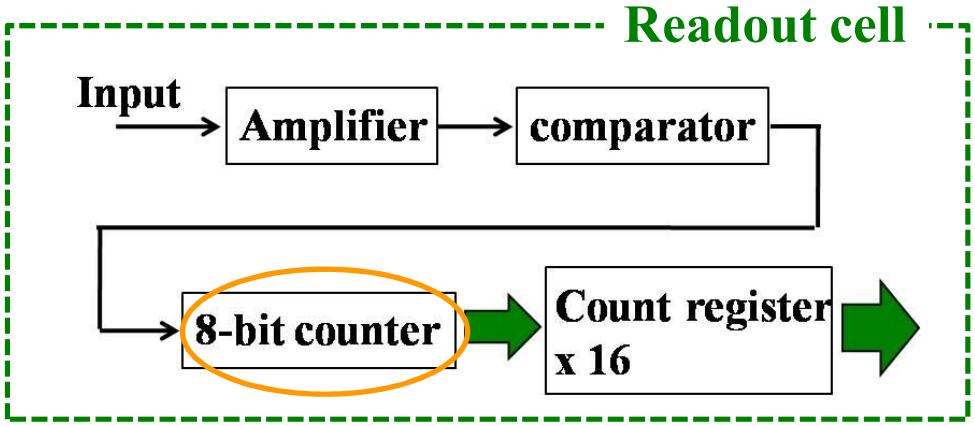
Response of counter block

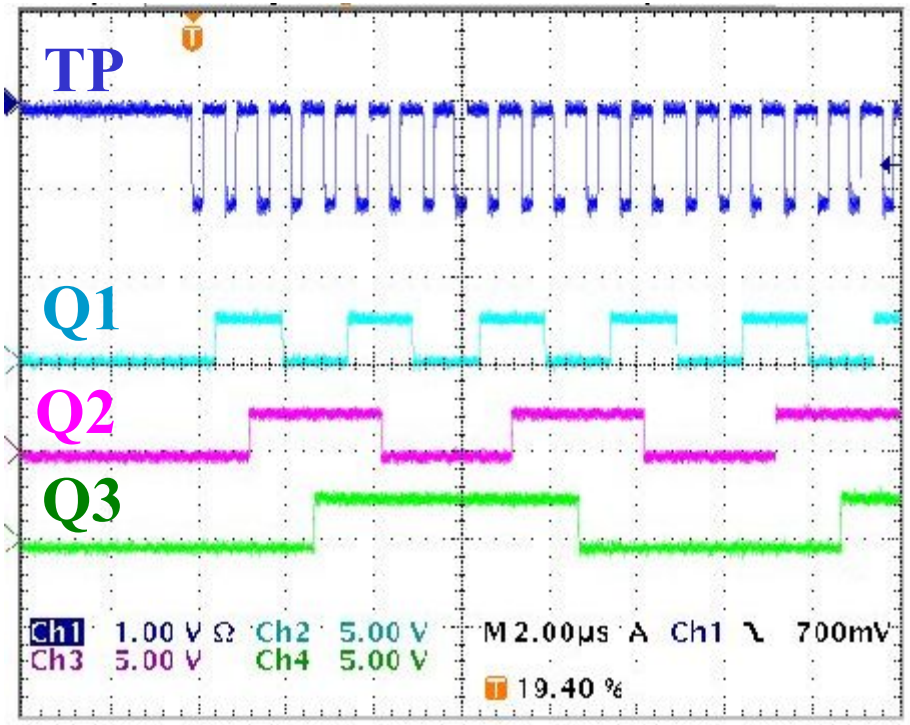
Response of the counter block was checked.

- Gray code is used for hit count.
- The hit count was output from readout ASIC.

→ **All the ASIC components work correctly!**

The hit counts was read from counter register by PC.



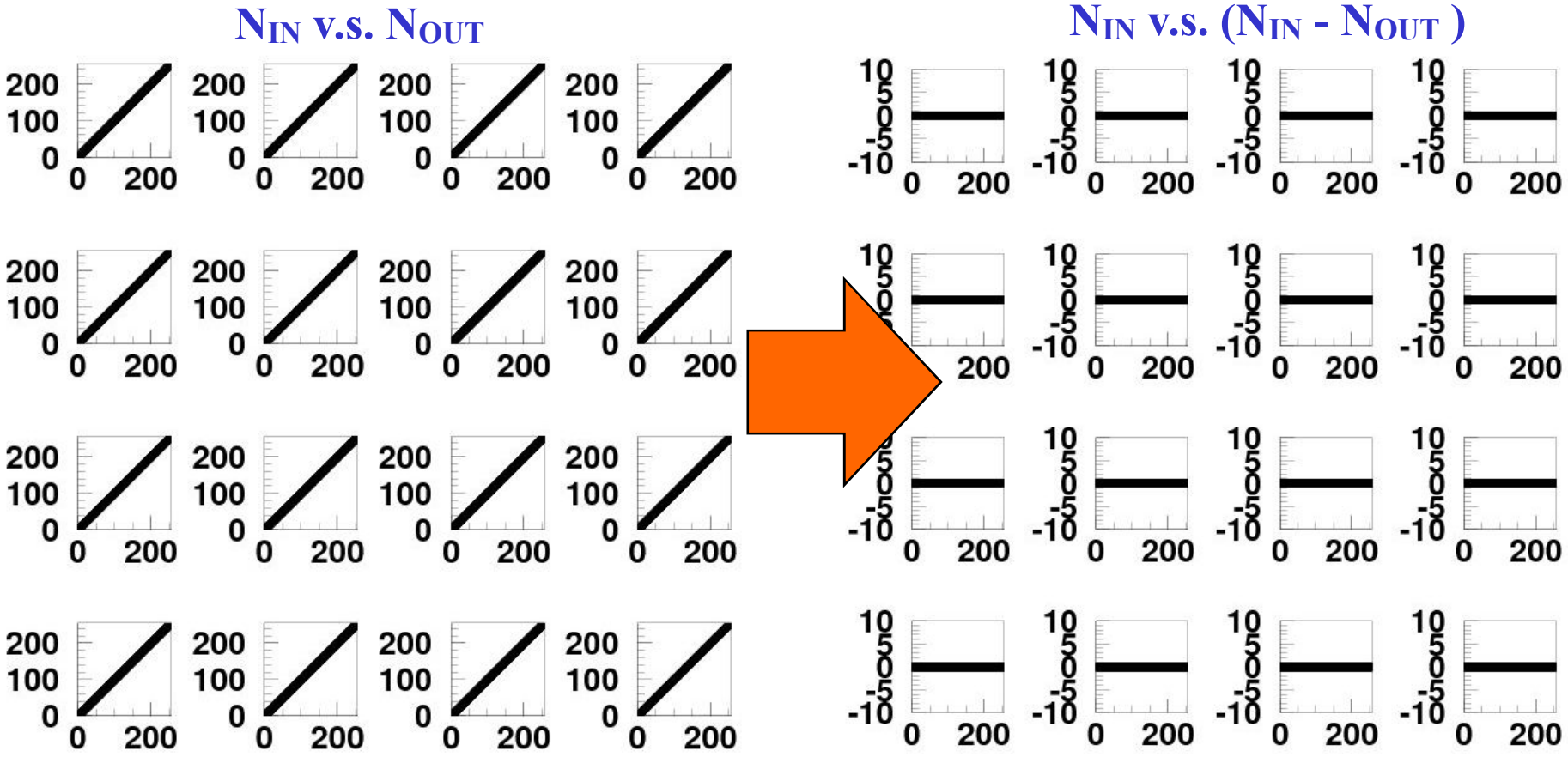


Readout-test of hit-count

The hit count was read from counter register with 1.1MHz pulse input.

→ The hit counts were read without any bit-lost.

→ **The readout ASIC was confirmed to work correctly as designed.**



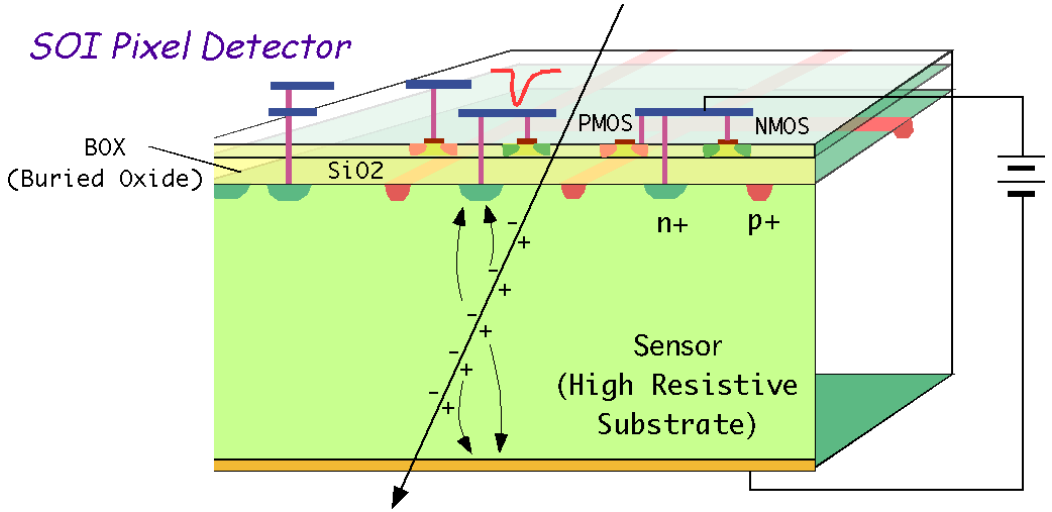
Pair monitor with SOI technology

Development of the pair monitor was started with SOI technology.

Pair monitor with SOI technology

- This project is performed as a collaboration with KEK and Tohoku university.
- The sensor and readout ASIC will be prepared in the same wafer.
  - For the next prototype, only the readout ASIC will be developed.
- The design was finalized and the layout was ordered.

The first prototype will be developed in 2009.



Summary

- Development of the pair monitor is studied.
- The new readout ASIC was developed in Oct., 2008.
  - In the previous ASIC, the MIM capacitor was not implemented between the pre-amplifier and differential amplifier.
  - All the circuit blocks work as designed.
  - The number of the hits could be read from hit registers correctly.
- Pair monitor will be developed with SOI technology.
  - The design of the readout ASIC was finalized.
  - The first prototype will be developed in 2009.

Problem in MIM capacitor

The reason of the snapping between the pre-amplifier and threshold block was investigated.

- MIM(Metal Insulator Metal) capacitors are used in the threshold block.
- The layout mask for the MIM capacitor was not prepared.

  → The layout mask was modified.

New readout ASIC will be delivered in Oct., 2008.