Continuous Acquisition Pixel detectors with time encoded binary readout

LCWS08 - Chicago

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University of Hawaii

SOI devices in Collaboration with
Y. Arai – KEK
M. Ohno – OKI Semiconductor

Contents

Brief status report – binary CAP detectors

- CAP4 and CAP5 (SOI): first binary prototypes in 2007
- CAP7: follow up in SOI, expected 11/2008
- Simulation

Binary readout concept

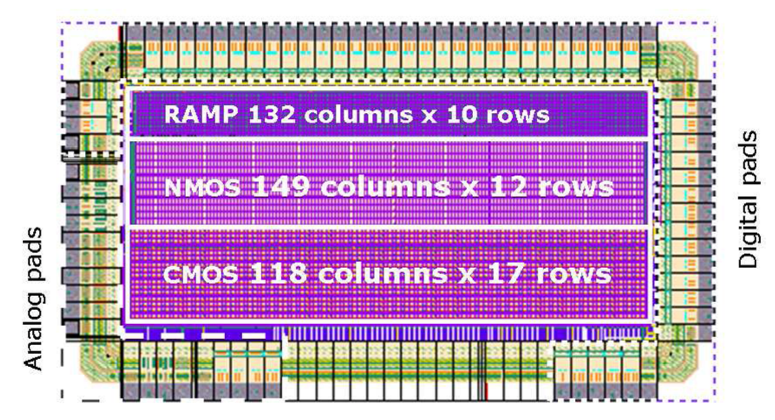
- Explanation of time encoding and reconstruction
- Fake hit reconstruction
- Implications for effective occupancy

New hexagonal binary readout

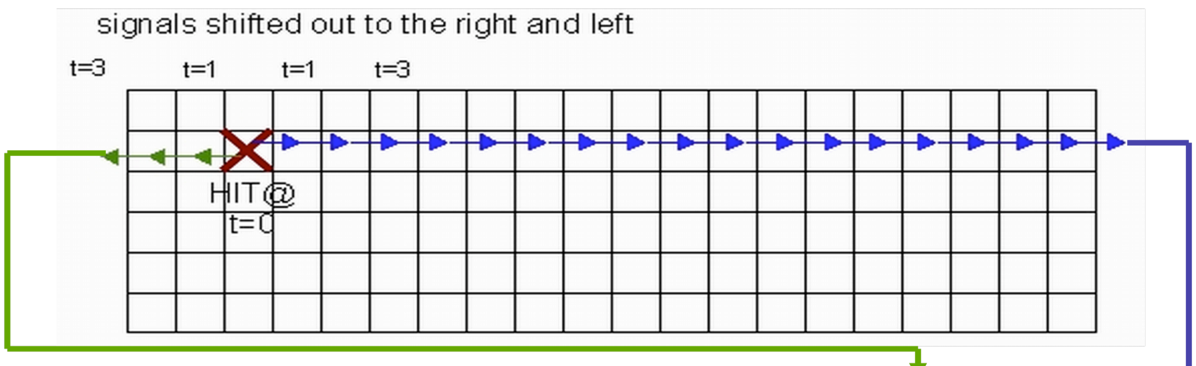
- Motivation of new concept: achieve very low occupancy
- Simulation results for occupancy
- Numerous advantages
- Prototype CAP7

Outlook

CAP4: binary concept in 0.35 µm AMS Opto

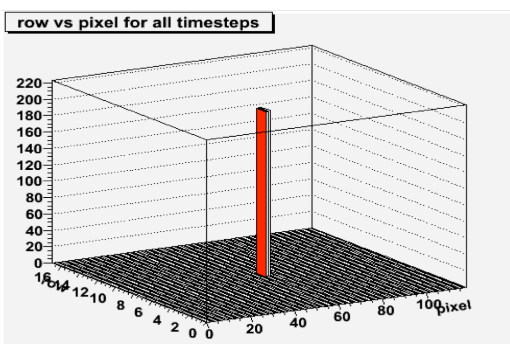


- CMOS array 118x17 pixel (25.5 x 30.9 µm^2)
- binary readout concept successfully tested with IR laser up to 2 MHz shift-cycle
- identified problem: pixel chatter
- designed by Elena Martin

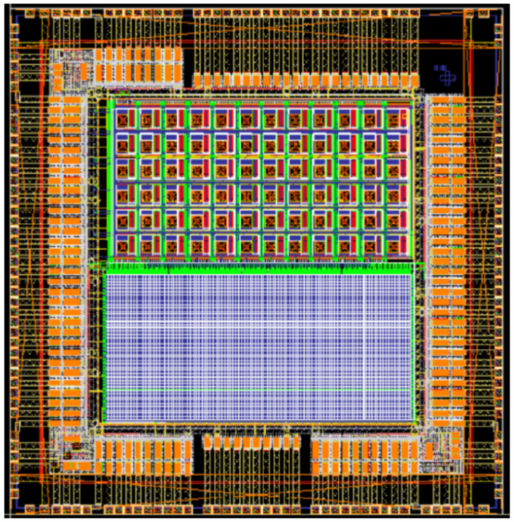


re-arranged data output:
left out signal : 00010000000000000000…
right out signal : 00000000000000000100…

hit reconstruction:
calculation of hit position and time from the timing of the left out and right out signals



CAP5 binary concept in .15 µm OKI SOI



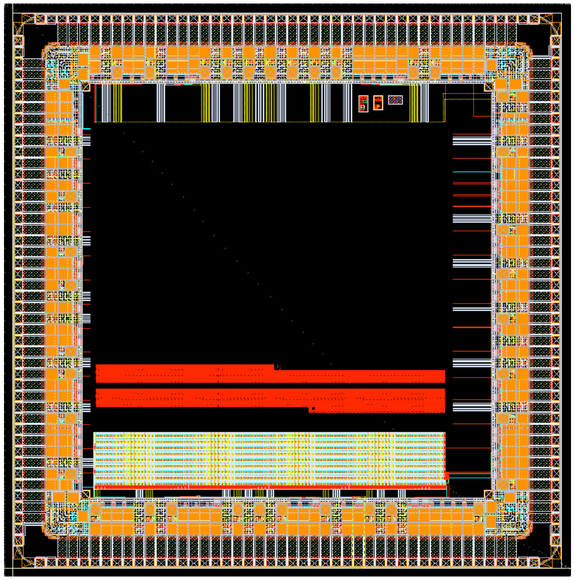
pixel matrix: 44 x 108
pixel size: 28.7 x 32.5 μm^2

designed by Elena Martin

- CAP5: binary design identical to CAP4
- participation in OKI/KEK MPW run 2007
- testing of sub-components of the pixel cell:
  - 3T cell works somehow, comparator does not
  - high sensitivity to HV: Back-Gate effect
  - discrepancies between model parameters and measured transistor characteristics
- testing on readout board unsuccessful

CAP7 design in .2 µm OKI SOI

- binary design as in CAP4/5 for 2008 OKI MPW SOI run
- transparent latch replaced by d-flip flop (no chatter)
- submitted 1/2008
- delayed due to fabrication issue
- received preliminary prototype without working diode implant – HV cannot be applied
- electronics tests of sub components check out
- final chip expected late 11/2008



total dimensions:	5mm x 5mm
active area:	~3mm x ~3mm
total pixels:	60,000
pixel cell:	35x50 μm^2
test structures	each sub-component

designed by M. Cooney

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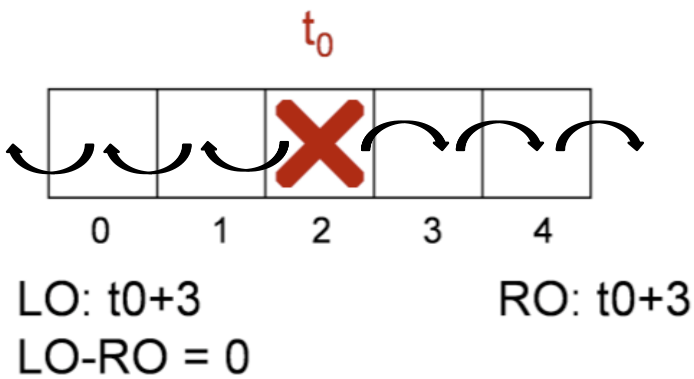
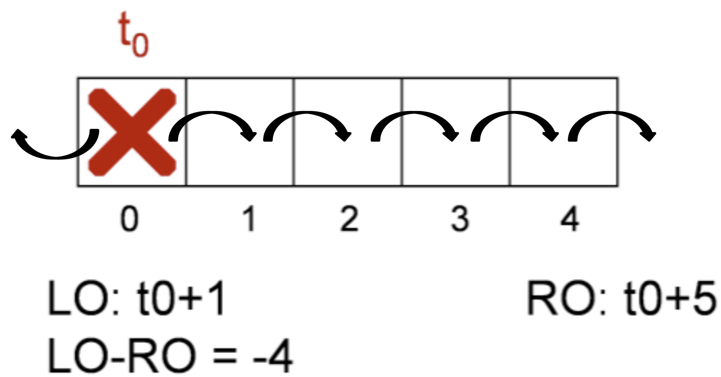
Hit reconstruction





number of pixels in a row: N

(= number of nodes in transfer line)

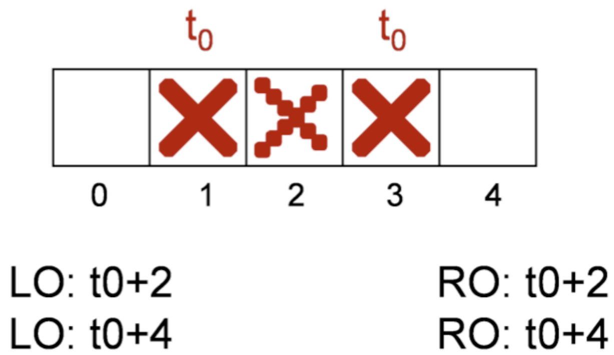
signal time difference: $\Delta t_{LR} = t_{LO} - t_{RO}$

hit address: $P_{hit} = \frac{N-1}{2} + \Delta t_{LR}/2$

hit time: $t_{hit} = t_{LO} - P_{hit} - 1$

max. time window for data collection: N-1 shift cycles

Fake hit reconstruction



- additional signals due to BG events during data collection window
- false signal pairs reconstructed as fakes
- can usually be rejected by trigger
- in larger arrays under high BG conditions fakes at trigger time are possible!

Fake hits have to be taken into account in calculation of effective occupancy

Effective occupancy

transfer line occupancy k:

i.e. average number of signals on transfer line during data collection window

$$k = r_{BG} \cdot (N-1) \cdot \Delta t_{shiftcycle} \cdot A_{sensitive} \cdot N_{cluster}$$

with r_{BG} .....BG rate per area and second
N.......number of nodes in transfer line (pixels in row)
$A_{sensitive}$.sensitive area associated with transfer line (pixel row)
$N_{cluster}$...cluster size

average number of fakes for a given trigger

$$\langle N_{fake} \rangle = \frac{k^2}{N}$$

details published in: H. Hoedlmoser *et al.*, Hexagonal pixel detector with time encoded binary readout, accepted for publication in Nucl. Inst. Meth. A, 2008 **NIMA_48977**

Effective occupancy

MC simulation (random BG generation + reconstruction):

	pixel matrix:		
	rows	240	
	columns	800	= N
	pitch [µm]	25	
	area per row [mm2]	0.5	
	total nr of pixels	192000	
	cluster:		
	nr. pixels / hit on row	2	
	shift clock [MHz]	2	10
	shift cycle [µs]	0.5	0.1
	transfer line occupancy k	282	56.4
	$\langle N_{rec} \rangle$ per row per trigger	99	3.98
	$\langle N_{rec} \rangle$ full matrix per trigger	23857	954
sBelle	**effective occupancy**	0.124	0.005
ILC		**0.0072**	**3E-04**

$$\langle N_{fake} \rangle = \frac{k^2}{N}$$

ILC BG estimation:	1.70E+05	hits/mm^2/s
sBelle BG estimation:	7.06E+05	hits/mm^2/s

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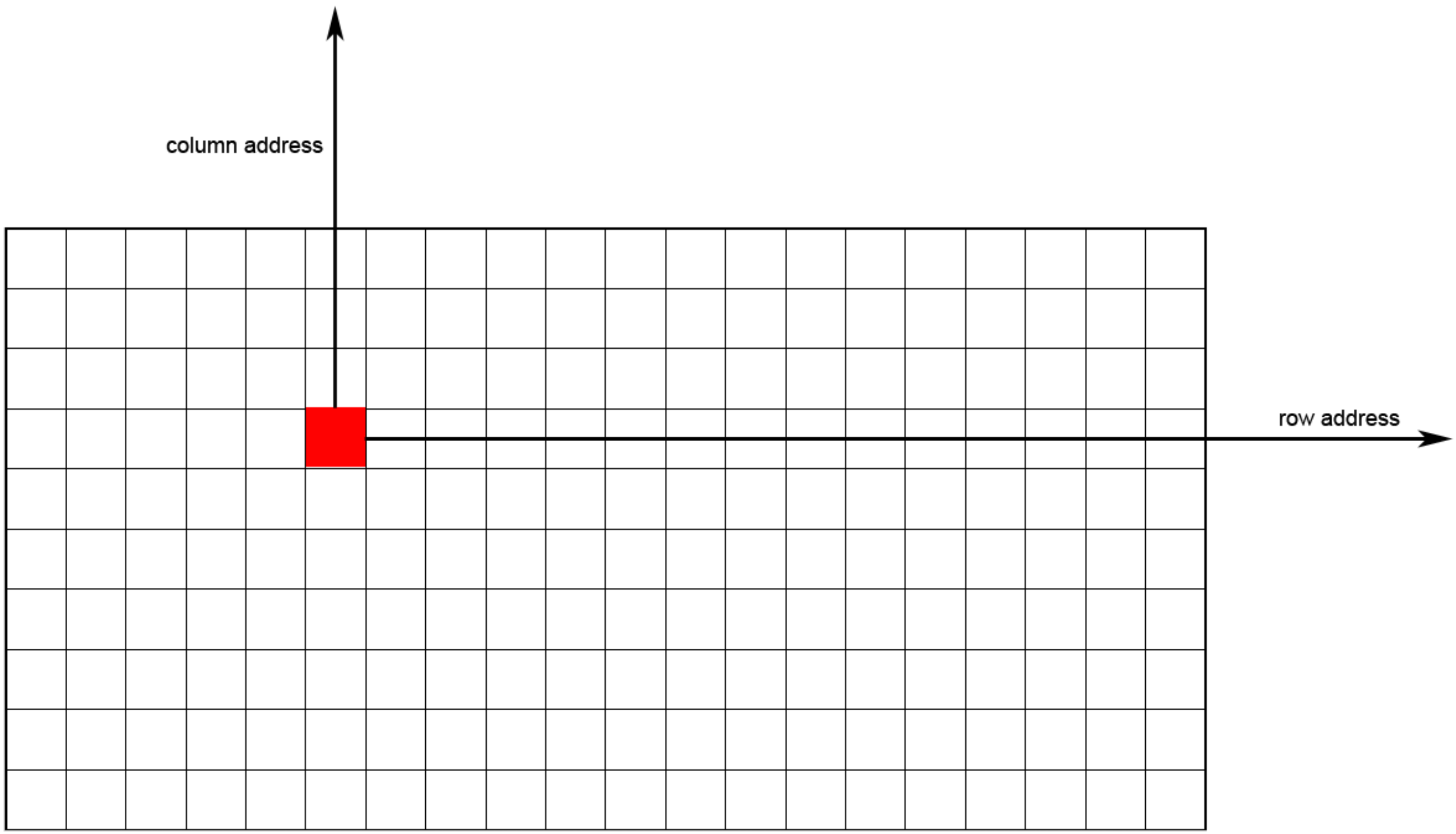
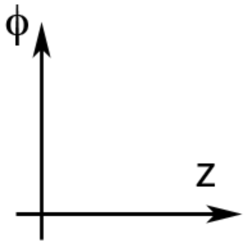
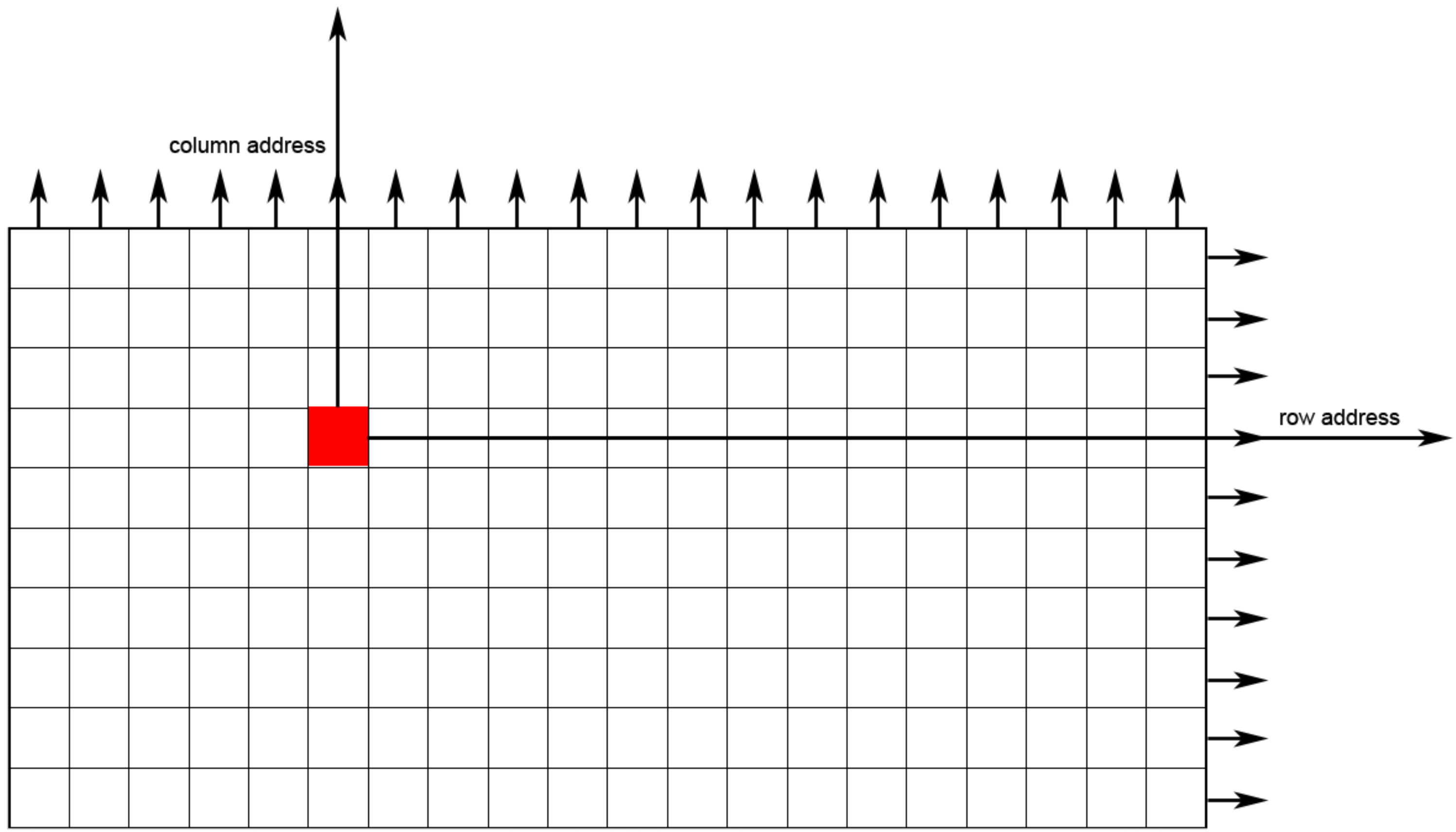
How to make a better/new pixel detector?

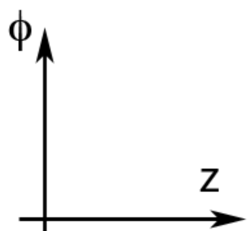




the simplest pixel concept has problems…

How to make a better/new pixel detector?

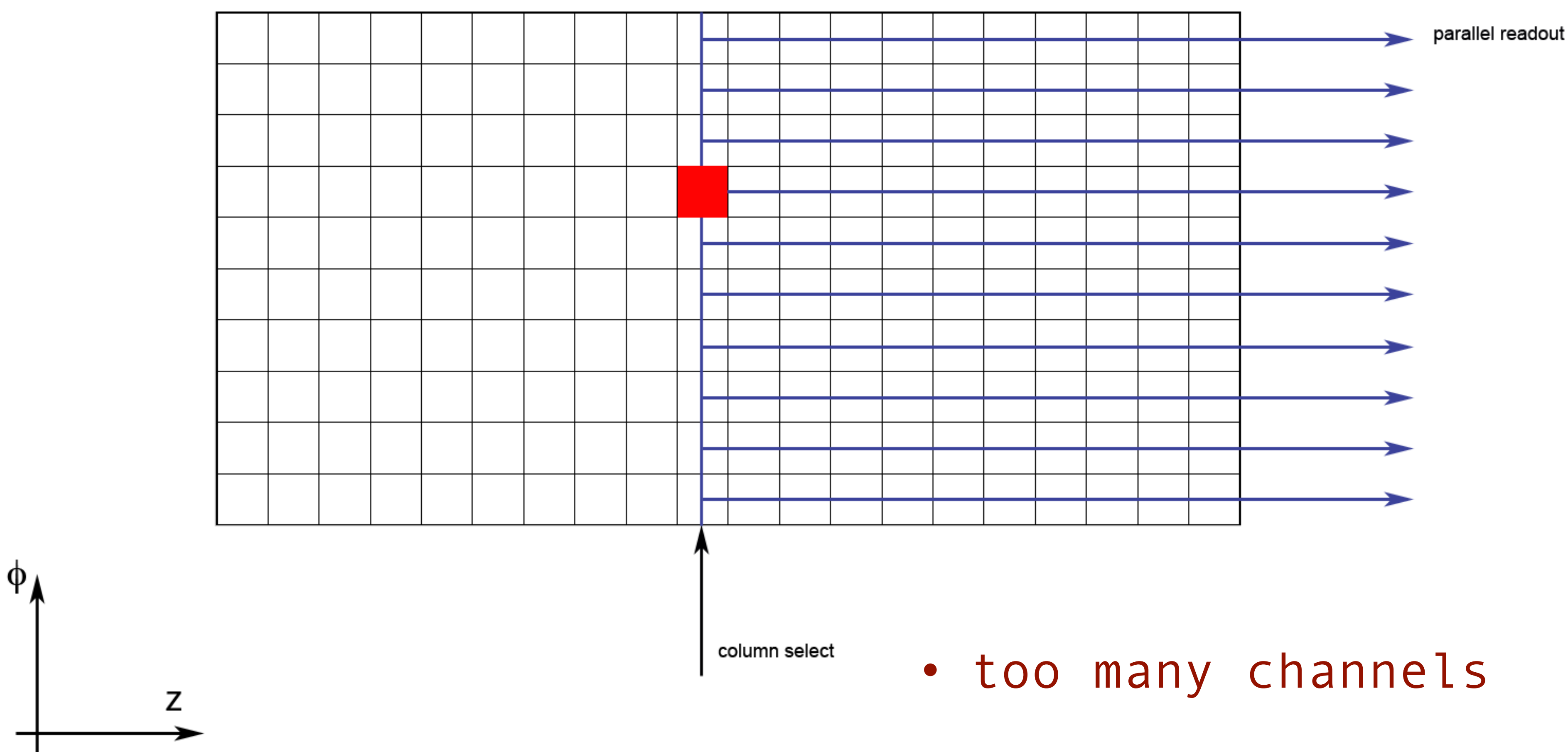




- too many channels

How to make a better/new pixel detector?

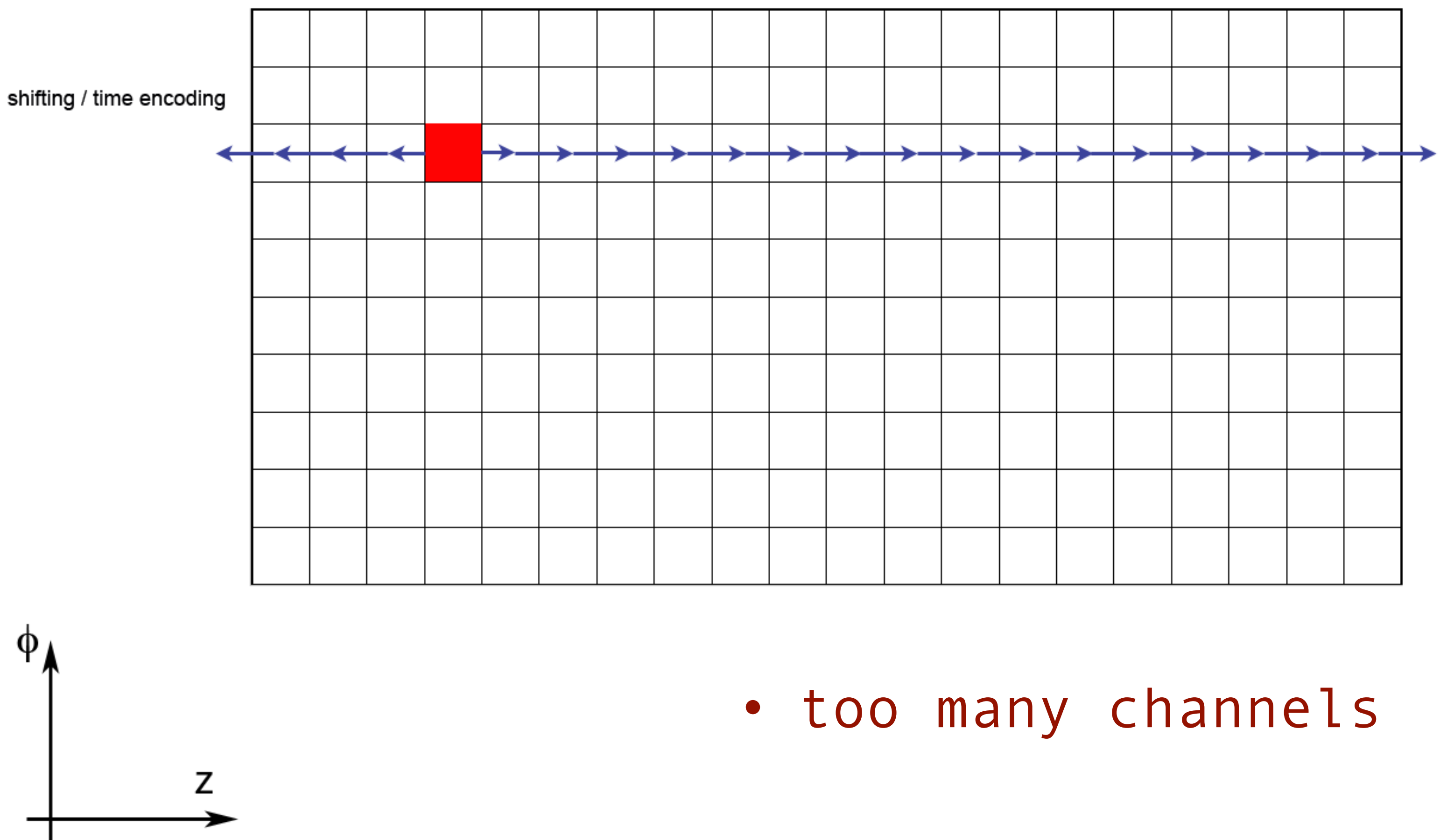
which is why one does this:



• too many channels

How to make a better/new pixel detector?

...or why we are doing this:



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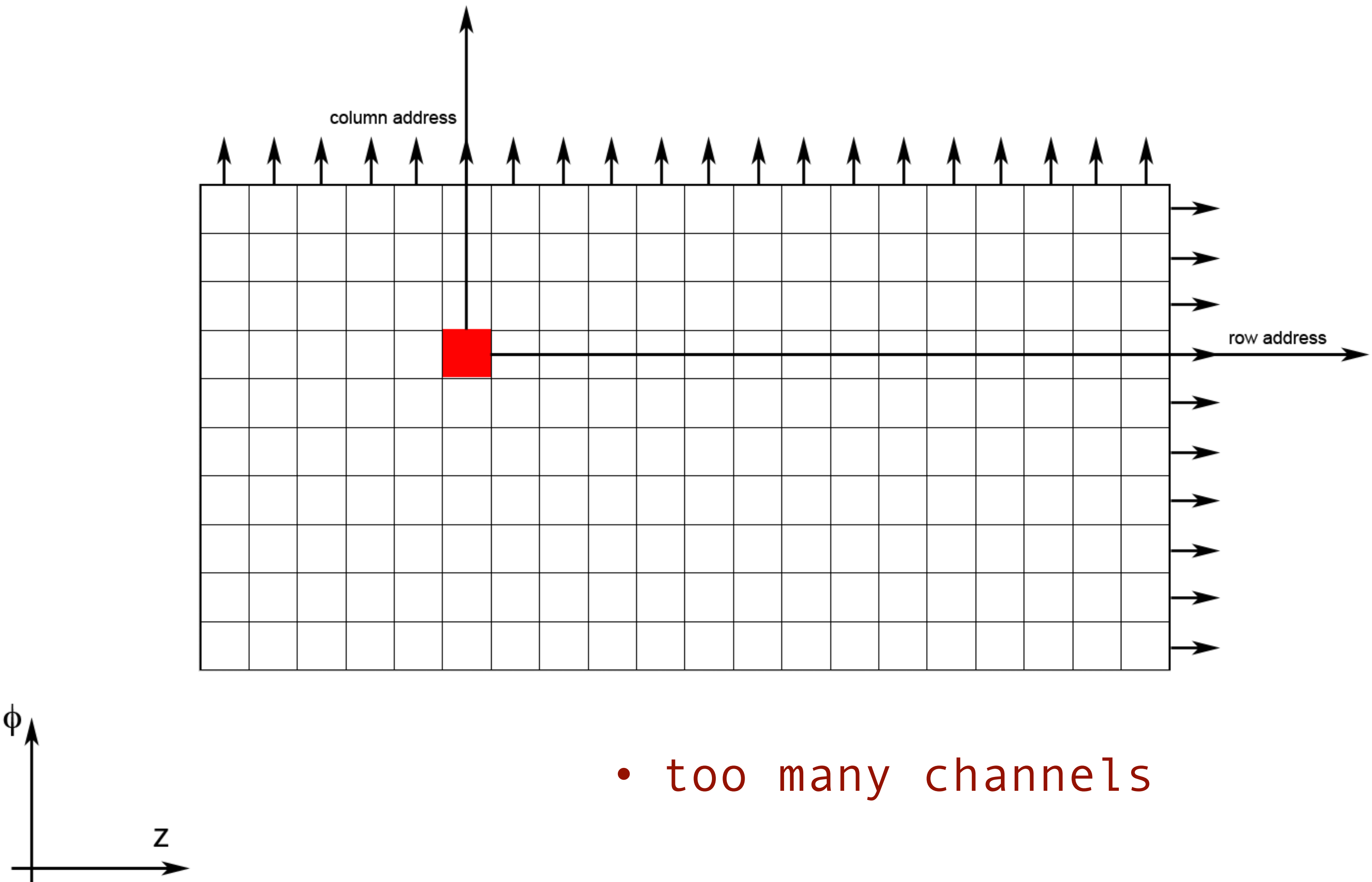

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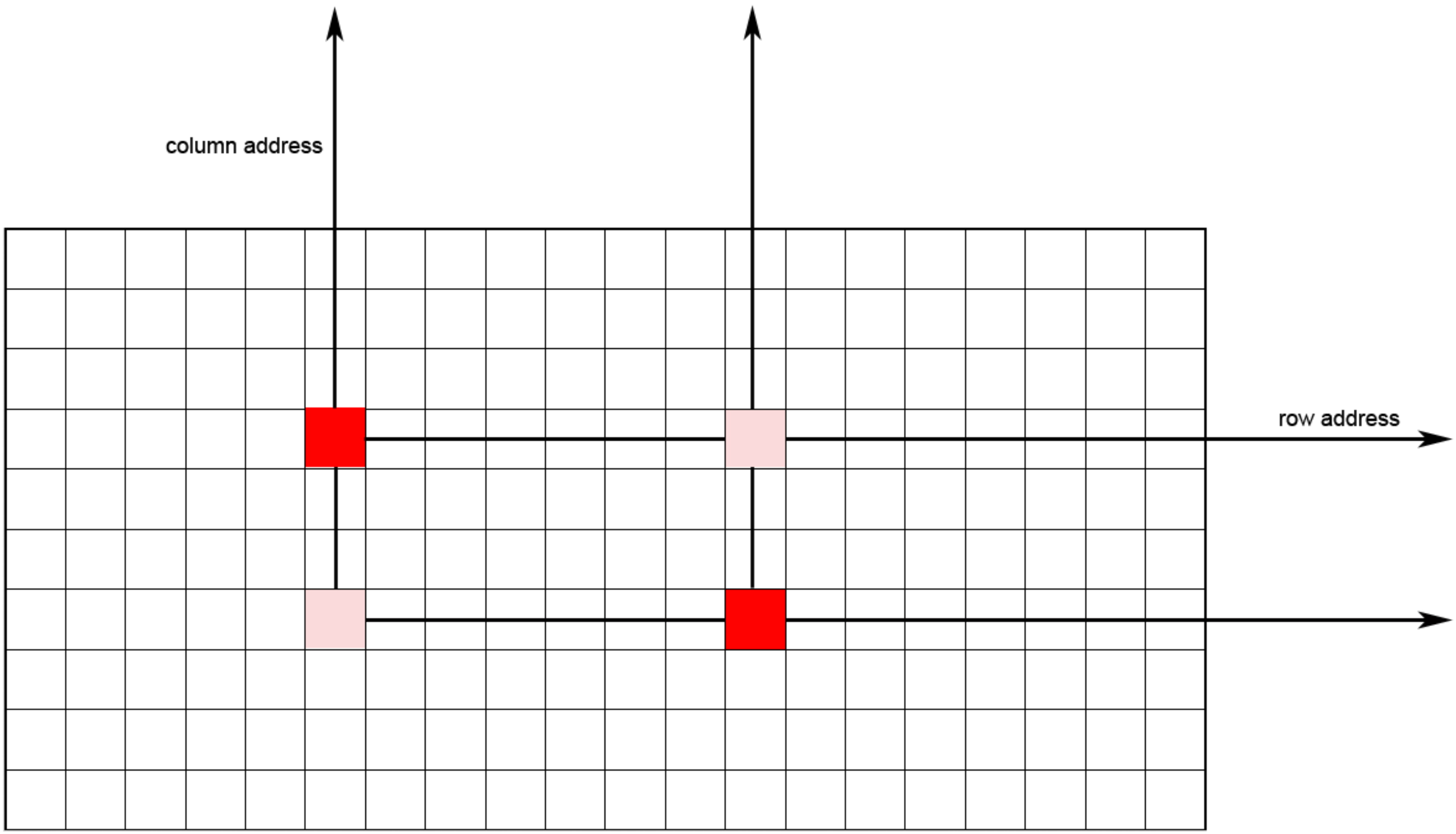
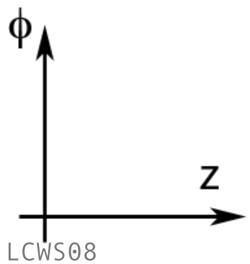
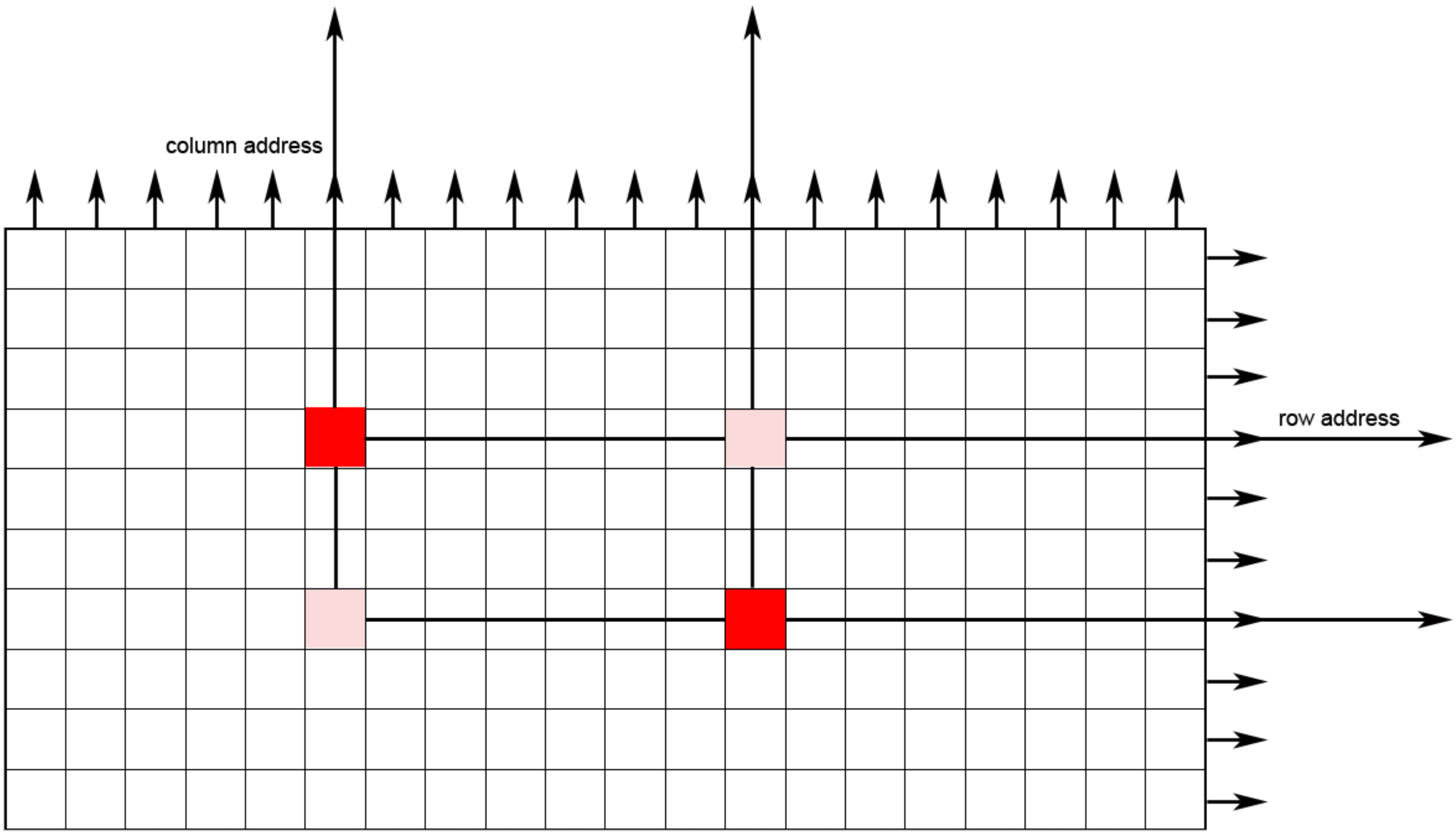




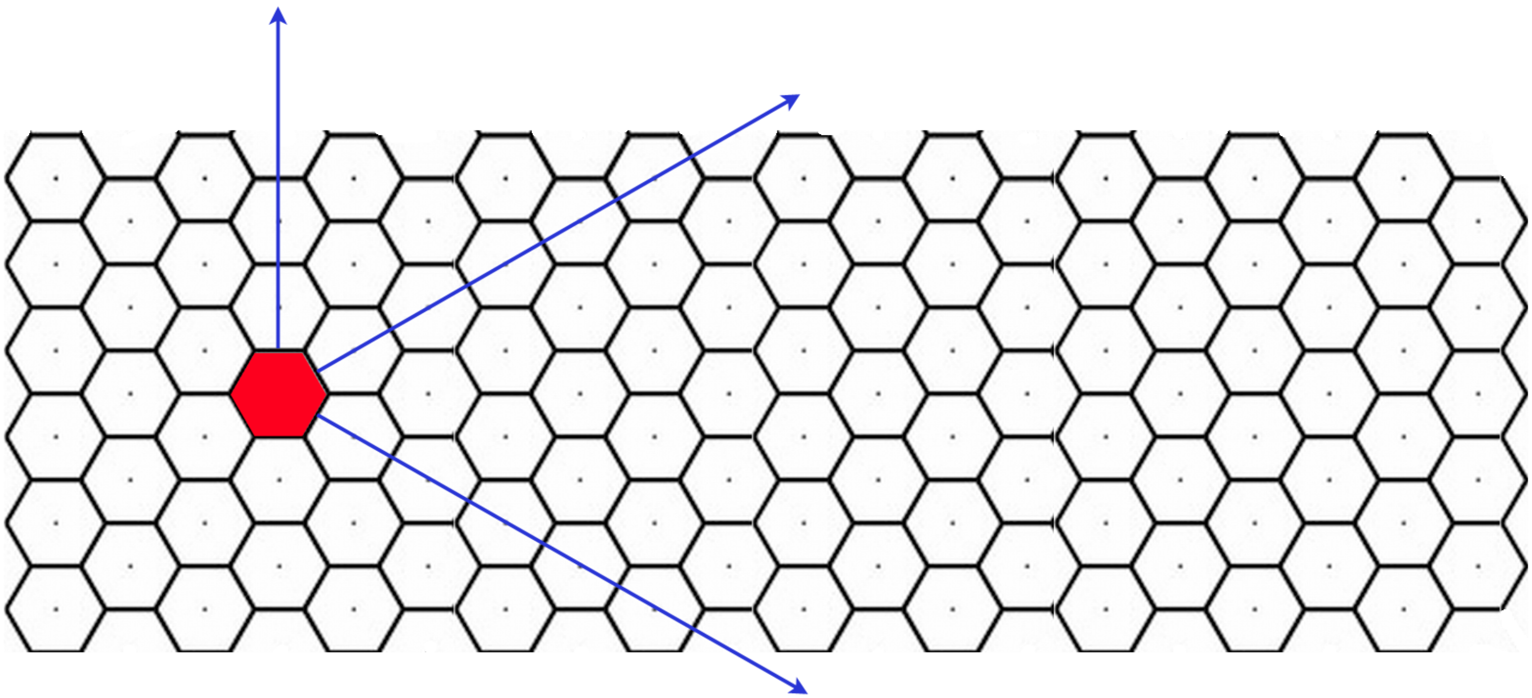
- ghost hits

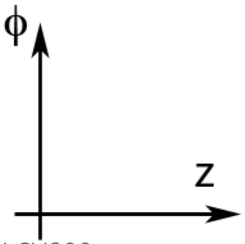
How to make a better/new pixel detector?



- too many channels
- ghost hits ...how can this be improved?

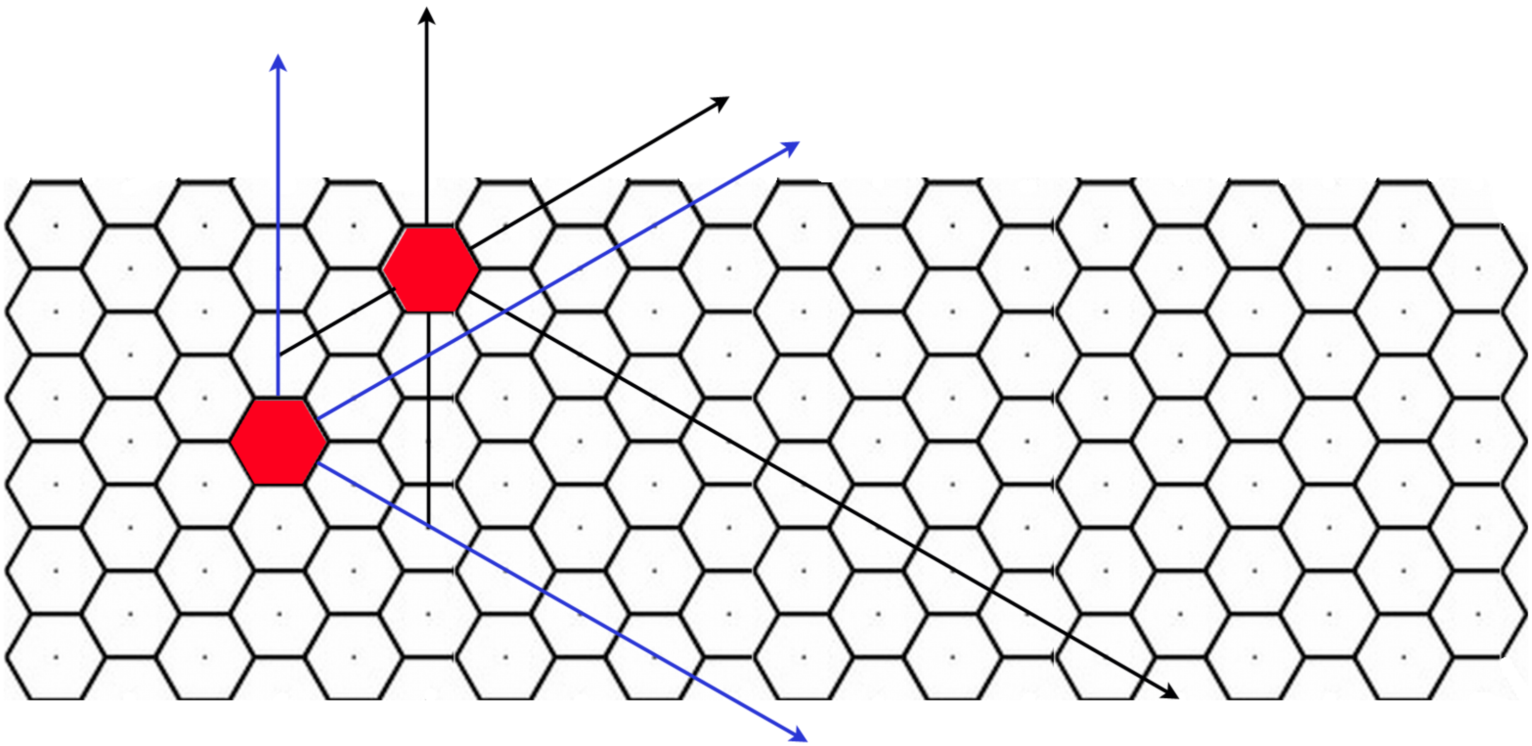
Get rid of ghosts: hexagonal routing

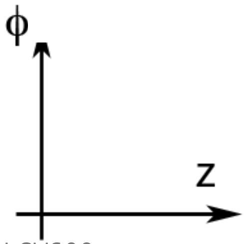




use 3rd independent coordinate

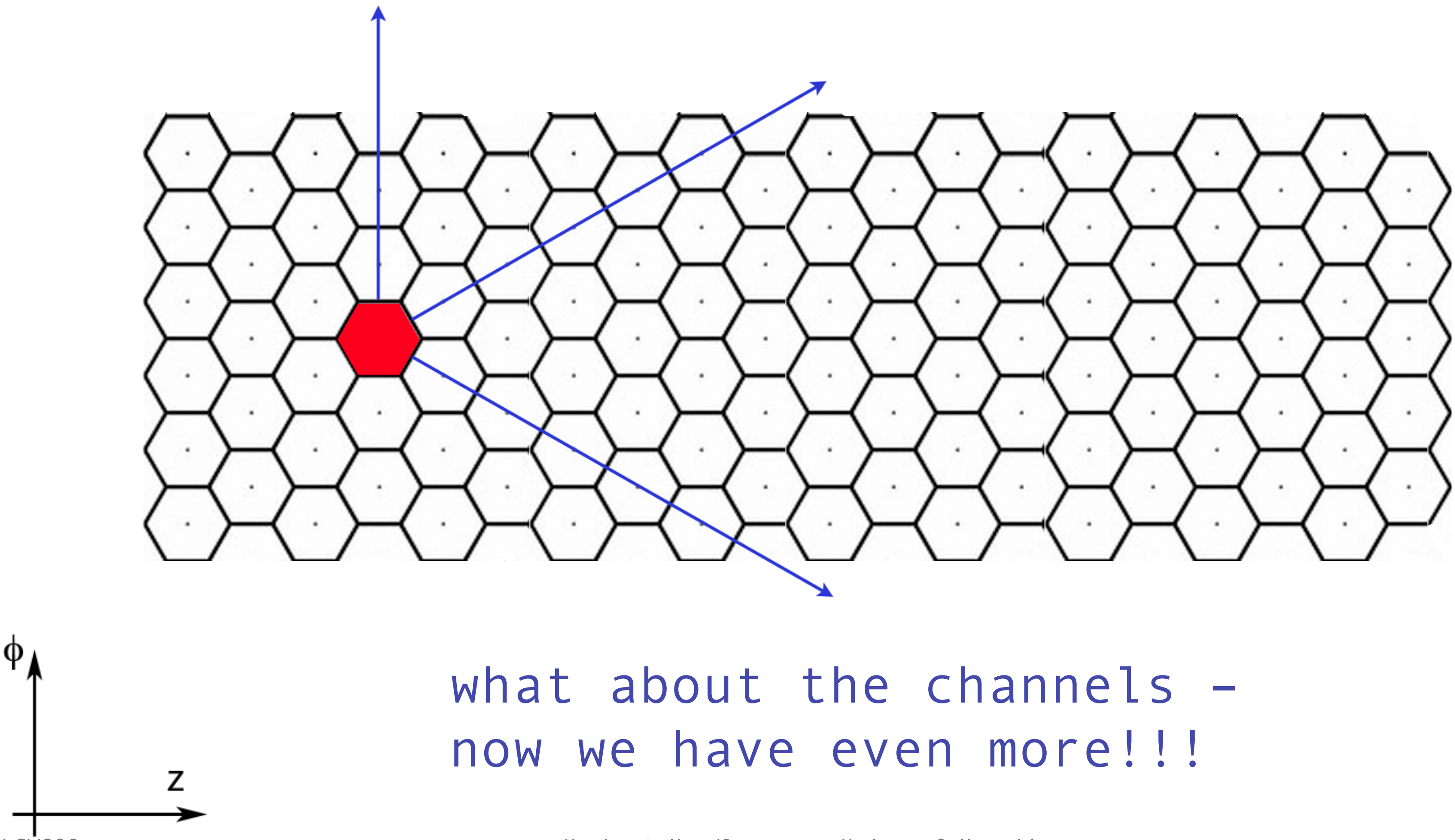
Get rid of ghosts: hexagonal routing





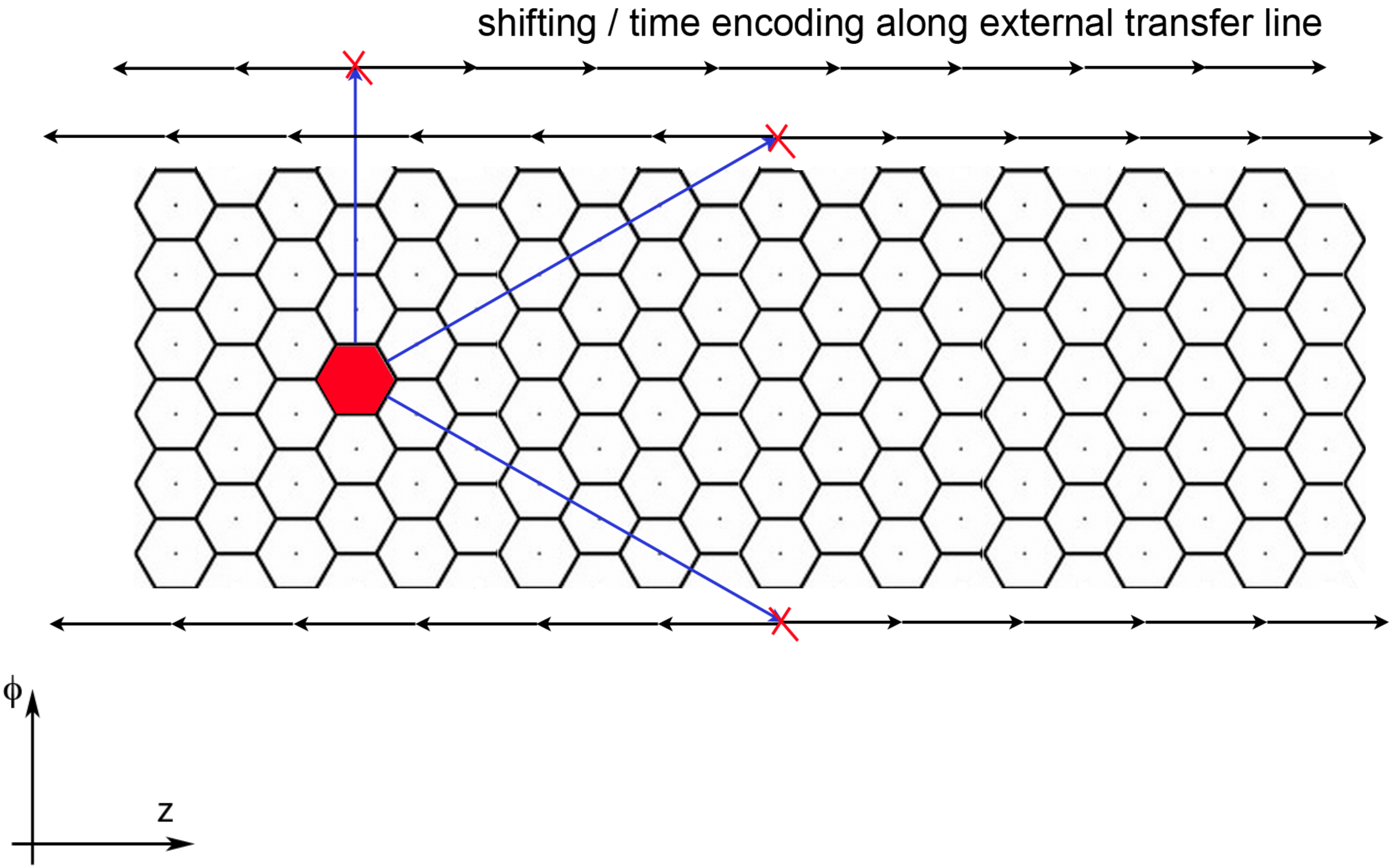
no ghosts.

Get rid of ghosts: hexagonal routing



what about the channels –
now we have even more!!!

Reduce channels: external transfer lines

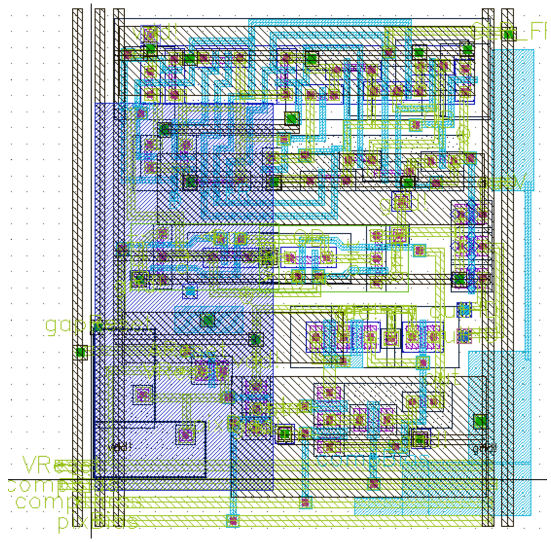



WARNING
HEXAGONAL PIXELS
DESIGNER
HIGH
LAYOUT COMPLEXITY
CAN CAUSE SERIOUS INJURIES OR DROWNING
IF IN DOUBT, DON'T GO OUT

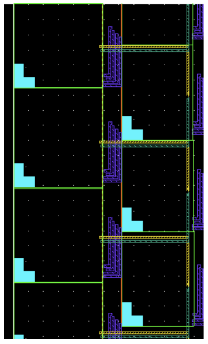

?

Hexagonal routing only

pixel cell itself
can be rectangular!



CAP6 pixel cell
designed by M. Cooney



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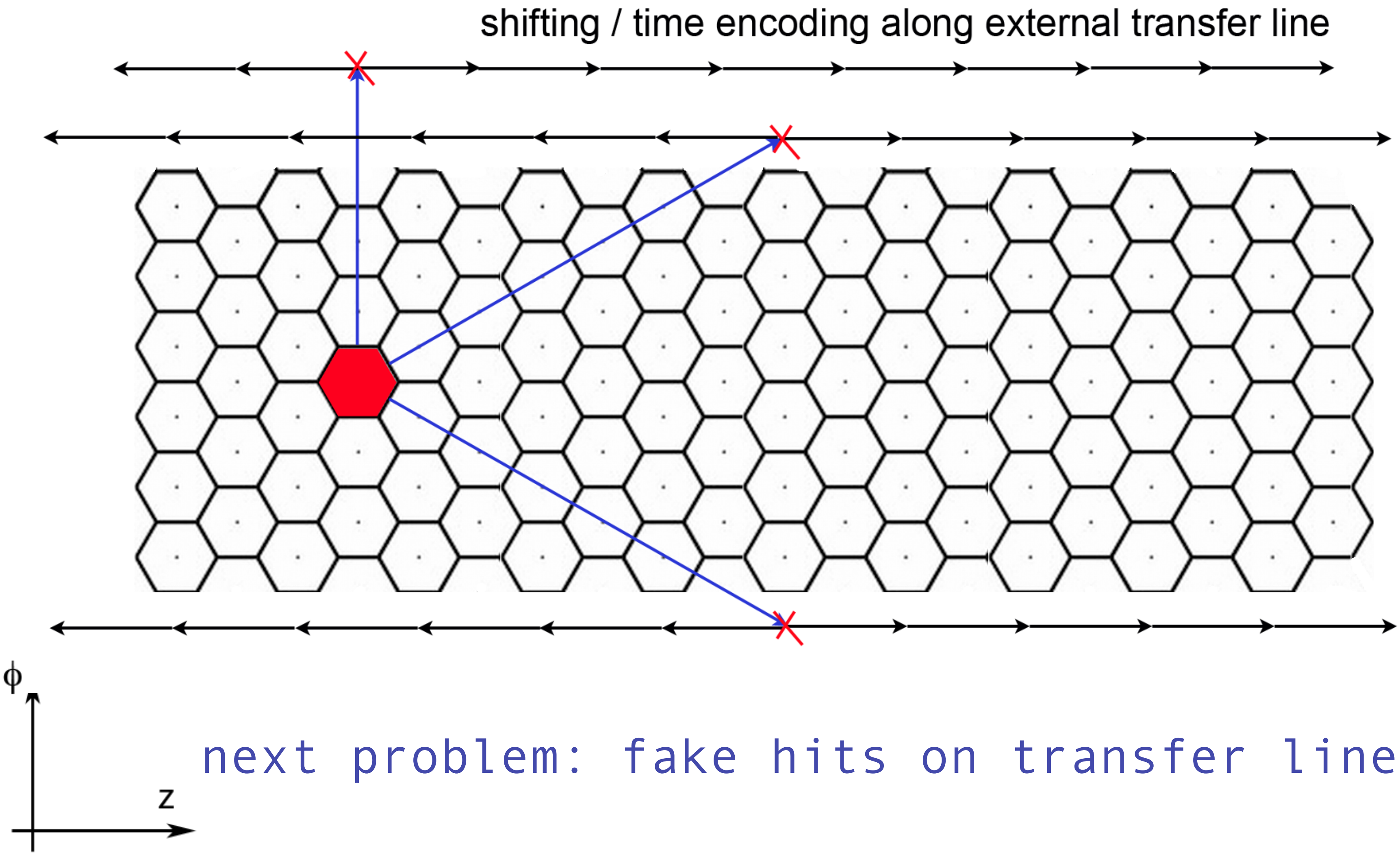
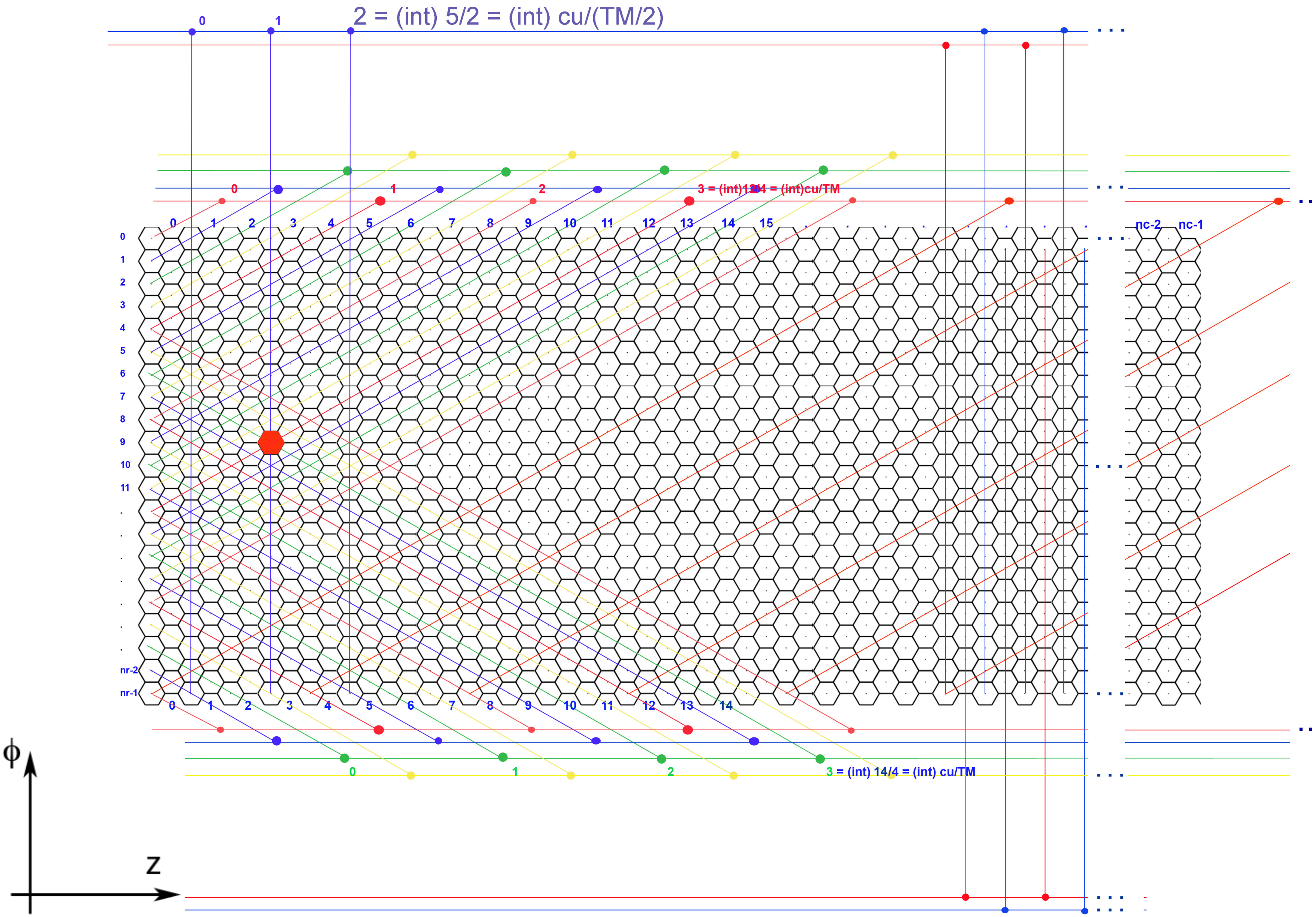
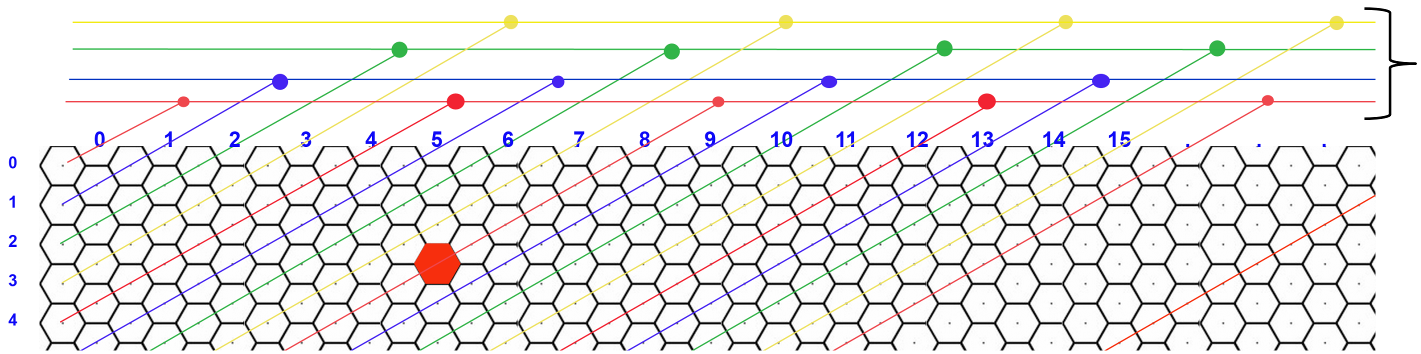


next problem: fake hits on transfer lines?

Multiple external transfer lines



Multiple external transfer lines



Fake hits: additional transfer lines help!

transfer line occupancy k:

$$k = r_{BG} \cdot \underbrace{(N-1)}_{\propto 1/TM} \cdot \Delta t_{shiftcycle} \cdot \underbrace{A_{sensitive}}_{\propto 1/TM} \cdot N_{cluster}$$

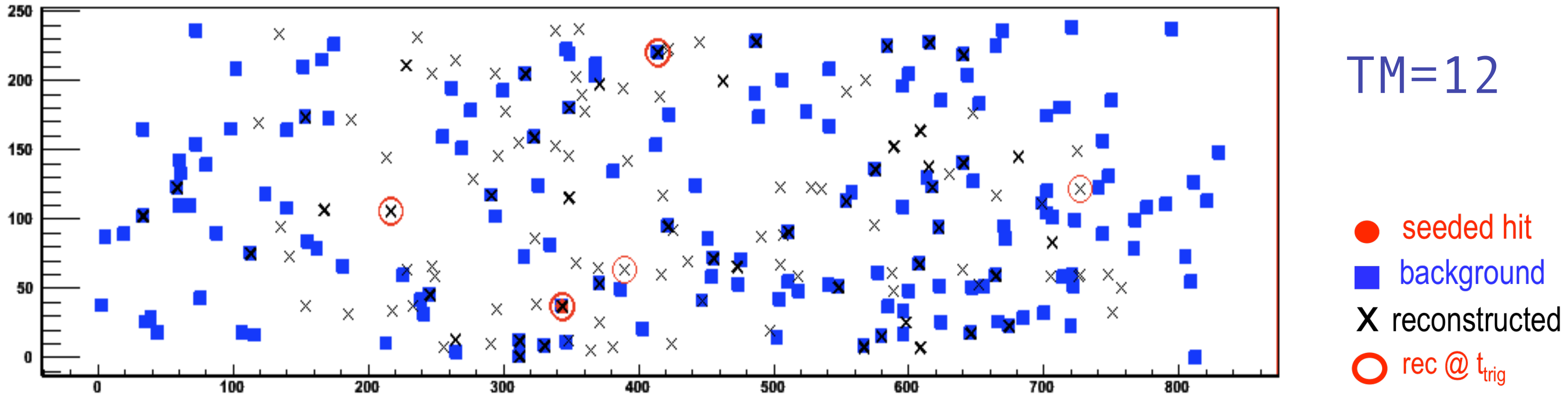
average number of fakes
for a given trigger

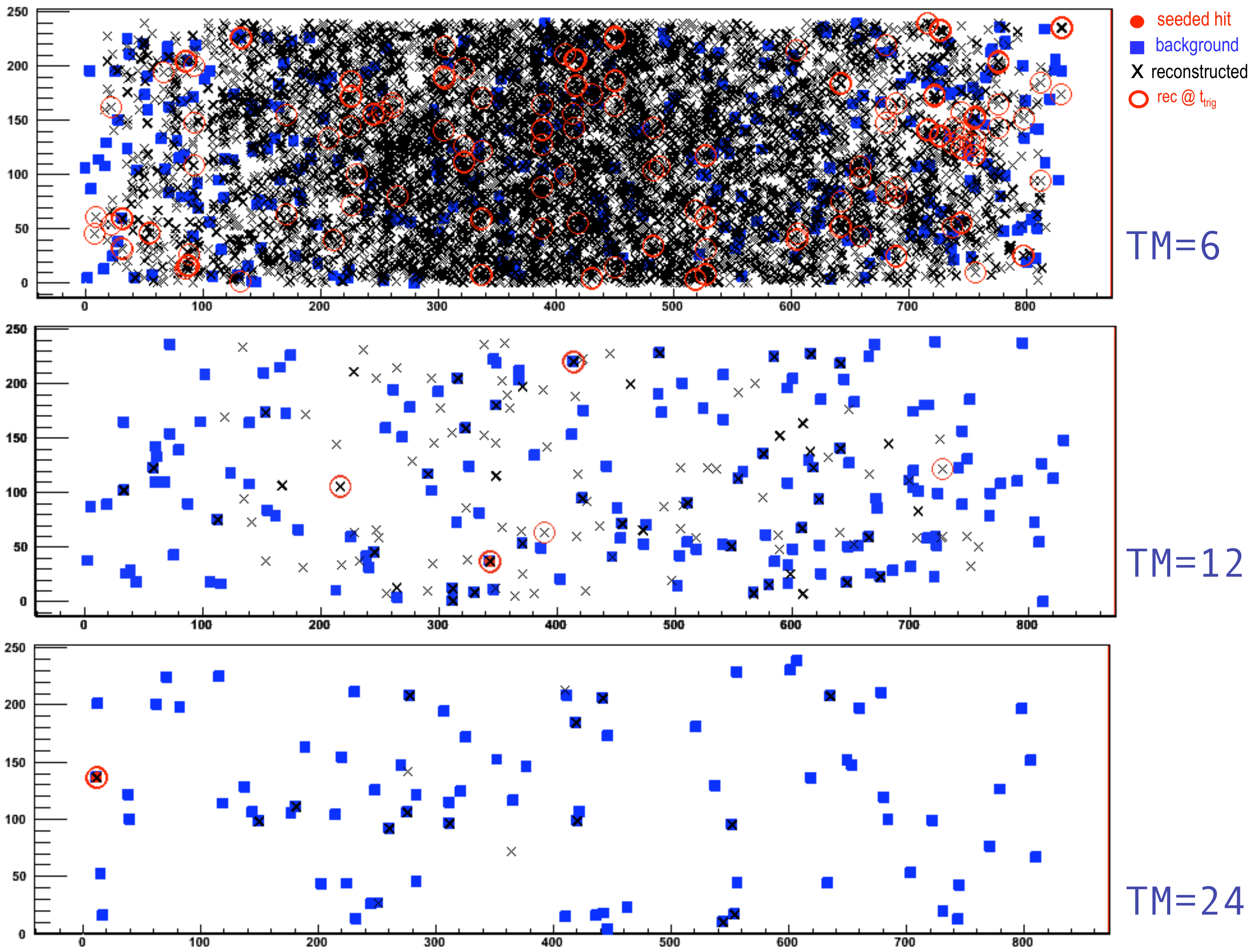
$$\langle N_{fake} \rangle = \frac{k^2}{N} \quad \propto 1/TM^3$$

reduction
in effective
occupancy!

MC simulation of occupancy

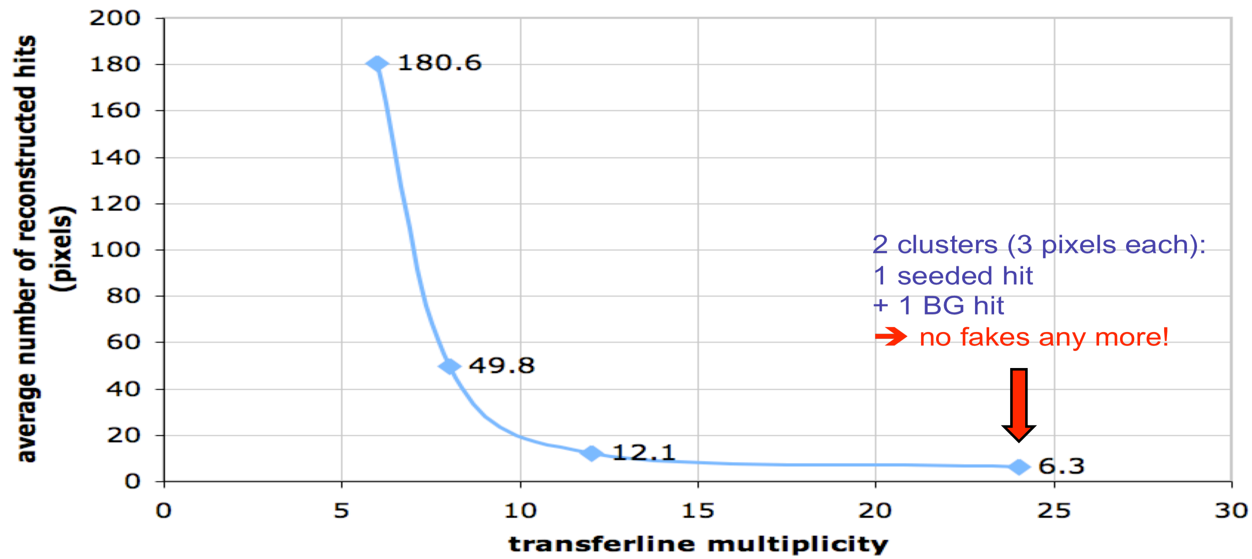
- full size array:
  - 21x6 mm^2, 25µm pitch, ~230 000 pixels
- simulation:
  - background generation + one seeded hit at time of trigger
  - calculation of all output signals
  - reconstruction
- statistics:
  - average number of reconstructed hits at trigger
  - including fakes
  - evaluation as function of transfer line multiplicity




seeded hit
background
reconstructed
rec @ t_{trig}
TM=6
TM=12
TM=24
250
200
150
100
50
0
0
100
200
300
400
500
600
700
800

MC simulation statistics

avg. nr. of rec. hits per trigger and effective occupancy



detector	matrix	pitch	shift clock	outputs	(effective) occupancy
binary	800x240	25 µm square	2 MHz (internal lines)	480	0.124
binary	800x240	25 µm square	10 MHz (internal lines)	480	0.005
binary hexagonal TM = 8	960x240	25 µm hexagonal	100 MHz (external lines)	48	2.2E-04
binary hexagonal TM = 12	960x240	25 µm hexagonal	100 MHz (external lines)	72	5.2E-05
binary hexagonal TM =24	960x240	25 µm hexagonal	100 MHz (external lines)	144	2.7E-05
analog rolling shutter	420x120	50 µm square	9 µs integration time	120	0.016

sBelle numbers! ILC even lower!

details: H. Hoedlmoser *et al.*, Hexagonal pixel detector with time encoded binary readout, accepted for publication in Nucl. Inst. Meth. A, 2008 **NIMA_48977**

Advantages of the hexagonal concept

- **low effective occupany:**
  - $5x10^{-5}$ at TM = 12

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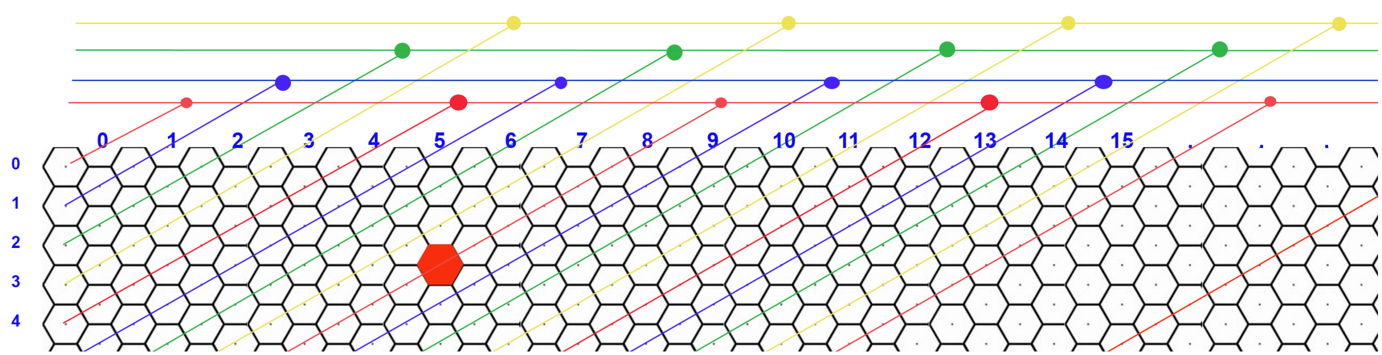
1. **low effective occupany:** 5×10^{-5} at TM = 12

- **fewer channels:**
  - 72(!) for 230 000 pixels at TM = 12

Advantages of the hexagonal concept

1. **low effective occupany:** $5x10^{-5}$ at TM = 12
2. **fewer channels:** 72(!) for 230 000 pixels

- **improved resolution:**
  - transfer logic moves from pixel to periphery!
  - smaller pixel size possible
  - 25 µm possible in .2 µm process



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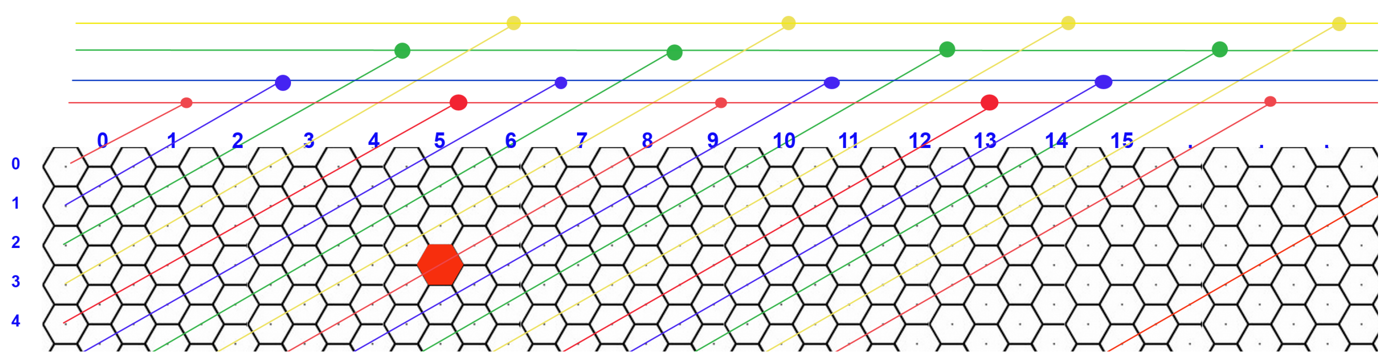
- **faster shifting:**

  at the periphery transfer logic can be optimized for speed ~ 100 MHz



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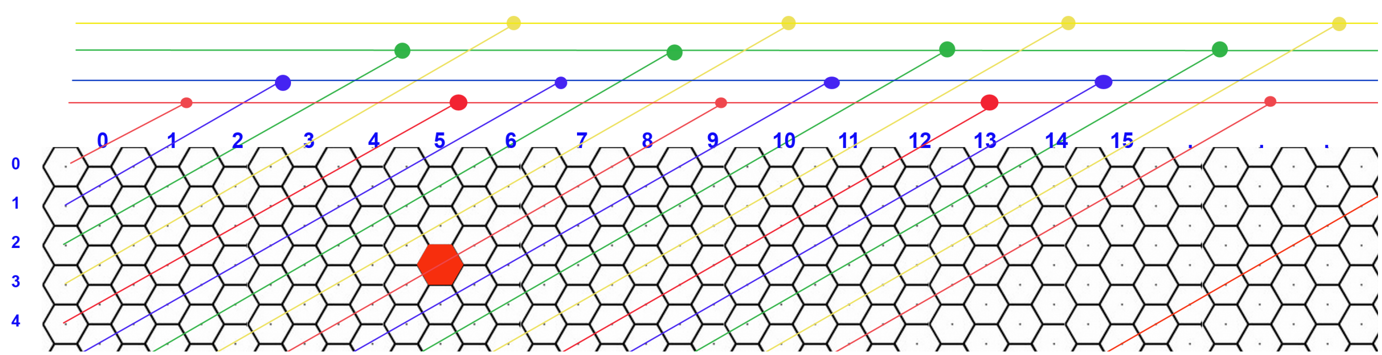
4. **faster shifting:** transfer at periphery

- **no ambiguities in cluster reconstruction:**

  -no ghosts due to hexagonal system
  -residual fakes in transfer lines spatially separated by many pitches



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  HEXAGONAL PIXEL DETECTOR

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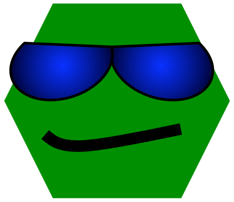
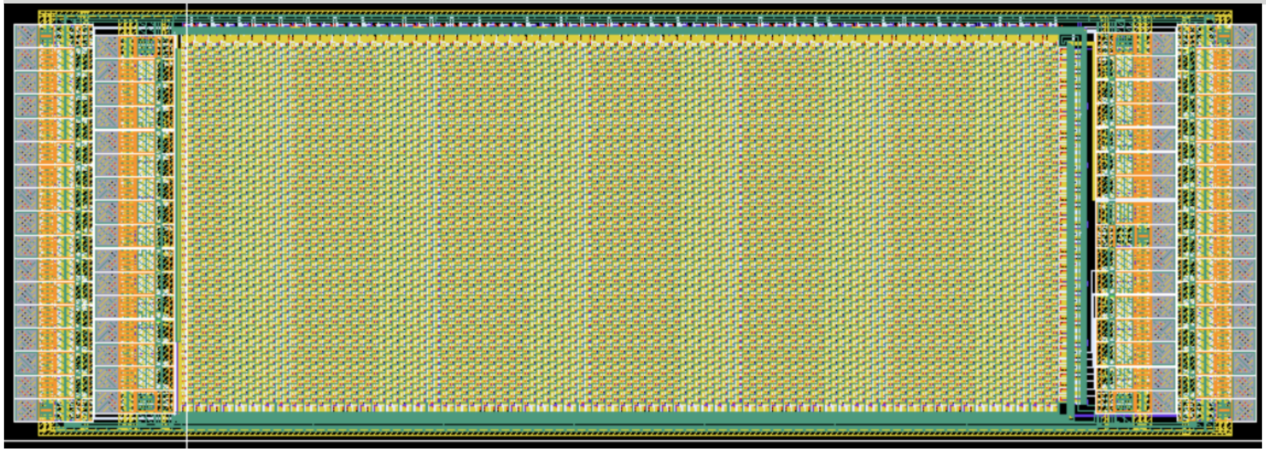
HIXEL DETECTOR



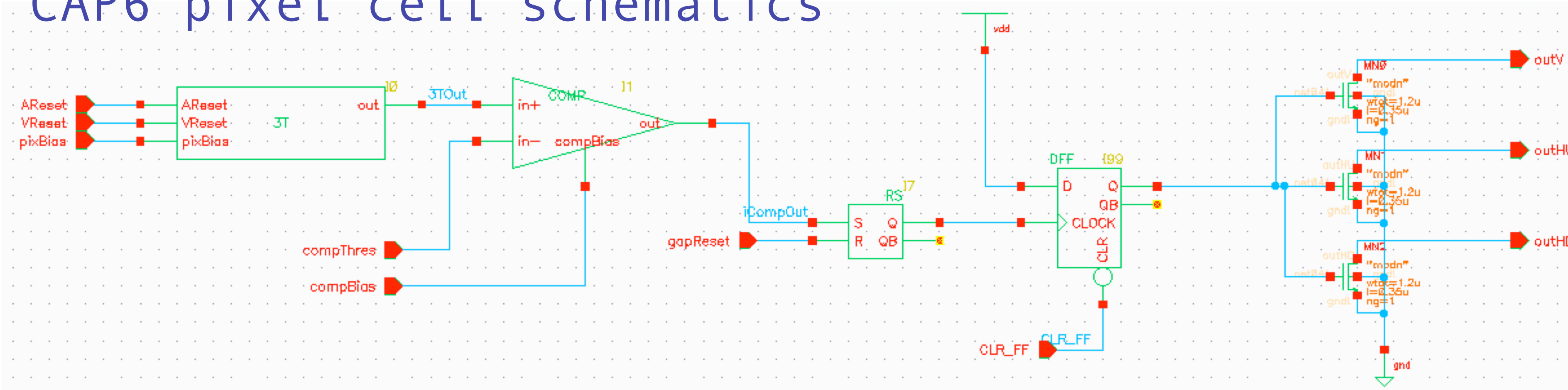
HIXEL Prototype: CAP6 in AMS 0.35 µm Opto



CAP6 matrix by Mike Cooney

Total Width	5,323	μm
Total Height	1,814	μm
Total Area	9.649	mm^2
Pixel Width	28.2	μm
Pixel Height	31.7	μm
Total Columns	128	
Total Rows	49	
Total Pixels	6,272	

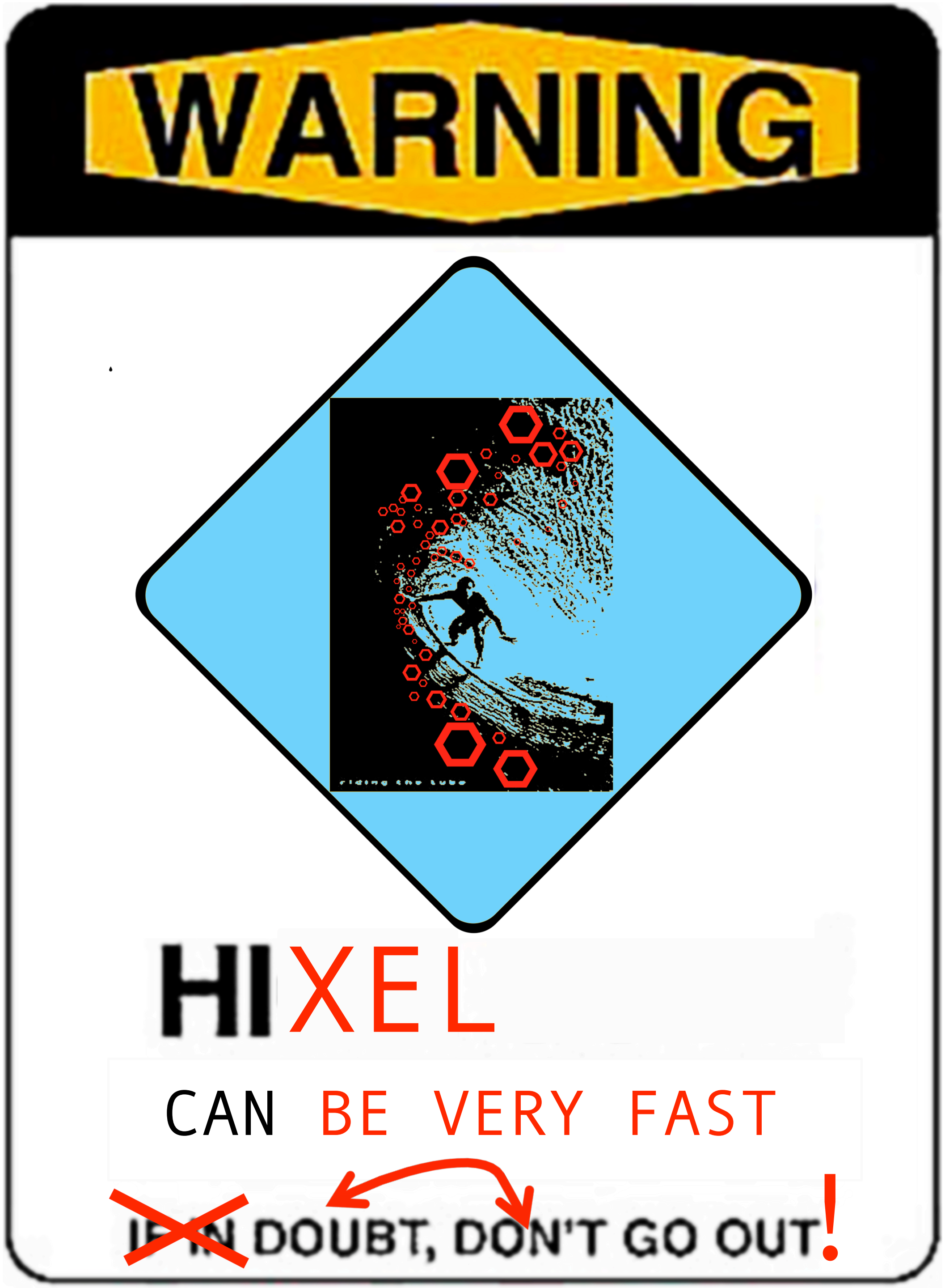
CAP6 pixel cell schematics



Planning: - CAP6 currently in fabrication
- delivery hopefully 1/2009

Summary and outlook

- binary readout concept working in CAP4
- awaiting improved prototype CAP7 (2008 OKI SOI run) for testing
- new hexagonal binary concept with promising simulation results could achieve $O(10^{-5})$ occupancies
- hexagonal prototype CAP7 expected early 2009
- new hexagonal prototype to be submitted in 2009 SOI run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HIXEL
CAN BE VERY FAST
IF IN DOUBT, DON'T GO OUT!

BACKUP

- CAP LIST
- CAP4 RESULTS
- CAP5 RESULTS (2X)
- GEANT4 SIMULATION
- HIXEL CELL ARRANGEMENT
- SCHEMATICS

Binary CAPs

CAP4 AMS 0.35 mm Opto
(E. Martin)

- Study of new analog and binary designs

CAP5 SOI prototype
(E. Martin)

- Study of 0.15 mm Fully Depleted OKI process

CAP7 SOI
(M. Cooney)

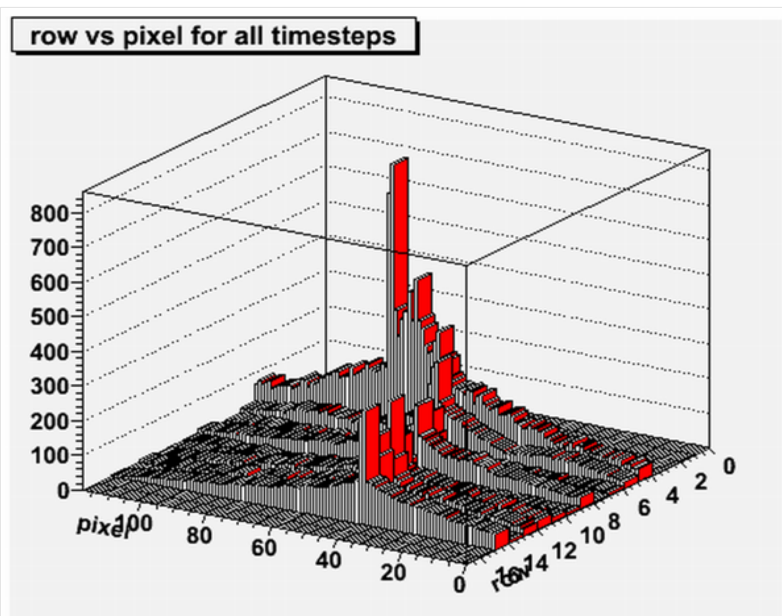
- 0.2 mm OKI SOI process submitted 01/2008
- improved binary design from CAP5

CAP6 hexagonal binary design in AMS 0.35 mm Opto
(M. Cooney)

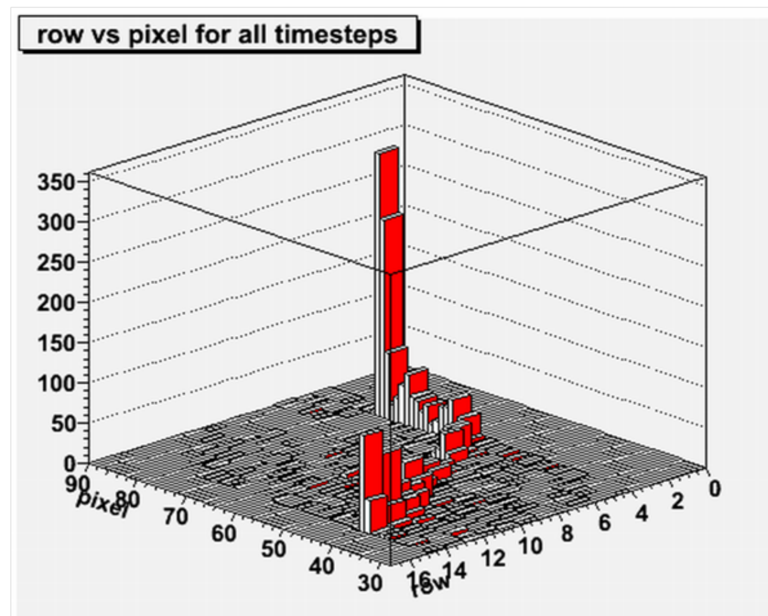
- completely new readout concept
- submitted 10/2008

CAP4 results

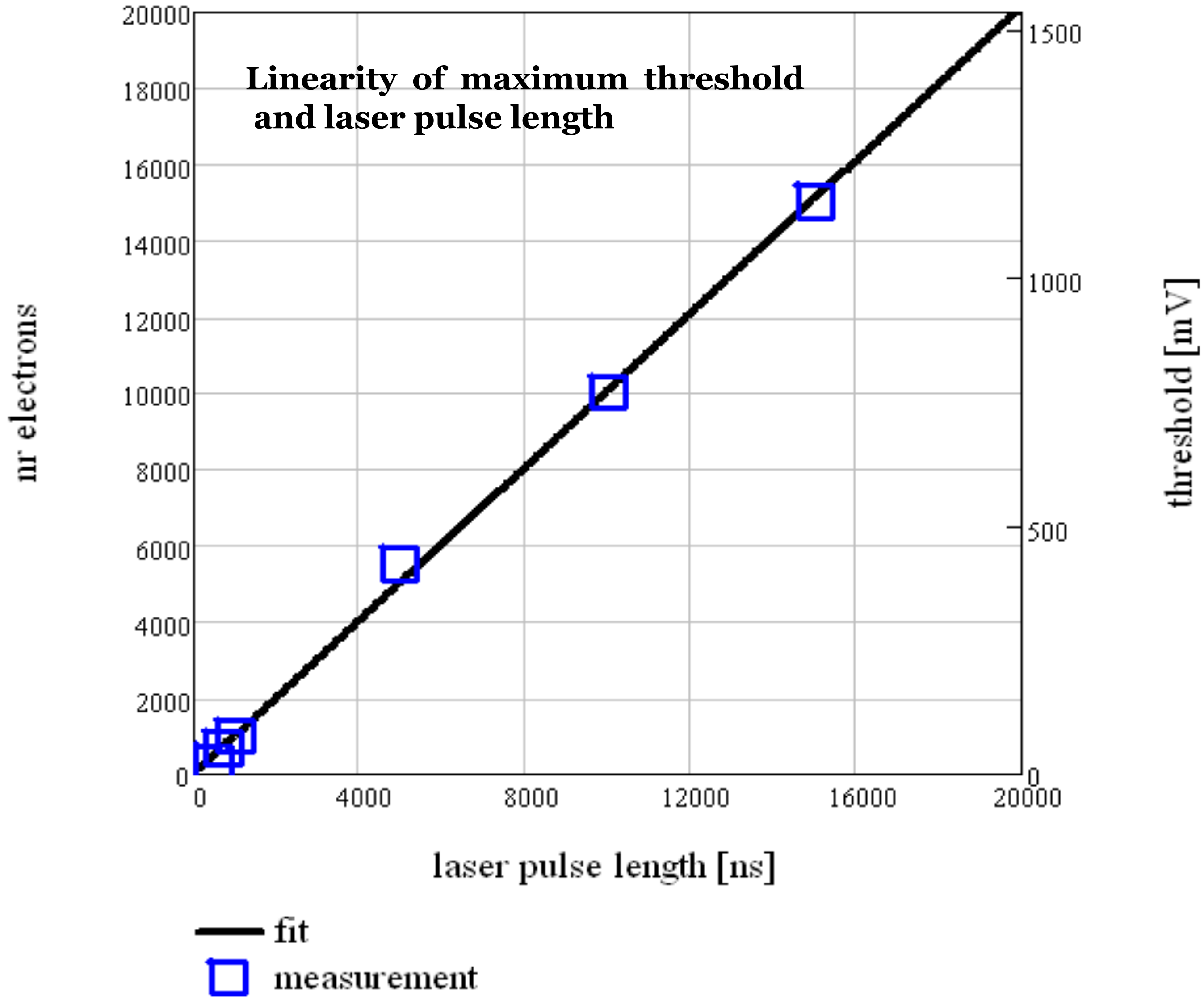
- position scans with IR laser sucessful
- linearity of charge and laserpuls shown in threshold scans
- identified problem leading to ghost reconstruction:
  pixel chatter = multiple output of signals close to threshold
  due to transparent latch in comparator
- latch replaced with d-flip-flop in CAP7 design
- noise measurement not possible due to chatter



software
filter
→

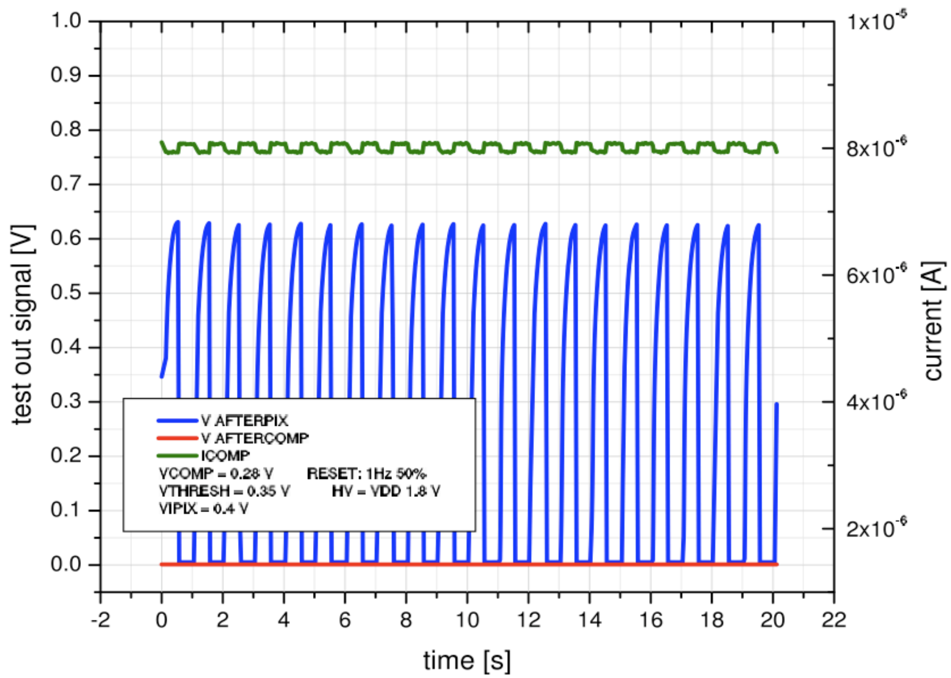


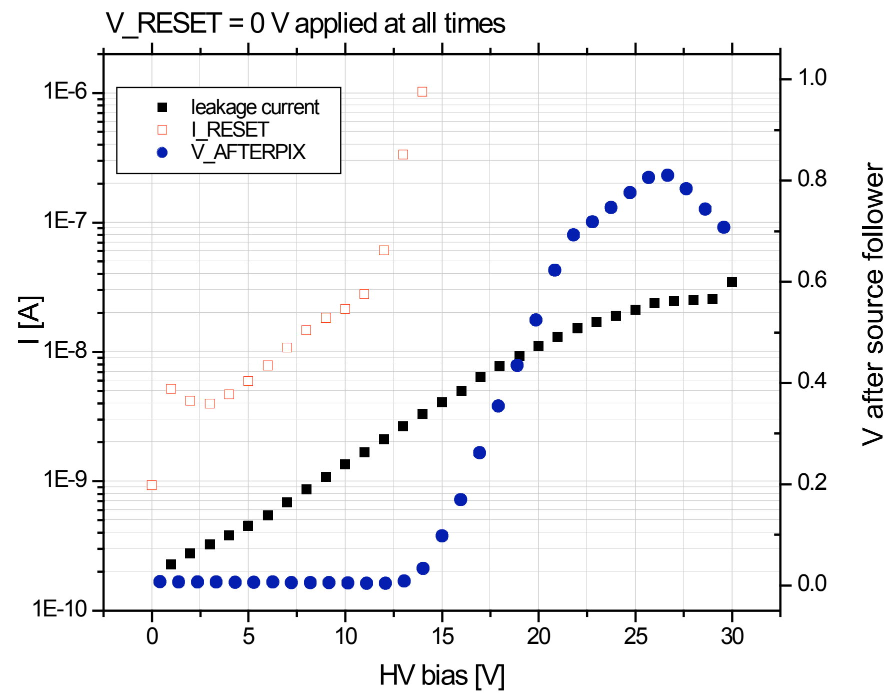
CAP4 results



CAP5 results

- chip could not be operated on readout board
- testing on probe station (test points and TEG) showed problems with SOI process (model parameters for design, back gate effect)





basic 3T cell works, comparator does not

even 3T cell cannot be reset for HV>12V

CAP5: identified problems

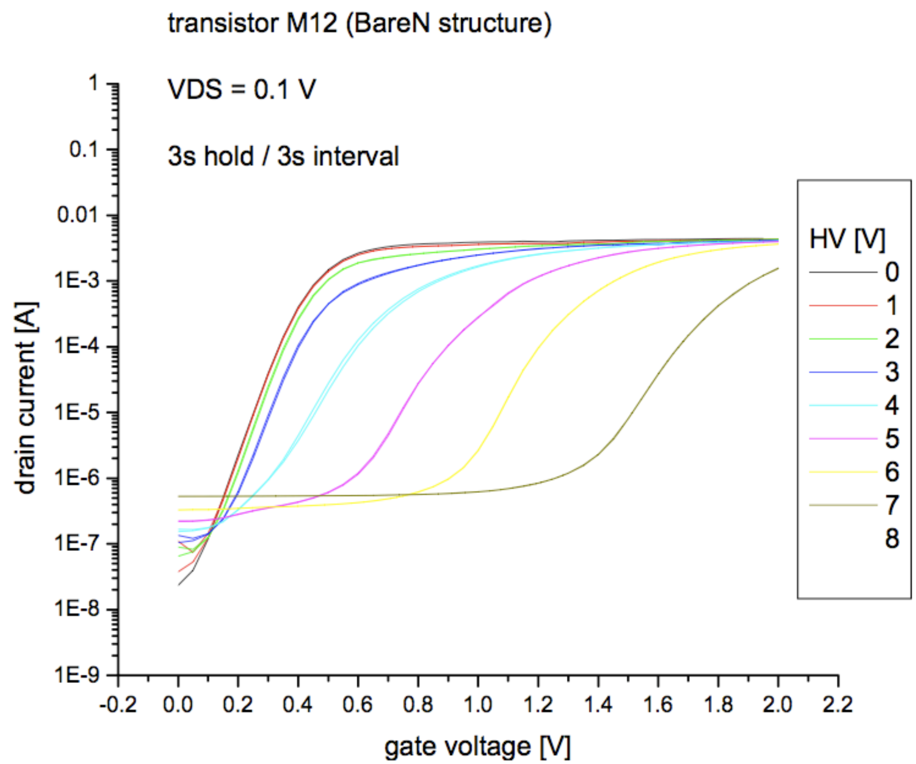
- discrepancies between transistor characteristics and OKI specifications
- extreme sensitivity of trans. characteristics to HV

Transistor type	high-VT basic logic	low-VT analog circuits	I/O (high-VT)
Voltage tolerance(V)	1.0	1.0	1.8
Gate oxide thickness(nm)	2.5	2.5	2.5
Minimum gate length(μm)	0.14	0.14	0.30
Threshold voltage(V)	0.4V	0.2	0.5

OKI specifications

Body Float Type				Body Tie Type			
Tr	$V_{threshold}$ (V)	Tr	$V_{threshold}$ (V)	Tr	$V_{threshold}$ (V)	Tr	$V_{threshold}$ (V)
M1	0.506	M5	0.787	M9	0.562	M13	1.443
M2	0.389	M6	0.866	M10	Non-Available	M14	1.120
M3	0.510	M7	0.617	M11	0.601	M15	0.387
M4	0.388	M8	0.387	M12	0.383	M16	0.879

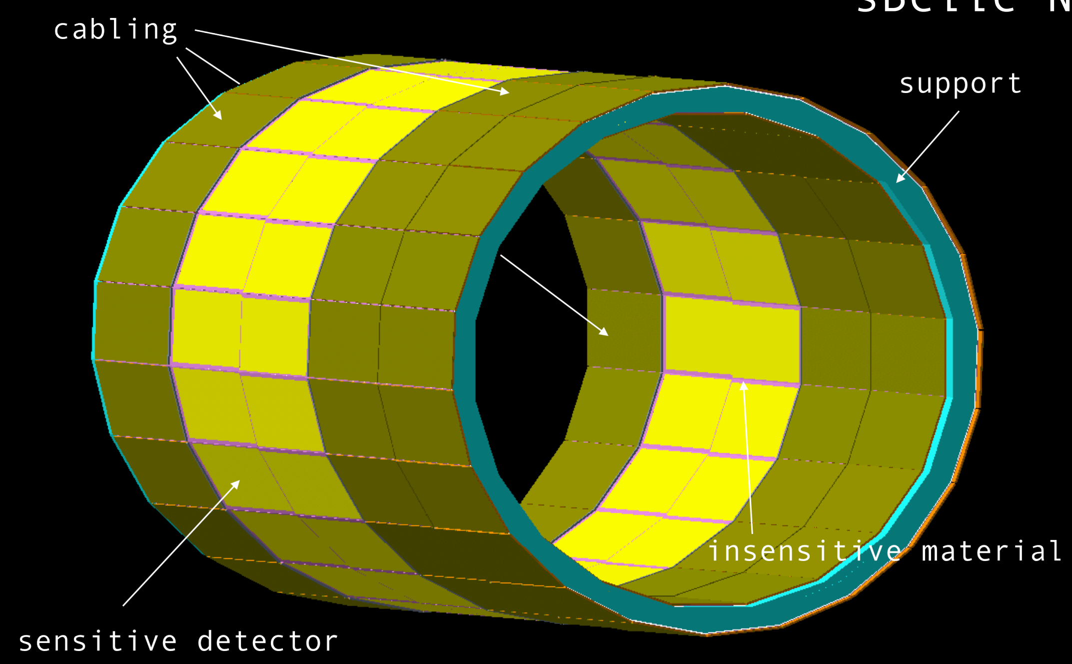
measured test transistors

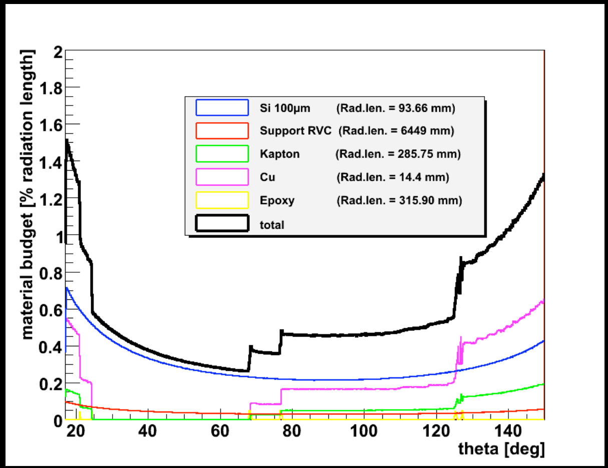


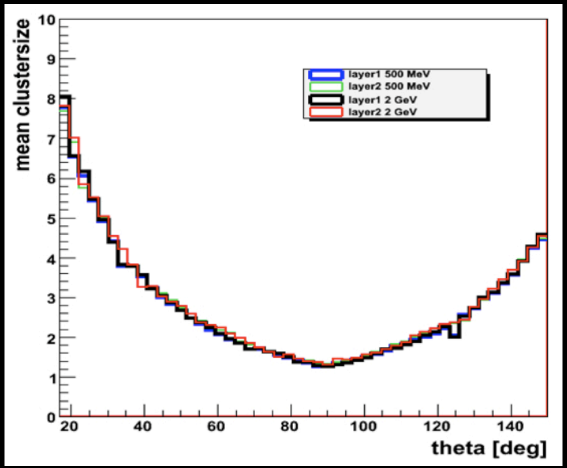
HV sensitivity of test transistor

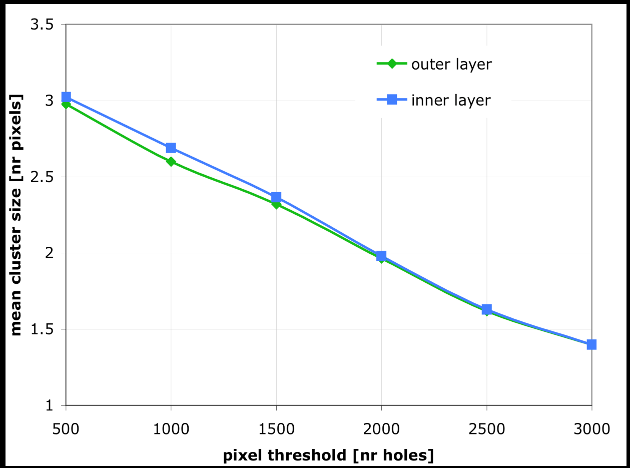
Geant4 simulation for SuperBelle

sBelle Note: sBN/0006









Hixel cell arrangement

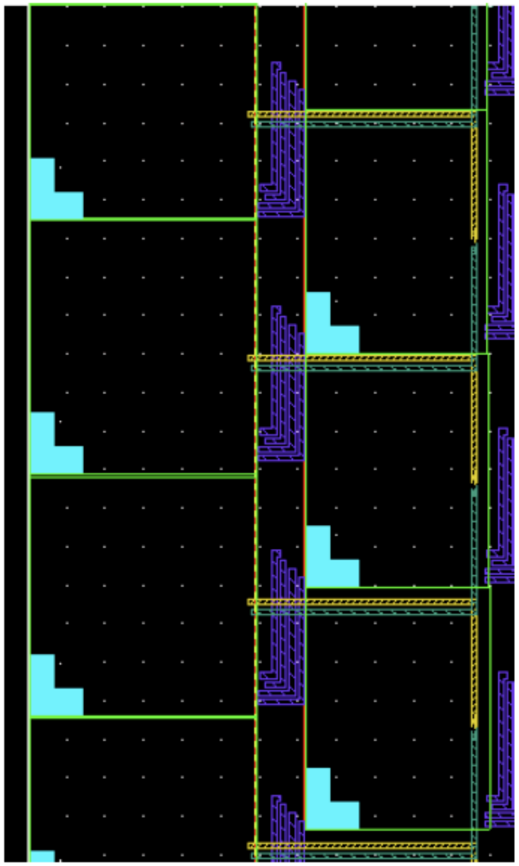


Figure 5.2: *A graphic showing the relative pixel discplacements. Each pixel is highlighted by a bright green box. Each collection diode is an L shaped box in each pixel. The dark blue, yellow, and dark green lines represent inter-pixel routing. For example: the dark green line is the up30 signal, the yellow line is the down30 signal. The vertical transfer line is not shown. The first column (on the left) is an odd numbered column and is therefore shifted up by 1/2 a pixel height in relation to the even column (the right column).*

Hixel 3T

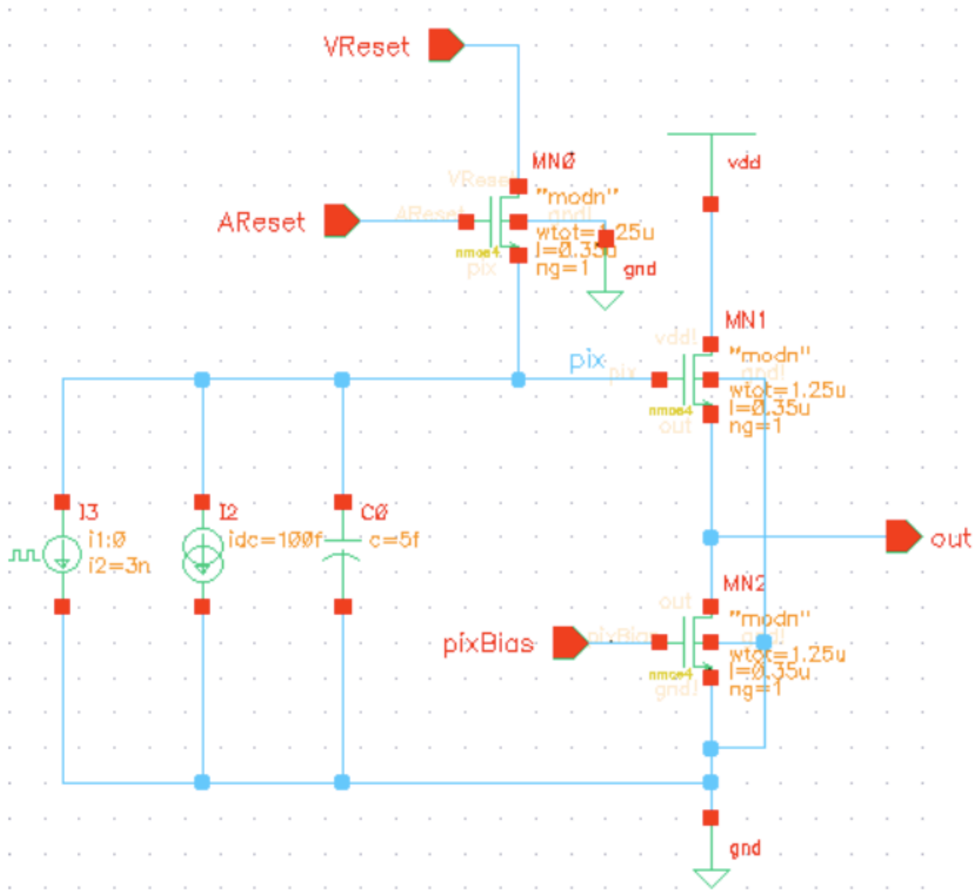


Figure 5.10: *The 3T cell schematic as seen in the CAP6. Note the current source, voltage source, and capacitor used for simulations. The layout ignores these components connected to the diode contact, listed as pix.*

Hixel transfer node