Status and perspectives of Deep N-Well CMOS MAPS for the ILC Vertex Detector

Valerio Re

Università di Bergamo and INFN - Pavia

International Linear Collider Workshop 2008

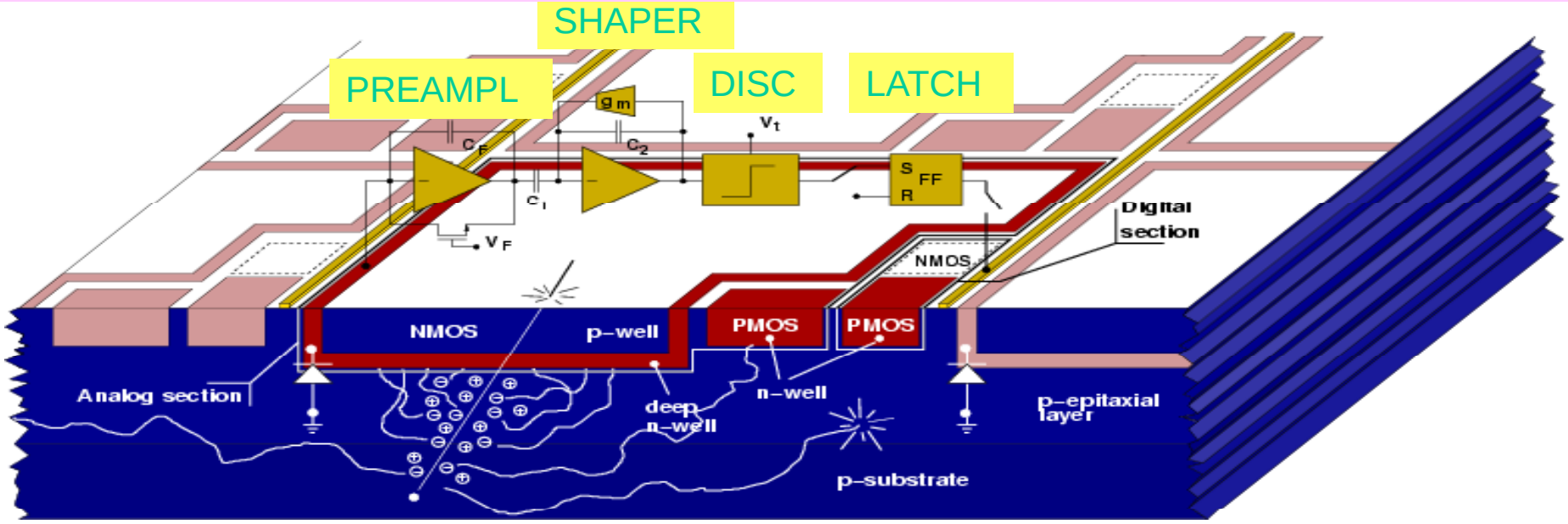
16-20 November 2008 Chicago, IL

Outline

- The first generation of Deep N-Well (DNW) MAPS with on-pixel data sparsification and time stamping, tested in a beam for the first time in September 2008
- ILC-class and SuperB-class 130nm DNW CMOS MAPS with different pixel pitch, analog signal processing and digital readout architecture
- The way forward to use DNW MAPS in actual experiments
- Impact of new technologies on the performance of DNW-MAPS

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



Classical optimum signal processing chain for capacitive detector can be implemented at pixel level:

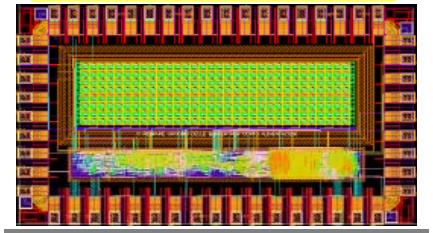
- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located
- Fill factor = DNW/total n-well area ~90% in the prototype test structures

After 5 years of R&D….

130 nm DNW MAPS: first generation of CMOS sensors with in-pixel sparsification and time stamping

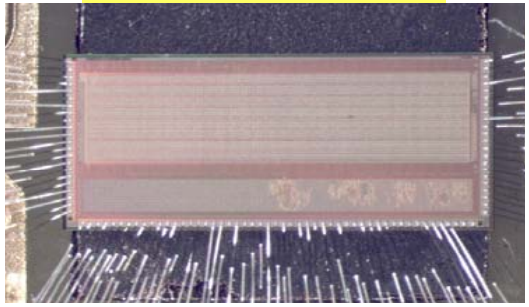
(130 nm STM CMOS process)

APSEL3D



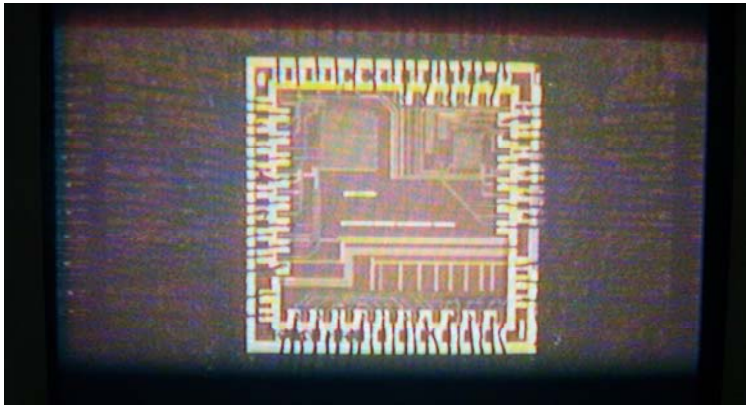
8x32 matrix.
Shielded pixel
Data Driven
sparsified readout

APSEL4D



32x128 matrix.
Data Driven,
continuously operating
sparsified readout
Beam test Sep. 2008

SDR0



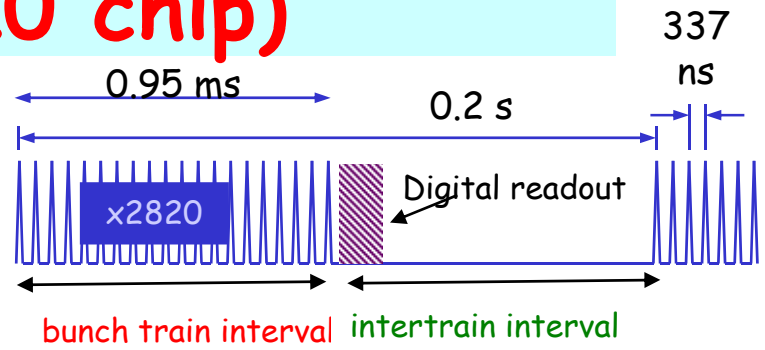
16x16 matrix + smaller test structures.
Intertrain sparsified readout

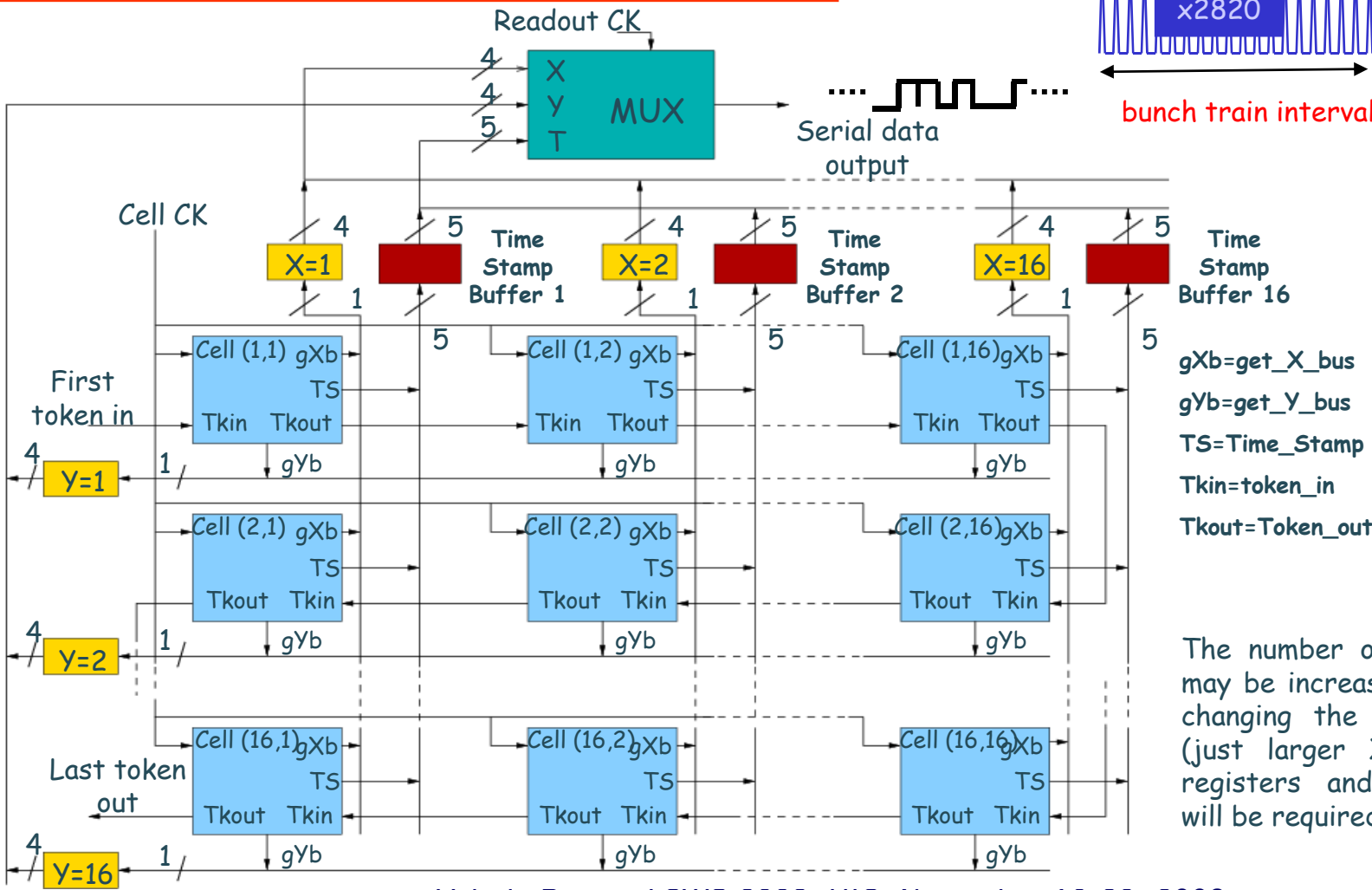
50x50 μm pitch

25x25 μm pitch

Intertrain Readout Architecture for "ILC" MAPS (SDRO chip)

Suggested by FNAL IC design group, first implemented in the VIP chip





gXb=get_X_bus

gYb=get_Y_bus

TS=Time_Stamp

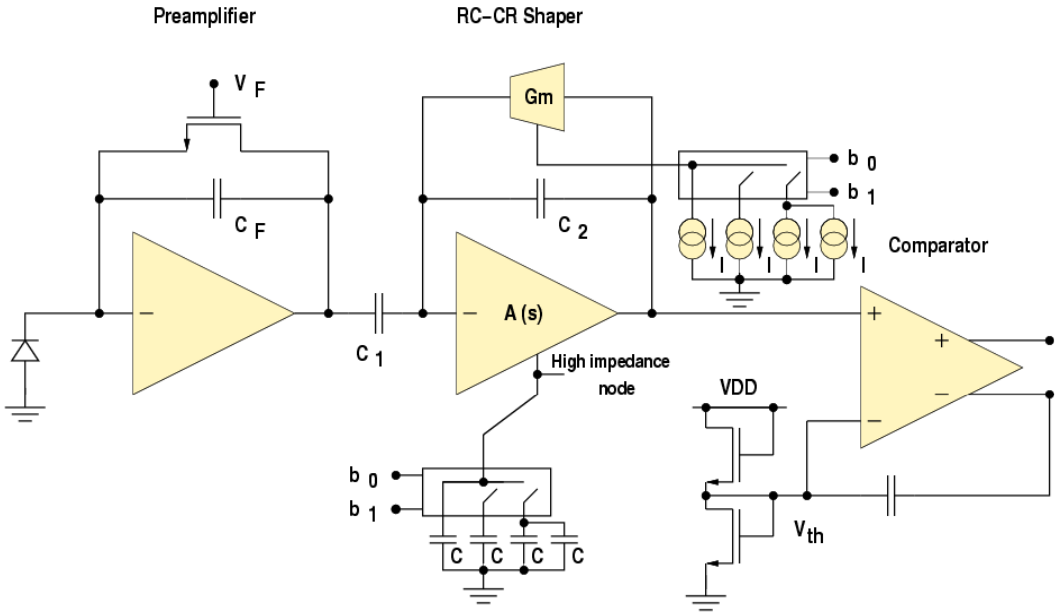
Tkin=token_in

Tkout=Token_out

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

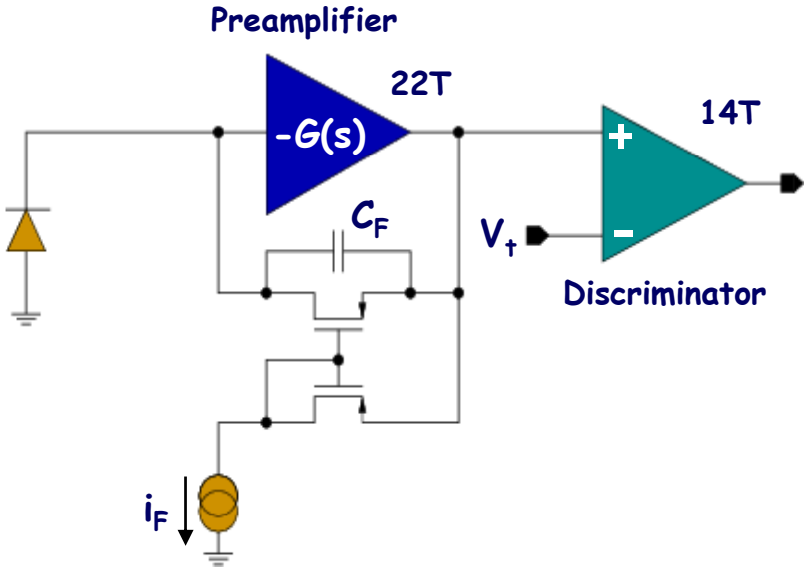
Two versions of the analog section for different pixel pitch

APSEL (SuperB VTX Layer0)



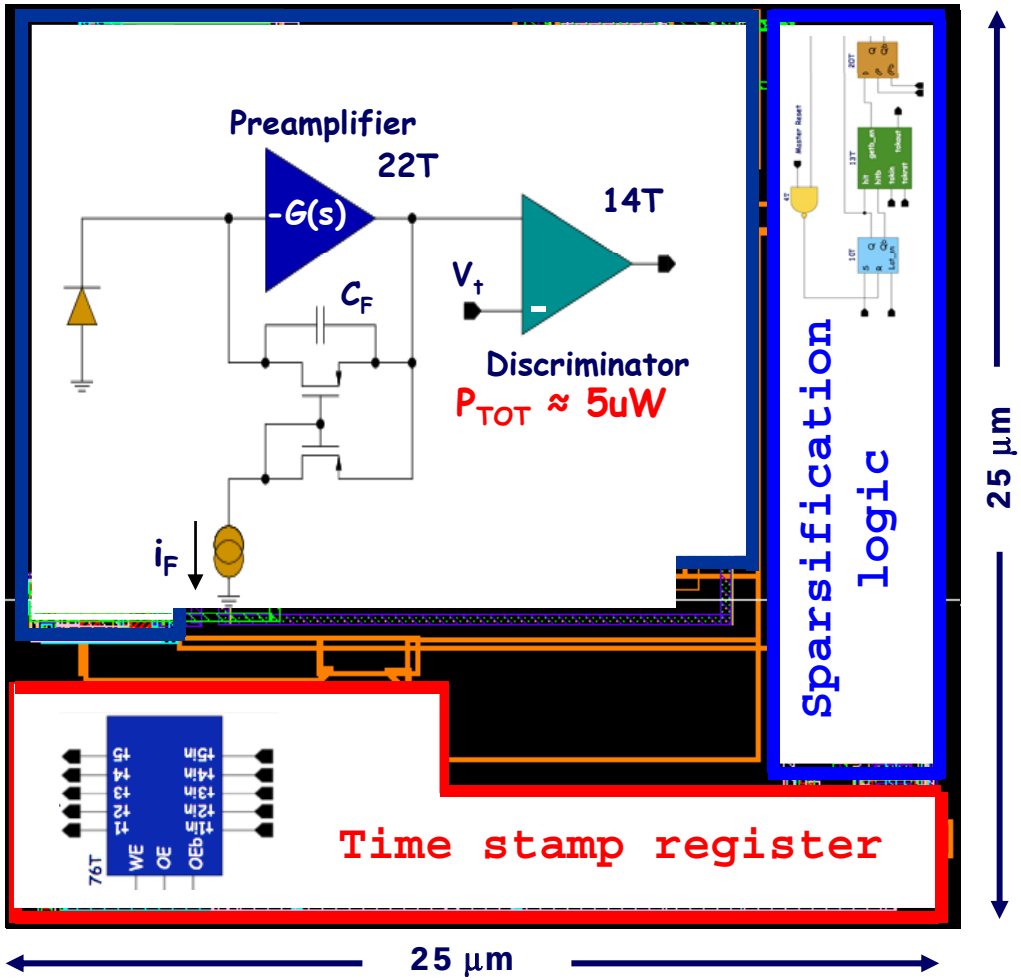
- Pixel cell: 50x50 μm^2
- Sensor capacitance: 400 fF
- Power dissipation: 30 μW

SDR0 (ILC VTX)



- Pixel cell: 25x25 μm^2
- Sensor capacitance: 150 fF
- Power dissipation: 5 μW

The SDRO pixel



analog front-end

+

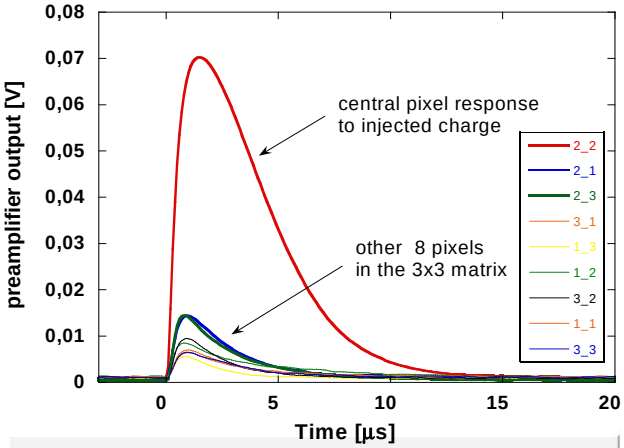
digital section

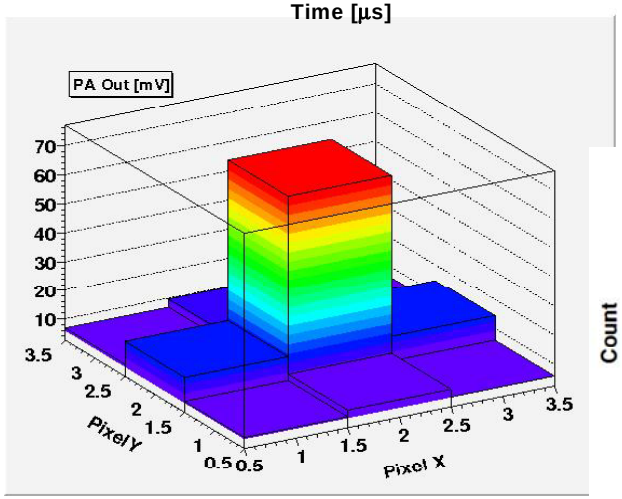
↓

164 transistors

SDR0 performance

Matrix response to infrared laser





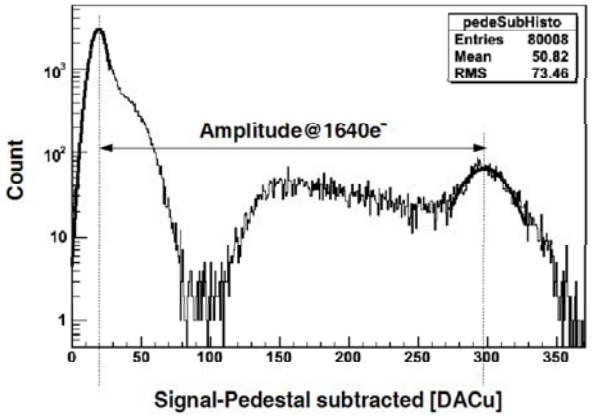
SDR0 - 16x16 pixels 25 µm pixel pitch

- Average charge sensitivity ≈ 0.7 V/fC
- ENC = 40 e rms @ C_D=120 fF

  (preamplifier input device: I_D = 1 µA, W/L = 22/0.25)
- Threshold dispersion ≈ 60 e

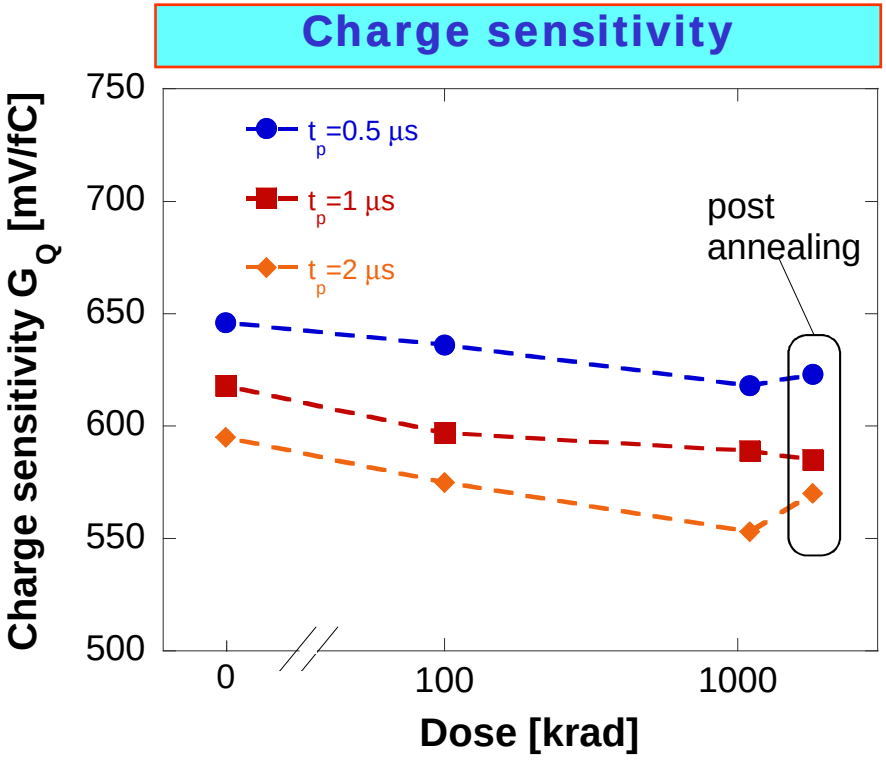
Digital readout is working fine

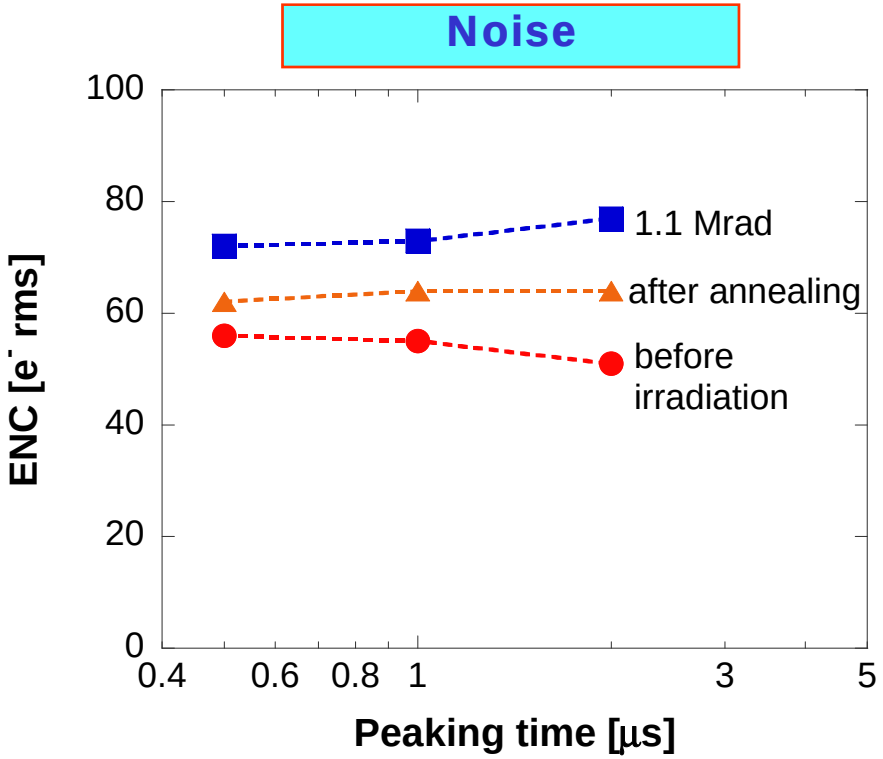
Test with ^{55}Fe



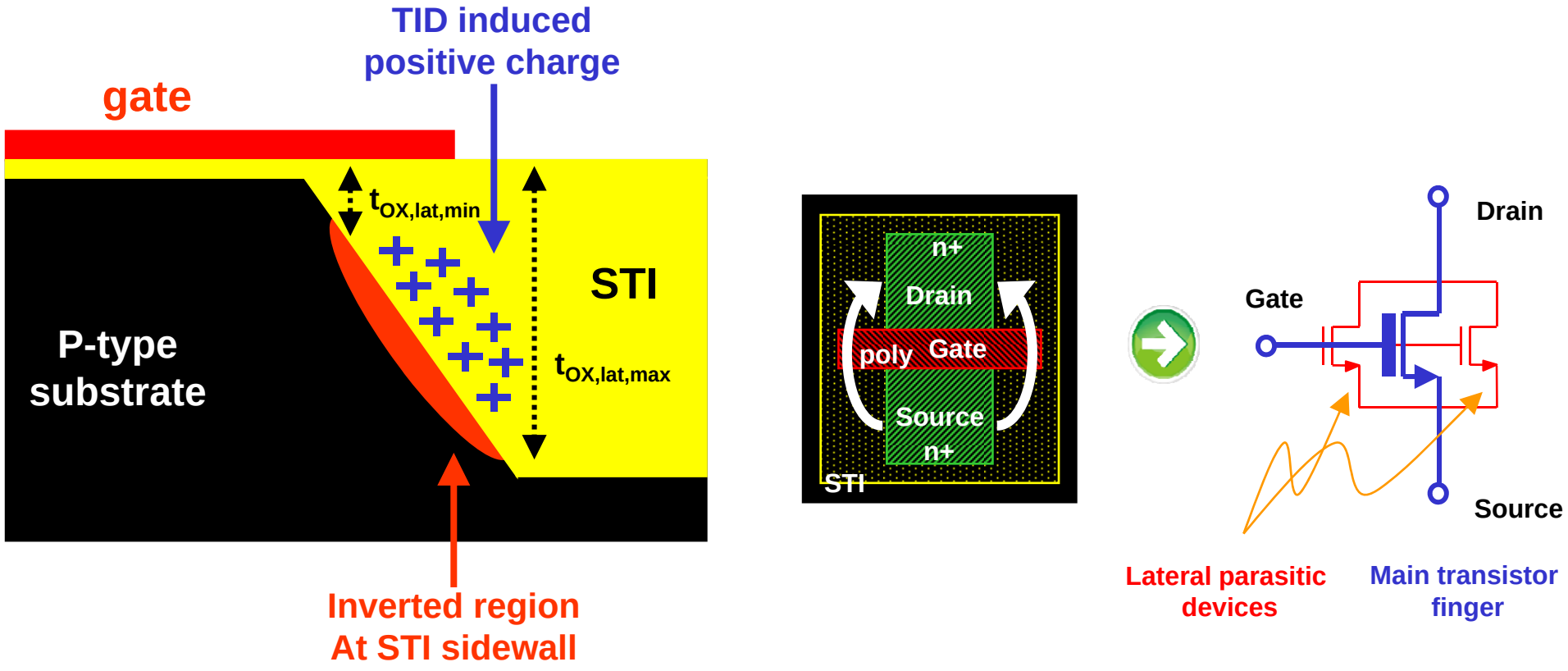
Radiation hardness

- Radiation tests on prototypes (APSEL chips) show that DNW MAPS sensors are rad-hard at ILC total dose levels (1 Mrad), even without any rad-tolerant design trick
- At these TID levels, sensor leakage current is still not a problem; radiation effects are associated to thick oxides (field oxide, STI)





Ionizing radiation effects on lateral isolation oxides



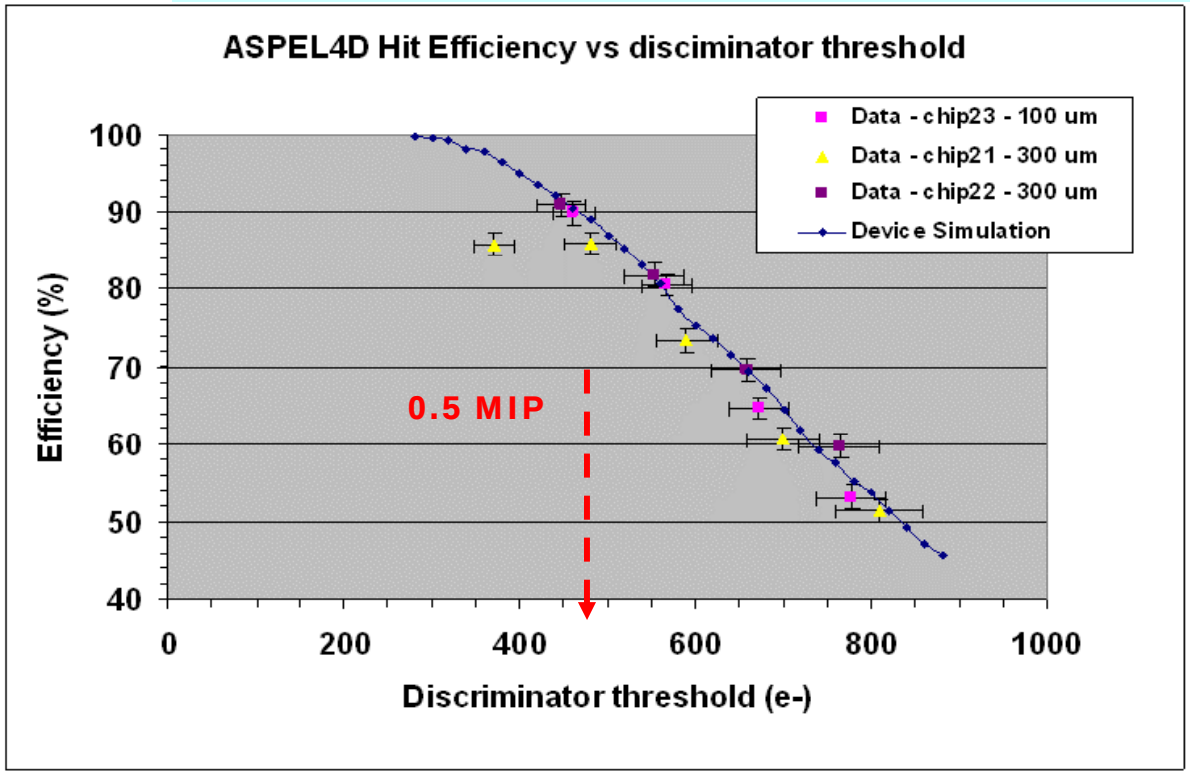
- Besides affecting static characteristics and leakage currents and lateral transistors are noisy as the main MOSFET device

SLIM5 Beam test

- A few numbers:
- Maps readout clock 20 MHz
- DAQ rate 30 kHz
- 90 M events on disk (40 Gb)
- Data analysis ongoing

APSEL4D chip

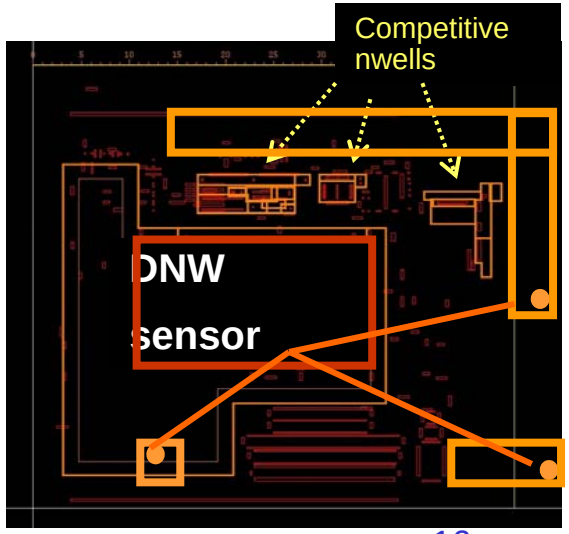
DNW MAPS Hit Efficiency measured in a beam test (APSEL4D)



Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

MAPS hit efficiency up to 90 % with threshold @ 450 e-
(~ 4σ_noise+2σ_thr_disp)

300 and 100 μm thick chips give similar results

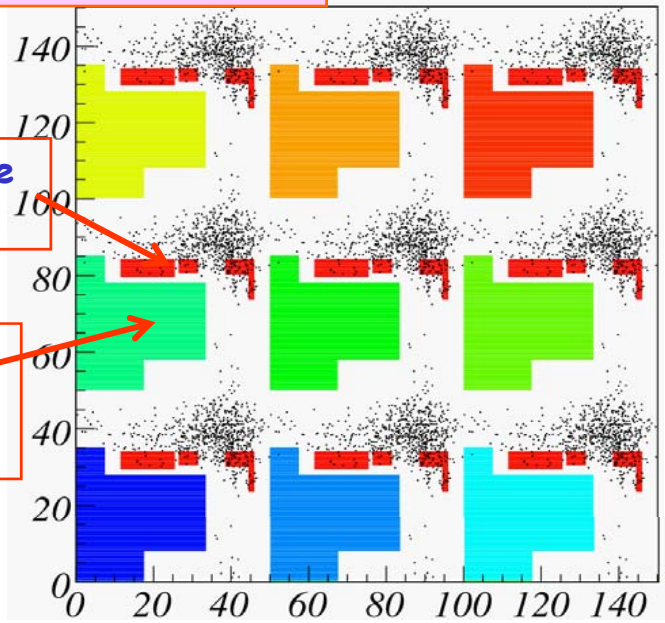


- Competitive N-wells (PMOS) in pixel cell can steal charge reducing the hit efficiency
  - Fill factor DNW/total N-well area ~ 90 % in present design
- Room for improvements with a different design of the sensor (multiple collecting electrodes around competitive N-wells)

Detection efficiency and charge collection

- Beam test results of APSEL4D show a ~90% efficiency, which agrees very well with TCAD simulations
- With APSEL4D sensor geometry (left), Efficiency ~ 93.5% from simulation (pixel threshold @ 250 e- = 5xNoise)
- Inefficient regions shown with dots (pixel signal < 250 e-)
- Optimized cell with satellite N-wells (right) Efficiency ~ 99.5%

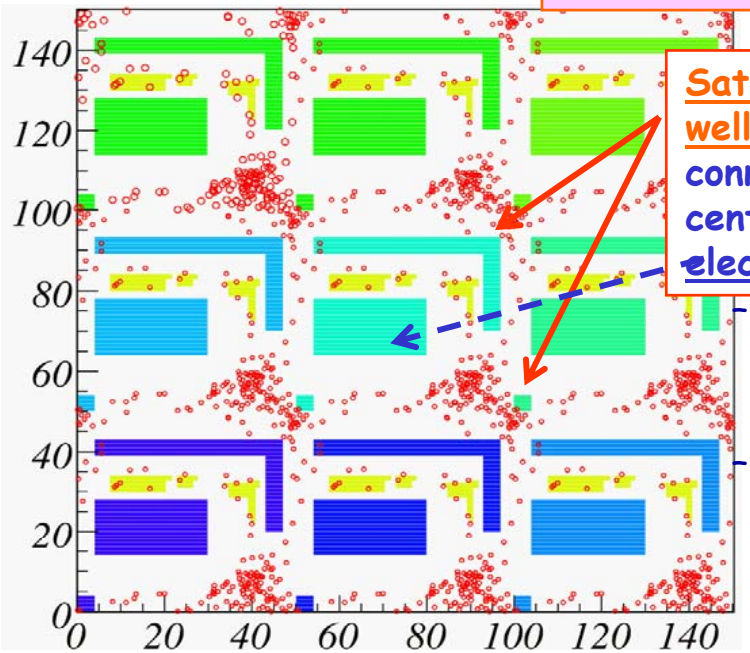
3x3 MATRIX
T sensor geometry



Competitive Nwells

DNW collecting electrode

3x3 MATRIX
optimized sensor



Satellite N-wells connected to central DNW electrode

Locate low efficiency region inside pixel cell

Add ad hoc "satellite" collecting electrodes

The way forward

- Next generation of DNW MAPS has to provide devices that approach actual experiment specifications more closely

  Several issues have to be addressed to meet ILC Vertex Detector specifications (pixel pitch, detection efficiency):

  - Binary readout: ILC VTX demands a **pixel pitch** < 20 μm to achieve required single point resolution < 5 μm.
  - **Detection efficiency** does not meet requirements (> 99 %) because of competitive n-wells (PMOS) decreasing the fill factor
  - Capability of **handling multiple pixel hits** has to be included without degrading efficiency and pitch

- Two different ways to approach this goal:

1) ***A gradual performance improvement***
   ⇒ better sensor layout, optimize interconnections and pixel cell
   ⇒ SuperB Layer0 test module

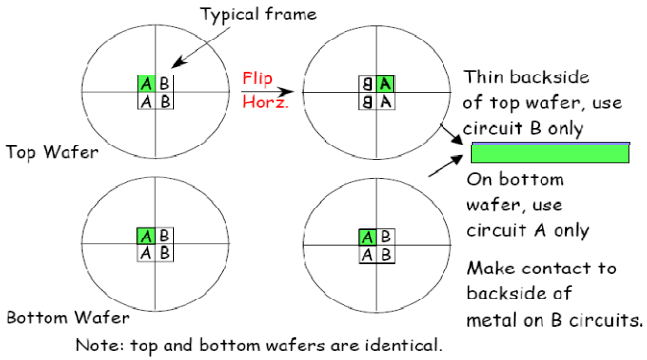
2) ***A technology leap***
   ⇒ Vertical integration

3D vertical integration and DNW MAPS

Use vertical integration technology to interconnect two 130nm CMOS layers

Overcome limitations typically associated to "conventional" and DNW CMOS MAPS:

- Reduced pixel pitch
- 100 % fill factor (few or no PMOS in the sensor layer, no competitive N-wells)
- Better S/N vs power dissipation (smaller sensor capacitance)
- Increased pixel functionalities

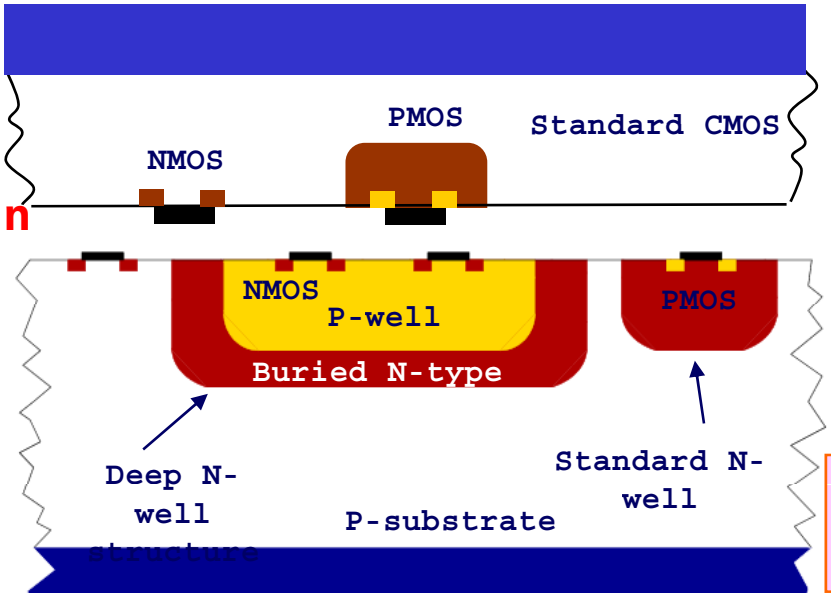


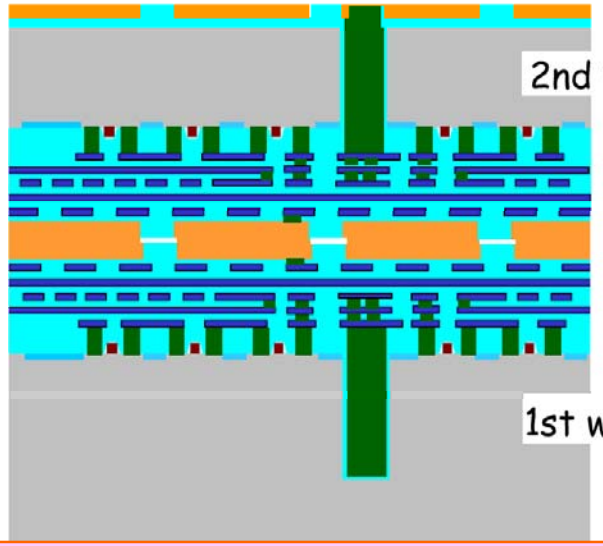
Face to Face Bonding

Mostly digital CMOS tier

Tier interconnection and vias

Analog and sensor CMOS (mostly NMOS) tier





Tezzaron/Chartered technology (Fermilab MPW run)

The Italian VIPIX collaboration

- "Pixel systems for thin charged particle trackers based on vertical integration technologies" - VIPIX
  (INFN Pisa, Pavia, Bologna, Trieste, Trento, Perugia, Roma3, Torino)

- Members of the CMOS-3DIT Consortium
  (FNAL-IN2P3-INFN)

1. **Interconnection between 2 (or more) CMOS layers,**
   one layer with a MAPS (DNW) device and analog front-end, and the other layer(s) with the digital readout

2. **Interconnection between a CMOS readout electronics chip (2D or 3D) and a fully-depleted high resistivity sensor**
   a) with bump bonding (standard, but low pitch may be needed)
   b) with a vertical integration technique (low material budget, more advanced)

Conclusions

- After several years of R&D, Deep N-Well monolithic active pixel sensors are reaching a good maturity level, but there is room for substantial improvements
- The performance of DNW MAPS needs to be upgraded if they have to fulfill ILC specifications
- DNW MAPS can benefit from technological advances

Acknowledgments

SLIM5-Silicon detectors with Low Interactions with Material

G. Batignani[1,2], S. Bettarini[1,2], F. Bosi[1,2], G. Calderini[1,2], R. Cenci[1,2], M. Dell'Orso[1,2], F. Forti[1,2], P.Giannetti[1,2] , M. A. Giorgi[1,2], A. Lusiani[2,3], G. Marchiori[1,2], F. Morsani[2], N. Neri[2], E. Paoloni[1,2], G. Rizzo[1,2] , J. Walsh[2]

C. Andreoli[4,5], E. Pozzati[4,5],L. Ratti[4,5], V. Speziali[4,5], M. Manghisoni[5,6], V. Re[5,6], G. Traversi[5,6], L.Gaioni[4,5]

L. Bosisio[7], G. Giacomini[7], L. Lanceri[7], I. Rachevskaia[7], L. Vitale[7],

M. Bruschi[8], B. Giacobbe[8],A. Gabrielli[8], N. Semprini[8], R. Spighi[8], M. Villa[8], A. Zoccoli[8],

D. Gamba[9], G. Giraudo[9], P. Mereu[9],

G.F. Dalla Betta[10] , G. Soncini[10] , G. Fontana[10] , L. Pancheri[10] , G. Verzellesi[11]

[1]Università degli Studi di Pisa, [2]INFN Pisa, [3]Scuola Normale Superiore di Pisa,

[4]Università degli Studi di Pavia, [5]INFN Pavia,

[6]Università degli Studi di Bergamo,

[7]INFN Trieste and Università degli Studi di Trieste

[8]INFN Bologna and Università degli Studi di Bologna

[9]INFN Torino and Università degli Studi di Torino

[10]Università degli Studi di Trento and INFN Padova

[11]Università degli Studi di Modena e Reggio Emilia and INFN Padova

ILC VTX - Italy

G. Traversi[a,b], A. Bulgheroni[b,c], M. Caccia[b,c], M. Jastrzab[b,c],

M. Manghisoni[a,b], E. Pozzati[b,d], L. Ratti[b,d], V. Re[a,b]

[a]Università degli Studi di Bergamo

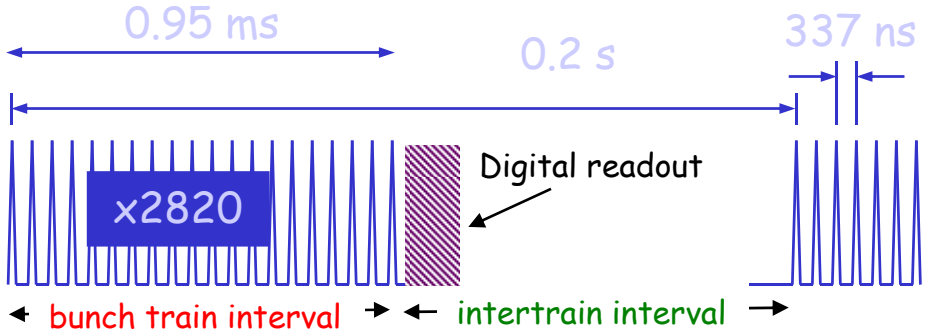
[b]INFN

[c]Università degli Studi dell'Insubria

[d]Università degli Studi di Pavia

Backup slides

Design specifications for the ILC vertex detector



- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a DC of 0.5%. Assuming:
- maximum hit occupancy 0.03 part./Xing/mm^2
- 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
- digital readout adopted: 5um resolution requires 17.3 um pixel pitch

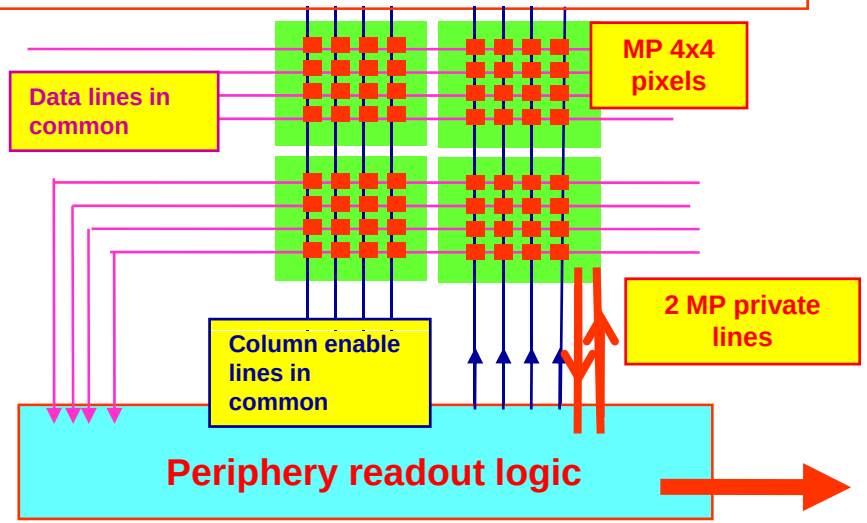
- 15 um pixel pitch → $O_c \approx 0.056$ hits/train → the probability of a pixel being hit at least twice in a bunch train period ≈ 0.0016 → there is no need to include a pipeline for storing more than one hit per pixel (more than 99% of events recorded without ambiguity)
- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)
- Data readout in the intertrain interval → system EMI insensitive
- Sparsified readout based on the token passing scheme. This architecture was first implemented in the VIP1 chip (3-D MIT LL technology) by the ILC pixel design group at Fermilab

Continuous Readout Architecture for "SuperB" MAPS (APSEL chips)

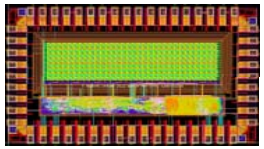
- Data-driven readout architecture with sparsification and timestamp information under development.
- In the active sensor area we need to minimize:
  - the logical blocks with PMOS to minimize the competitive nwell area and preserve the collection efficiency of the DNW sensor.
  - digital lines for point to point connections to allow scalability of the architecture with matrix dimensions and to reduce cross talk with the sensor underneath.

Matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:

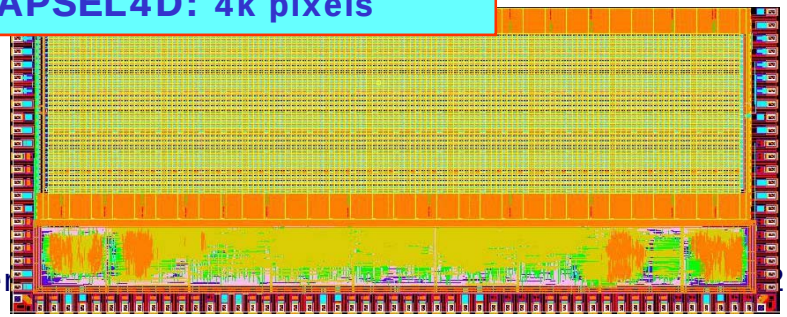
- Register hit MP & store timestamp
- Enable MP readout
- Receive, sparsify, format data to output bus



APSEL3D: 256 pixels



APSEL4D: 4k pixels



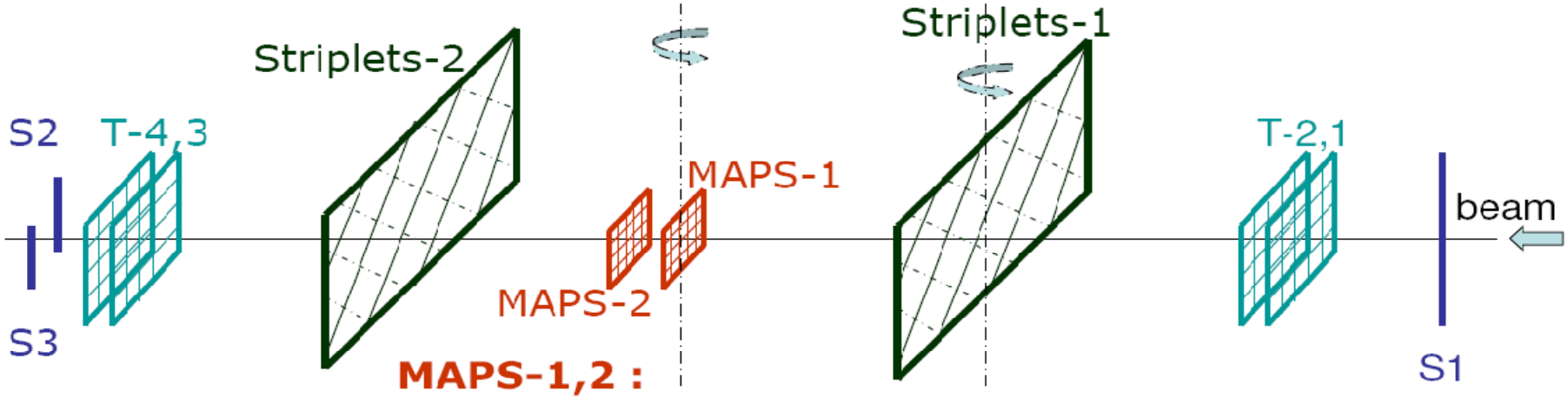
50x50 um pitch

SLIM5 CERN beam test with APSEL4D

The "DEMONSTRATOR"

(conceptual)

S-1,2,3 scintillator (coinc. NIM/TTL output to the DAQ)



MAPS-1,2 :
active area ~10 mm²
Cell:50x50 μm² (300→100 μm-thick)

Reference telescope T-1,2,3,4:
area~2x2 cm²
DSSD 300μm thick
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch
(3 chips FSSR2/side)

Striplets-1,2:
area 1.29x6.0 cm²
DSSD 200μm thick (∠45°)
25 p-side, 50 n-side μm pitch
50 μm r.o. pitch
(3 chips FSSR2/side)

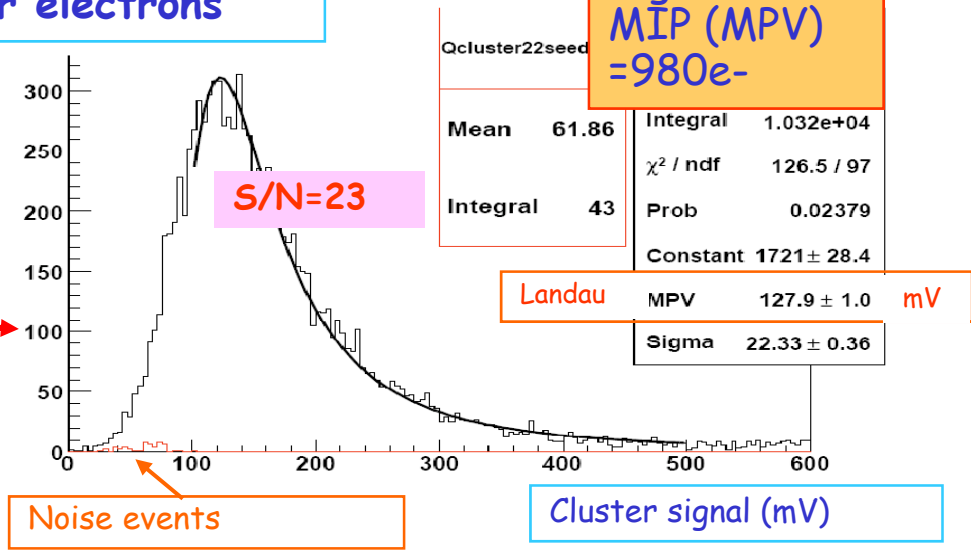
APSEL4D performance

APSEL4D - 32x128 pixels 50 μm pixel pitch

Tests of the APSEL4D chip:

- Optimization of the Deep NWell MAPS pixel with respect to previous versions
  - S/N up to 25 with reduced power consumption (~30 μW/ch)
- Fast readout architecture (sparsification and timestamp) implemented in a 4k pixel matrix.
- Good sensitivity to e- from ^{90}Sr and to γ from ^{55}Fe source
- Must operate at DVDD = 1V to reduce interferences

^{90}Sr electrons

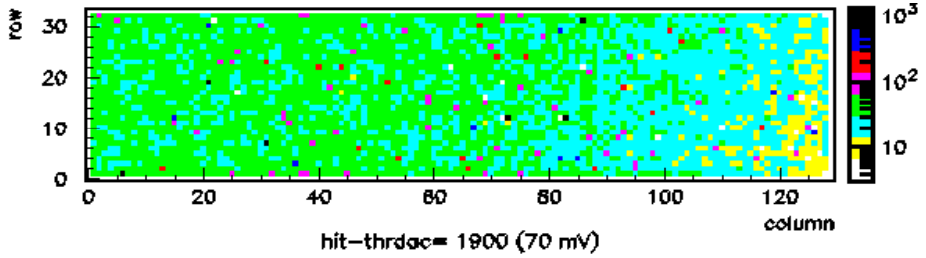


Average Signal for MIP (MPV) =980e-

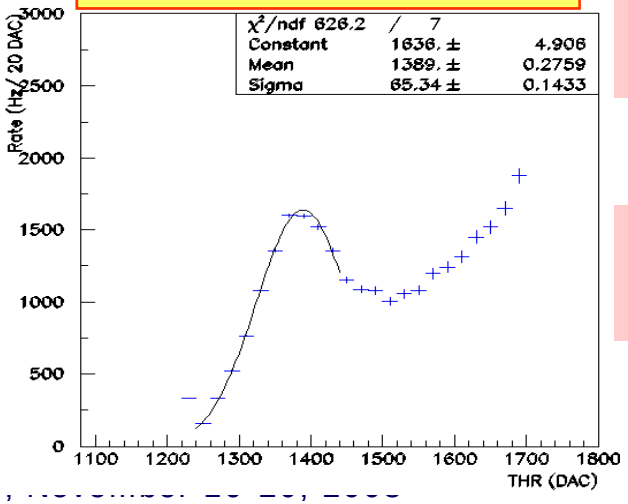
APSEL4D – ^{90}Sr test

Fired pixel map with threshold @ ½ MIP

Good uniformity (the source was positioned on the left side of the matrix)



APSEL4D - ^{55}Fe 5.9 keV calibration peak

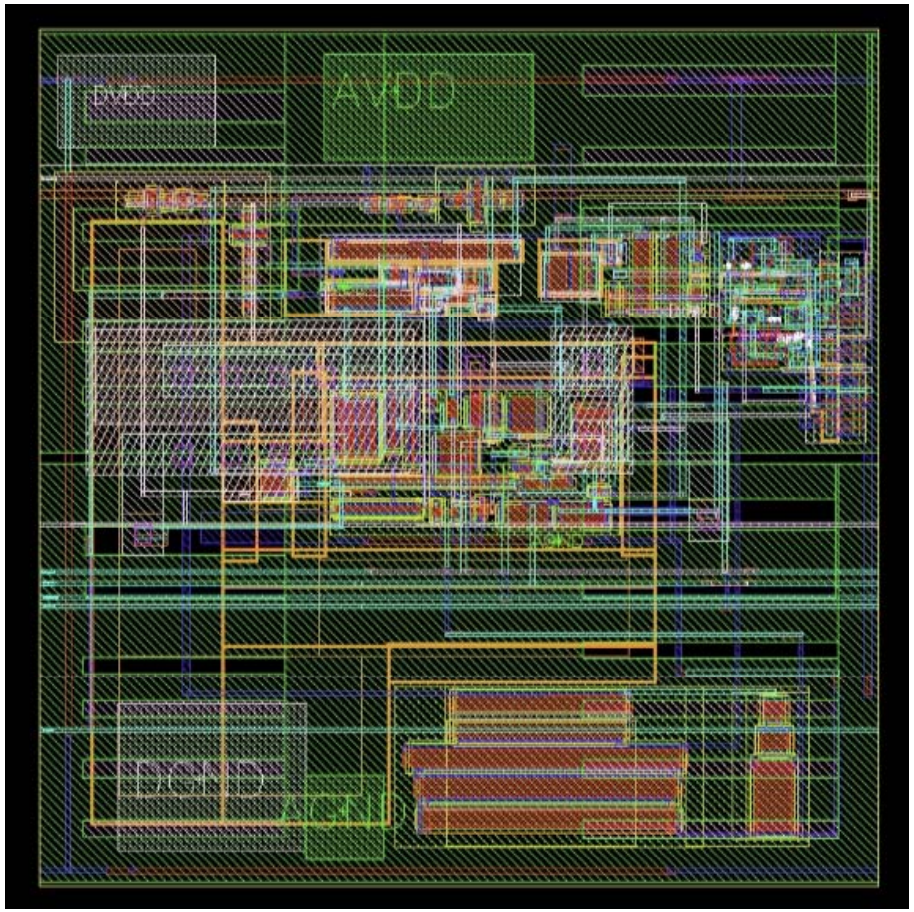


Threshold dispersion = 60 e

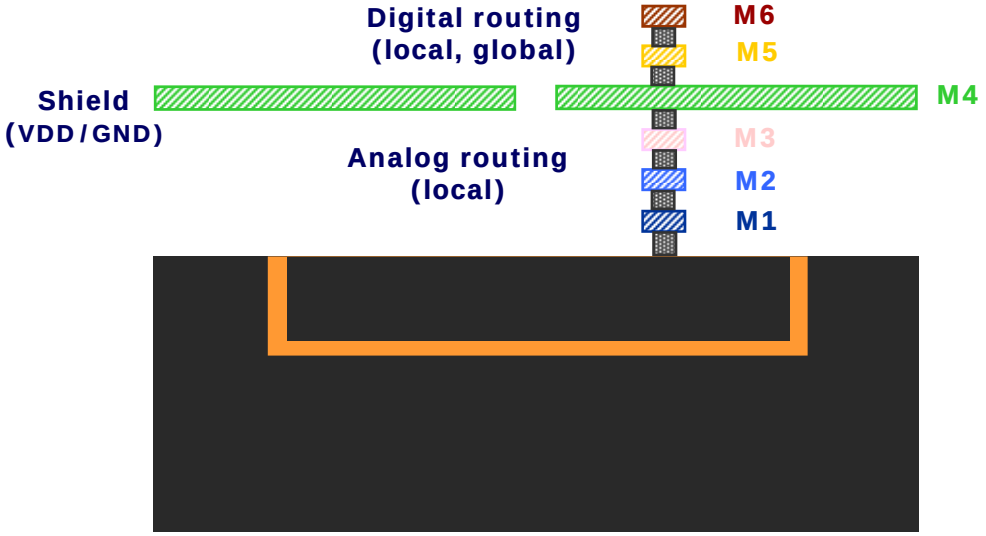
Average gain = 860 mV/fC

The APSEL4D pixel

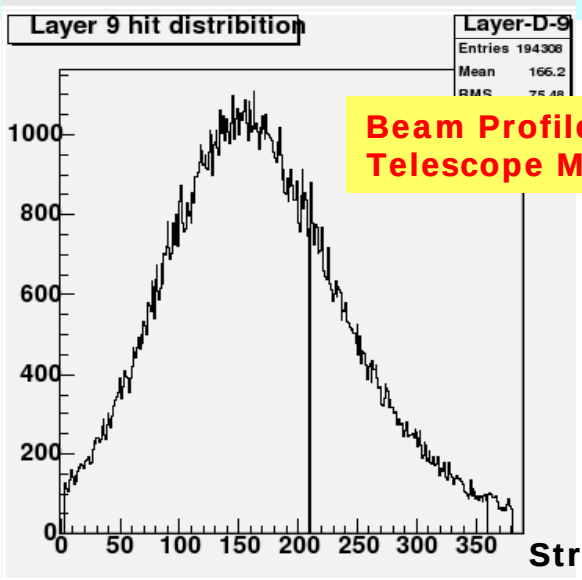
The sensing electrode has a T-shaped geometry, from the Deep N-Well and standard N-well extensions (A = 900 μm^2)



Sensor and analog lines had to be shielded from digital lines (continuous readout)



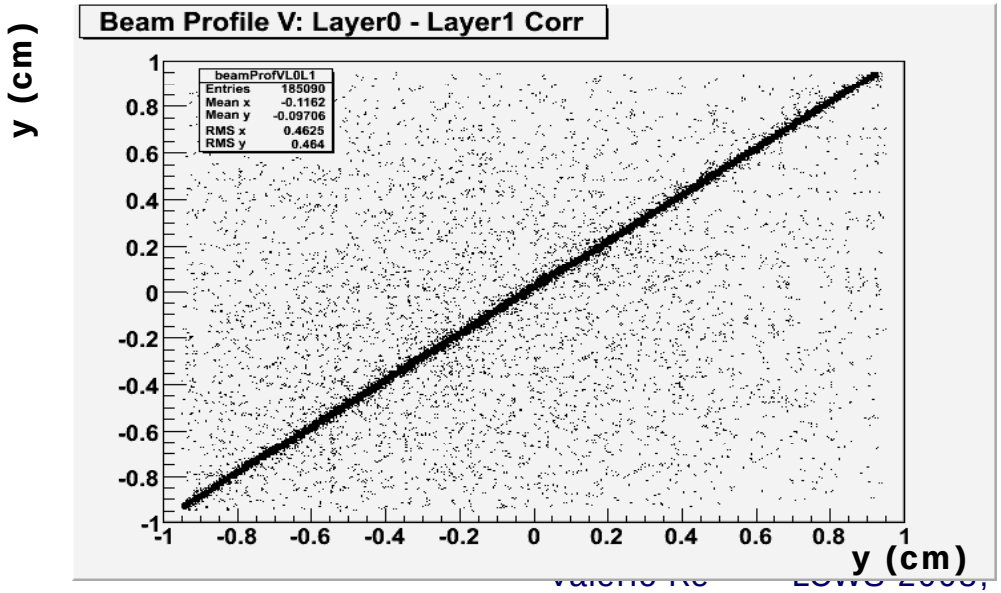
A first look to the CERN beam test data



Beam Profile – Telescope Module

- Beam test started last week @ CERN (T9). Main goals:
  - DNW MAPS matrix resolution & efficiency
  - Thin (200 μm) striplets module with FSSR2 readout chips
  - Demostrate LVL1 capability with tracker information sent to Associative Memories
  - New DAQ system developed for data push architecture

Y hit correlation Telescope T2 vs T1



Y hit correlation MAPS vs Telescope T1