A new 130 nm FE readout chip for microstrip tracking detectors

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Synopsis

- Results from SiTR_130-4
- Design and foundry of the new SiTR_130-88
- Perspectives

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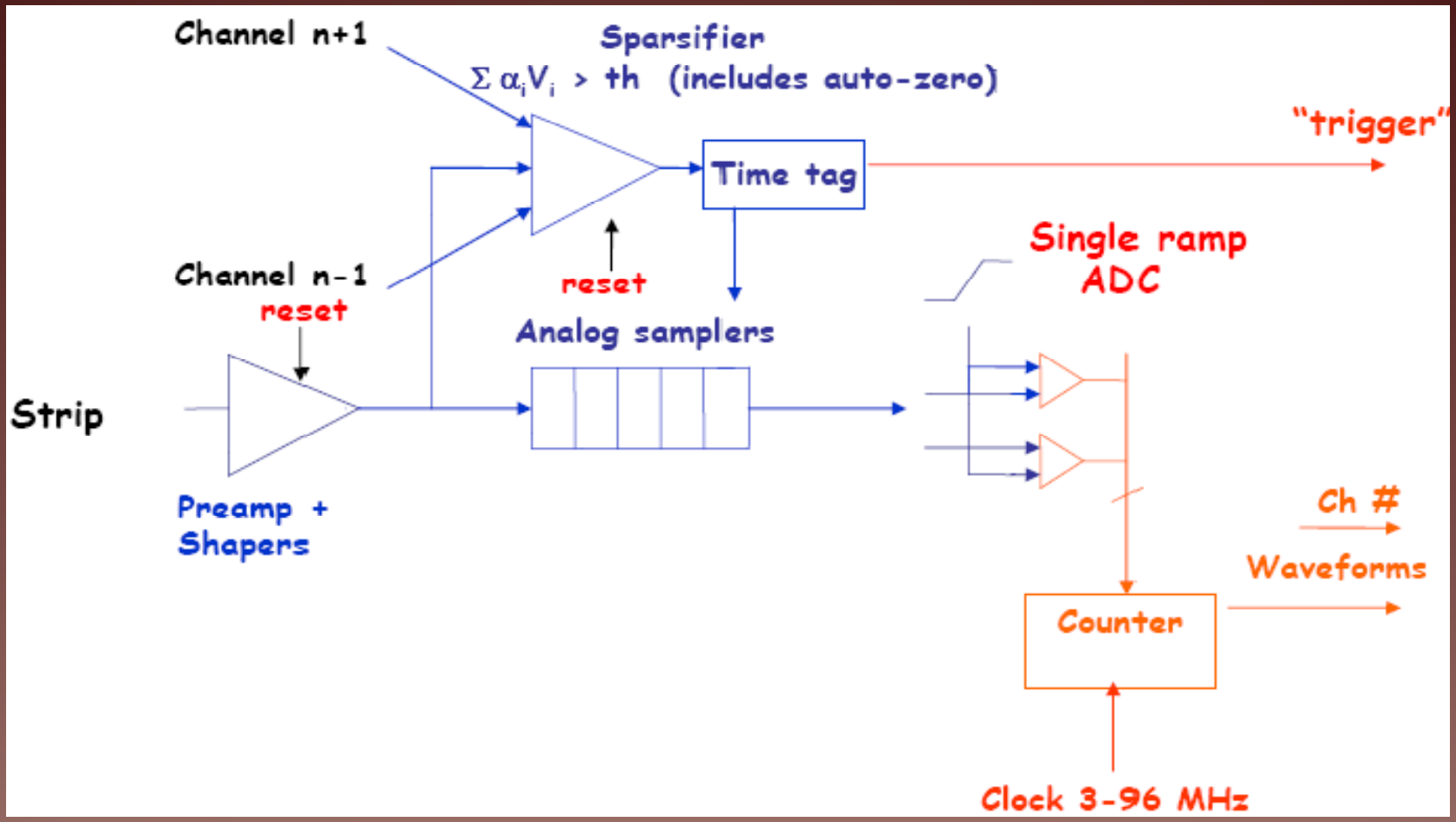
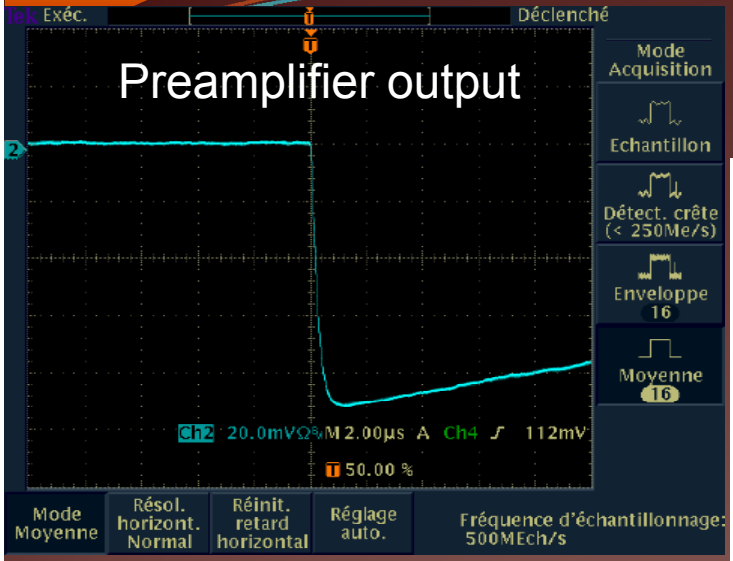
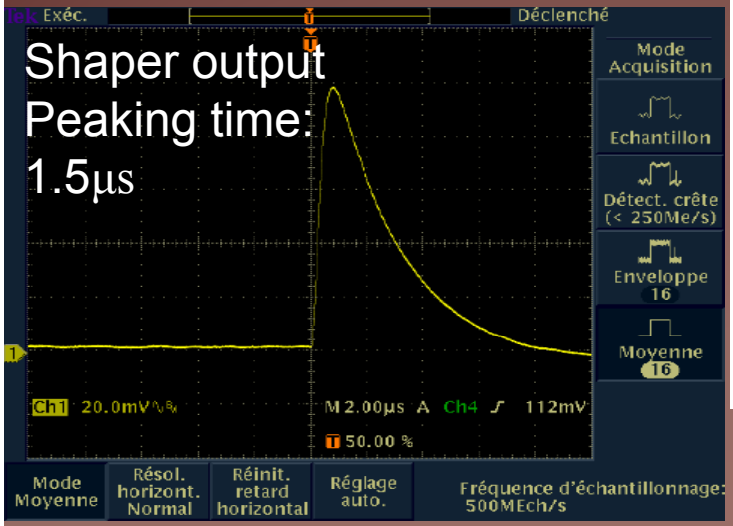
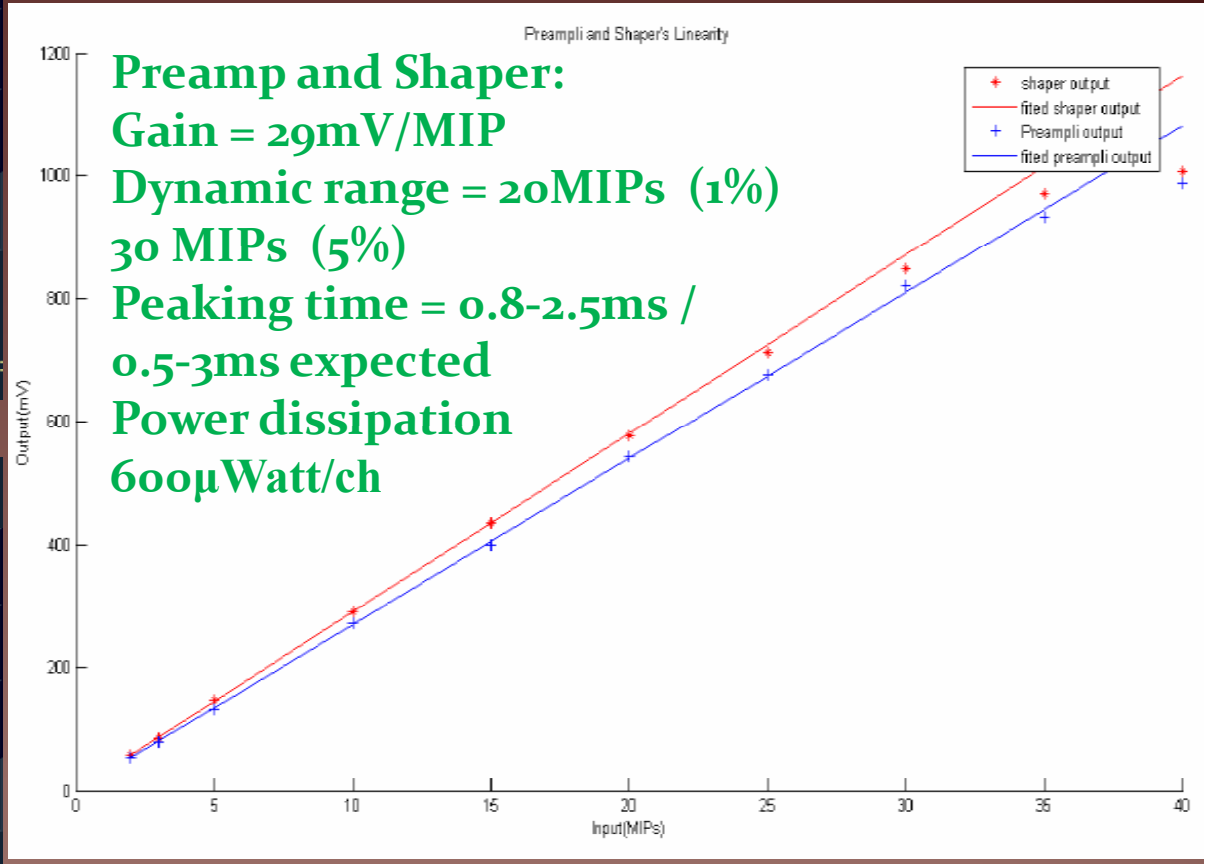
SiTR_130-4


Channel n+1
Sparsifier
$\Sigma \alpha_i V_i$ > th (includes auto-zero)
"trigger"
Time tag
Channel n-1
reset
reset
Analog samplers
Single ramp ADC
Strip
Preamp + Shapers
Ch #
Waveforms
Counter
Clock 3-96 MHz

SiTR_130-4: performances

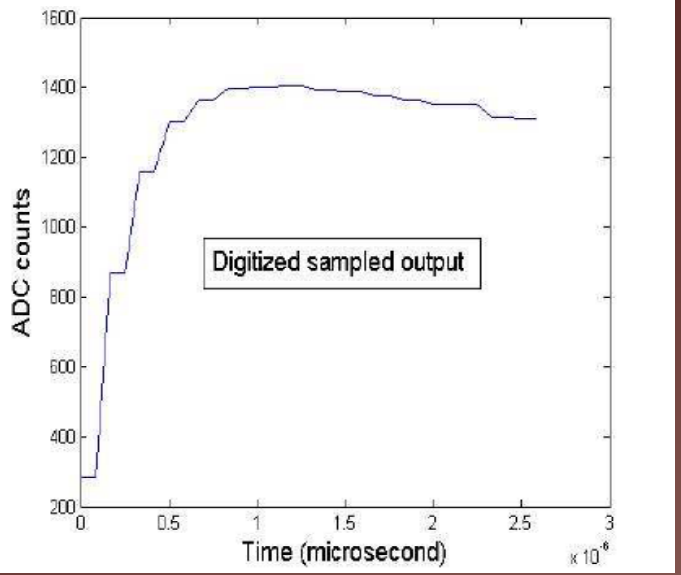






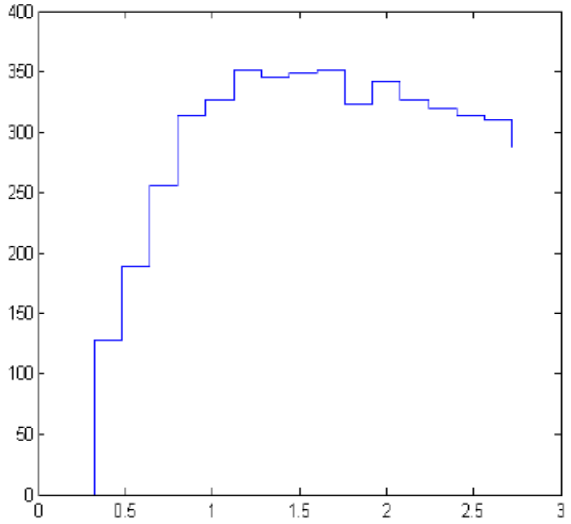
Preamp and Shaper:
Gain = 29mV/MIP
Dynamic range = 20MIPs (1%)
30 MIPs (5%)
Peaking time = 0.8-2.5ms / 0.5-3ms expected
Power dissipation 600µWatt/ch

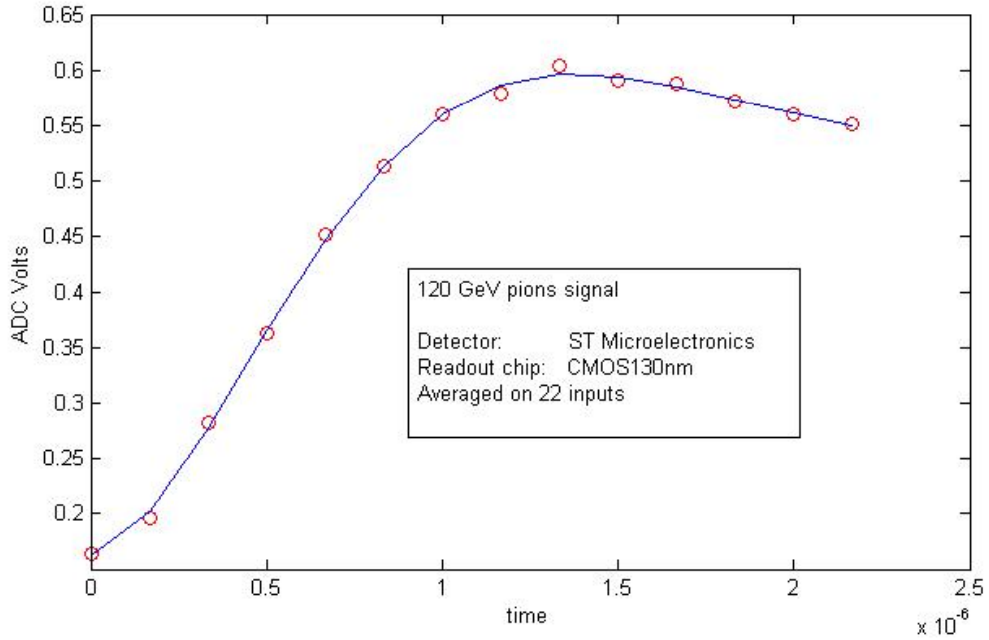
SiTR_130-4: performances (cont'd)



Digitized analogue pipeline output test pulse (left) and Laser response of detector + 130nm chip (right)

Digital oscilloscopy

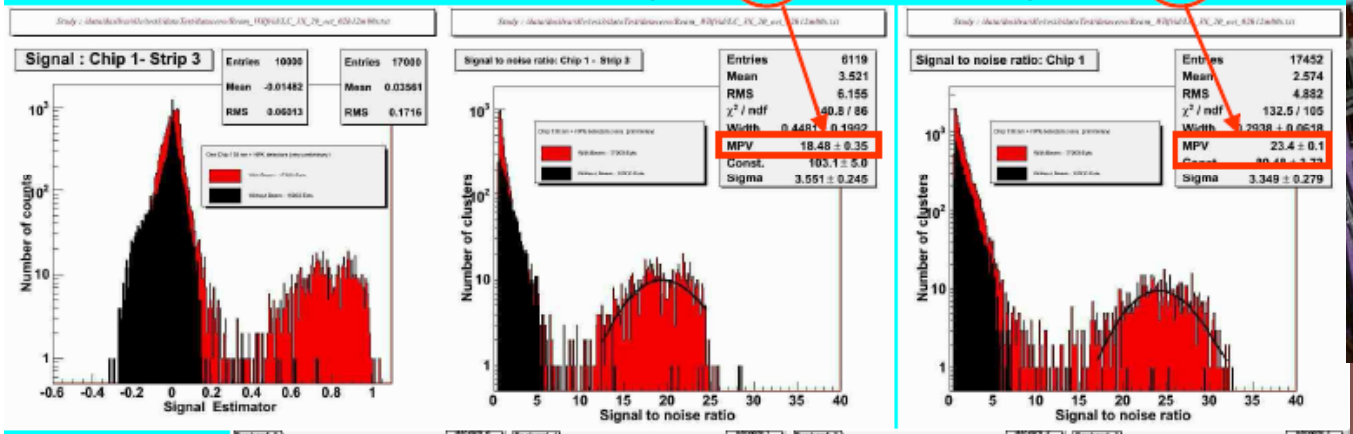




SiTR_130-4: test beam performances

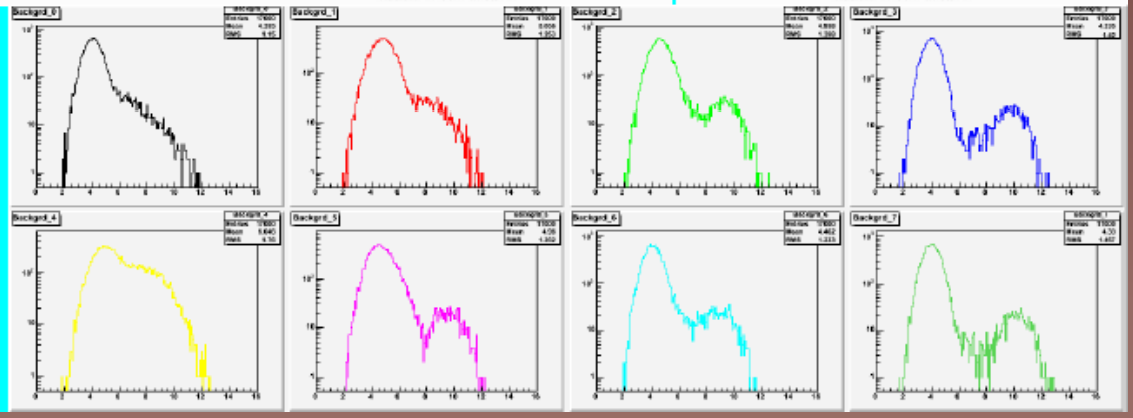
Results with the new HPK + SiTR-130

Black=beam off, red=beam on; 1 strip S/N 18 1 chip: S/N ~ 23



Test beam at SPS CERN, Oct 2007 combined with EUDET MAPS telescope

Strip length = 18,5 cm



Also extensive studies with Sr90 source at Lab test bench

The beam test includes a collaborative effort with several SiLC institutions (CU Prague, IFCA, IEKP, HEPHY, LPNHE, OSU, Torino U./INFN, CERN and DESY collaboration as well)

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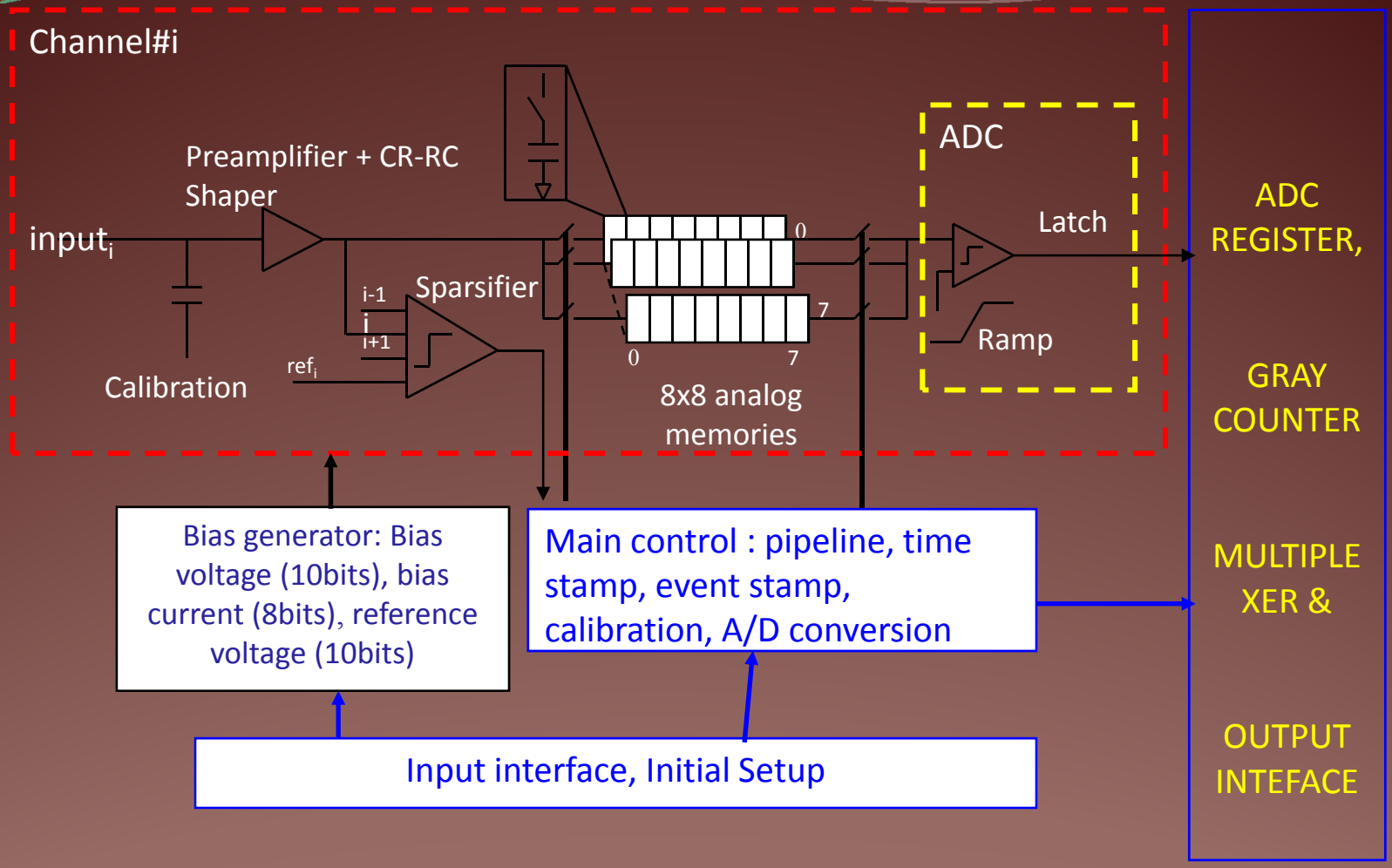
SiTR_130-88 schema



After very encouraging results obtained with the first pre-prototype

Go to the full version: SiTR_130-88

Main features of new circuit

88 channels (1 test channel): Preamplifier, shaper, sparsifier, analogue pipeline (8x8 cells), 12 bits ADC

2D memory structure: 8x8/channels

Fully digital control:

- Bias voltage(10 bits) and current (8 bits)
- Power cycling (can be switched on and off)
- Shaping time programmable
- Sampling frequency programmable
- Internal calibration (fully programmable 10 bits DAC)
- Sparsifier's threshold programmable per channel
- Event tag and time tag generation

=> High fault tolerance

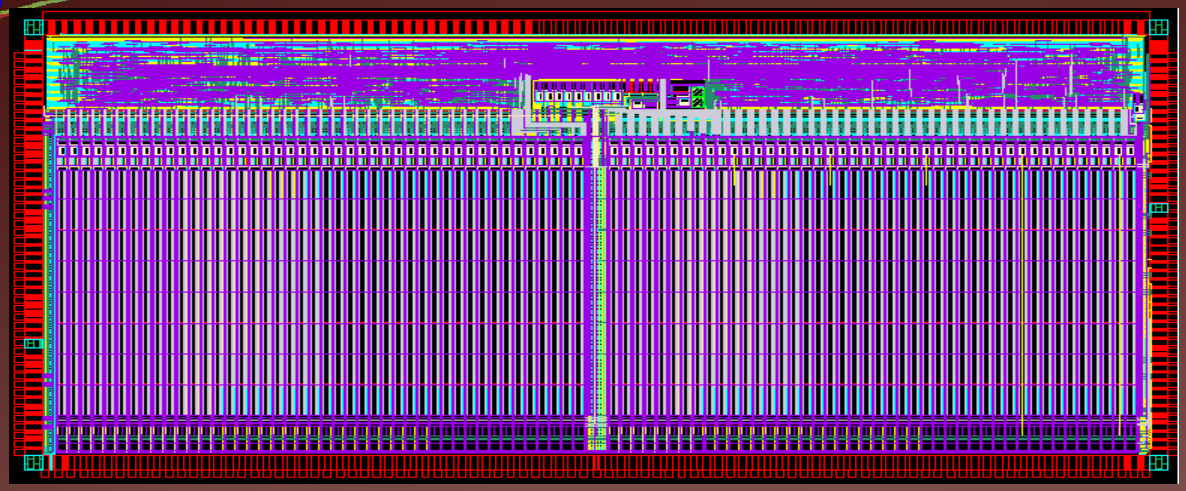
=> High flexibility, robustness

.....

2 Trigger modes: Internal (Sparsification integrated)

External (LVTTL) for beam test

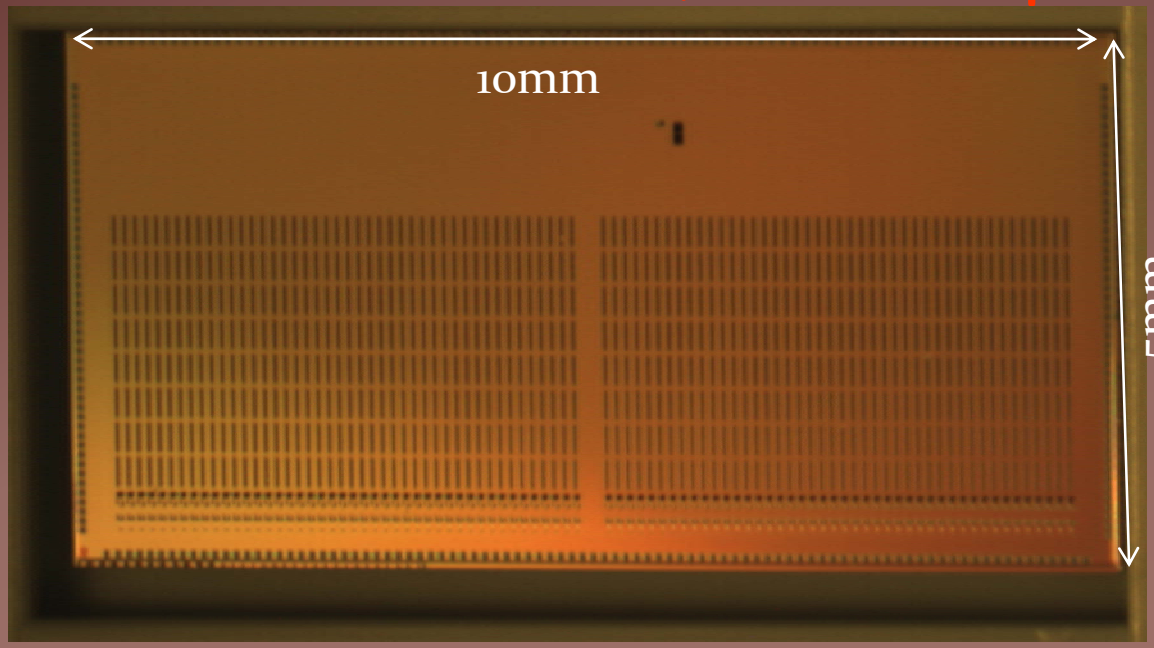
LAYOUT VIEW and PHOTOGRAPH



Size: 5mmx10mm
88 channels (105um pitch)
105umx3.5mm/channel

Analog: 9.5mmx3.5mm
Digital : 9.5mmx700um

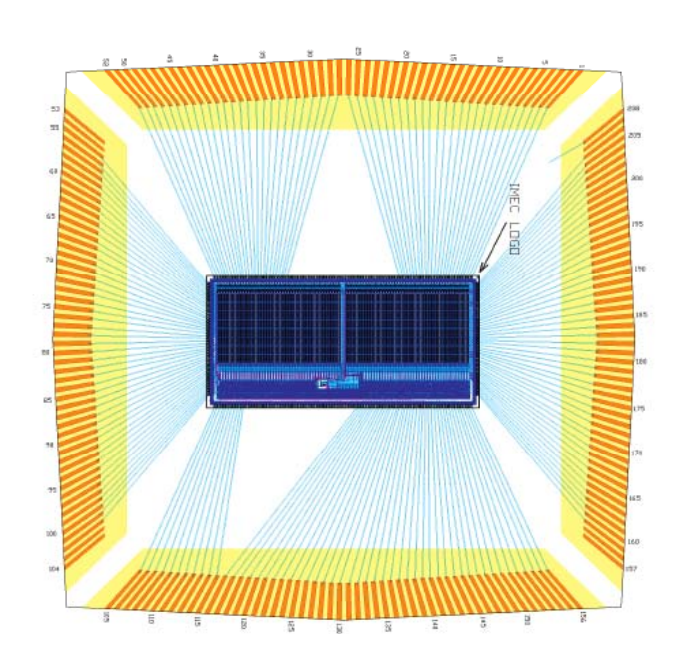
Submitted June 24th '08, received September 12 the naked chips



Photograph of the new chip SiTR_130-88

New readout chip in 0.13 µm: packaged version

BONDING DIAGRAM FOR CQFP208 PACKAGE



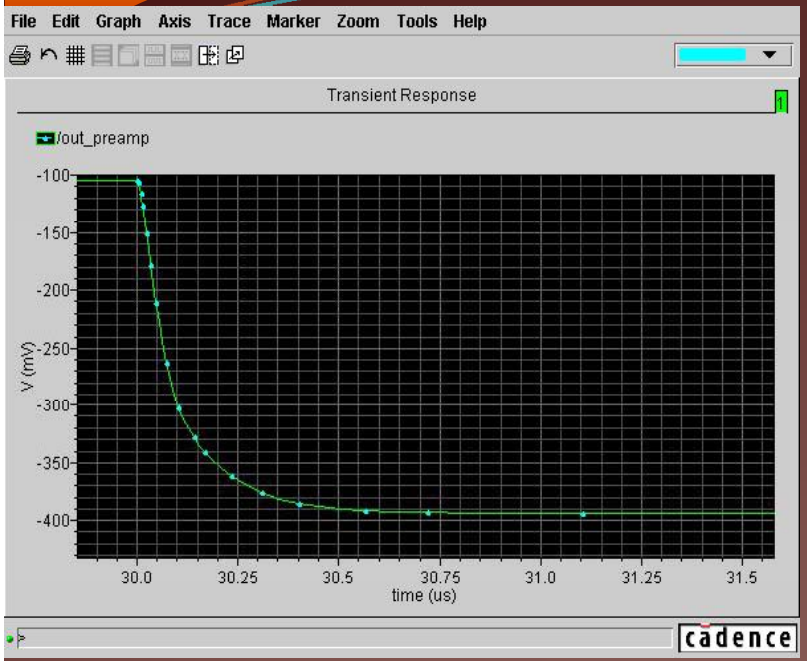
Package 208 pins
- 50 analog input
- 21 analog test out
- 33 digital pin (22 test pins)
- 107 supply pins

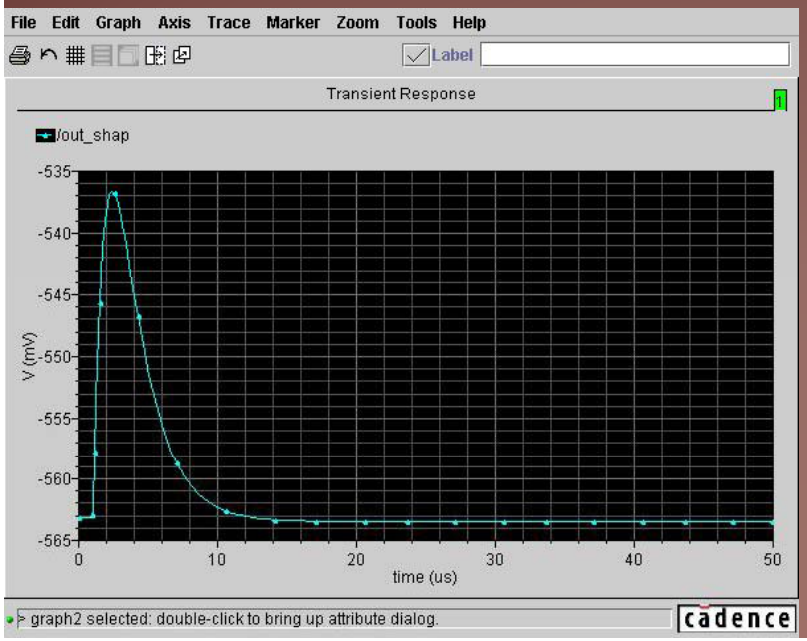
20 packaged chips
delivered October 15th

For a a detailed test of chip functionality & performances

Test is “easy” because the chip is “fully programmable”

Summary of simulation studies





Main present results from the simualtion studies
Preamplifier:
Charge gain: 27mV/MIP 5%
Linearity: 17 MIP (1%) to 29 MIP (5%)

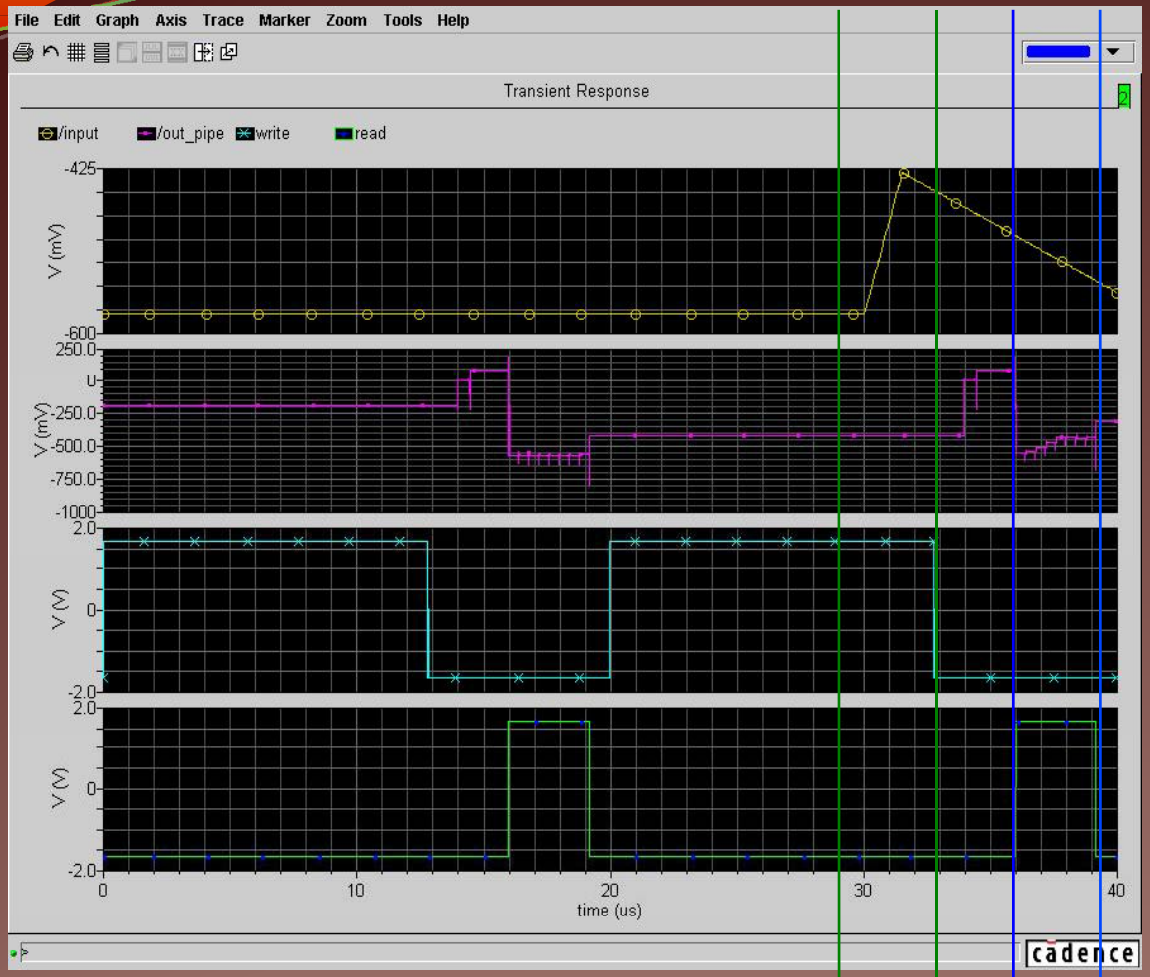
Shaper: 30mV/MIP ± 5%
Shaping time: 0.5 to 1.5 μs
Linearity: idem premaplifier
Noise: 625 + 9 e-/pF (1.5 μs)

Pipeline (8x8)
Sampling rate (2)
Linearity: idem premaplifier

ADC conversion time: about 85 μs (48 MHhz clock)

Calibration:
Integrated capacitor: 100 fF
Calibration pulse amplitude: 10 bits DAC (same as bias generator)
Overall power dissipation per channel: about 1mWatt
Total, not including power cycling

Summary of simulation studies (con’td)



Pipeline Input

Pipeline Output

Write command

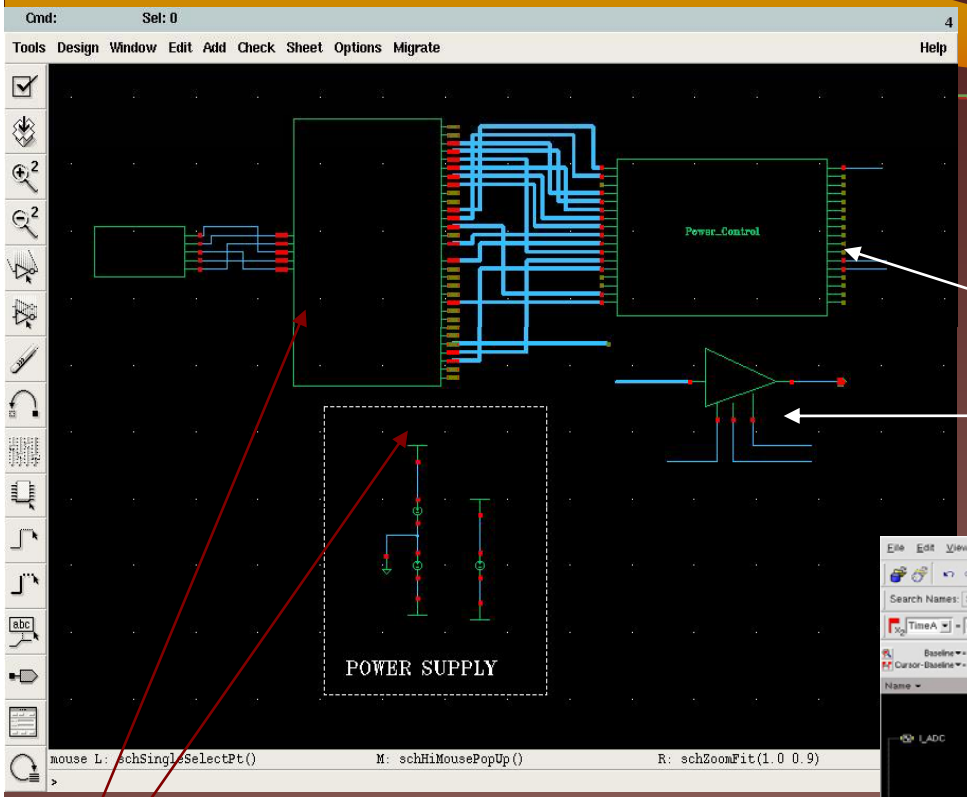
Read command

Pipeline simulation

Writing phase

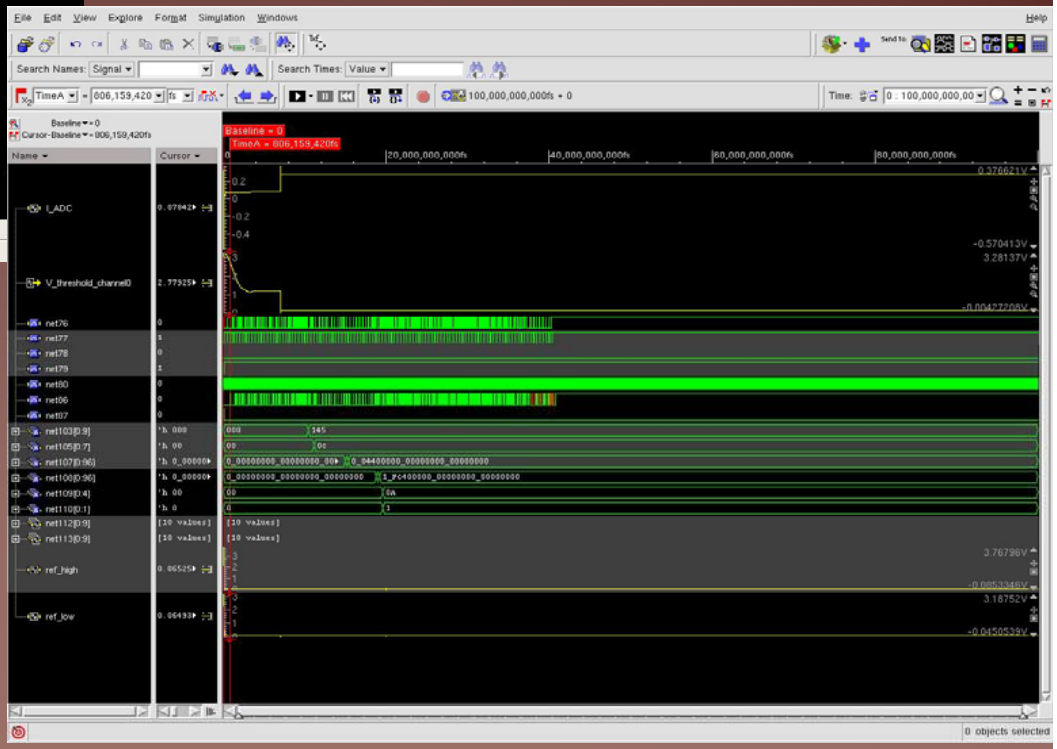
Reading phase

Among the big challenges in designing this chip: to find a way to perform the mixed mode simulation



Analogue

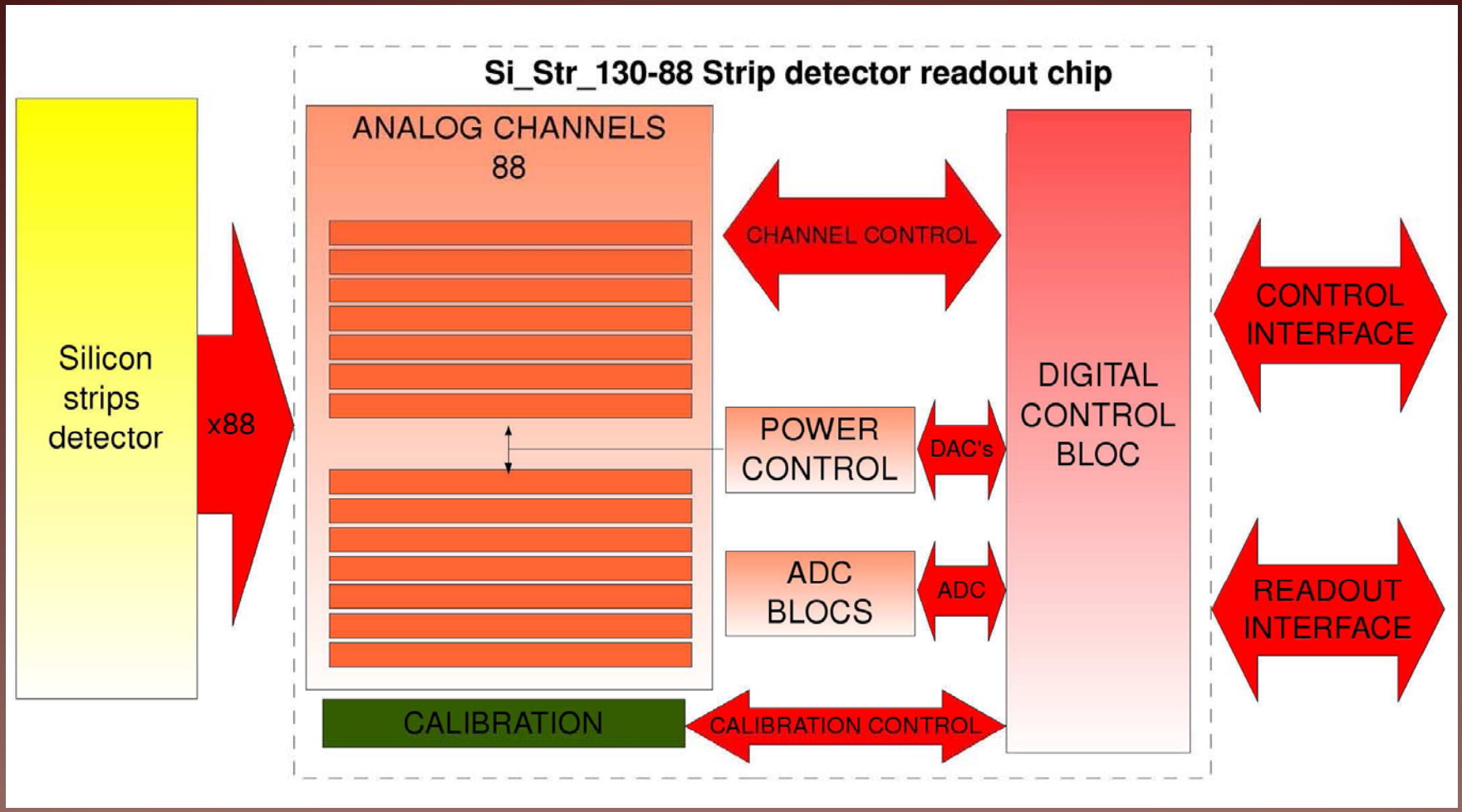
Mixed Mode simulation using AMS Designer - Cadence



Digital

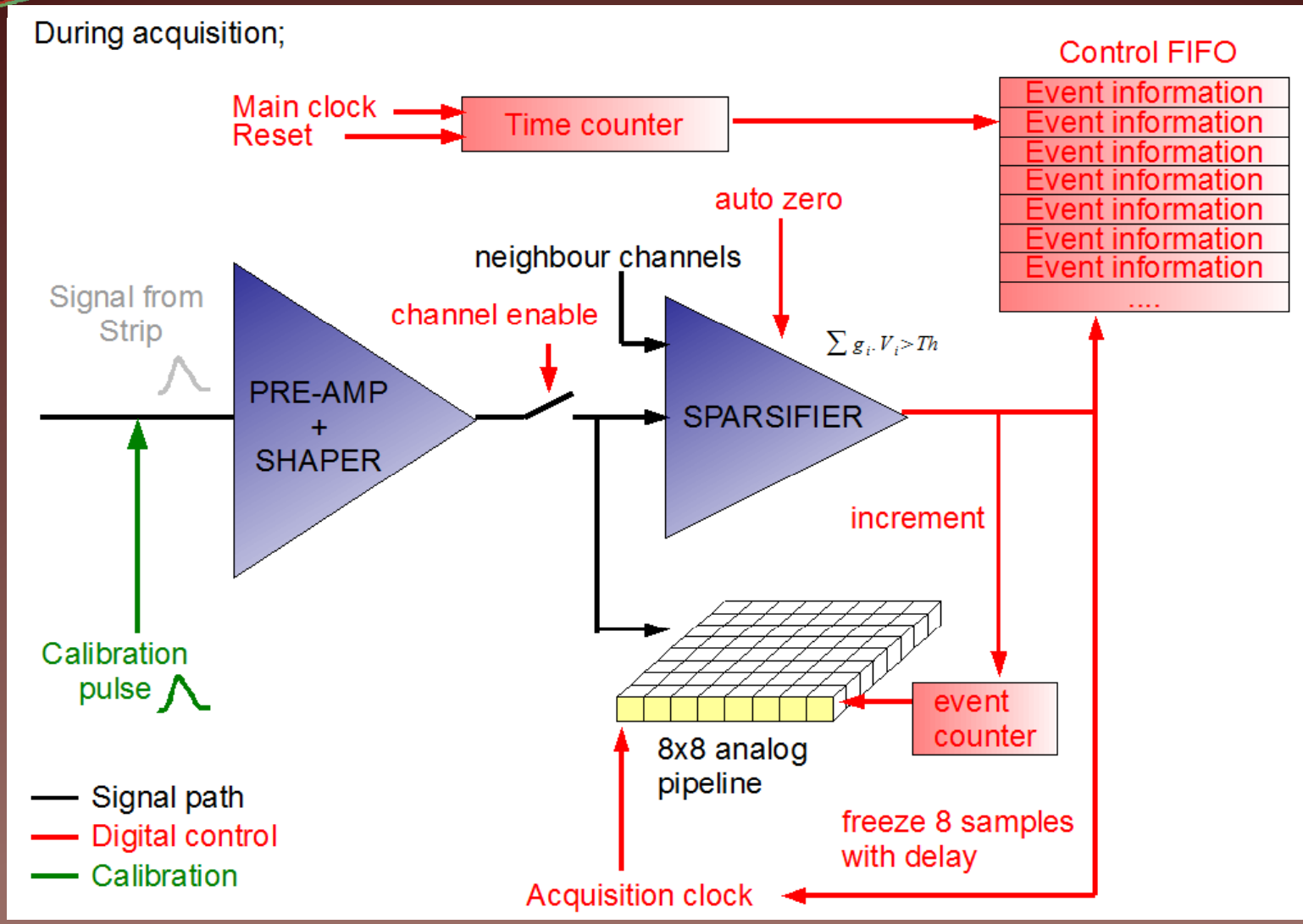
Simulation result
Yellow : Analogue signal
Green : Digital signal

Digital part

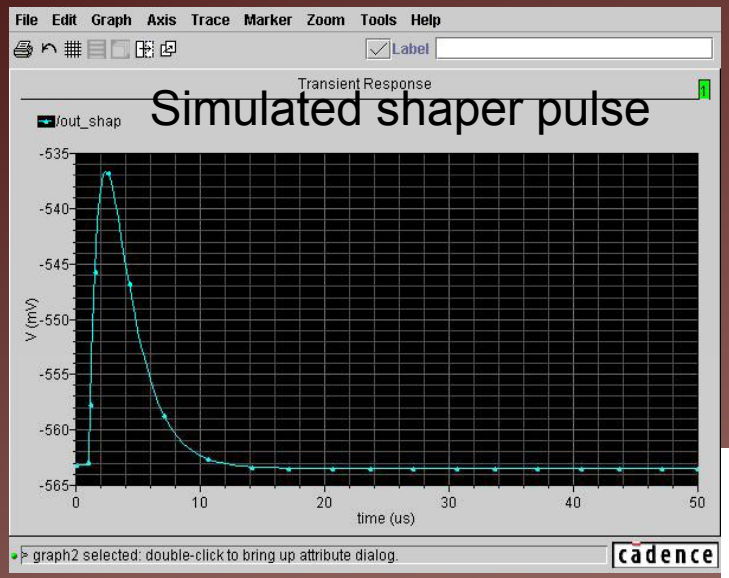


SiTR_130-88: System overview

DAQ during the bunch train

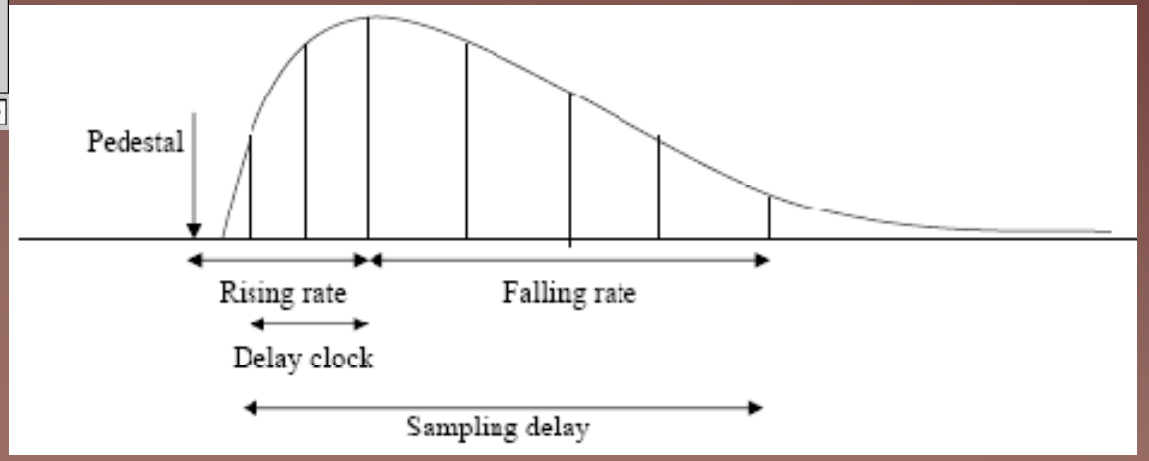


Sampling and conversion time:
All the 88 channels of the chip are converted in parallel.
There are 8x8 samples to be converted per channel; the conversion time per channel
Is approximately 85 μs thus a total of 5.44 ms is needed for the conversion

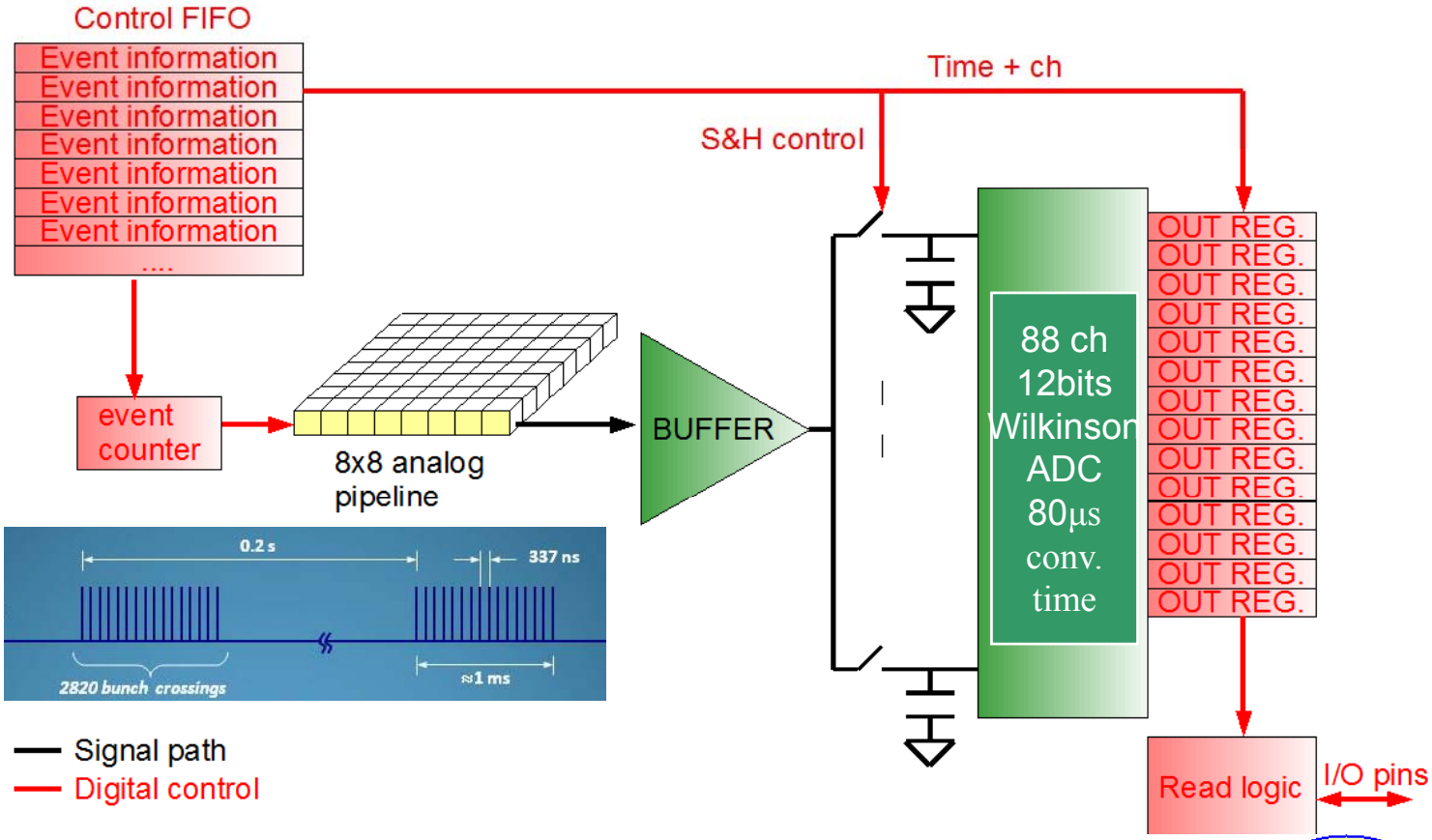


Simulated shaper pulse

Reconstruction of the pulse height: 8 samples including pedestal

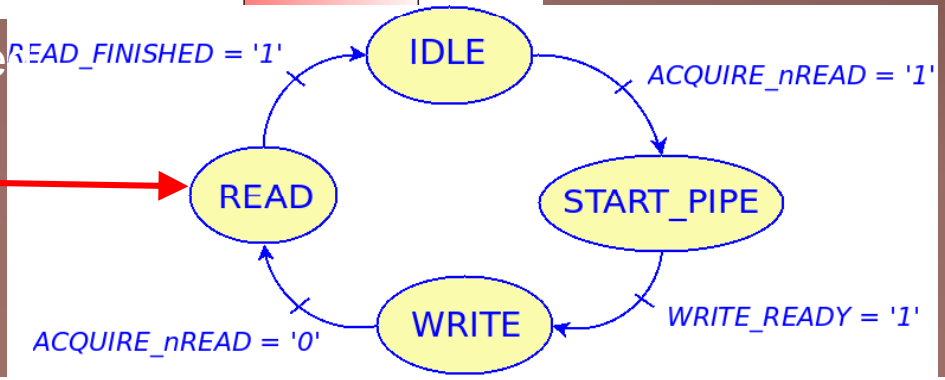


During IDLE time;



The acquisition control block is constructed around a finite state machine (fsm), with 4 states

(For more information see presentation at the DAQ session)



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Next version improvements

- Go to basic blocks of 256 channels and build modules of 512 channels or 1024 out of them (multiplexing factor is still under investigation)
- Thinning of the chip
- Next version in full wafer process (gain in space)
- Include latest results from the tests on the present chip
- Try the 90 nm CMOS technology

- For the longer term it is intended to prepare a fast version CLIC-like
- Pursue the direct connection chip onto the strip detector (bump bonding now, and starting to investigate 3D vertical interconnect as part of the global effort)

NOW WE ARE WORKING ON TESTING THIS CHIP!!