LLRF (WP02) Update

S. Simrock
for the LLRF Team

with contributions of VU-graphs from:
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Outline

- Status of Collaboration
- LLRF at FLASH
  - New Master Oscillator
  - Operational Experience
  - Machine Studies
  - Beam Feedback
  - 3.9 GHz system
- ATCA development
  - ATCA Hardware
  - ATCA Demonstration

Outline (C'nt)

- LLRF developments for the XFEL
  - Transient Detection
  - Piezotuner
  - MIMO Controller
  - Downconverter
  - Direct Sampling
  - Cavity simulator
  - Development system
- Documentation Projects

Status of the LLRF Collaboration

Status of Collaboration

- August 2008: Decision that LLRF will be German in-kind contribution
- Sept. 08 : Annex for remainder of 2008 signed with DMCS (Lodz), ISE (Warsaw), IPJ (Swierk)
- Sept. 08 : Collaboration meeting on Documentation of the LLRF (WP02)
- Oct. 08 : IFJ (Krakow) joined (installation work)

Attachment 1

Task / Item	Subtask / Item	Responsible person	Institute	Schedule	Cost [k€]
WP 1.2 Collaboration		Dariusz Makowski	DMCS	08-12.2008	0
deliverable	*Paper work: agreements, deliverables verification and acceptance, reports, etc…*				
WP 2.2 Detectors and Actuators	Preparation of requirement for digital vector modulator in Enterprise Architect	Szymon Tarnowski (100%)	DMCS	1.09.2008	0
deliverable	Requrements preparation	Szymon Tarnowski	DMCS	1.09.2008	
WP 2.2 Detectors and Actuators	Mathematical analysis and simulations of numerical modulation	Szymon Tarnowski (100%)	DMCS	1.09./2008	0
deliverable 1	Parameters for filters (bandwith vs cost vs stability)	Szymon Tarnowski	DMCS	1.10.2008	
deliverable 2	Sampling frequency, samples count, sample width	Szymon Tarnowski	DMCS	1.10.2008	
deliverable 3	Optimal FPGA implementation of hardware	Szymon Tarnowski	DMCS	1.10.2008	
WP 2.2 Detectors and Actuators	Tests and measurements of the digital upconverter at DESY	Szymon Tarnowski (100%)	DMCS	1.12.2008	2
deliverable 1	Development of testboard	Szymon Tarnowski	DMCS	1.11.2008	
deliverable 2	Tests at DESY site	Szymon Tarnowski	DMCS	1.12.2008	
WP 2.3 Digital feedback	Preparation of requirement for Digital Feedback in Enterprise Architect	Dariusz Makowski (50%), Adam Zawada (50%)	DMCS	1/10/2008	0
deliverable	*The requirements for ATCA carrier boards and AMC modules will be delivered in Enterprise Architect. Requirements and documentation for submodules of the ATCA-based feedback system.*				
WP 2.3 Digital feedback	Development of PCIe drivers for ATCA carrier	Dariusz Makowski (50%), Grzegorz Jabłoński (50%)	DMCS	1/09/2008	0
deliverable	*Source codes for low level drivers for the first version of carrier board*				
WP 2.3 Digital feedback	Development of LLL driver for ATCA carrier	Wojciech Jałmużna	DMCS	1/09/2008	0
deliverable	*VHDL codes for low latency link drivers for the first version of carrier board*				
WP 2.3 Digital feedback	Development of diagnostic application for ATCA carrier board	Dariusz Makowski (100%)	DMCS	1/11/2008	0
deliverable	*Application with GUI for PC computer and procedures written in C/C++ for the IPMC microcontroller will be delivered. ATCA carried with IPMC controller will be used as a demonstrator.*				
WP 2.3 Digital feedback	Design of PCIe Root Complex mezzanine board with Power Quick III processor (hardware)	Dariusz Makowski (50%) , Piotr Krasiński (50%)	DMCS	1/12/2008	8
deliverable	*Mezzanine module with PowerQuick III processor with high-speed connectors.*				
WP 2.3 Digital feedback	Development of IPMI ATCA board with Renesas microcontroller	Dariusz Makowski (100%)	DMCS	1/10/2008	3
deliverable	*ATCA carrier board with Renesas Microcontroler.*				
WP 2.3 Digital feedback	Development of IPMI software for Atmega microcontroller	Adam Zawada (100%)	DMCS	1/10/2008	3
deliverable	*Software and low level drivers for ATMEGA 1281 microcontroller for ATCA-IPMI carrier board.*				
WP 2.3 Digital feedback	Development of IPMI software for Renesas microcontroller	Dariusz Makowski (50%), Adam Zawada (50%)	DMCS	1/11/2008	1
deliverable	*Software and low level drivers for Renesas M16C65 microcontroller for ATCA-IPMI carrier board.*				
WP 2.3 Digital feedback	Application for management and monitoring of ATCA devices using IPMI standard (software)	Dariusz Makowski (50%), Adam Zawada (50%)	DMCS	1/10/2008	1
deliverable	*Application with GUI for PC computer and set of procedures written in C/C++ will be delivered. ATCA carried in version one with IPMC controller will be used as a demonstrator.*				
WP 2.3 Digital feedback	Application for configuration data storage in configuration data base (software)	Dariusz Makowski (50%), Bartosz Sakowicz (50%)	DMCS	1/11/2008	0
deliverable	*The set of procedures for storing and reading firmware from database will be delivered.*				
WP 2.3 Digital feedback	Development of second version of ATCA carrier board	Dariusz Makowski (50%), Wojciech Jalmuzna (50%)	DMCS	1/11/2008	13
deliverable	*Schematic diagrams will be created and the ATCA carrier board will be delivered.*				
WP 2.3 Digital feedback	Development of operating system and low level drivers for Power Quick III processor	Adam Piotrowski (50%), Dariusz Makowski (25%) Grzegorz Jabłoński (25%)	DMCS	1/09/2008	0
deliverable	*Source code for low level drivers for diagnosis of PCI Express subsystem, several patches for Linux operating systems to enable the MSI interrupt support, port for Freescale Board Support Package to RadiSys board.*				
WP 2.3 Digital feedback	ATCA and AMC PCB templates for Mentor Graphics	Dariusz Makowski (100%)	DMCS	2/08/2008	0
deliverable	*A library with ATCA and AMC template for Mentor Graphics will delivered*				
WP 2.4 Piezo compensation	Preparation of requirements for Piezo Control in Enterprise Architect	Konrad Przygoda	DMCS	30.11.2008	0
deliverable	*The requirements for Piezo Control will be delivered in Enterprise Architect. Requirements and documentation for various submodules (Piezo Drivers, 32-channel control system with Gigalink, ATCA-based Piezo Controller)*				
WP 2.4 Piezo compensation	Piezo controller development with SimCon-DSP board	Konrad Przygoda	DMCS	30.09.2008	0
deliverable	*The multichannel scope for online detuning measurements (microphonics identification), the multichannel Lorentz force detuning compensation system as well as automatic control algorithms will be developed*				
WP 2.4 Piezo compensation	Piezo controller development with PowerQUICC III processor and Virtex 5 FPGA and external 32-ch DAC card	Konrad Przygoda (50%), Dariusz Makowski (25%), Grzegorz Jabłoński (25%)	DMCS	30.08.2008	3
deliverable	*A prototype system based on Frescale and Xilinx starter kits, firmware for Xilinx, PowerQuick processor will be delivered.*				
WP 2.4 Piezo compensation	Design and laboratory tests of Piezo Drivers prototypes 2 prototypes ver.1 and ver.2 was designed and tested.	Konrad Przygoda (25 %), Tomasz Pożniak (75 %)	DMCS	30.11.2008	6
WP 2.4 Piezo compensation	Design and development of 8-channels Piezo Drivers for permanent installation in the FLASH accelerator The 3 boxes with 8-channels Piezo Drivers was designed and tested. These Piezo Drivers are ready to the permanent installation in the FLASH accelerator	Konrad Przygoda (25 %), Tomasz Pożniak (75 %)	DMCS	30.11.2008	6
WP 2.4 Piezo compensation	Design and development of 8-channels piezo driver	Konrad Przygoda (50%), Tomasz Pożniak (50%)	DMCS	30.11.2008	6
deliverable	*8-channels piezo driver units integrated with ATCA based architecture and 32-channels control system with GigaLink*				
WP 2.4 Piezo compensation	Design and development of 32-channels control system with GigaLink	Konrad Przygoda (50%), Dariusz Makowski (50%)	DMCS	30.10.2008	4

Development of IPMI software for Atmega microcontroller

Employees: **Adam Zawada (100 %)**

Task description: The software for the first version of IPMI development Carrier board (currently available) will be developed. The software communicates with ShelfManager and allows for ATCA carrier board activation. The software supervises AMC modules and forward messages to the main dual ShelfManager.

Deliverables: Software and low level drivers for ATMEGA 1281 microcontroller for ATCA-IPMI carrier board.

Total credit: 2,86 ke Required time: 4 mwks

Development of IPMI software for Renesas microcontroller

Employees: **Dariusz Makowski (50 %), Adam Zawada (50 %)**

Task description: The software for the second version of IPMI development Carrier board with Renesas microcontroller will be developed. The software communicates with ShelfManager and allows for ATCA carrier board activation. The software supervises AMC modules and forward messages to the main dual ShelfManager.

Deliverables: Software and low level drivers for Renesas M16C65 microcontroller for ATCA-IPMI carrier board.

Total credit: 4,29 ke+1 ke Required time: 6 mwks

Application for management and monitoring of ATCA devices using IPMI standard (software)

Employees: **Dariusz Makowski (50 %), Adam Zawada (50 %)**

Task description: The aim of this task is to develop an application for communication with ShelManager to monitor and control all subsystems of the board directly from the PC computer connected to the ShelManager via Ethernet cable. All functionality defined by ATCA standard will be supported. The application allows to develop custom functions, e.g. FPGA firmware download via IPMI link. The application can be easily updated in the future to introduce new funcions.

Deliverables: Application with GUI for PC computer and set of procedures written in C/C++ will be delivered. ATCA carried in version one with IPMC controller will be used as a demonstrator.

Total credit: 2,86 ke+0,5 ke Required time: 4 mwks

Application for configuration data storage in configuration data base (software)

Employees: **Dariusz Makowski (50 %), Bartosz Sakowicz (50 %)**

Task description: The aim of this task is to develop the application that allows to store and recover FPGA configuration in external database. The method of FPGA programming requires to be discussed, Ethernet, IPMI or other medium will be used.

Deliverables: The set of procedures for storing and reading firmware from database will be delivered.

Total credit: 4.29 ke Required time: 4 mwks

Development of second version of ATCA carrier board

Employees: **Dariusz Makowski (50 %), Wojciech Jałmużna (50 %)**

Task description: The aim of this task is design and fabricate second version of the ATCA carried board with Virtex V5 FPGA, DSP, IPMC and PowerQuick III socket. The carried board will allow to carry out first physical experiment with controller. No software/firmware for will be delivered.

Deliverables: Schematic diagrams will be created and the ATCA carrier board will be delivered.

Total credit: 5,71 ke+10 ke Required time: 8 mwks

Development of operating system and low level drivers for Power Quick III processor

Employees: **Adam Piotrowski (50%), Dariusz Makowski (25%), Grzegorz Jabłoński (25%)**

Task description: In the frame of this task, several improvement of Linux operating system will be proposed and implemented. The most important of them are: implementations of MSI interrupt support in Linux kernel, porting

LLRF at FLASH
New Master Oscillator

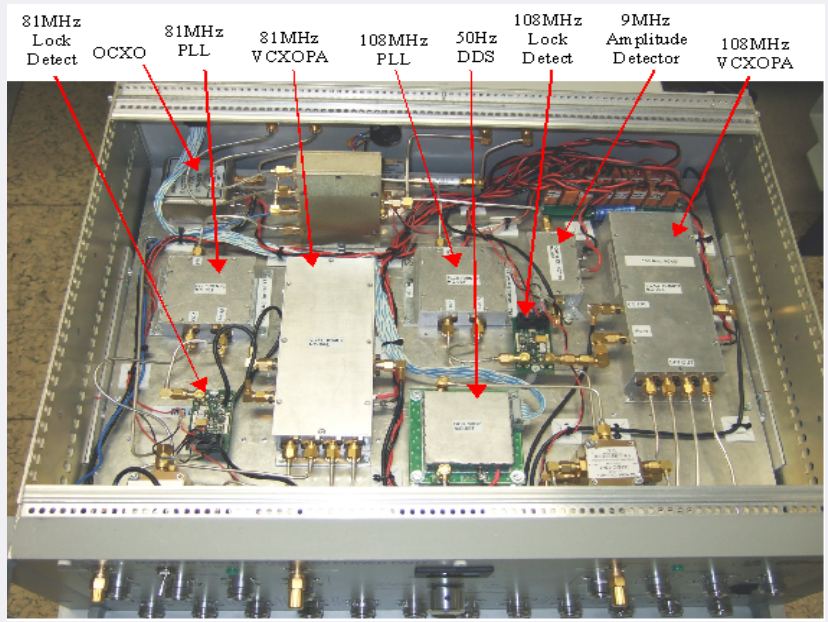
Some History

- In 2001 a 20 page requirement document created by H.W. was sent to industry. Only one company offered building the MO. Others claimed they could not do it or offered very expensive research

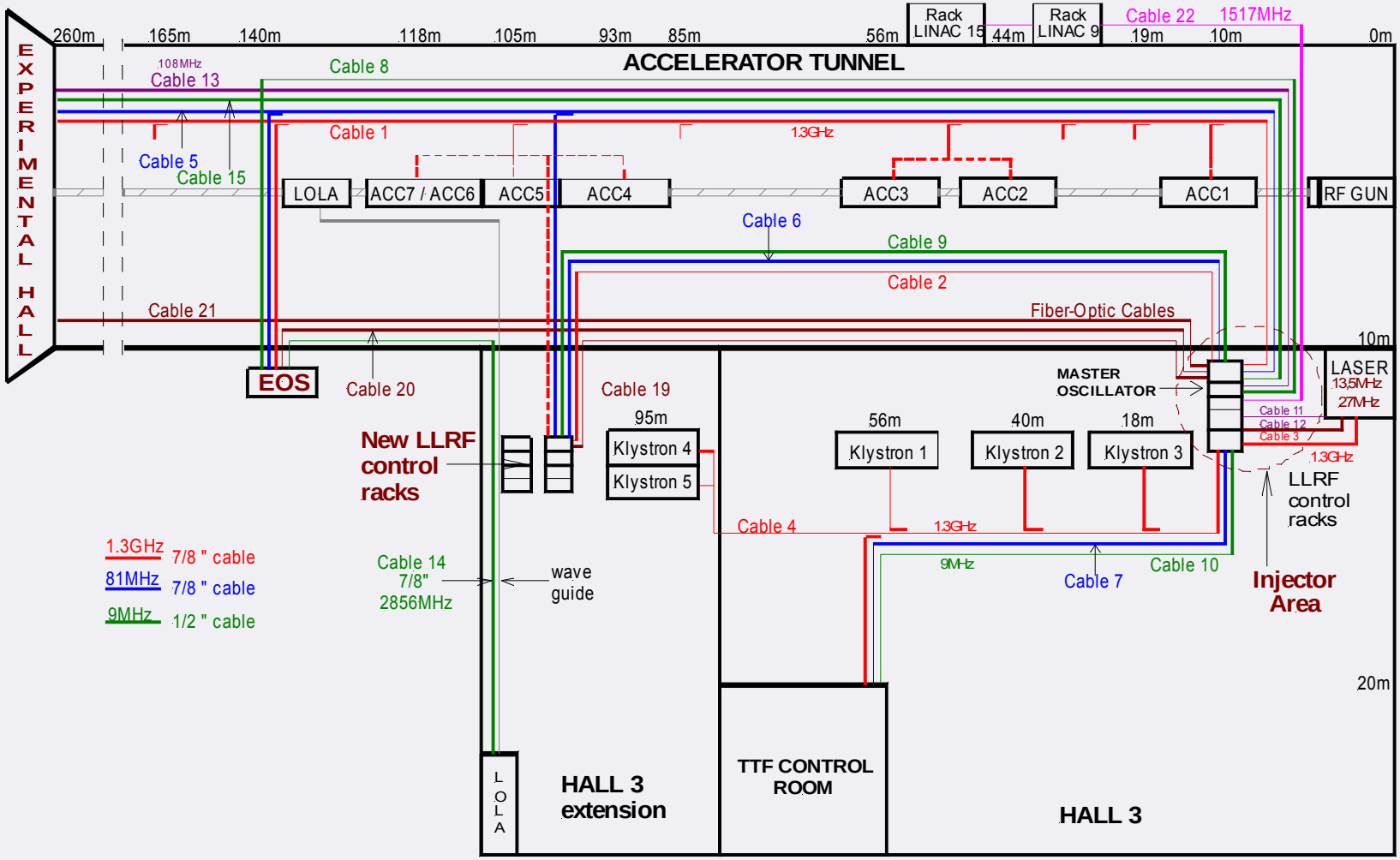
Very first New MO
1 crate!

- Requests for new signals, frequencies and powers, more tap points forced changing concept and rebuilding ready boxes. This influenced the growth of the diagnostic system and the power supply.
- Many problems had to be solved: e.g. cabling, power supply filtering, ground loops, heat dissipation, sensitivity to mechanical vibrations, parts breaking down (manufacturer error), commercial components not fulfilling specs....

New Master Oscillator installed at FLASH

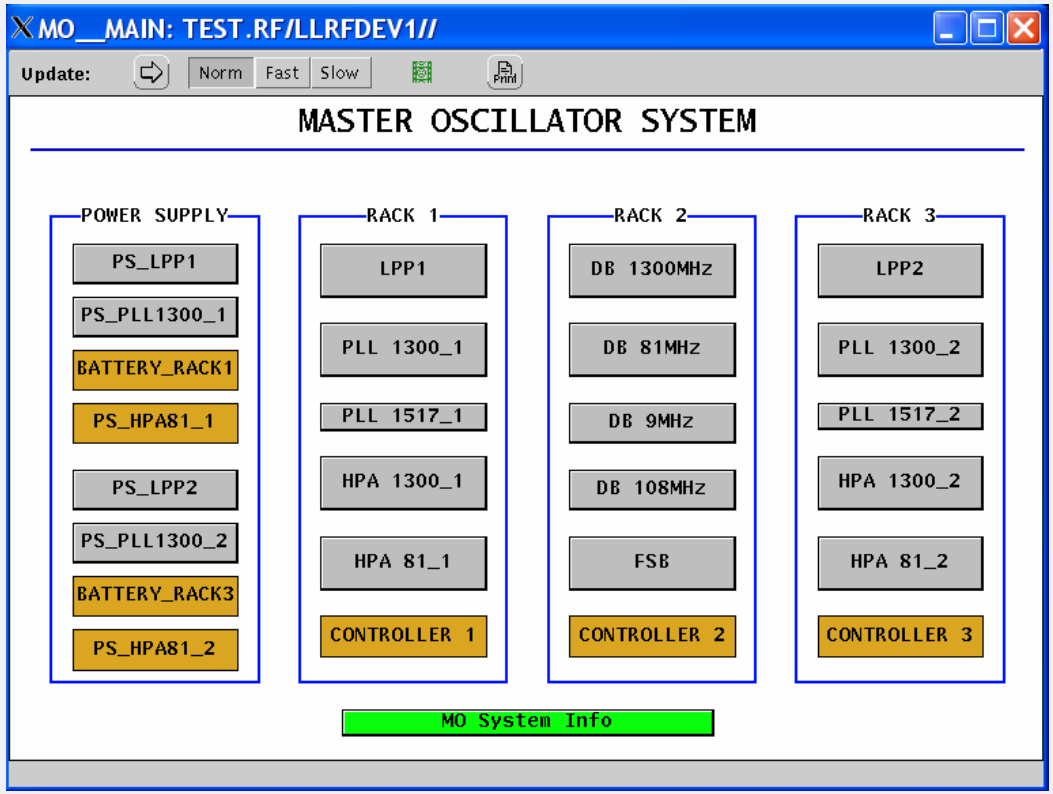


MO Distribution



MO Diagnostics

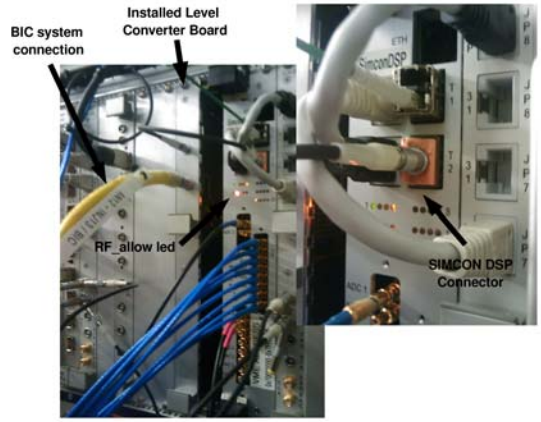
- Measured are:
- Power levels
- Phase changes over amplifiers
- VSWR of most important cables
- Crate temperatures
- PLL lock status
- VCO control voltages
- Power supply voltages and currents

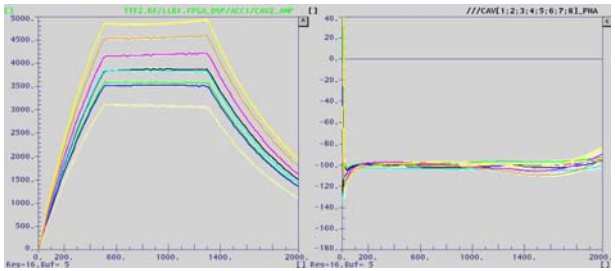


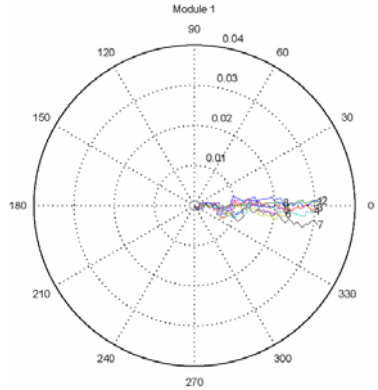
FLASH LLRF
Operation and Machine Studies

Progress on ACC1 Control

- New Simcon DSP system
- Beam based Adaptive FF
- BIC interlock interface
- Amplitudes and phases are available from controller for individual cavities (easy to calibrate)







Improvements on RF Operation

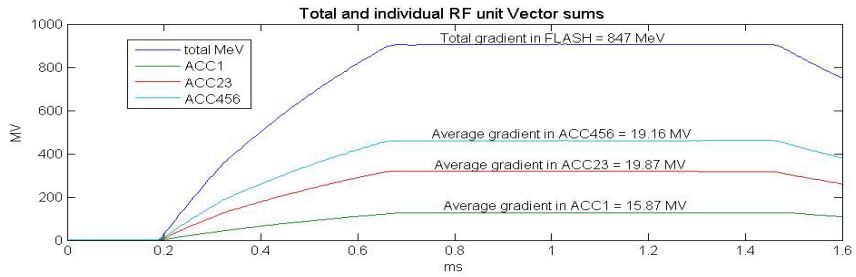
- More stable condition of ACC1 operation by changing power distribution and adjusting the phases (Energy gain from ACC1 ~130MeV)
- New diagnostics for DSP ADC readout for ACC2-ACC6 (DSP67 systems)
- More diagnostics for LLRF/HPRF chain measurement (Example: Investigation of ACC23 amplitude and phase jumps)
- Improved Adaptive Feedforford procedure for ACC2-ACC6
- Less phase drifts after installation of new MO

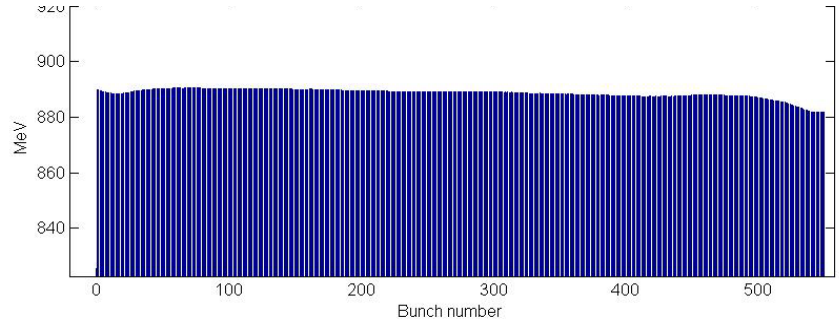
Machine Studies

- ACC1 control with Simcon DSP system
- LLRF control test at ACC23 with Simcon system
- LLRF Application Study
- Test of 24 channel FPGA based controller
- Lorenz force detuning compensation demonstration using ATCA prototype system
- Piezo control Automation
- New Master Oscillator Installed and commissioned
- Sufficient LLRF performance during long pulse 9mA experiment

9mA Experiment: RF Performance

- Successful RF operation with 900 MeV energy and 800us flat-top for all accelerating modules
- ~500 bunches at ~2.6nC (1MHz) with low losses
- Set-up all modules with 800us flat-top and 1GeV total energy
- RF control worked well, and ramping up the number of bunches was smooth and rapid





Operational experience during FLASH operation

General problems with LLRF

- Drifts and jumps caused by various reasons
- Broken cable connection
- Lack of diagnostics and automation

Some examples:

- Unstable Gun operation (frequently) – reason unclear, may be wrong calibration of virtual probe signal or operation very close to limits – problem is investigated.
- Unstable ACC operation – wrong VS calibration and/or operation close to limits
- Drifts in the machine – the situation is much better after MO upgrade.
- Jumps in phase and amplitude – e.g. in ACC1 there was a long fight (over 2 months) against subtle timing problem in DOOCS server, finally workaround was applied and problem disappeared. Another example is jumps caused by bad cable connection (happen from time to time).

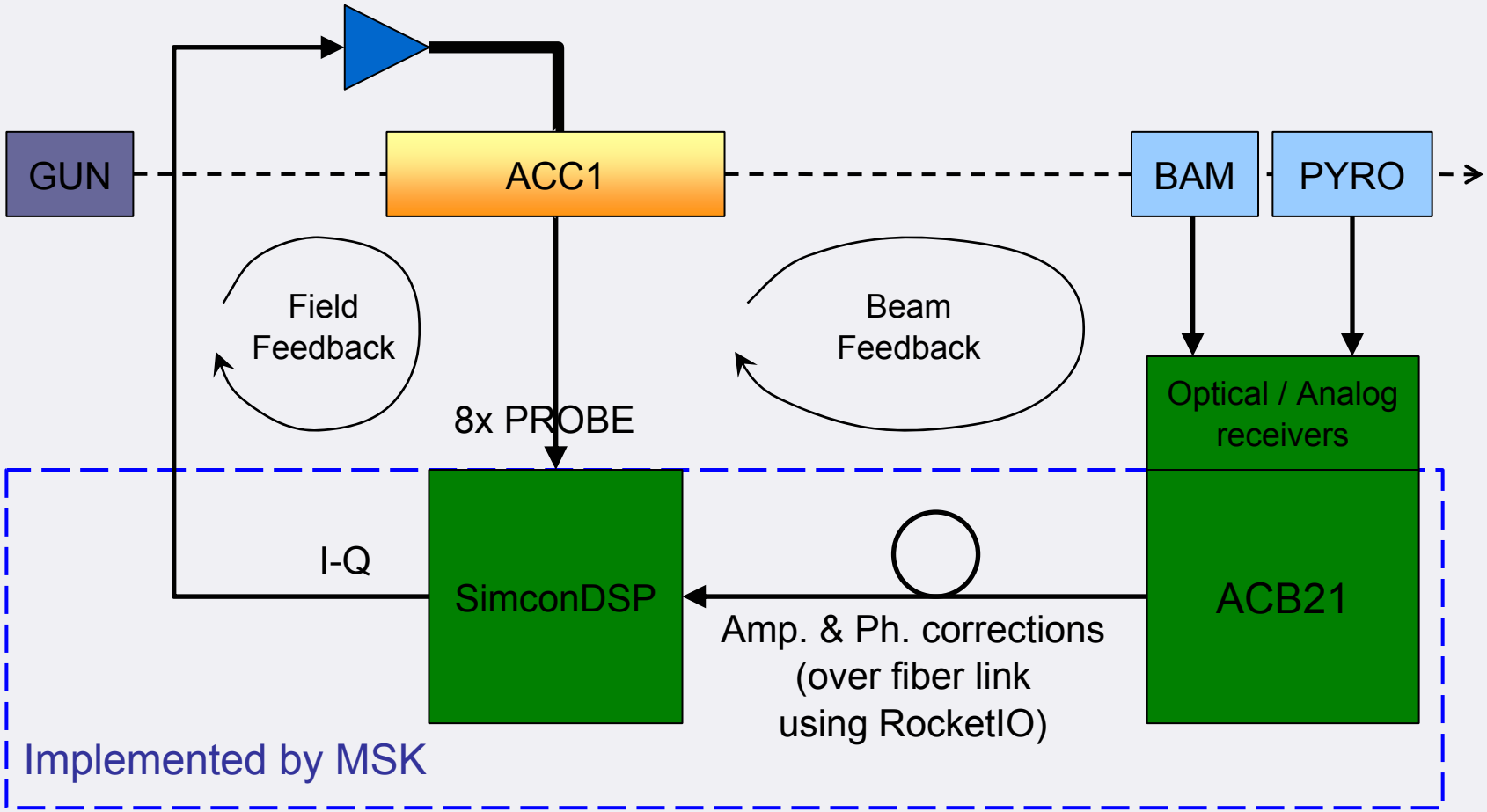
Operational experience during FLASH operation

Further examples:

- Machine state messed after studies – several times the particular parameters (e.g. klystron HV settings) and/or hardware configuration (e.g. terminators missing, cable disconnected) were not restored after studies caused problems during operation. Automation and diagnostics would help to deal with that.
- Operators mistakes (e.g. rebooting of hang up server without stopping RF, not stopping AFF algorithm after event).
- Wrong hardware configuration – after reboot the hardware did not initialize correctly.
- Hardware failures.

FLASH LLRF
Beam Feedback

Scheme of beam based feedback at FLASH



Beam based feedback

Tasks done by MSK:

- ACB 2.1 board designed manufactured and assembled
- Implemented firmware for ACB 2.1 board to receive signals from detectors (BAM and PYRO) and calculate amplitude and phase corrections
- ACC1 controller firmware improved to receive beam based feedback corrections from ACB
- The installation of ACC1 LLRF controller upgraded to SimconDSP
- New DOOCS server for ACC1 written and installed for operation (it supports new BBF features implemented in the controller)

Results:

- Bunch arrival time jitter decreased from 150-200fs to 25-50fs

FLASH LLRF
3.9 GHz System

Realization

LLRF control for the 3.9 GHz system is **in principle identical** to the 1.3 GHz concept:

- VME based with as many as possible standard hardware boards
- SIMCON DSP based
- -> Standard fallback LLRF solution with modified downconverters

We expect additional developments in:

- LO-Generation hardware (3.9 GHZ out of 1.3 GHz with low noise)
- Downconverters hardware (new IF-scheme, drift-calibration)
- FPGA firmware and DOOCS server modifications

Status (1)

1. We are assempling one **VME crate + SIMCON based hardware** including a 3.9 GHz **converter box** with a LLRF system capable of regulation of 4 3.9 GHz Cavities and on RF station. We build this from parts we already have or which are available. Some parts are still missing –> delay. The **noise performance** of this system is going to be charackterized in the laboratory to end of August and alternative concepts for the receiver can then be worked out if necessary. From experiences at FLASH and the simulations we can estimate the impact on the beam parameters (jitter, energy fluctuations, bunch length).
2. We are trying to aquire diploma or Phd students for following projects (4-5 months, supervised by M. Felber, F. Ludwig, M. Hoffmann):
   - RF-Bord design, PCB filter design
   - Upgrade of DWC VME board to 3.9 GHz operation
   - Driftfree detectors 1.3 GHz + 3.9 GHz

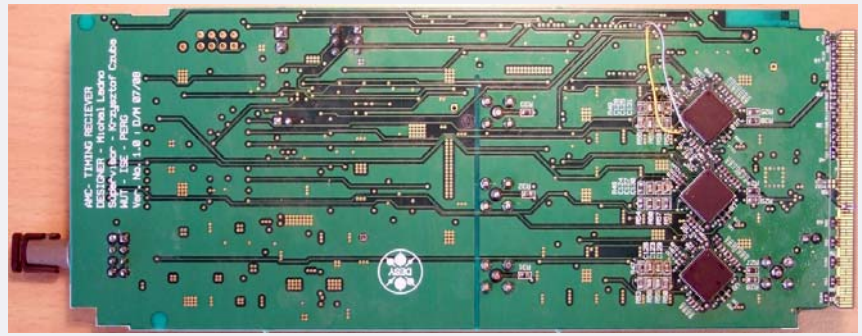
Status (2)

3. **simulation software** is beeing worked on to understand:
   - Impact of Field stability on beam parameters
   - The necessary requirements for LLRF control
   - Stability and max. gain of controller
4. FPGA firmware is beeing modified for noise charackterization tests.
5. DOOCS server installation, comissioning, maintainance turned out to be **problematic**. There is no active support from MCS so far. We will have to find a solution here.

ATCA Hardware Development

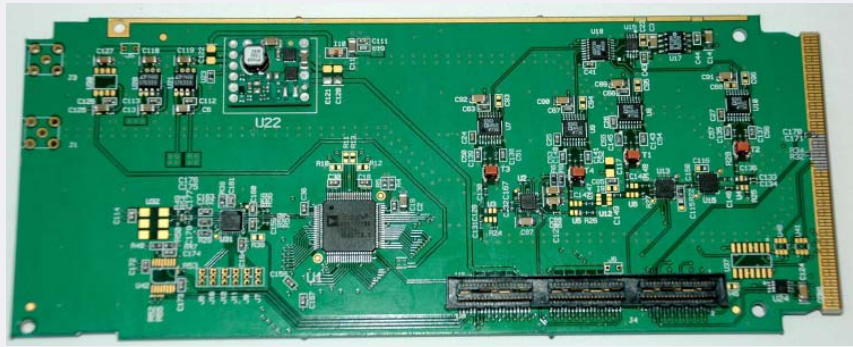
Achievement : AMC – Timing Module

Prototype has been tested.
Modules provides clock signals to the carrier board

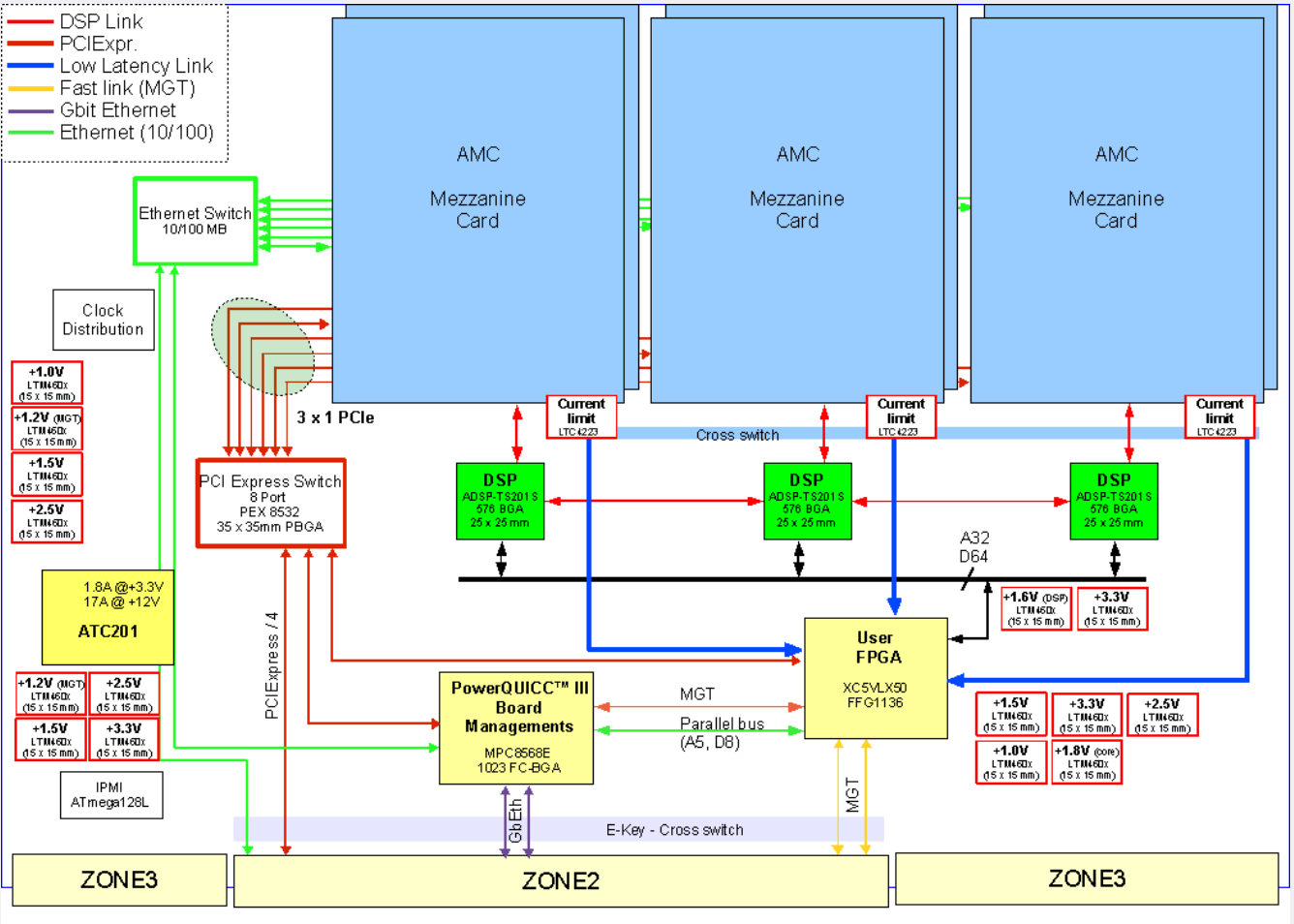


Achievement : AMC – VM (Vectro Modulator)

Digital up-converter has been tested. Modules provides output signal from the control system to the klystron.



Achievement : New concept and design for the ATCA Carrier Board



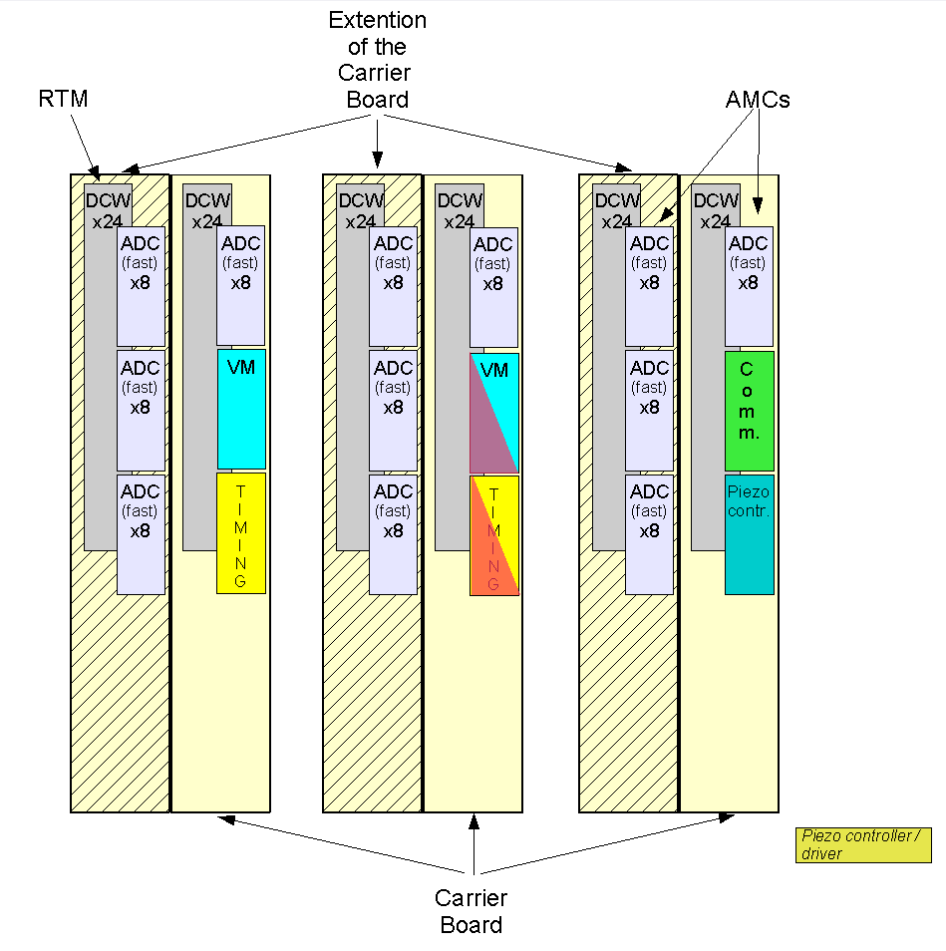
Carrier Board

- design ready for manufacturing
- several technical (mechanical) problem have been solved

CB consists of 2 boards:
- processor board
- extention board

- implemented „flexible" communication schema

Basic elements of the LLRF system



Carrier Board (main board + extension)

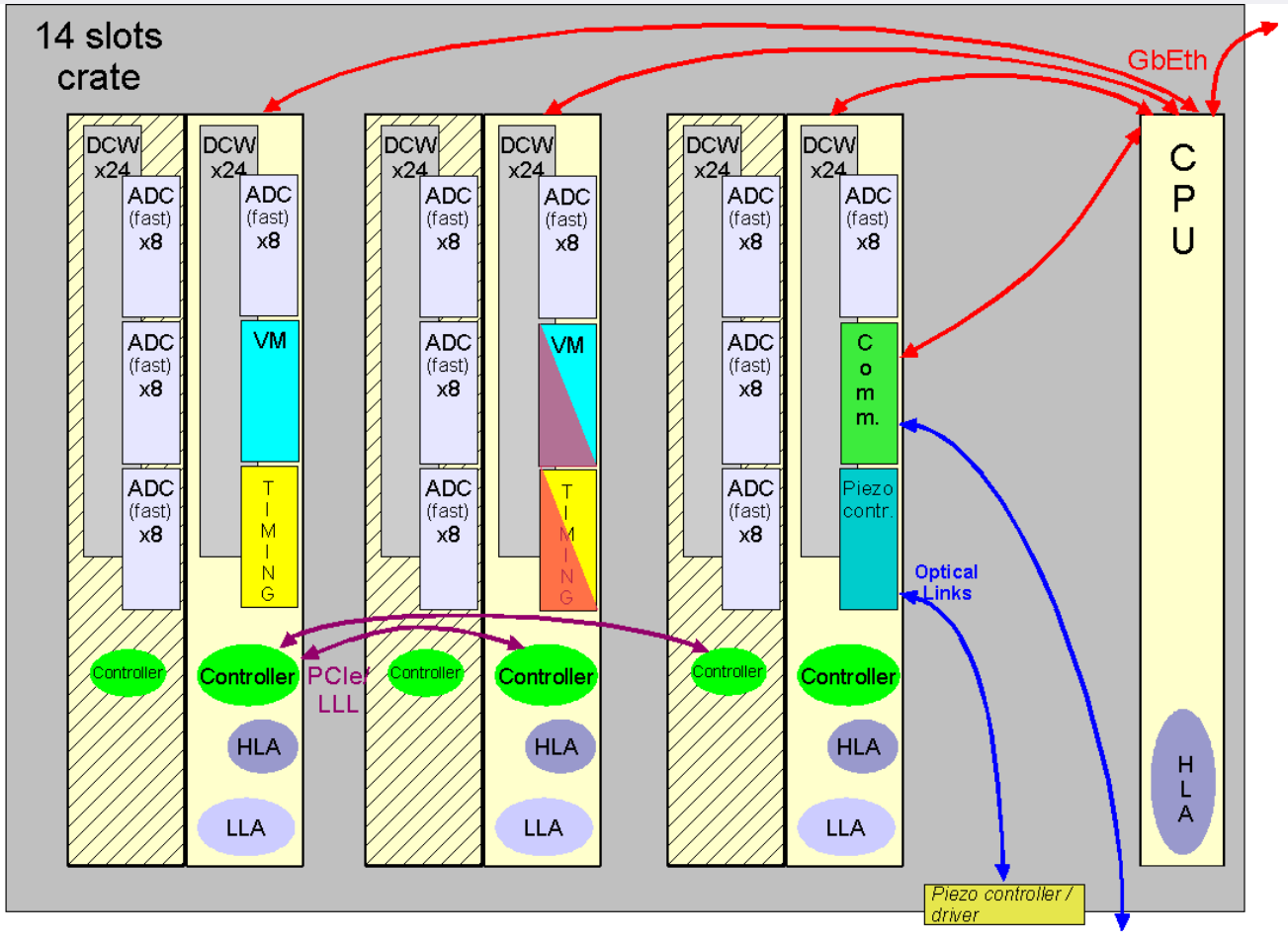
AMC Modules

- ADC
- VM
- Timing
- Communication
- Piezo-controller

RTM

- Downconverter

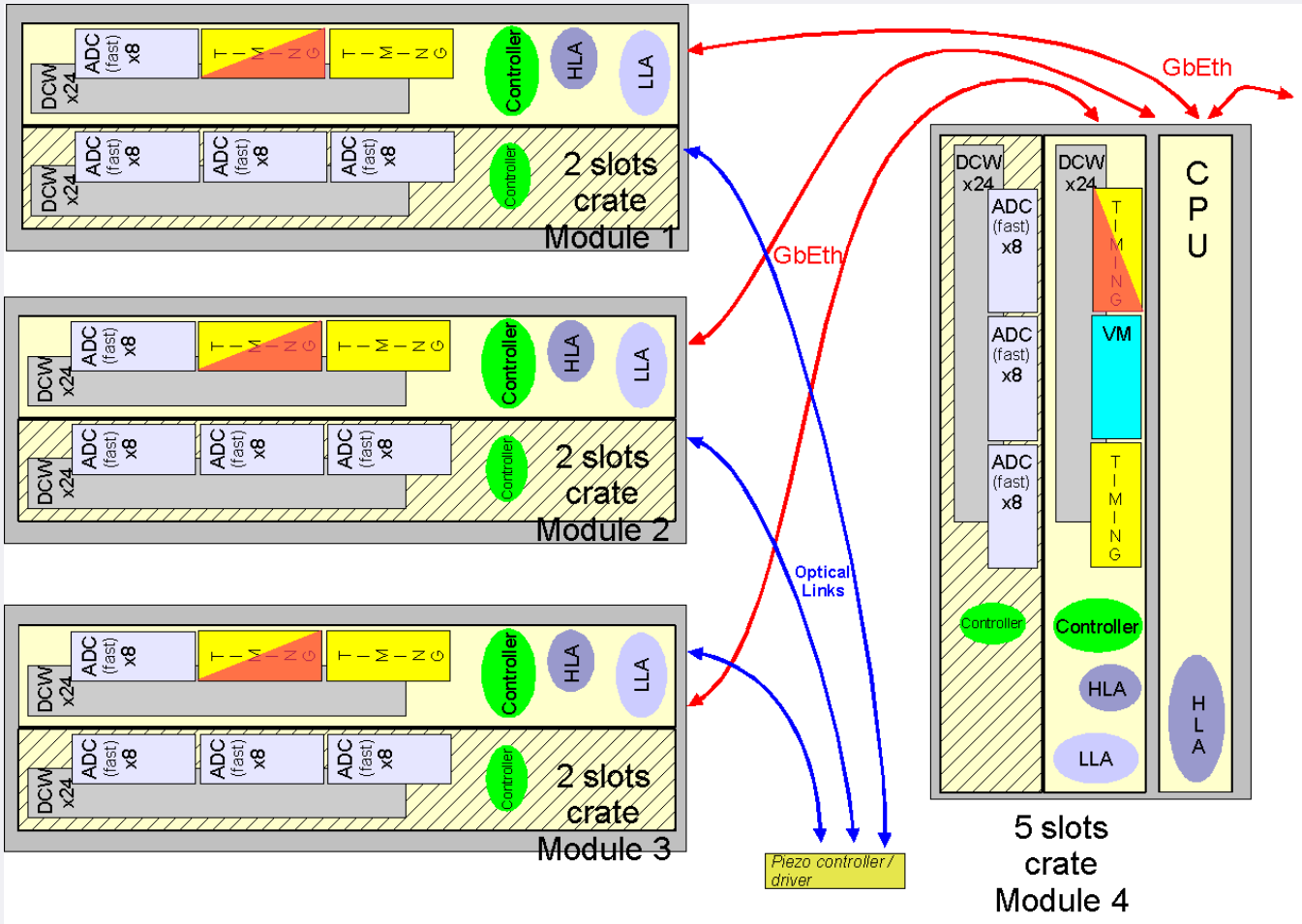
Centralized system for the LLRF



All boards are in the central 14 slot ATCA crate

Communication vi:
- PCIExpress
- GbEthernet

Distributed system for the LLRF



Electronics modules are distributed along Cryomodules and located in four ATCA crates

Communication vi:

- PCIExpress
- GbEthernet

Delays

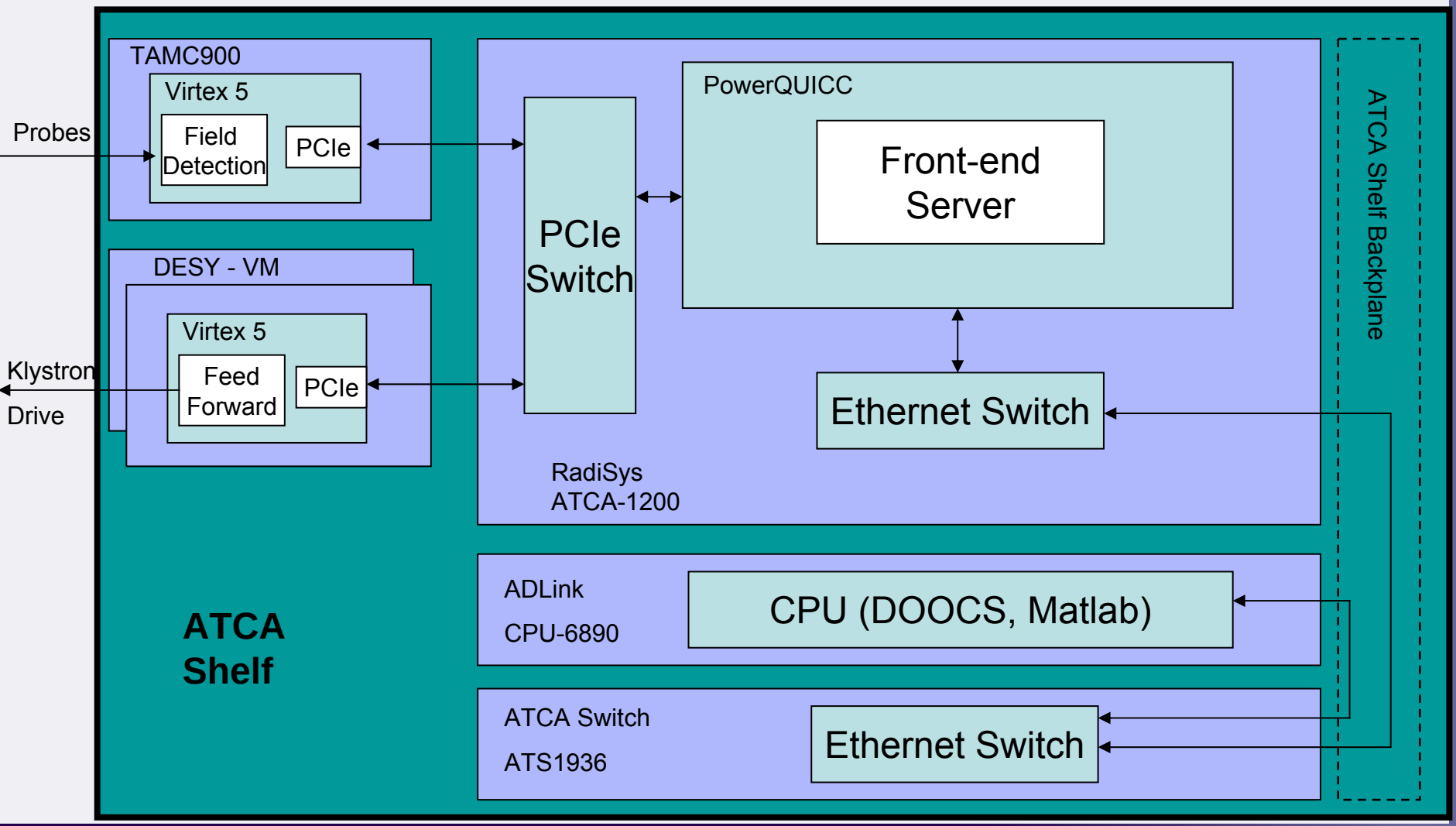
- Some delay was caused by difficulties to access documentation (data sheets, application notes for fast chips), it was necessarily to sign NDAs (Non Disclosure Agreement), no reference designs available

- ATCA Carrier Board - complicated design, 2/3 of team work remotely

- New halogen free materials caused problem with manufacturing of pcb boards (metallization of deep blind vias). For that reason two boards are delayed :
  - o AMC-Carrier Module
  - o Carrier Board

ATCA demonstration

ATCA Demonstration – Hardware & Software Architecture



ATCA Demonstration – AMC Modules

AMC Module
TEWS – TAMC900

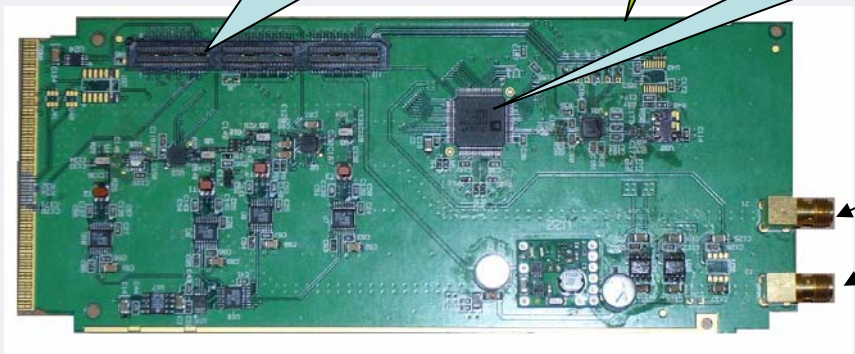
x8, 14-bit ADC,
Fs = 81MHz

FPGA Xilinx Virtex 5
Field detection
algorithms

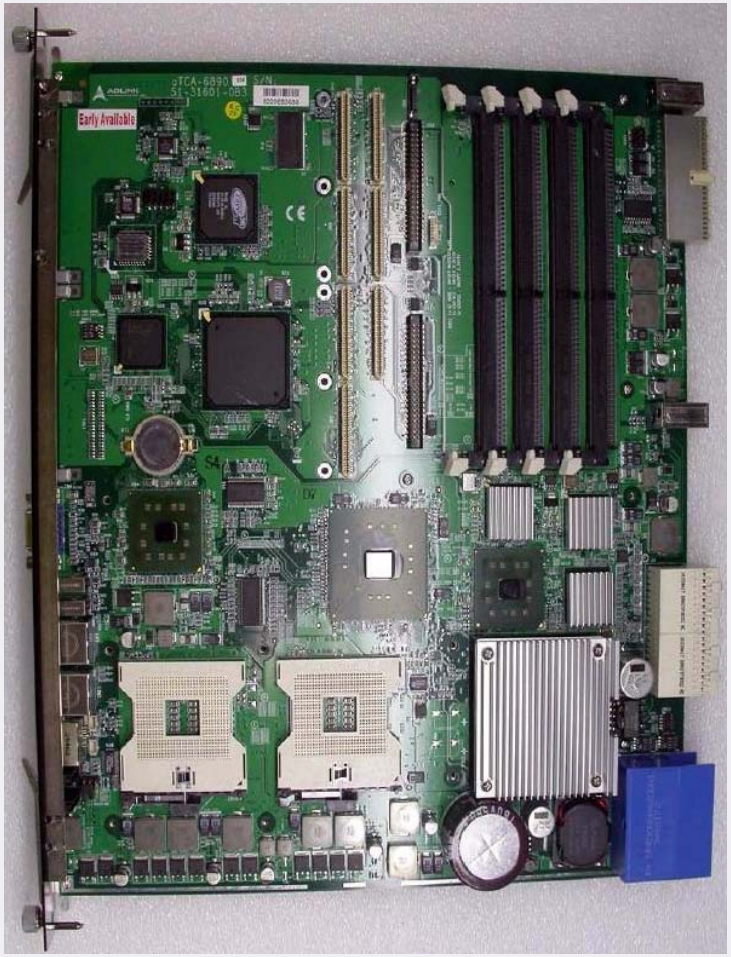
AMC Module
DESY - VM

Digital control,
DAC input,
Diagnostic ADC out

Dual DAC,
160MHz



ATCA Demonstration – used hardware (2)



ATCA CPU Blade
ADLink CPU-6890

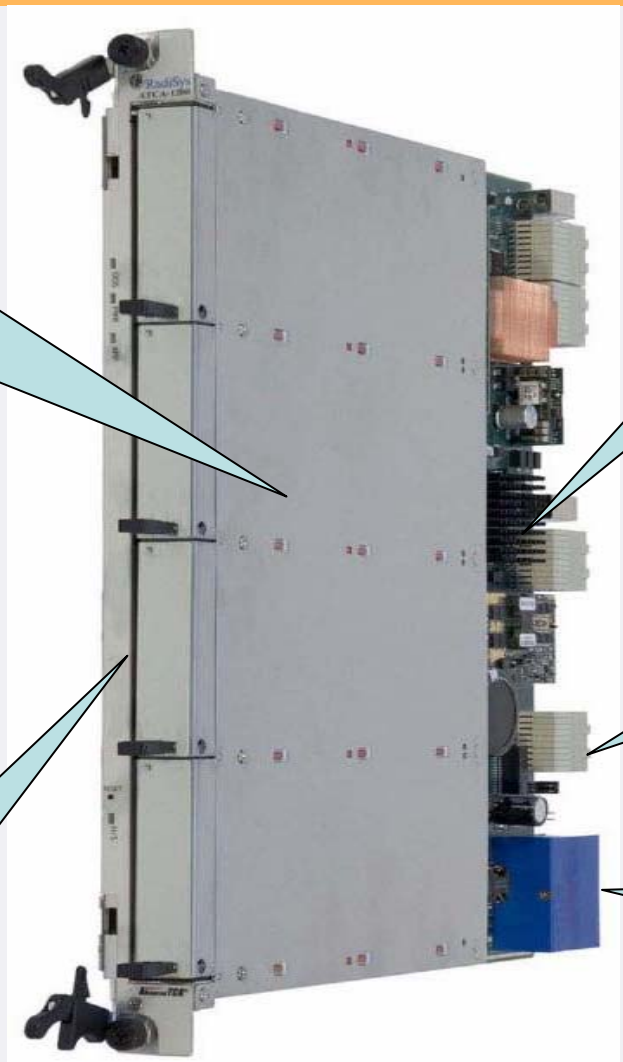
Includes:
- DESY Linux

-DOOCS server for communication and management of front-end servers on carrier blades

-client applications – DOOCS panels, Matlab

ATCA Demonstration – hardware & software architecture

ATCA Carrier Blade
RadiSys ATCA-1200



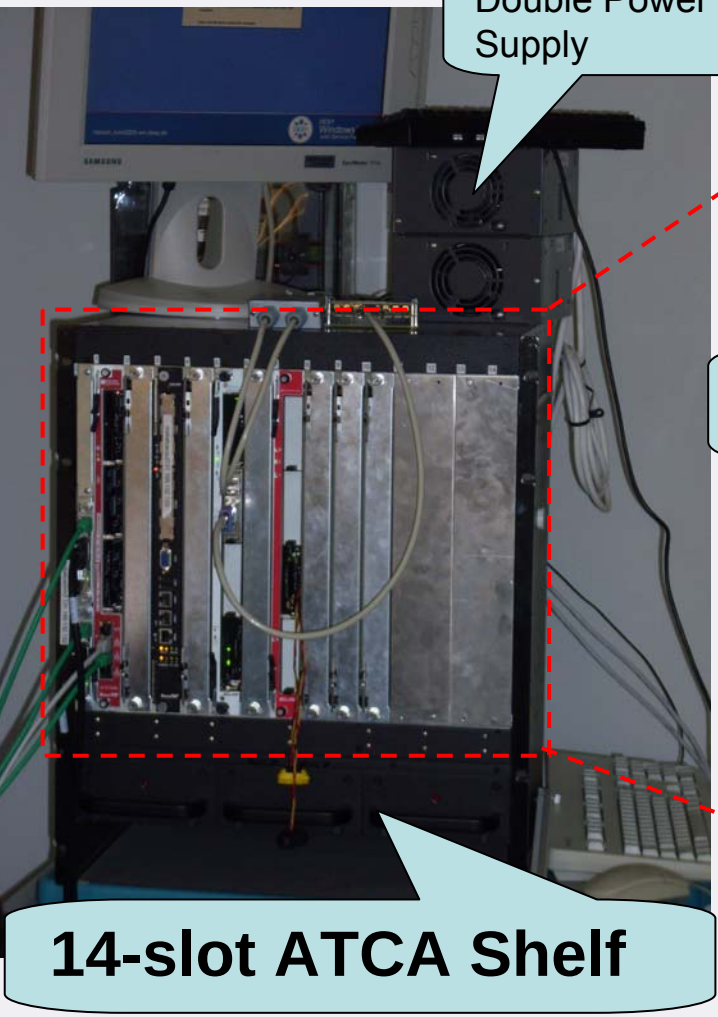
Processor PowerQUICC for front-end server

Ethernet links to shelf backplane

Power & IPMI connector

x4 AMC Bays

ATCA Demonstration – Laboratory Teststand

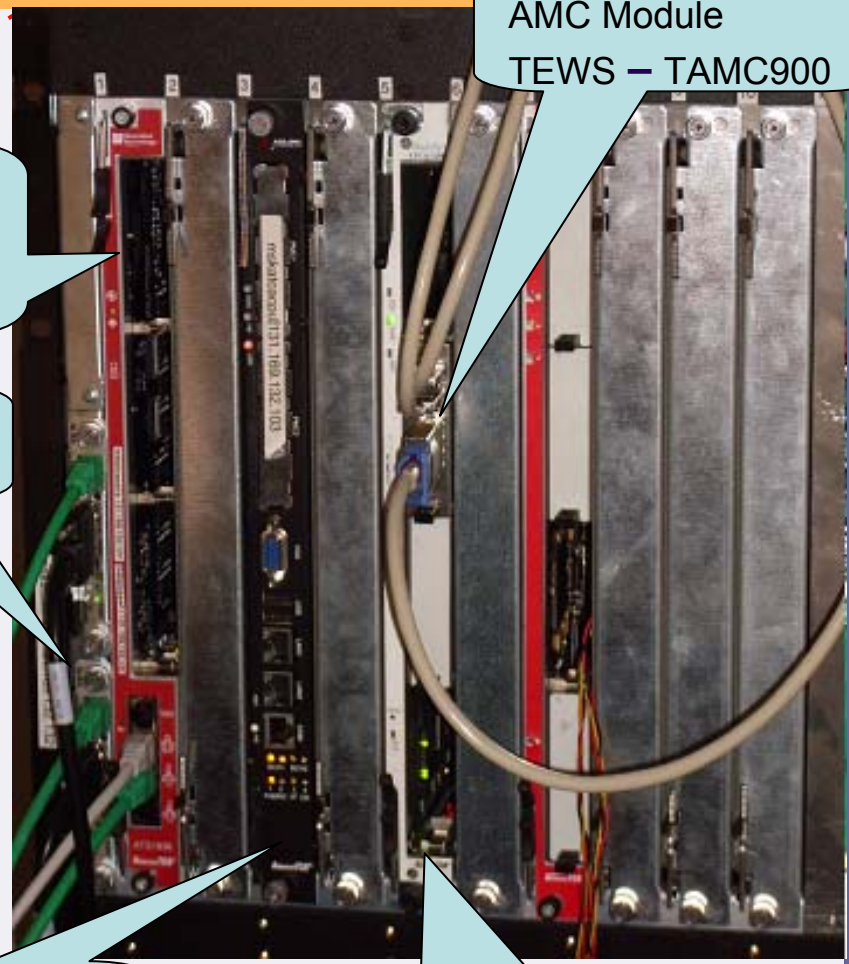


Double Power Supply

ATCA Ethernet Switch DTI-ATS1936

Redundant Shelf Manager

14-slot ATCA Shelf

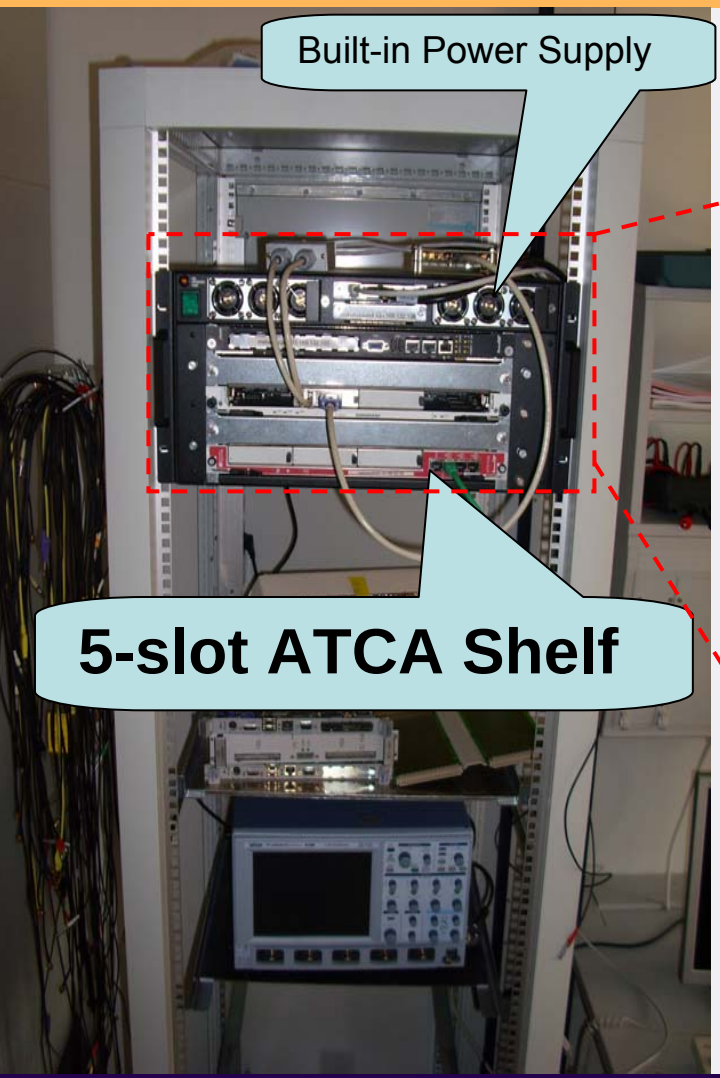


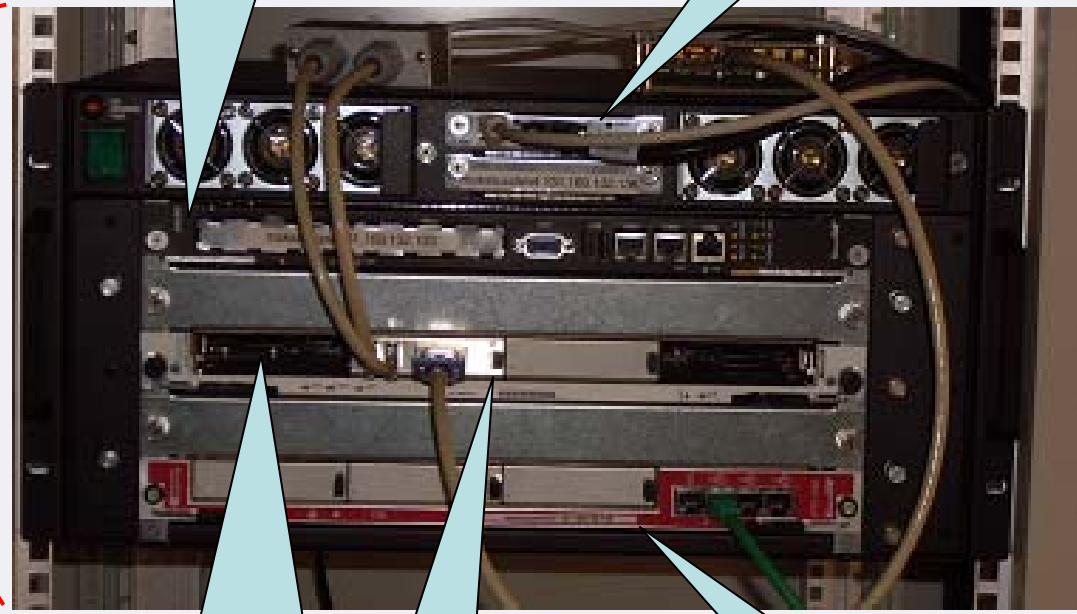
AMC Module TEWS – TAMC900

ATCA CPU Blade ADLink CPU-6890

ATCA Carrier Blade Radisys ATCA-1200

ATCA Demonstration –Teststand for ACC4/5/6





ATCA Demonstration – Software development

Done:

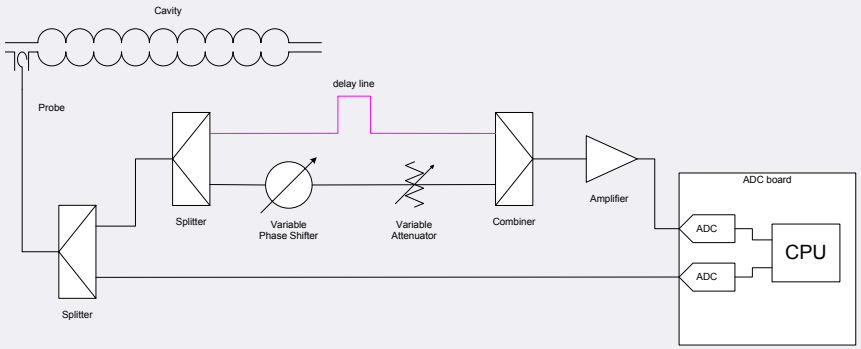
- **TAMC900 Firmware in VHDL**
  - readout of 8 ADCs on TAMC900 with external clock and trigger,
  - PCIe end-point for communication with
- **Radisys Carrier Blade ATCA -1200 Software**
  - Linux ported on PowerQUICC with cross-compiler for custom applications
  - front-end server:
    - communication and management of AMC modules through PCIe
    - communication with client applications through Ethernet on the shelf backplane
    - ring buffers for ADC readout
- **ADLink CPU-6890 Software**
  - universal DOOCS server for readout of hardware registers
  - MEX functions in Matlab for direct communication with hardware

ATCA Demonstration – Status

- Tests in laboratory
  - Hardware setup tested in laboratory with ATCA-1200, TAMC900, CPU-6890
  - Test of readout of ADC through ATCA-1200 to DOOCS server in CPU-6890
  - Initial tests of AMC-VM module – only analog part
- Installation of hardware in Extension Hall for ACC4/5/6 – in progress
- Difficulties
  - problems with PCIe express communication on RadiSys ATCA-1200 – solved by the manufacturer
  - problems with porting Linux on ATCA-1200 – no good support from RadiSys
  - problems with production of DESY AMC module for AMC-VM – still not produced

XFEL LLRF Development
Transient Detection

Transient Detection System (ver. 1)

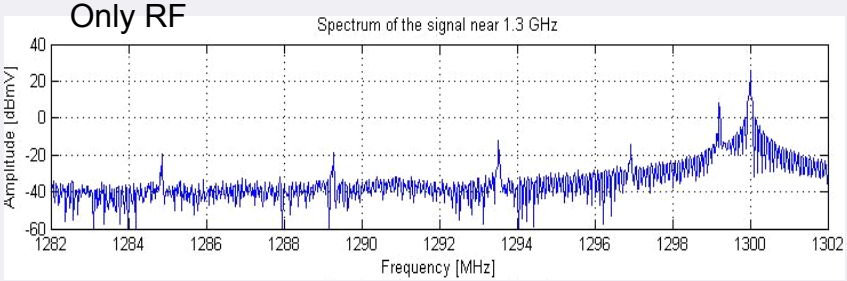


Delay line 20 ns (cable)

Main difficulties

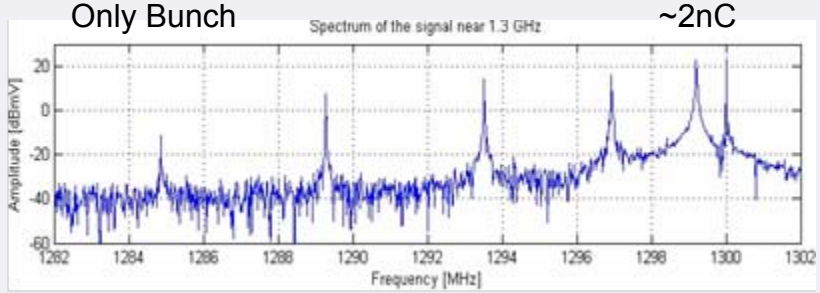
- Manual adjustment of the transient detection system
  - very sensitive
- Other modes of a cavity (8/9 π, …)
  - not possible to filtering during 20 ns
- Reduce the price from ~40.000€ to acceptable

Only RF



$$A_{\pi} - A_{8/9\pi} = 20dBmV$$

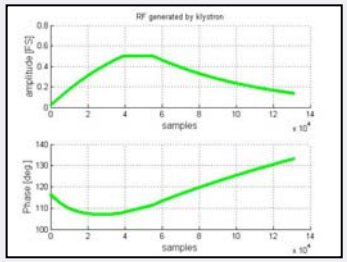
Only Bunch ~2nC

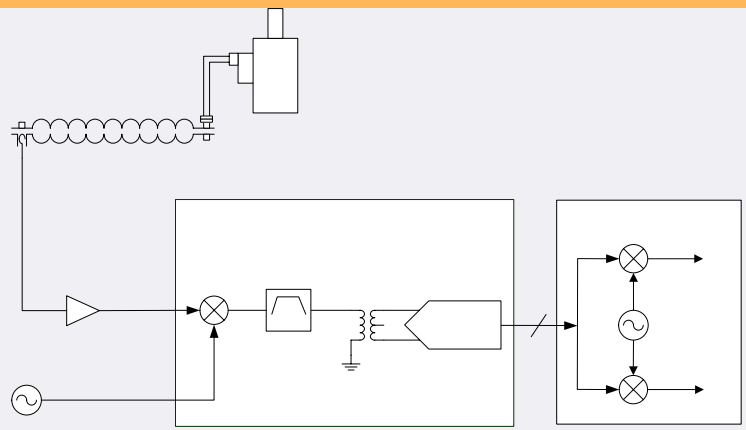


$$A_{\pi} - A_{8/9\pi} = 10dBmV$$

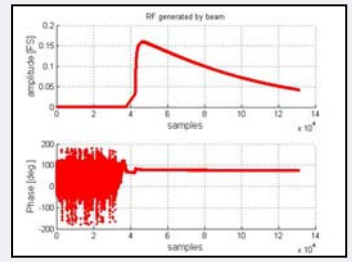
Transient Detection System (ver. 2)

RF - on
Beam - off

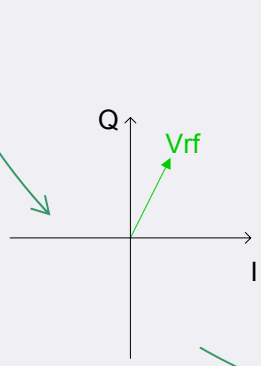


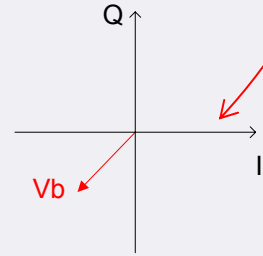


RF - off
Beam - on

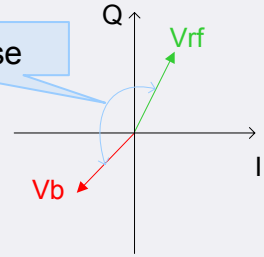


In both cases MO as reference



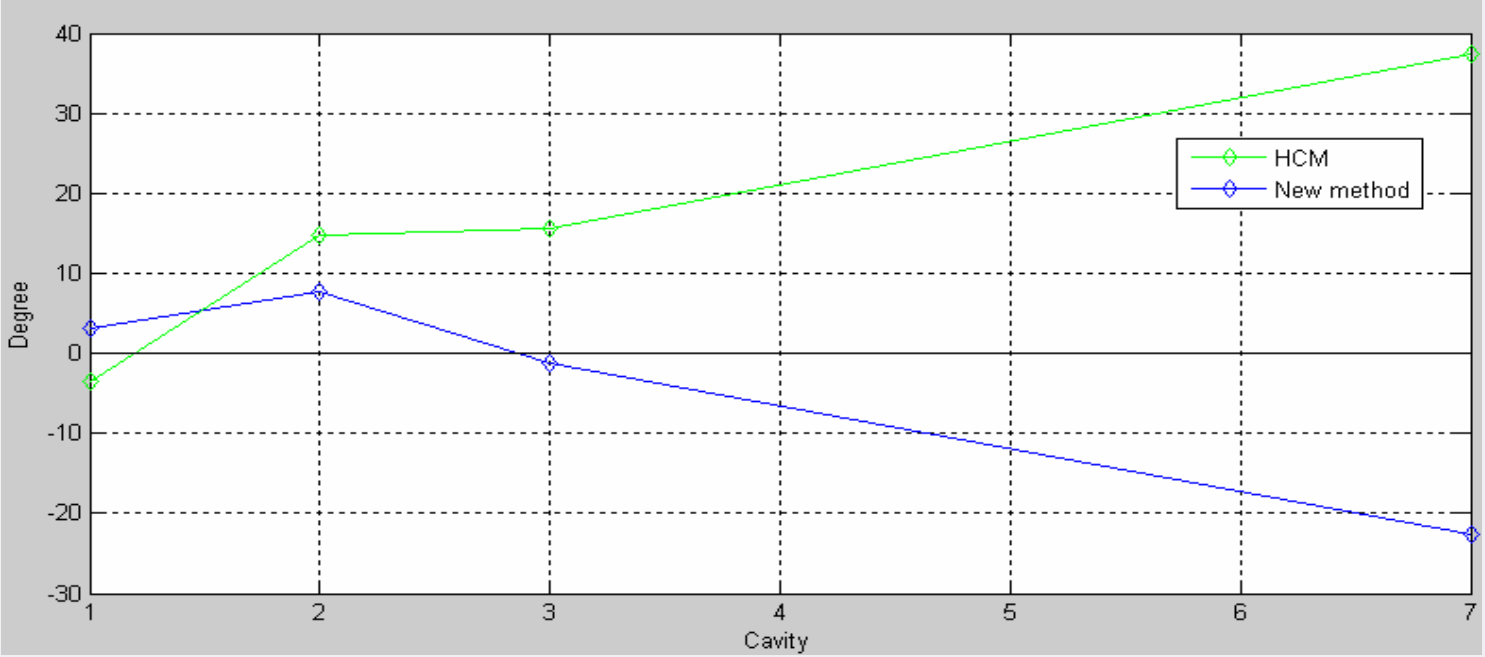


Beam phase



Measured phase comparison

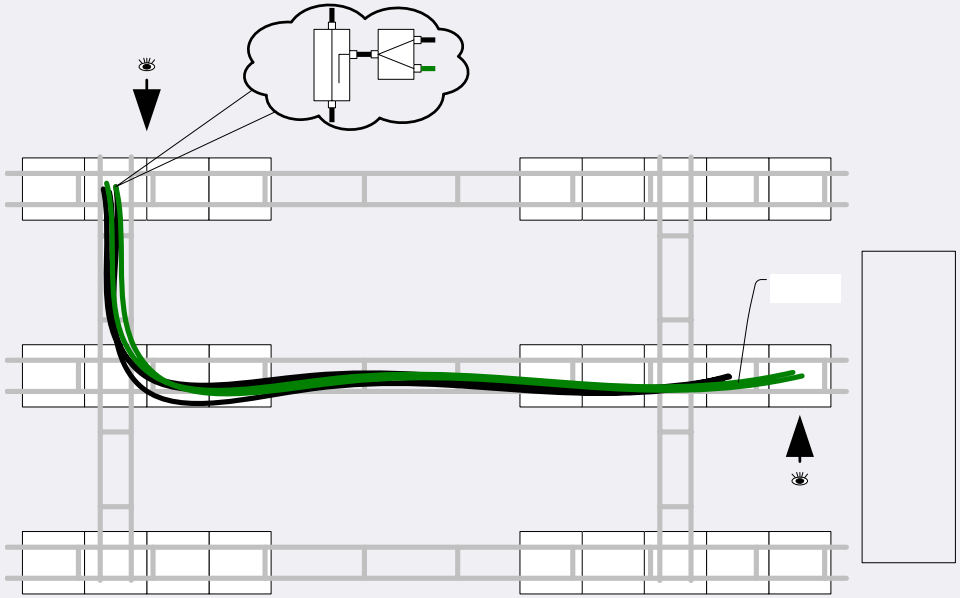
New:	-3.57	14.80	15.52	37.49
HCM:	3.16	7.72	-1.33	-22.57

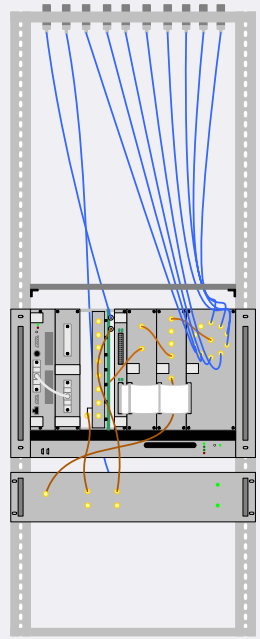


HCM – High Charge Measurement

New – Transient Detection System ver. 2

Measurement setup for ACC4 (future plan)



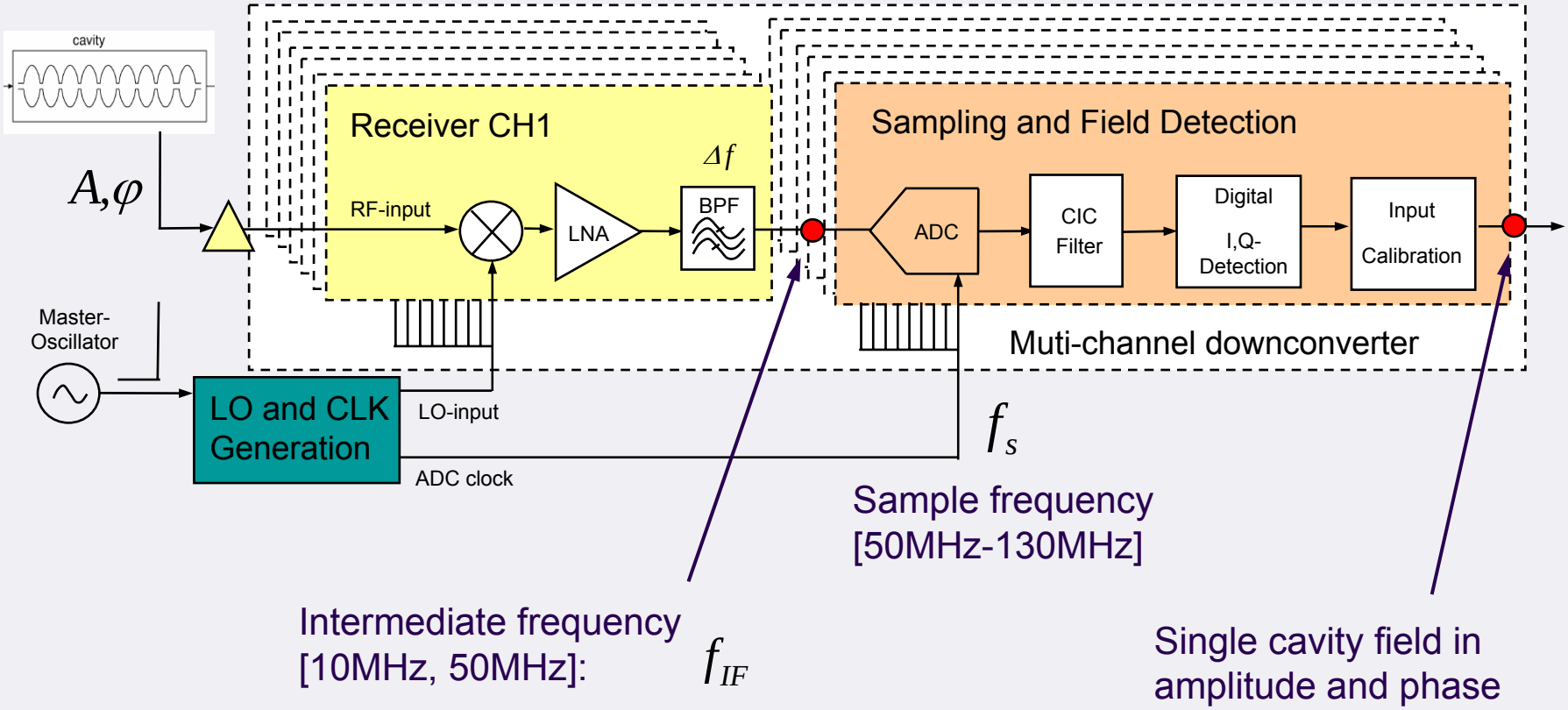


- Confirm the ACC1 results at ACC4
- RF leakage from Gun eliminated
- Bunch energy at ACC4 (450MeV) to compare with at ACC1 (5MeV)

XFEL LLRF Development
Downconverters

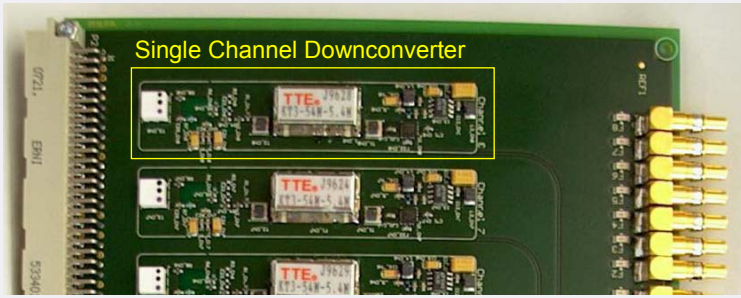
Downconverter for LLRF

- Non-IQ-sampling scheme :



Achieved Performance at FLASH

- Multi-channel downconverter :



8 channel Gilber-mixer receiver VME based
+ SIMCON DSP (14-bit ADCs) VME based

- Stability results (single channel) :

Short-term, bunch-to-bunch (800us) :

$$\Delta A / A_{rms} = 0.015\%, \quad \Delta\varphi_{rms} = 0.0092\ deg$$

Mid-term, pulse-to-pulse (10min) :

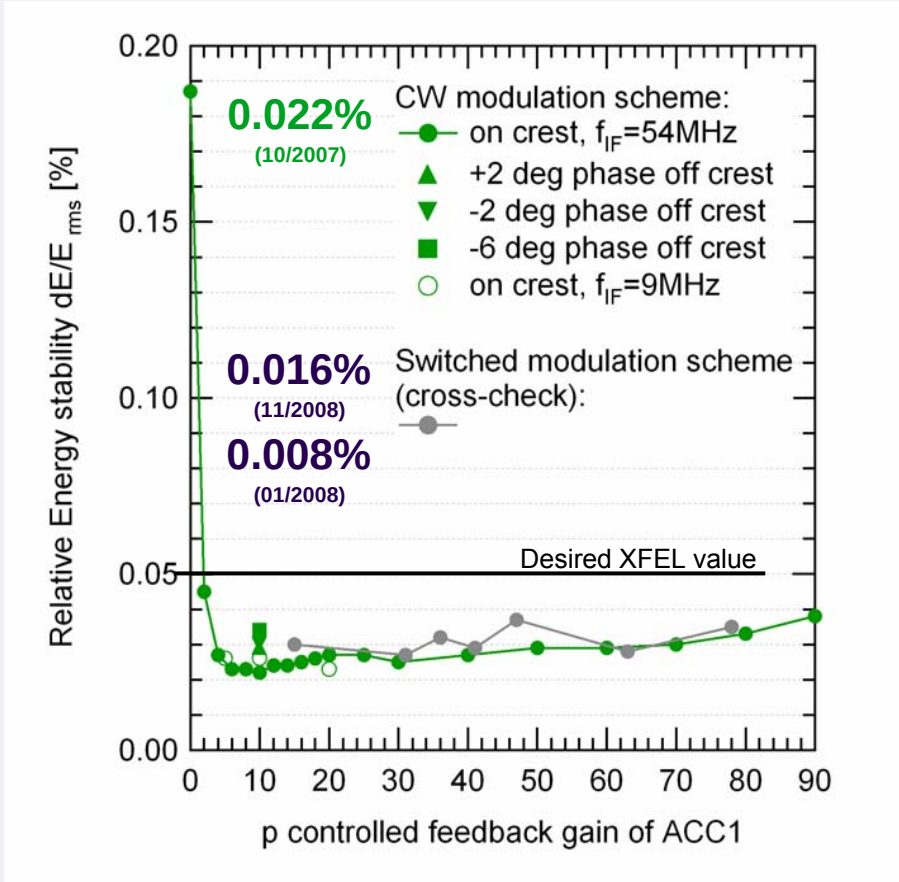
$$\Delta A / A_{rms} = 0.016\%, \quad \Delta\varphi_{rms} = 0.0147\ deg$$

Long-term, drifts (1hour) :

$$\Delta A / A_{pkpk} = 0.09\%, \quad \Delta\varphi_{pkpk} = 0.05\ deg$$

θ_A = 2e-3/°C, θ_P = 0.2°/°C

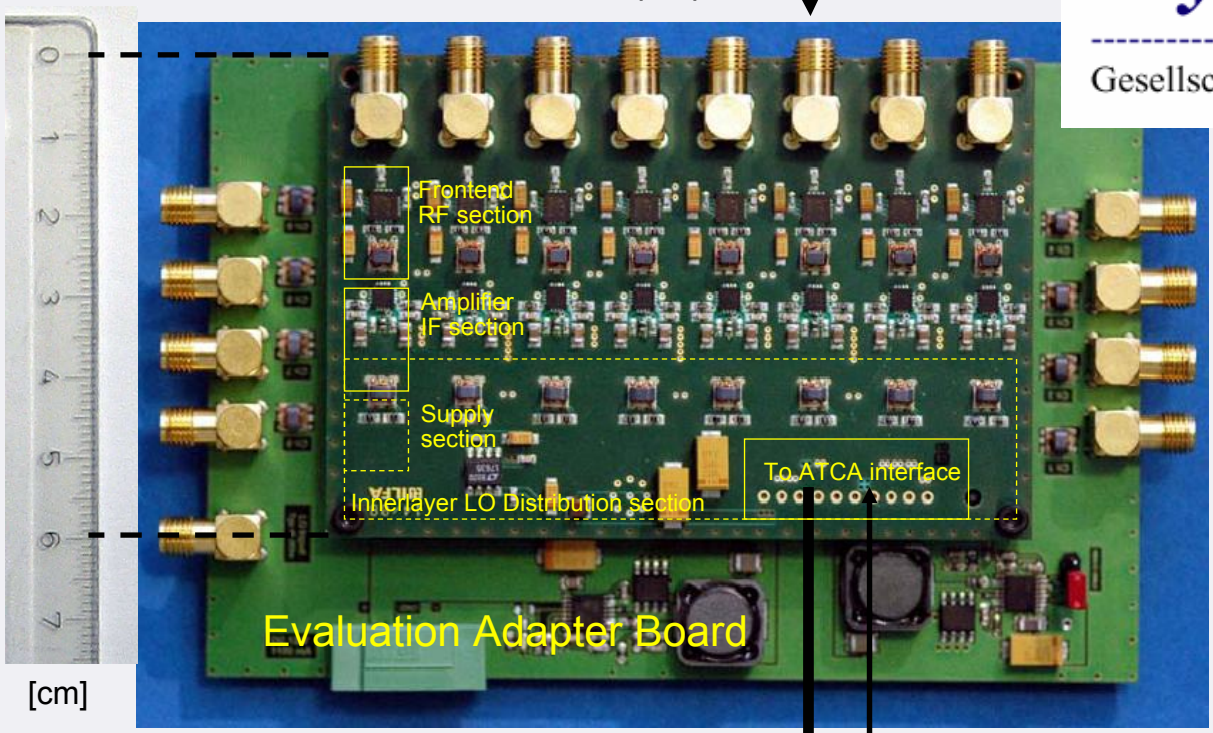
- Pulse-to-Pulse Beam Stability :



RTM Downconverter for the ATCA System

- Very compact **R**ear **T**ransition **M**odule (RTM) :

RF inputs (8 channels):
1300MHz, +0dBm input power



IF Outputs (8 channels):
[10MHz,60MHz]

LO input:
[1310MHz, 1350MHz]

Cryoelectra

Gesellschaft für kryoelektrische Produkte mbH

Receiver Type : LT5527 (Gilbert-Mixer)
RF: 1300MHz , <10dBm
LO: [1310MHz, 1350MHz], 10dBm

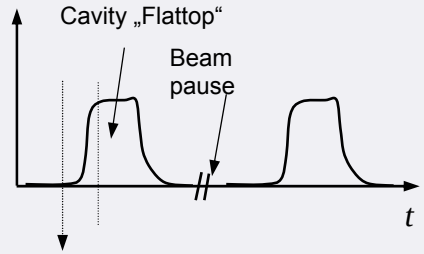
CHARACTERISTICS	RATING
IF Frequency, MHz	1 - 50
Conversion Loss, dB	-2 (typ)
Noise Figure (incl. the accessory card), dB	18 (typ)
IF Spurious Signals, dBc	<-60
IF Filter cut-off, MHz	60
IF Harmonic Distortion (IF < 15 MHz, RF input power < 0 dBm), %	1
IF Harmonic Distortion (IF > 30 MHz, RF input power < 9 dBm), %	0.25
Inter-Channel Crosstalk, dB	>65

Pulse-to-Pulse and Drift Calibration schemes

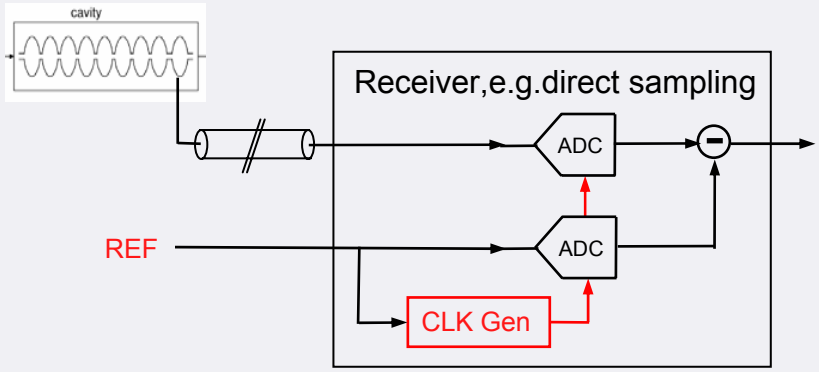
Is needed to eliminate pulse-to-pulse fluctuations and drifts from

- Cavity pickup cables (4 module) $5\ fs\ m^{-1}K^{-1}, \pm 125fs\ K^{-1}\ (\pm 25m), \Delta T \approx 1K$
- Downconverter (mixer) θ_A = 2e-3/°C, θ_P = 0.2°/°C
- LO generation (dividers, amplifiers, filters) (Injector)
- ADC CLK generation (timing system, less critical)

to have a robust machine operation.

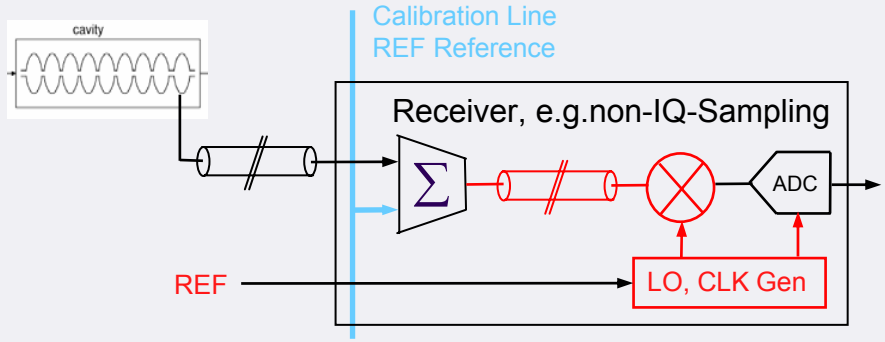


1) Tracking the reference :



+ Demonstrated, e.g. with direct sampling

2) Injection of the reference signal :

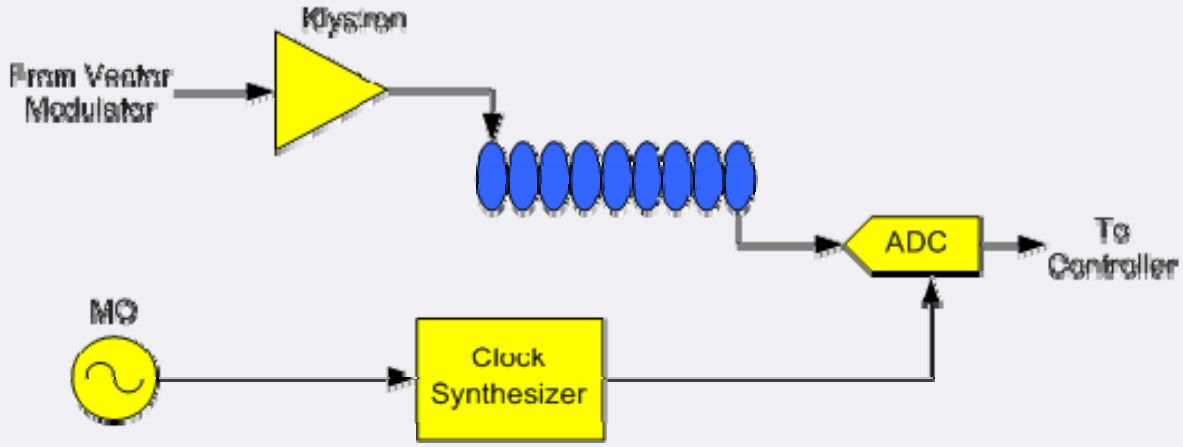


3) Reflection at the cavity :

+ Compensates in addition antenna to cavity pickup

XFEL LLRF Development
Direct Sampling

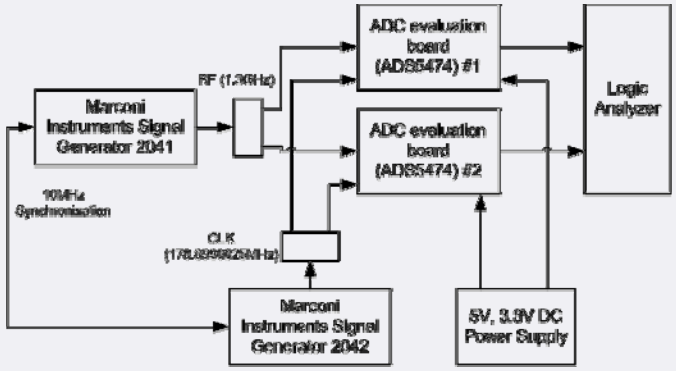
Direct Sampling RF Signal Receiver

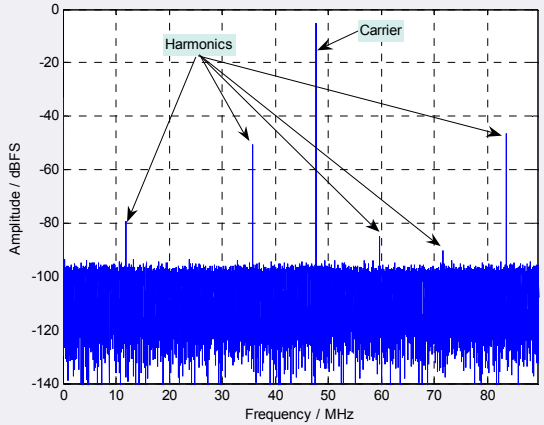


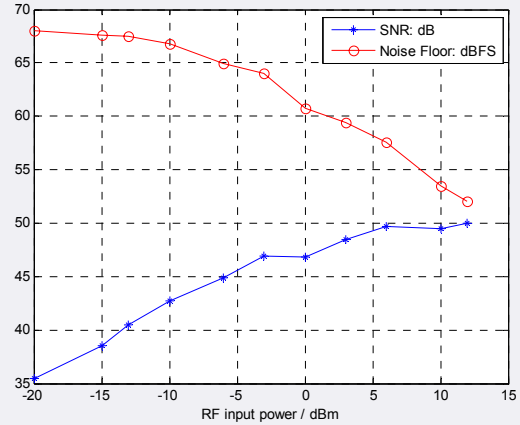
- Sample the 1.3GHz signal directly with ADC without down converter
- Need precise clock signal, time jitter < 300 ps RMS

- ADS5474, 14-bit, 1.4GHz bandwidth, 400 MSPS

Direct Sampling ADC Evaluation at Lab







With full Nyquist bandwidth (89.45 MHz)

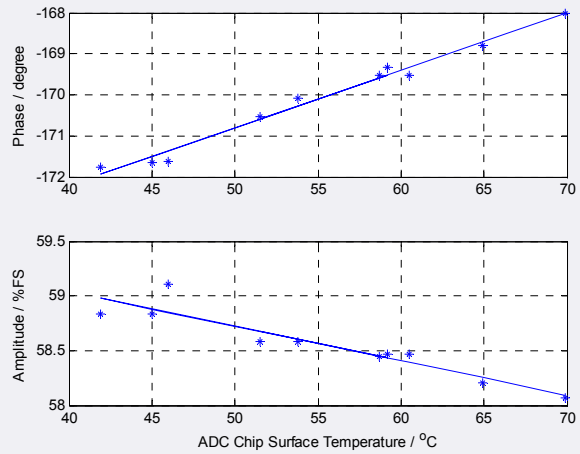
SNR	: 50.5 dB
Phase jitter	: ~0.2 degree RMS
Amplitude jitter	: ~0.2% RMS

With closed loop bandwidth of 50 kHz (TESLA typed cavity with feedback gain of about 250), we expect

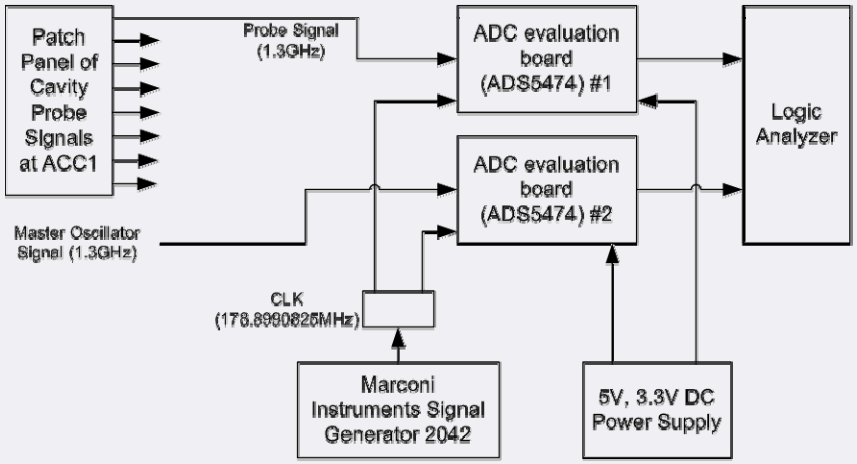
SNR	: 83 dB
Phase jitter	: ~0.01 degree RMS
Amplitude jitter	: ~0.01% RMS

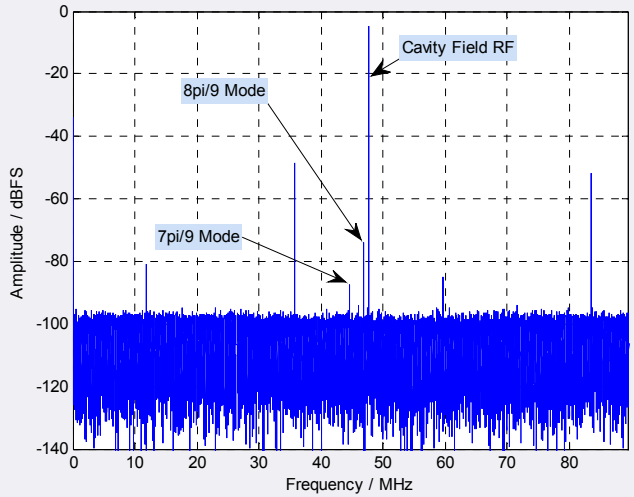
Temperature Coefficients:

Phase Sensitivity	: 0.14°/°C
Amplitude Sensitivity	: -0.03 %FS/°C



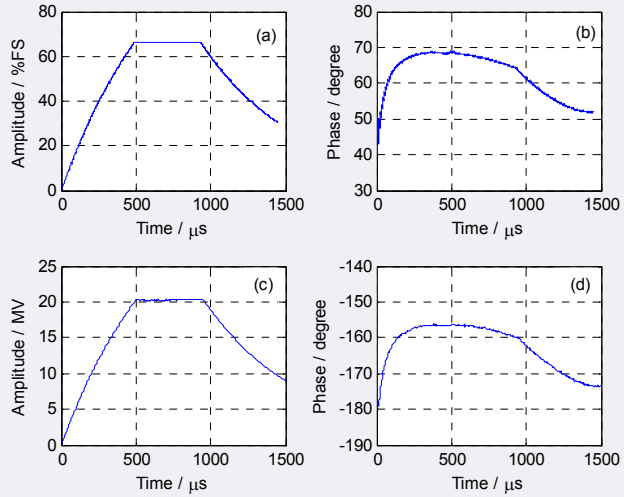
Direct Sampling ADC Evaluation at FLASH





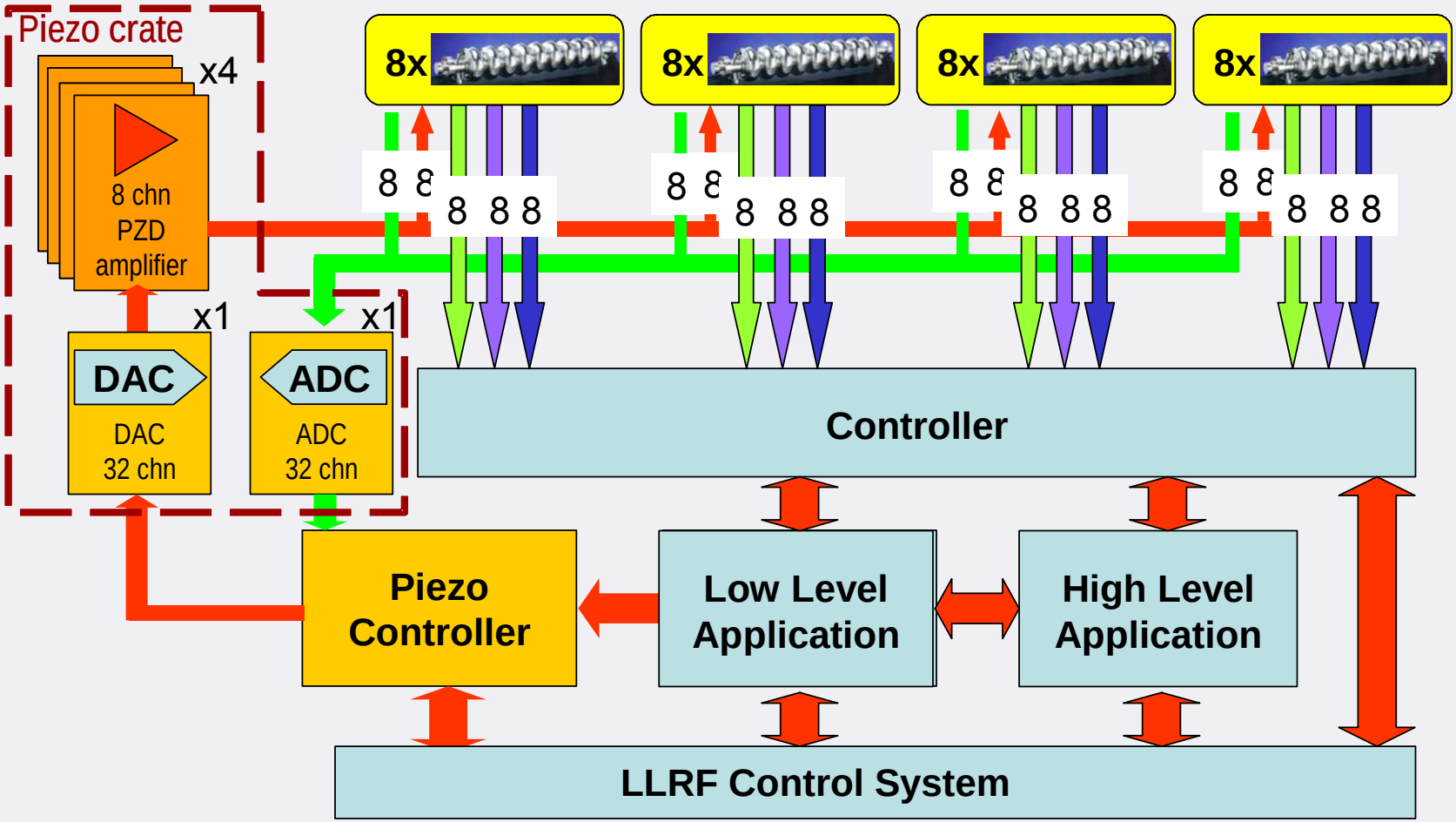
Measurements by direct sampling ADC shown in (a),(b)
- Phase jitter : 0.05 degree RMS (10 MHz bandwidth)
- Amplitude jitter : 0.054% RMS (10 MHz bandwidth)

Measurements by monitor ADC with 250 kHz IF shown in (c),(d)
- Phase jitter : 0.09 degree RMS (500 kHz bandwidth)
- Amplitude jitter : 0.078% RMS (500 kHz bandwidth)

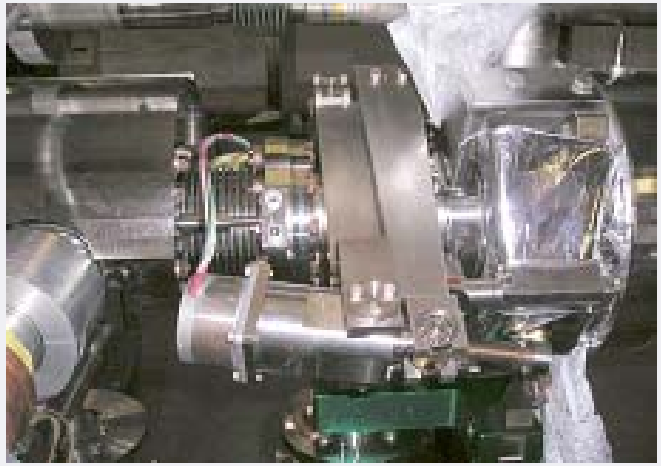


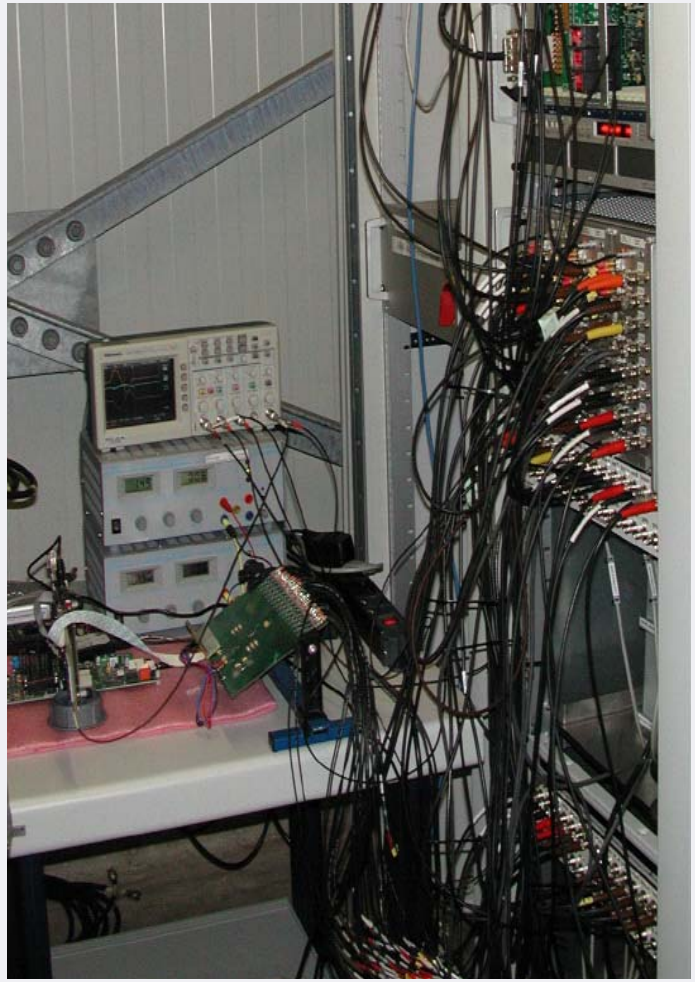
XFEL LLRF Development
Piezo Control

Placement of the piezo control in LLRF system



Piezo control components



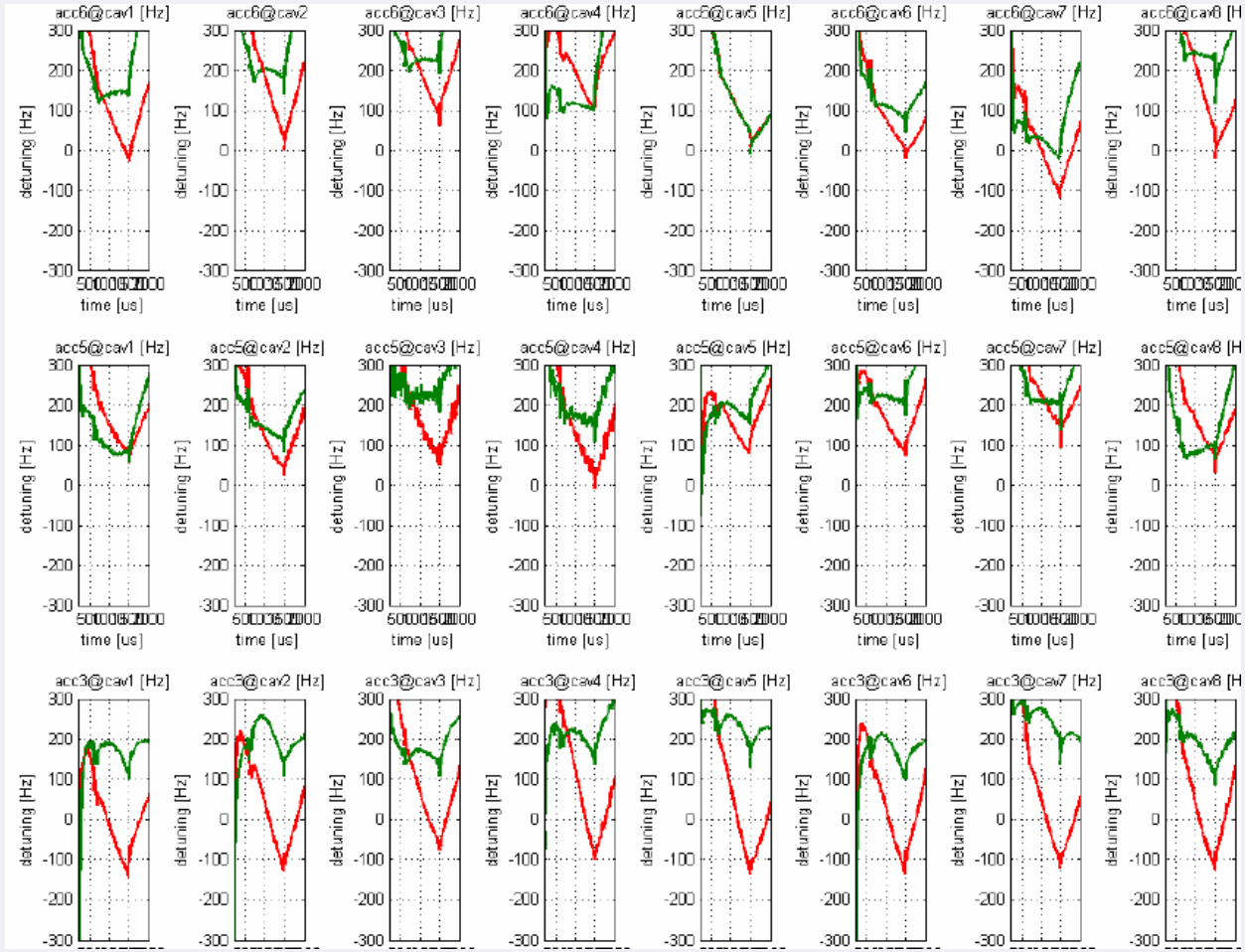


cavity	piezo	model	ACC3/M7	model	ACC5/M5	model	ACC6/M6
1	1	PI	4,93uF	Noliac	2,1uF	PI	4,13uF
	2	-	Unavailable	-	Unavailable	PI	4,45uF
2	1	PI	4,61uF	Noliac	2,22uF	PI	4,4uF
	2	-	Unavailable	-	Unavailable	PI	4,2uF
3	1	PI	4,91uF	Noliac	2,28uF	PI	4,21uF
	2	-	Unavailable	-	Unavailable	PI	4,1uF
4	1	PI	4,6uF	Noliac	3,12uF	PI	3,86uF
	2	-	Unavailable	-	Unavailable	PI	4,2uF
5	1	Noliac	2,6uF	Noliac	2,2uF	PI	4,22uF
	2	-	Unavailable	-	Unavailable	PI	4,28uF
6	1	Noliac	2,13uF	Noliac	2,13uF	PI	3,73uF
	2	-	Unavailable	-	Unavailable	PI	4,41uF
7	1	Noliac	2,22uF	Noliac	2,19uF	PI	4,69uF
	2	-	Unavailable	-	Unavailable	PI	4,41uF
8	1	Noliac	2,21uF	Noliac	2,17uF	PI	4,31uF
	2	-	Unavailable	-	Unavailable	PI	4,2uF

Automatic LF detuning of 3 ACC modules

The prototype piezo control system was designed, manufactured and tested (32 channel DAC board, piezo driver board – the 32 channels ADC board is under development).

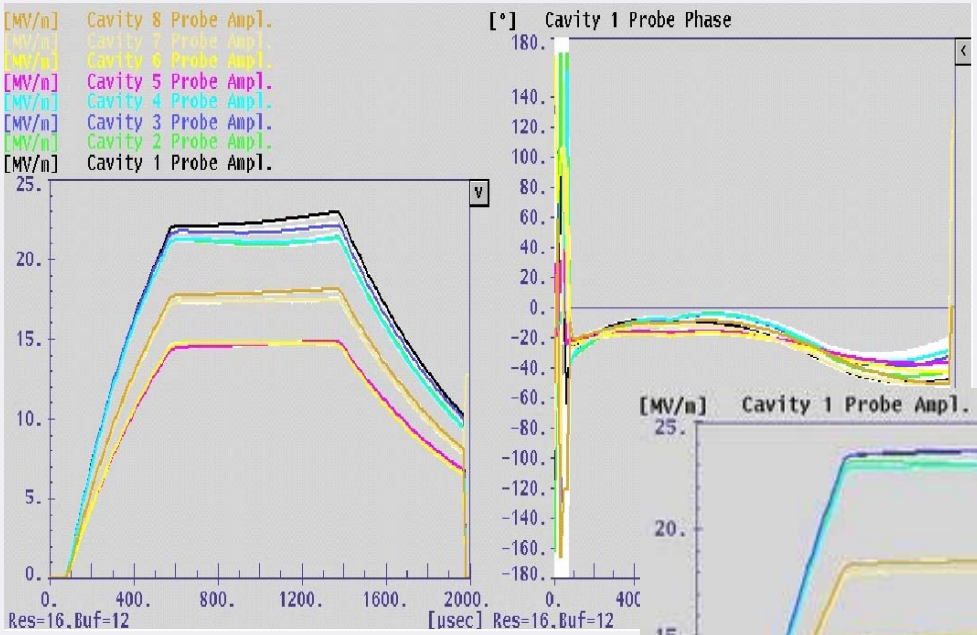
The adaptive detuning compensation algorithm was implemented and tested.



Red – before compensation

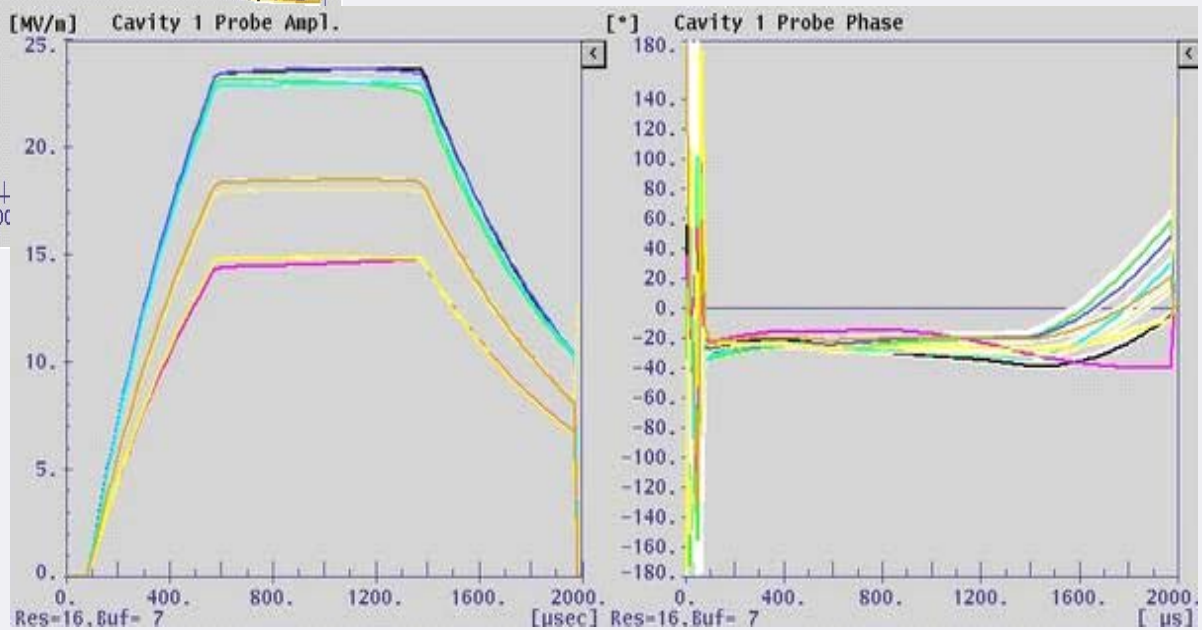
Green – after automatic LF compensation

ACC6 - Field in the cavities before and after compensation



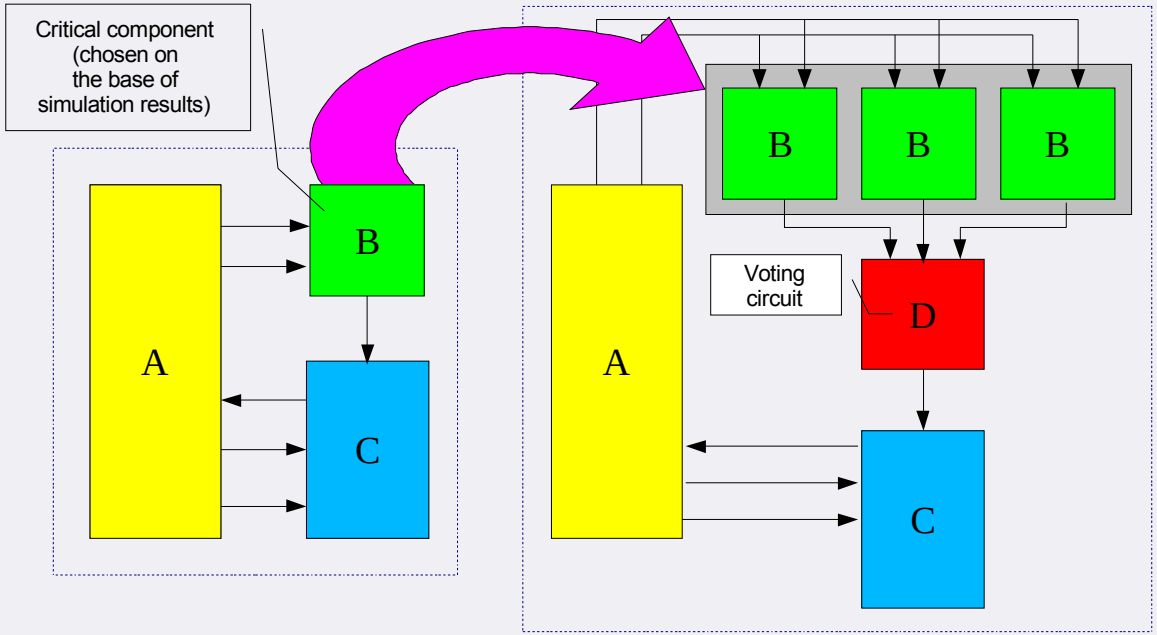
before

after



XFEL LLRF Development
SEU Immunity

Automatic generation of Tripple Module Redundancy for SEU tolerance



Resource	used	out of	percent
Slices	5288	13696	38
Slice Flip Flops	5366	27392	19
4 input LUTs	8307	27392	30
BRAMs	84	136	61
MULT18X18s	45	136	33

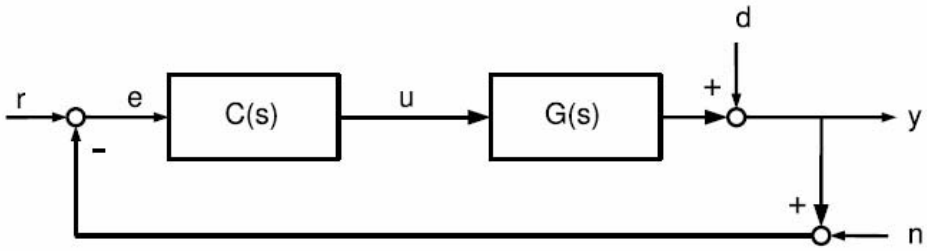
TMR

Resource	used	out of	percent
Slices	10410	13696	76
Slice Flip Flops	10148	27392	37
4 input LUTs	18520	27392	67
BRAMs	92	136	67
MULT18X18s	135	136	99

TMR was applied only to computational path
(it would be not possible to apply it to the whole circuit due to resource limitation)

XFEL LLRF Development
MIMO Controller

Controller design objectives

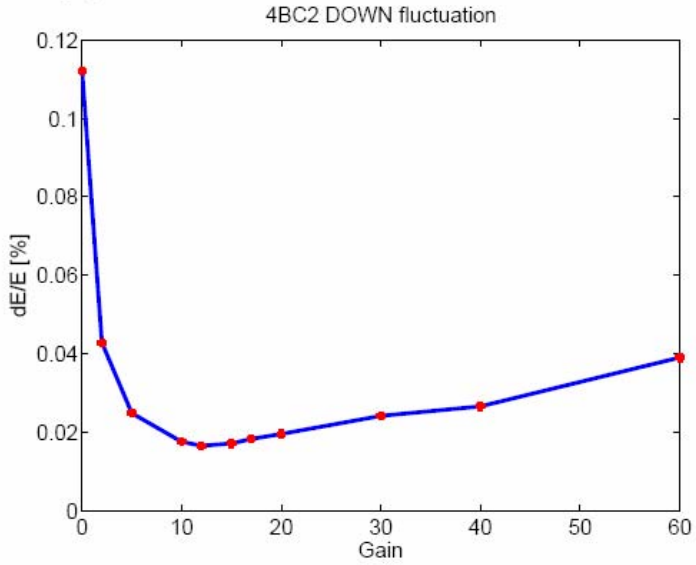


$$y = \underbrace{(I + G\,C)^{-1}\,G\,C}_{T(s)}\,(r - n) + \underbrace{(I + G\,C)^{-1}}_{S(s)}\,d \quad , \quad S + T = I$$

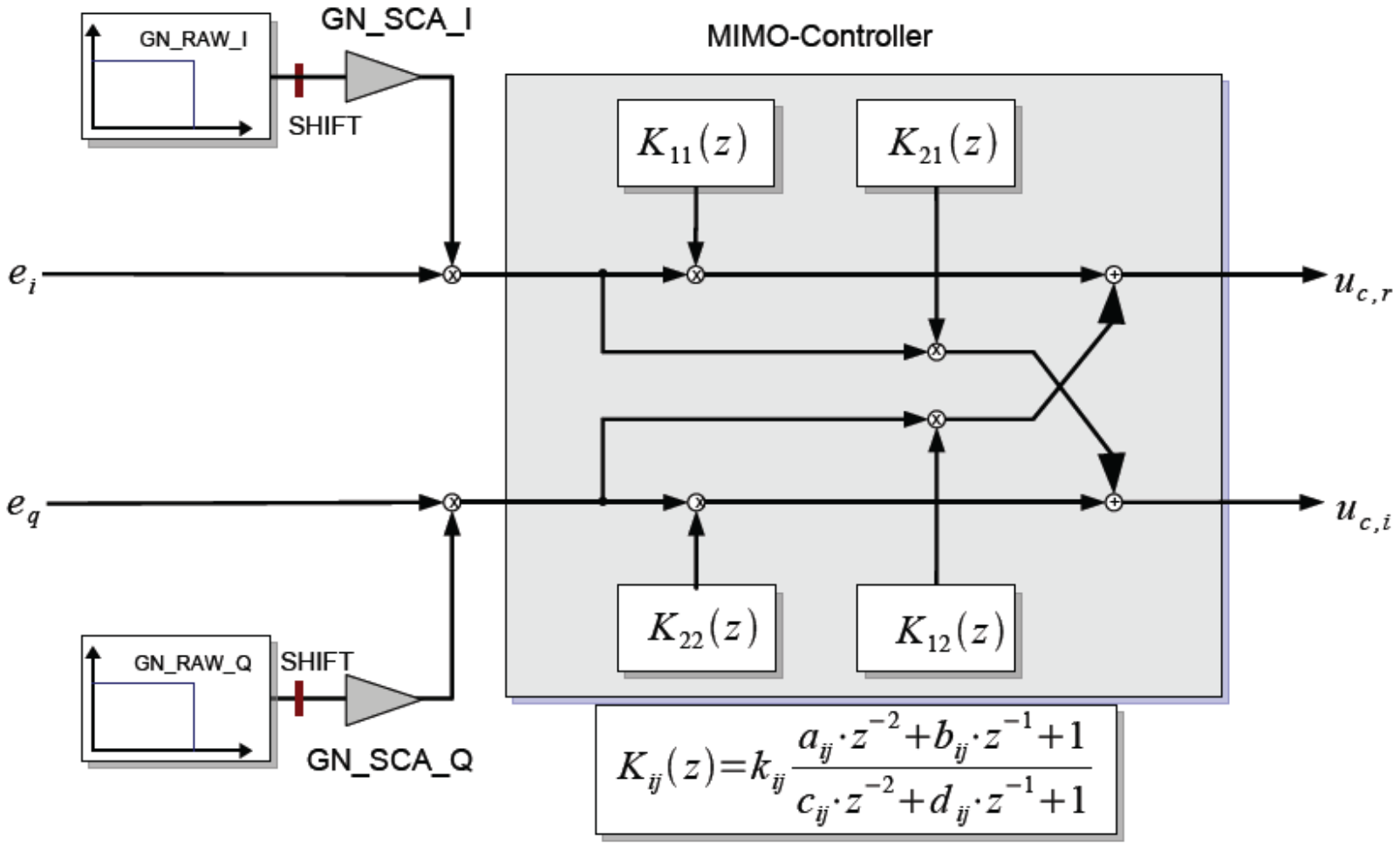
$$\begin{aligned} y &= T\,(r - n) + S\,d \\ e &= S\,(r - n - d) \end{aligned}$$

- Perfect tracking $T = 1\,,\ S = 0$
- Noise rejection $T = 0\,,\ S = 1$

↷ conflicting design objectives

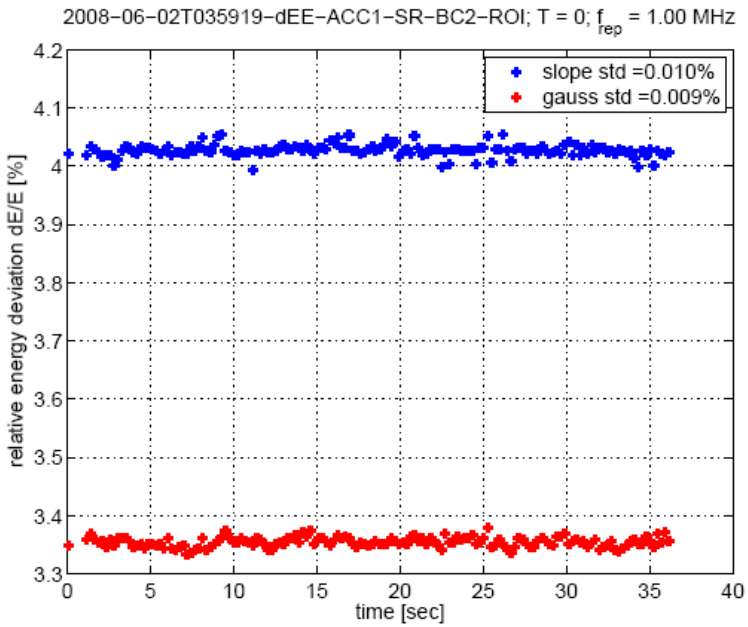


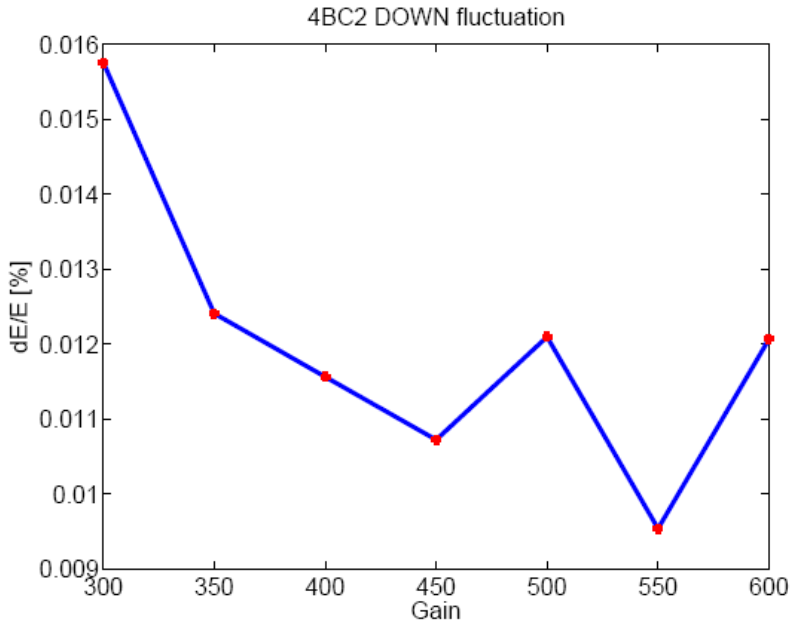
MIMO-Controller structure



Measurement results

- beam energy stability measurements done with synchrotron radiation camera (4BC2-Down)
- gain values are scaled proportional gains
- best achieved beam stability with MIMO-Controller so far





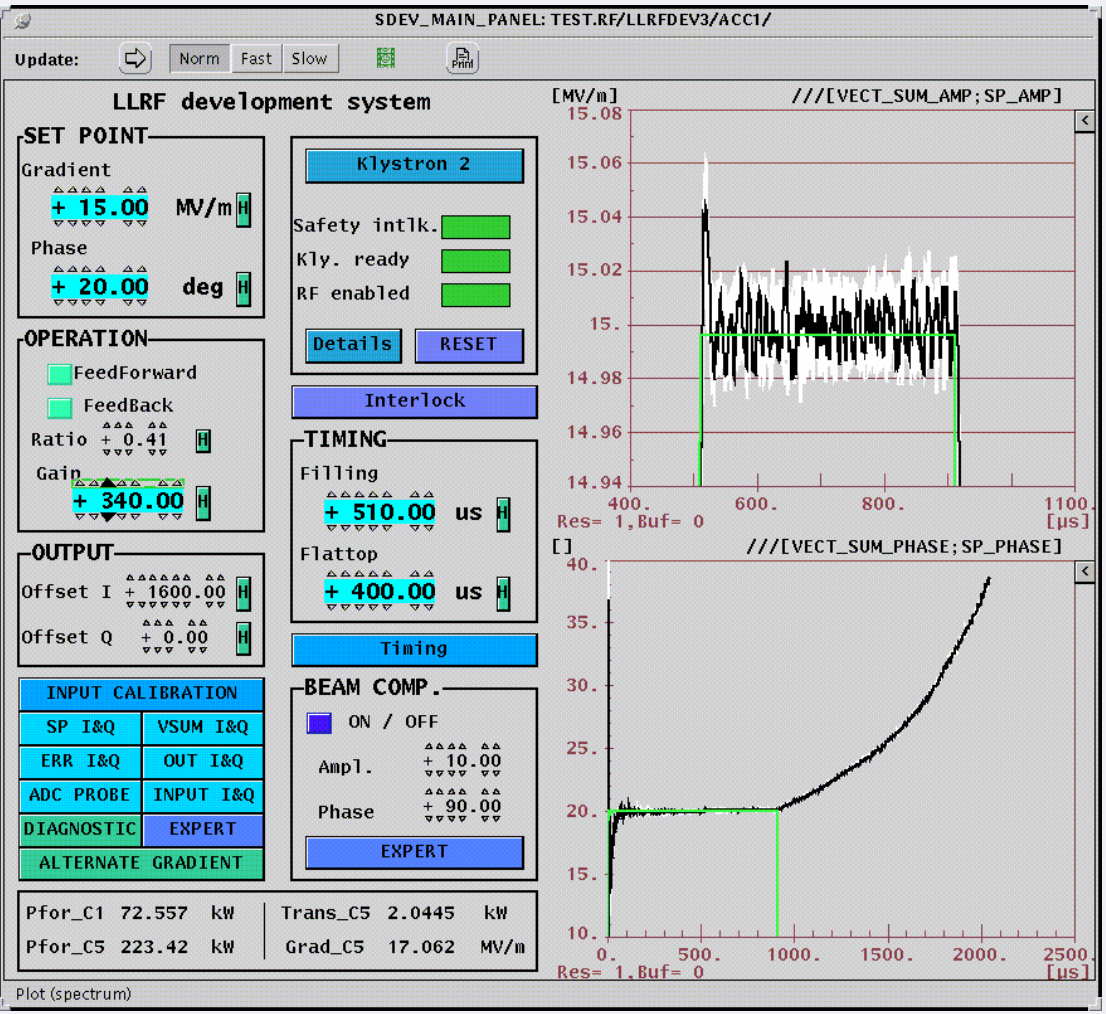
Modeling and design procedure under investigation to achieve better performance.

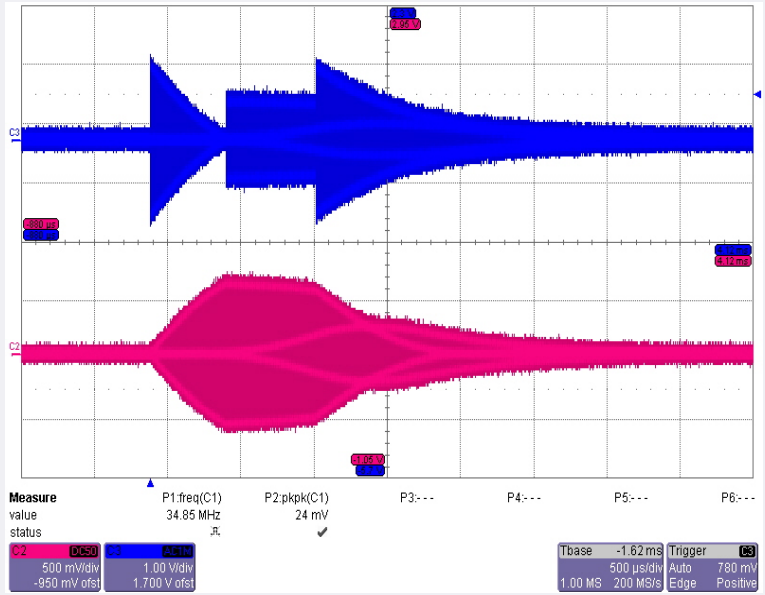
XFEL LLRF Development
Cavity Simulator

Simulation

- Cavity simulator installed in ACC1 development system – algorithms development for XFEL
  - Running on SIMCON DSP board
  - Baseband input and output
  - Features:
    - 4 cavities with LFD, pre-detuning.
    - Klystron model with nonlinearities (amplitude and phase).
    - High power distribution system (power dividers, phase shifters)
    - Measurement path simulation (attenuation and phase change)
    - Selectable output (probe, forward or reflected power)
    - Driven from ADCs or from internal tables (loaded through MATLAB)

Cavity simulator driven by ACC1 controller in the development system





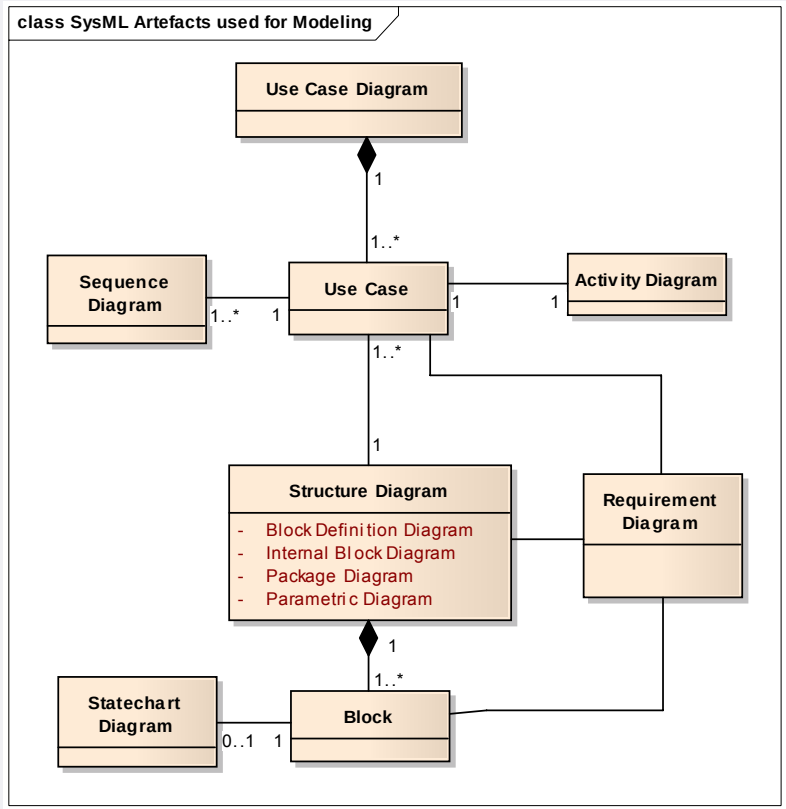
Documentation Projects

LLRF Documentation with SysML (1)

Modelling Process

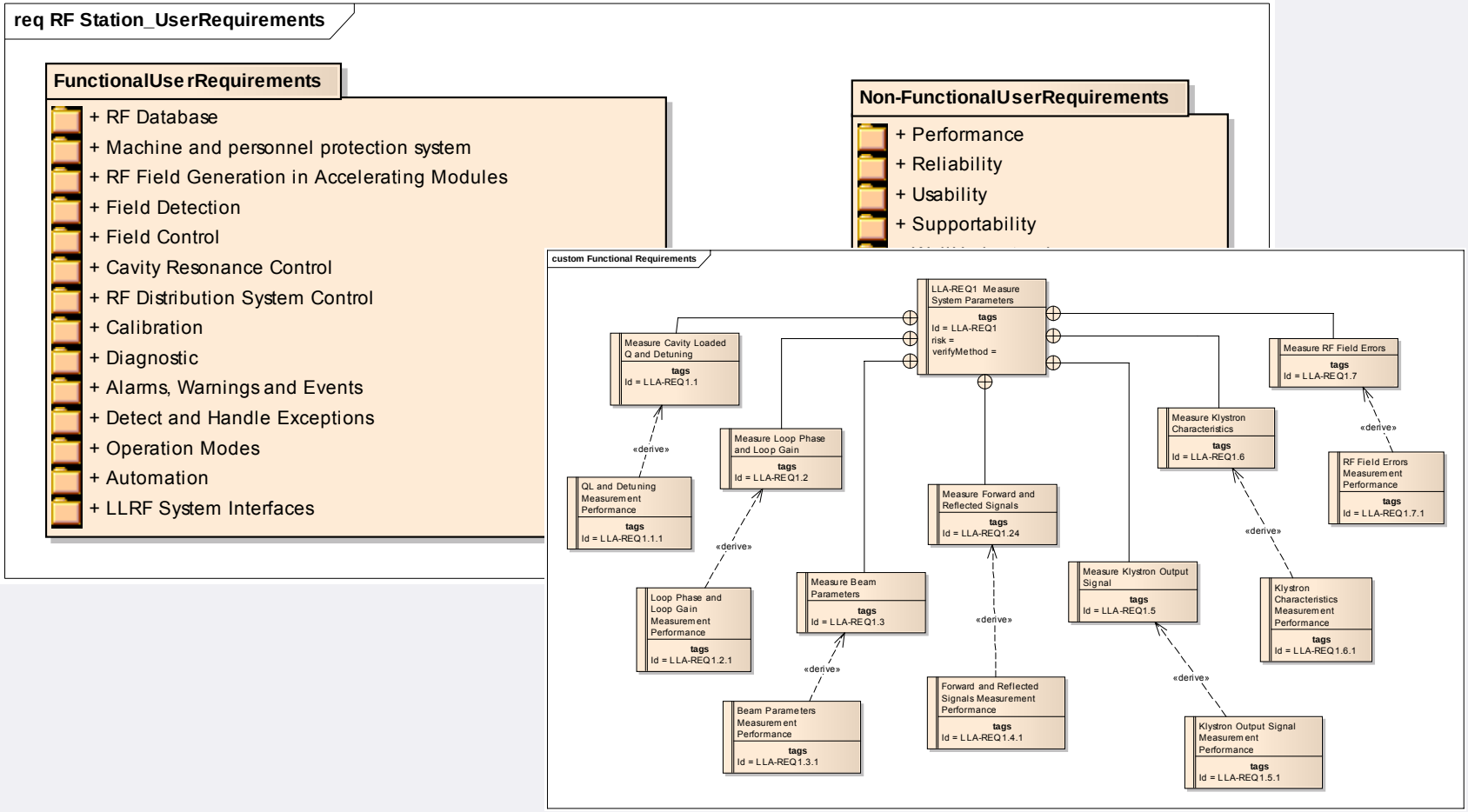
- Identification of necessary system models, aspects and views
- Requirements analysis and requirements capture
- Definition of use cases
- Modelling of system hierarchies
- Modelling the system structure
- Modeling of system and subsystem interfaces
- Definition of activities and state machines
- Definition of parametric diagrams

SysML Artefacts used for Modeling



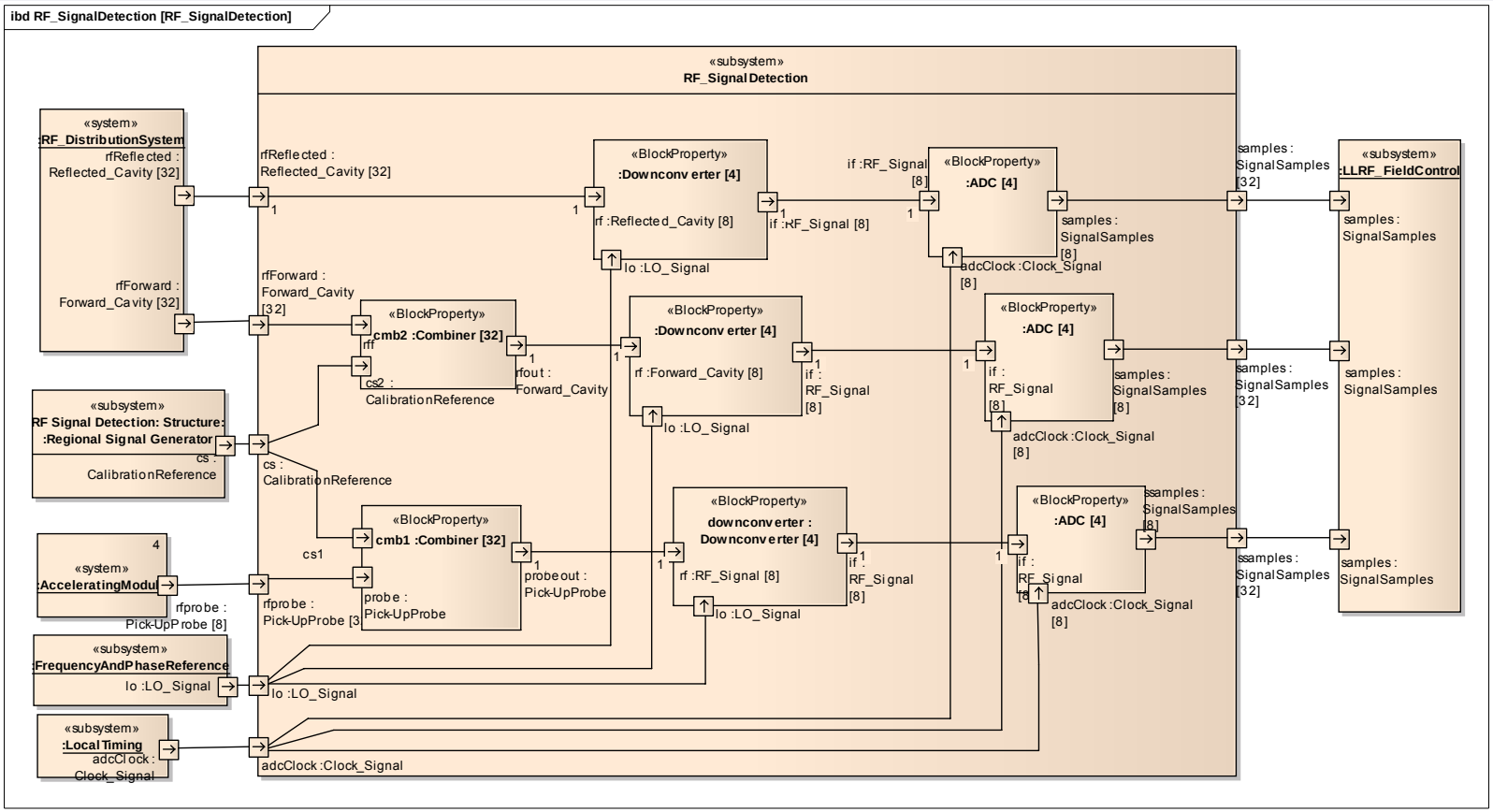
LLRF Documentation with SysML (2)

Example: Requirement Diagrams for LLRF



LLRF Documentation with SysML (3)

Example: Internal Block Diagram for LLRF Subsystem



LLRF Documentation with SysML (4)

Major model parts

- LLRF System model, Signal Library, Hardware Component Library, Units Library

Abstraction levels

- Functional, Structural, Physical (Deployment?) View

Model statistics

- about 270 use cases
- about 450 diagrams
- about 4200 model elements

Plan forward

- Add more and more details in depth (subsystems, blocks, diagrams …)

Tools

- Enterprise Architect 7.1
- SysML - Enterprise Architect MDG Add-In

Sources for LLRF Information

LLRF Wiki Pages:
http://mskpc14.desy.de/wiki/index.php/Main_Page

LLRF System Documentation:
http://tesla.desy.de/~simrock/EA/index.htm

LLRF News:
http://wofwiki10.desy.de/xfel/index.php/LLRF_News