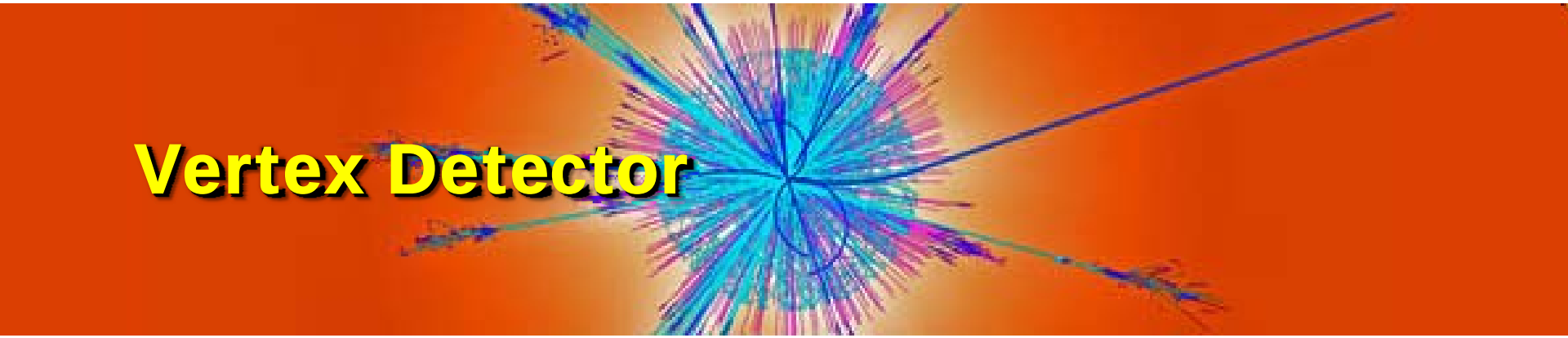
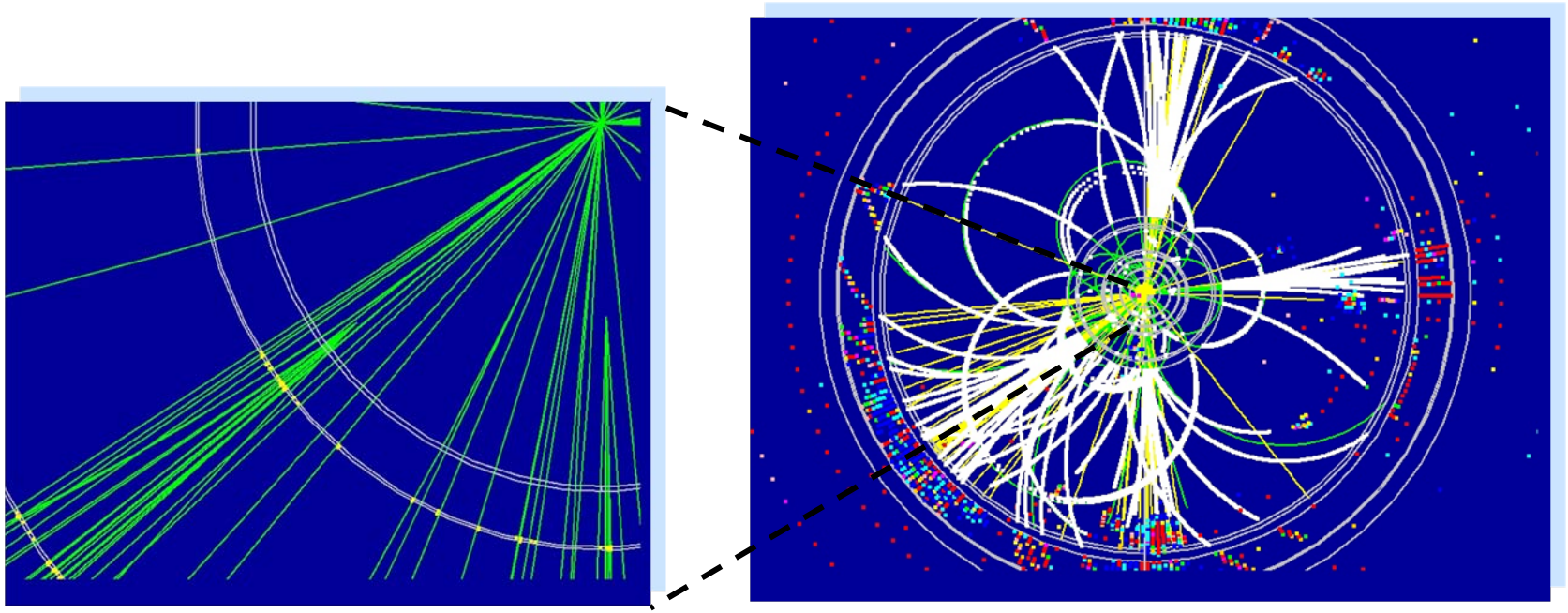
Tracking and Vertexing Summary

Suyong Choi
SKKU, Korea

Vertex Detector



Physics Requirements for ILC Vertex Detector



$$\sigma_{IP} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$

	a (μm)	b (μm GeV)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC II	14	12
ILC	5	10

Vertex Requirements for ILC

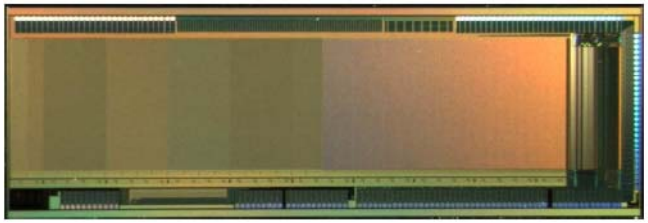
- Geometry
  - Coverage $|\cos\theta| < 0.96$
  - Radii 1.5 cm ~ 6.0 cm
- Fine pixels
  - 20 μm x 20 μm
- Thin Detector
  - 0.1% X_0 per layer
- Sparsified readouts
  - 1 Gpixels
  - zero suppression and/or time stamping

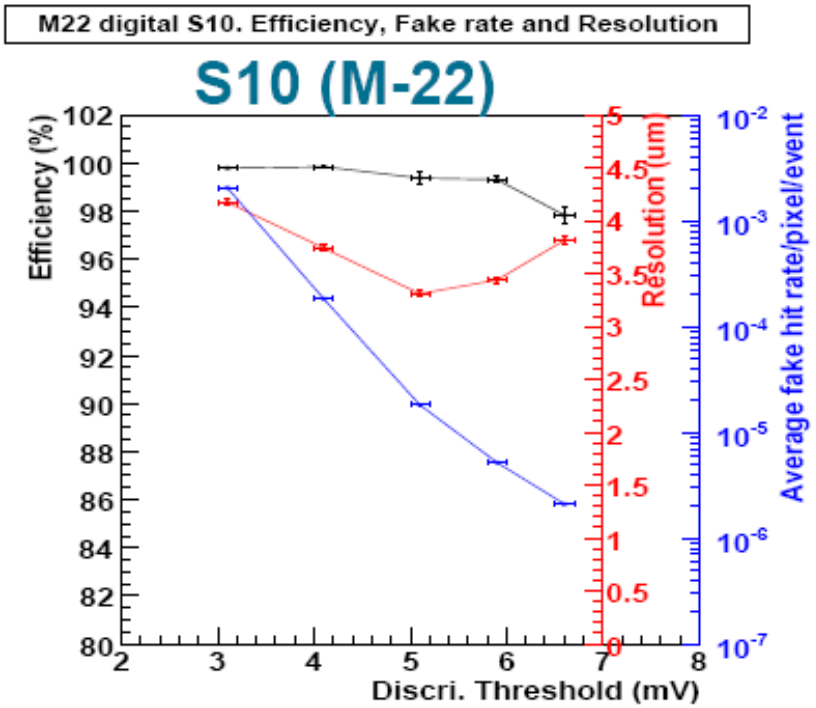
MIMOSA

M. Winter

- On pixel integrated CDS with discriminator
  - CMOS
- Mimosa-22
  - 128 col x 576 pixel, 18.4 μm pitch
  - 10 k/s readout
  - 99.9% det. eff
  - S/N: 16 ~ 20
  - ENC: 11e ~ 14e
  - 3.5 μm pos. resolution
- Irradiation test
  - 300kRad ENC: 10e → 15e

➔ Performance requirements met





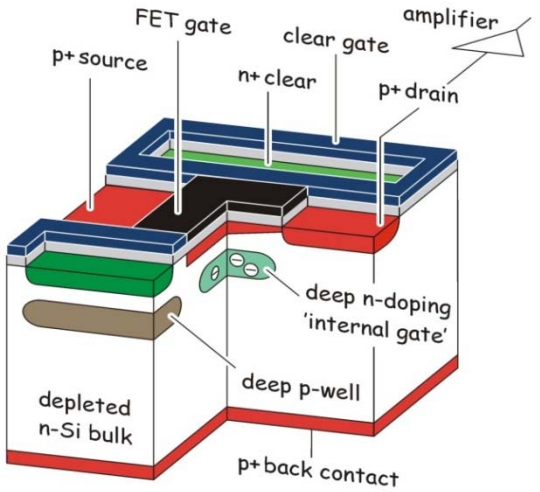
MIMOSA

- Add zero sup circuit for 2009 EUDET beam tests
  - 1152 columns
- A variant will be used for STAR VXD
  - Being fabricated
  - Physics in 2010
- 3-D in collaboration with INFN and FNAL
  - 130 nm 2-Tiered Chartered-Tezzaron process

DEPFET

C. Pardo
L. Andricek

- Charge drifts to FET gate → current flow

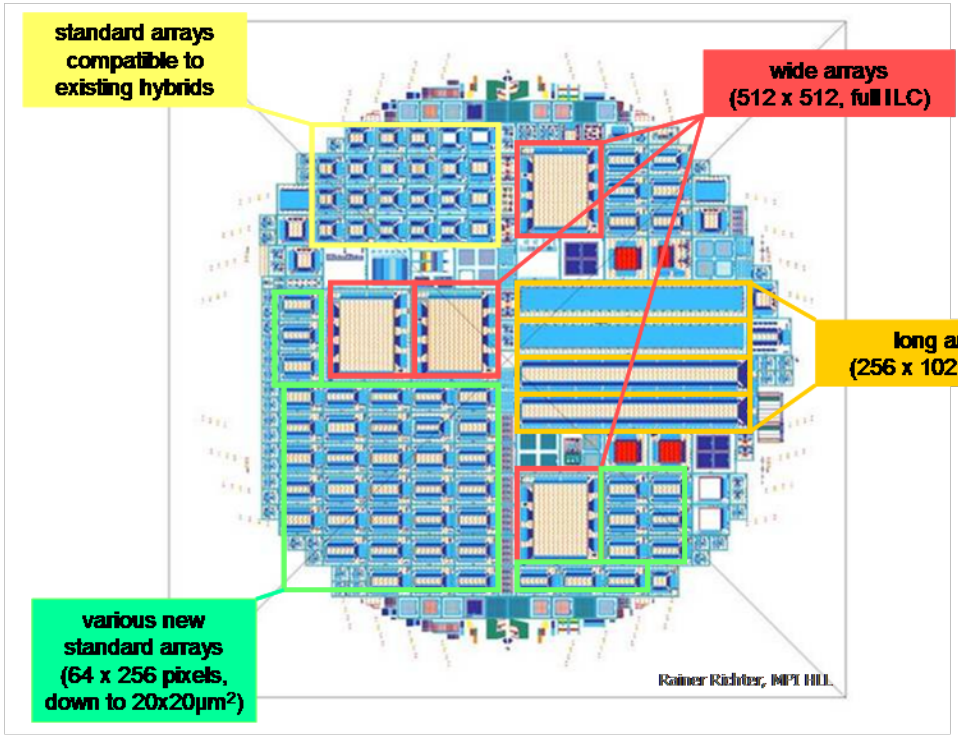


- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ many test beams @ CERN and Desy:
  - ✓ S/N≈140 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. with 24 µm pixels: 1.3 µm @ 450 µm ←→ goal ≈ 3.4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm), design goal 0.11 % X_0
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2

DEPFET

C. Pardo
L. Andricek

- New PXD5 DEPFET



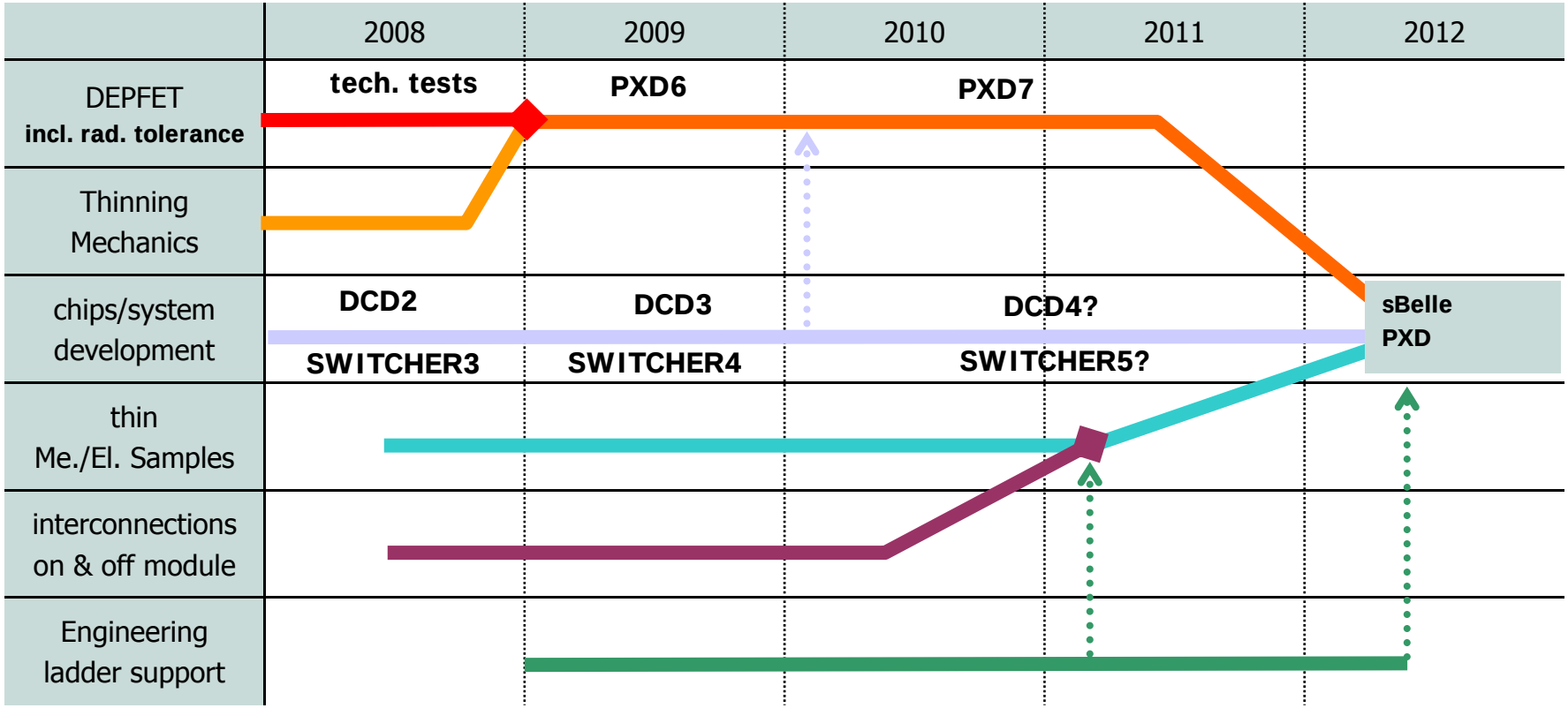
- 20 micron pixel
- smaller gate length -greater gain
- smaller clear voltage

- New quieter readout – DCD2
  - 100e- ENC

DEPFET

C. Pardo
L. Andricek

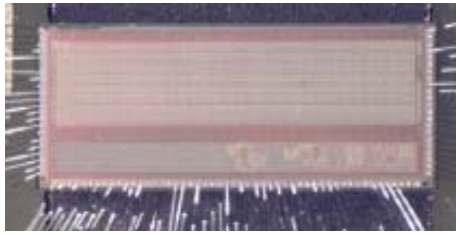
- PXD6 will be first thinned DEPFET
- Work on SuperBelle detector will be beneficial



Monolithic Active Pixel Sensors – MAPS

- On-chip sparsification and time stamping

- Deep N-Well MAPS — V. Re
  - APSEL4D -32x128
  - 50 μm pitch – move to smaller process
  - Beam test - 90% efficiency
    change layout to improve efficiency
  - should implement multiple pixel hit



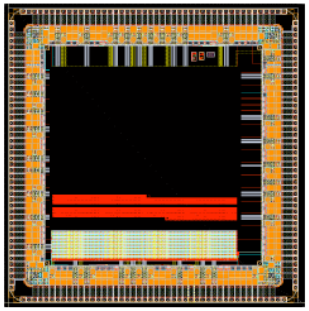
- Mimoroma2 — E. Spiriti
  - Analog readout
  - threshold scan works as simulation

- Going to 3D will help

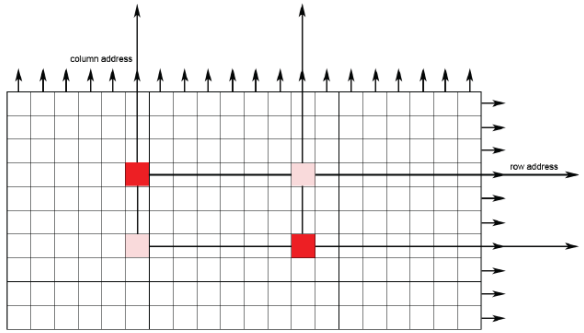
Continuous Acquisition Pixel Detectors (CAP)

H. Hoedlmoser

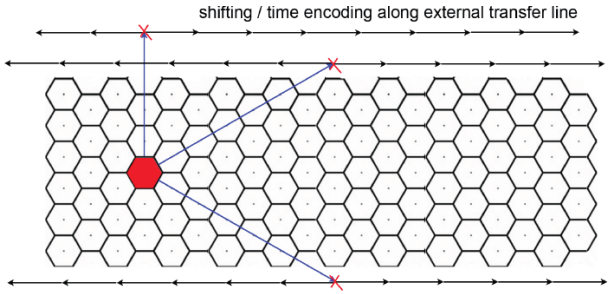
- SuperBelle application
- MAPS with in-pixel signal storage
  - after charge to V conv.



- CAP7
  - 60k pixels – 5 mm^2
  - pixel: 35 x 50 μm^2
  - 0.2 micron OKI on SOI
  - Chip expected this month



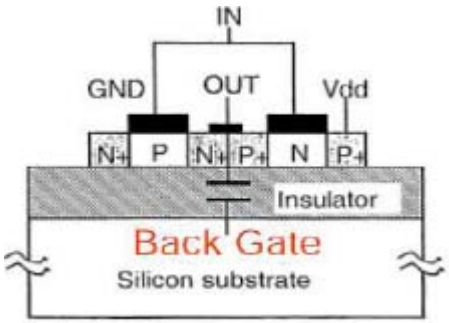
- New ideas for Hexagonal routing of signals
  - Reduced fakes, improved resolution, faster transfers

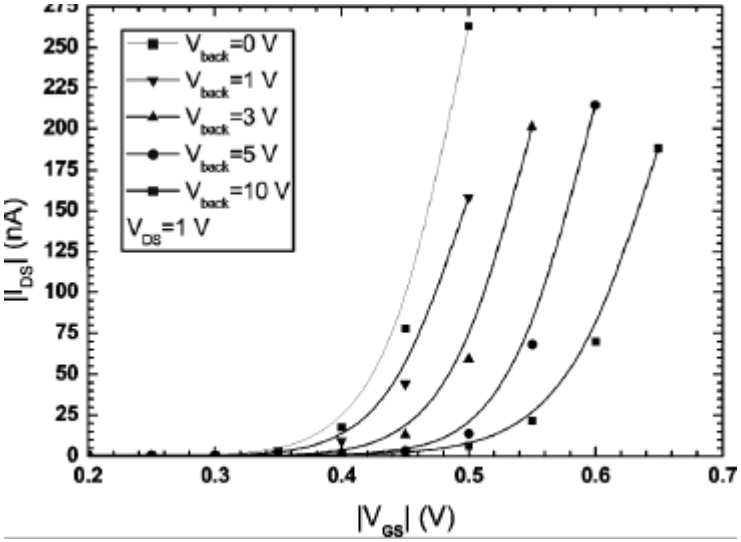


SOI – Silicon-on-Insulator

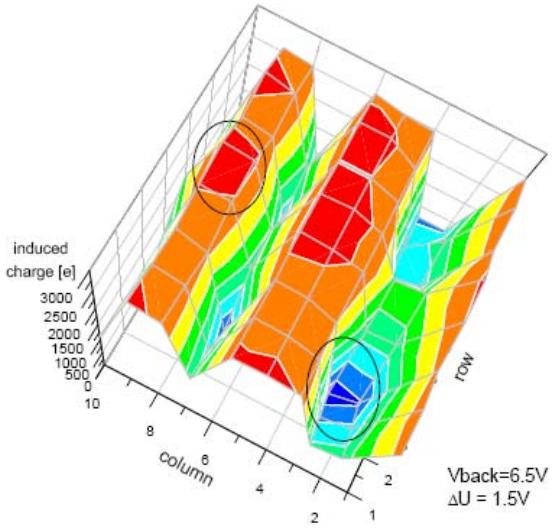
M. Trimpl

- Backgate effect
  - can be mitigated but not eliminated





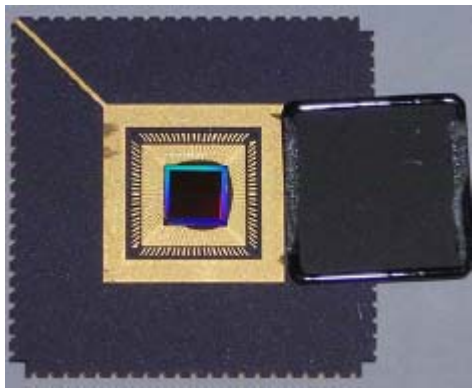
- Cross talk
  - No Cadence tools to analyze this

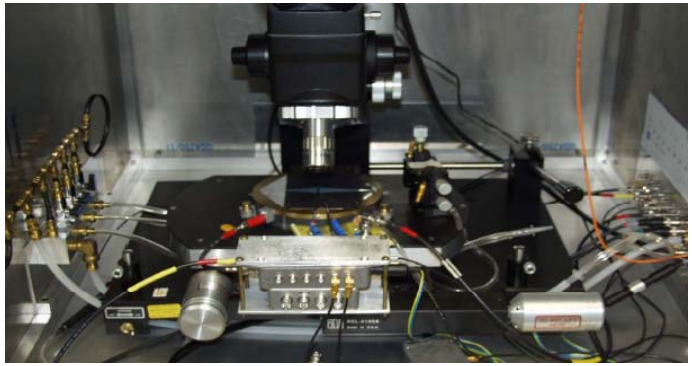


Chronopixel

N. Sinev

- Monolithic CMOS
  - In-pixel sparsification
  - Single bunch time stamp
  - 4 hits/pixel/train
- 80 chips fabricated
  - 80x80 pixel, 50 micron pitch
- Status
  - Test equipment ready in Jan. 2009
  - Simulation of expected performance
  - Design deep p-well device (improves eff), looking for manufacturer
  - move to 45 nm process

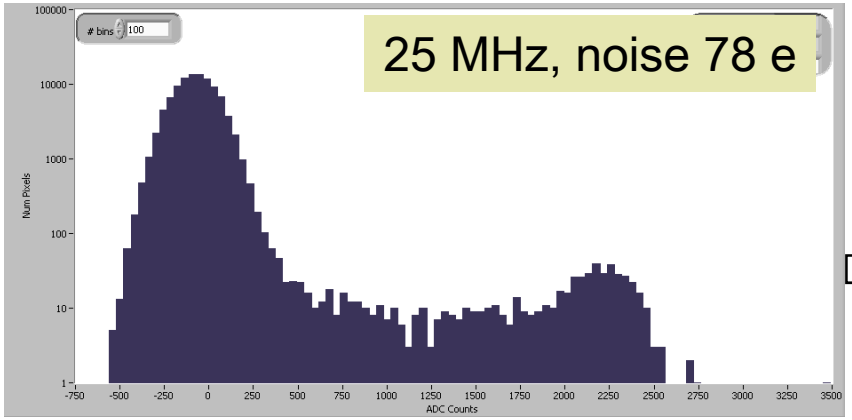


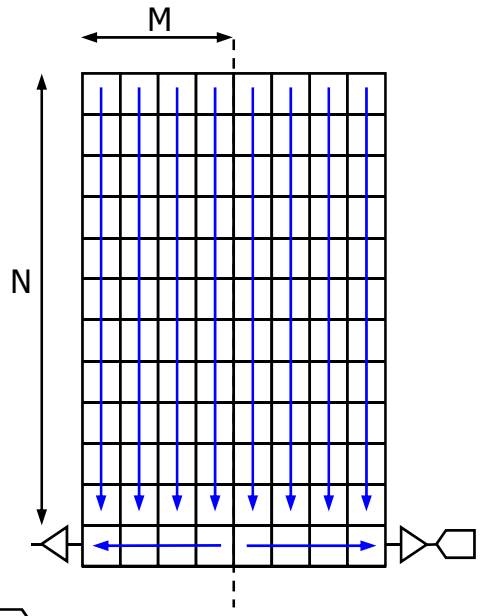


Column Parallel CCD (CPCCD)

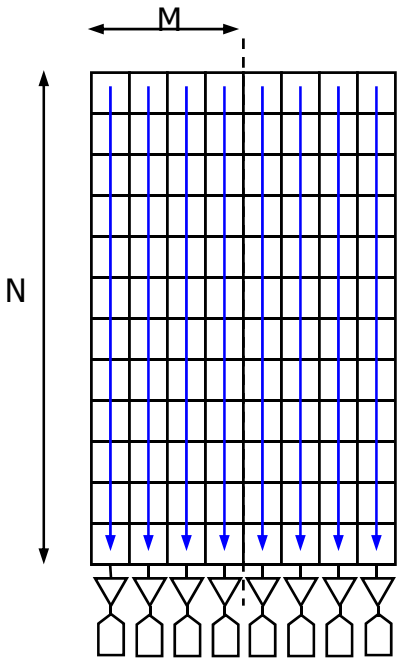
A. Nomerotski

- LCFI Collaboration
- Need 50MHz operation to keep occupancy <1%
  - CPC2 works up to 45MHz





"Classic CCD"
Readout time ≈ N×M /f_{out}



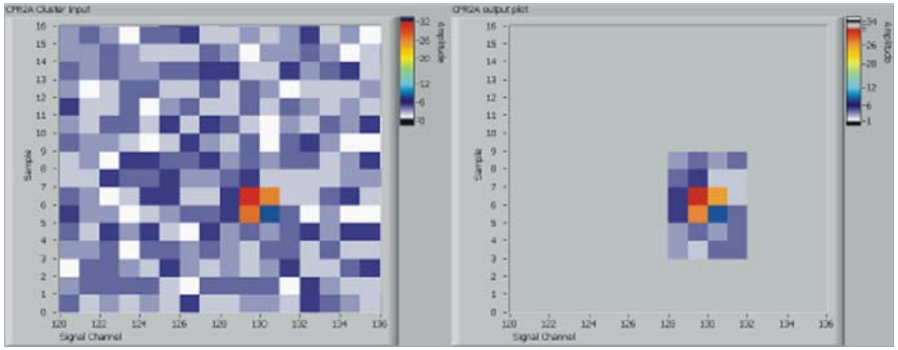
Column Parallel CCD
Readout time = N/f_{out}

- Lower capacitance variant successfully operating

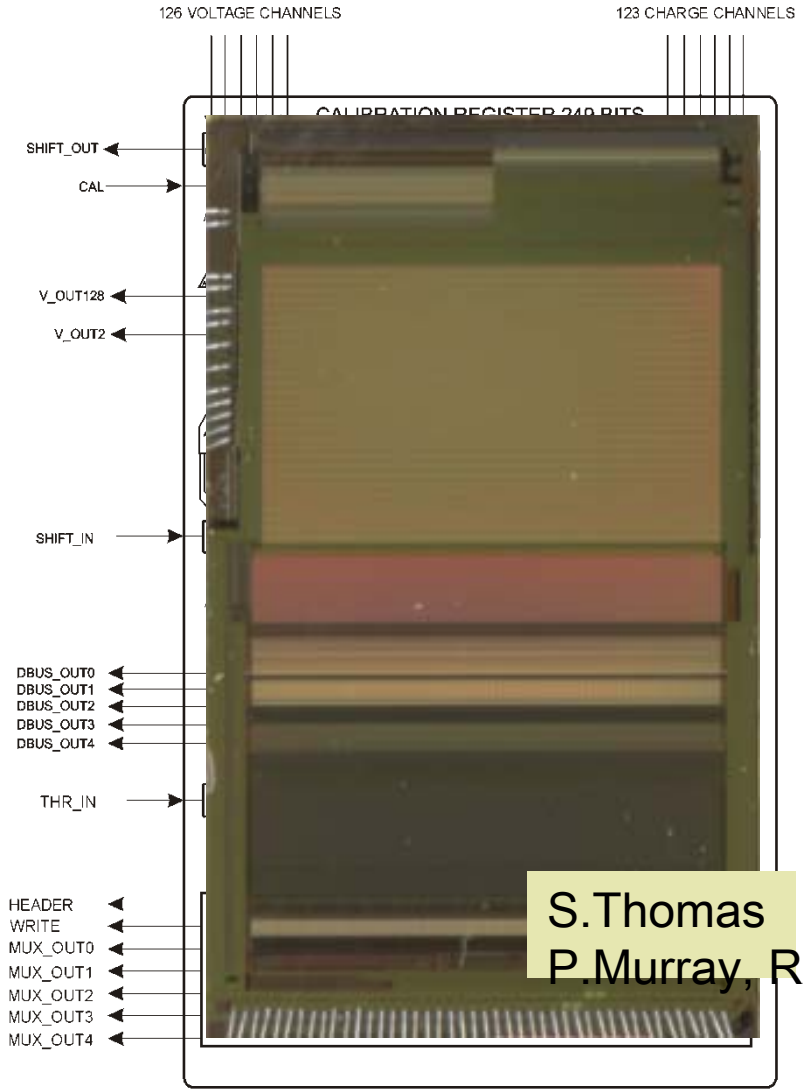
CPCCD Readout –CPR2A

A. Nomerotski

- Voltage and Charge
- 5 bit Flash ADC
- Cluster finding

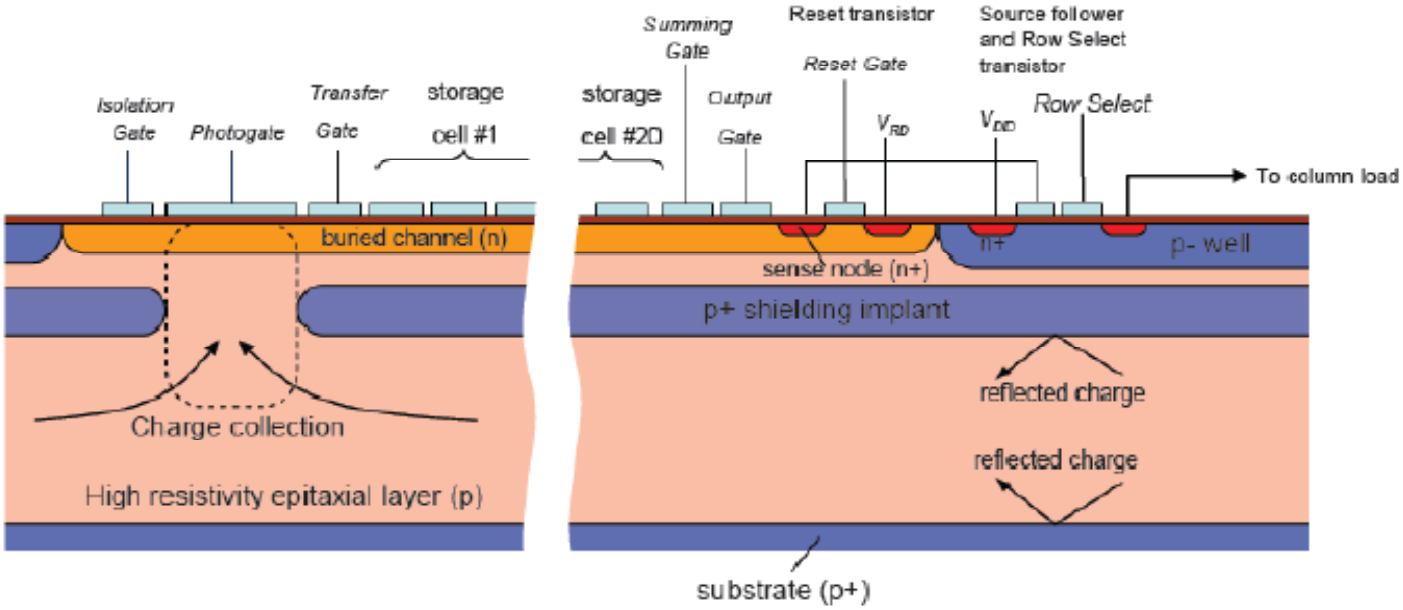


- Sparsified readout
- Performs up to specs



In Situ Image Sensor (ISIS)

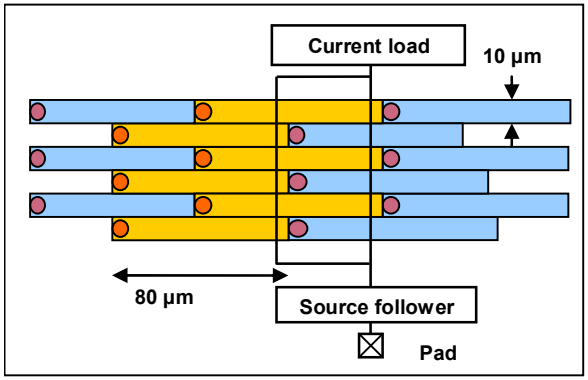
A. Nomerotski

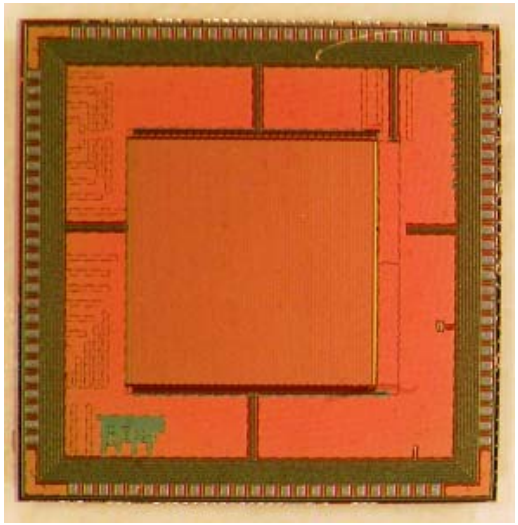


- Charge collected in "photogate"
- Charge transferred to 20 CCDs in the pixel
- Read out during 200ms quiet time
  - 1MHz operation
- CMOS and CCD technology

ISIS

- ISIS2
  - Pixels 80 x 10 μm^2
  - Imaging pixels 40 x 20 μm^2
  - Total area 1 cm^2
  - p-well
  - just delivered





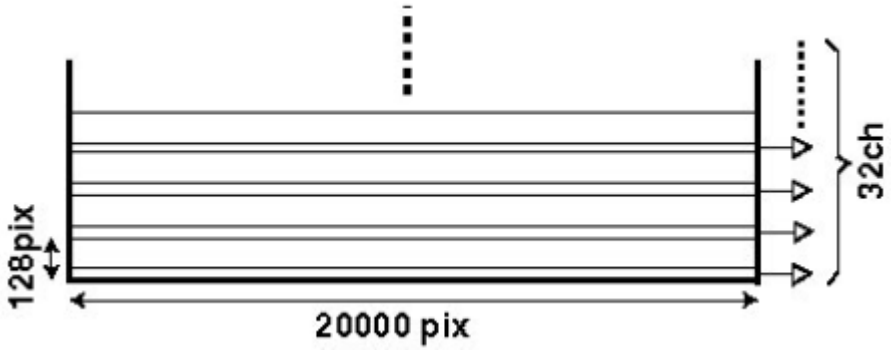
- Future of UK Silicon project
  - New proposal SPIDER (Silicon Pixel DEtector R&D)
  - Continue ISIS program
  - Develop MAPS based on 4T process

Fine Pixel CCD (FPCCD)

Y. Sugimoto
Y. Takubo

- Integrate for 1 train, readout in the quiet time

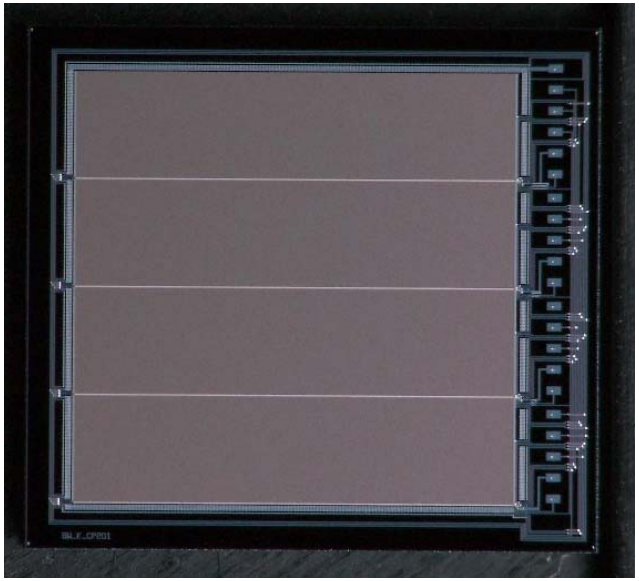
- To keep the occupancy below %1 / train reduce pixel size
  - goal: 5 micron pitch
  - fully depleted epitaxial layer 15, 24 micron thickness
  - moderate clock speed, small power dissipation
  - goal: signal level <2000e, noise <50e

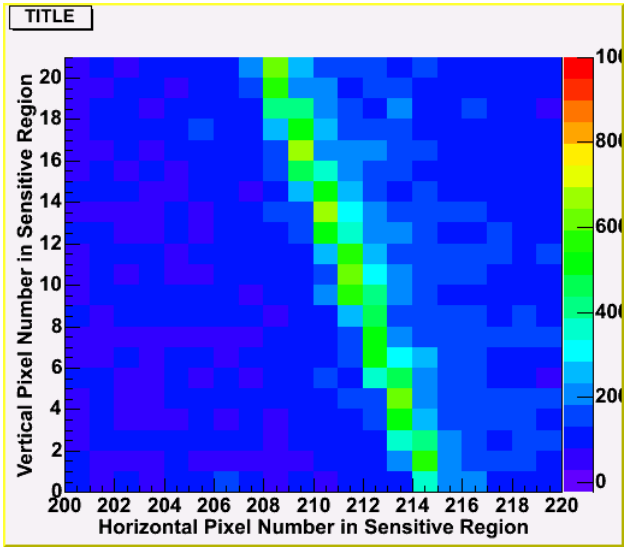


FPCCD

Y. Sugimoto
Y. Takubo

- First prototype delivered by HPK
  - 512 x 512, 12 micron pitch
  - 50 micron wafer thickness, epitaxial layer: 15 and 24 micron
  - 10 MHz readout
  - 10 mW/channel
  - gain 5~6 μV/e
  - Detailed testing in progress
- Readout chip
  - ENC = 40 e- > 30 e- (target)
    - production problem
  - not yet in their target 10Mpix/s
- Small prototype in 2010 for beam tests
- construction-ready EDR by 2012 – 2013

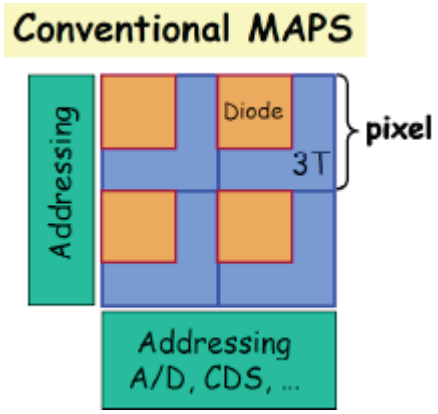


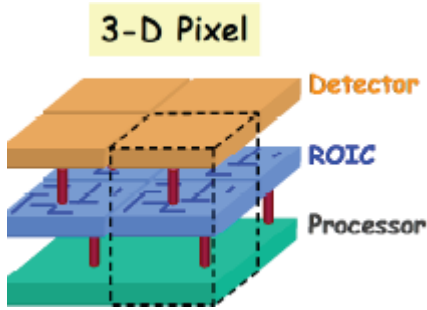


3-D Vertical Integration

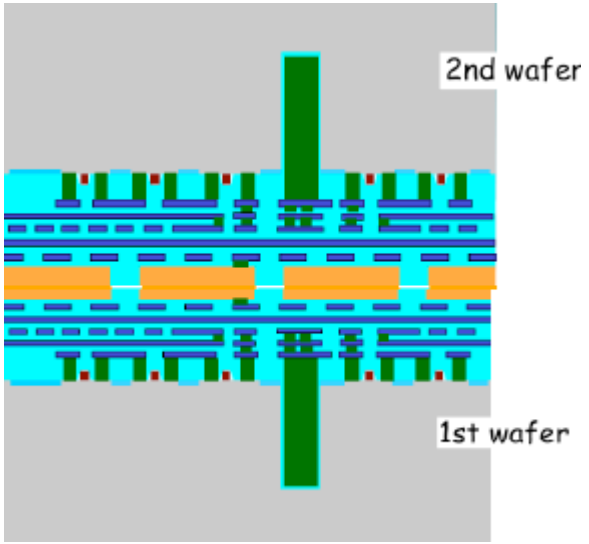
R. Lipton
Z. Ye

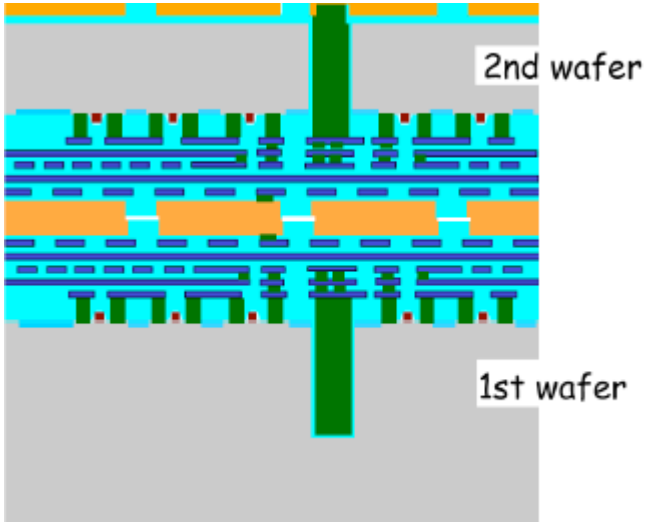
- Vertical integration of electronics
  - reduces interconnection lengths
  - heterogenous device integration





- Tezzaron 3D process

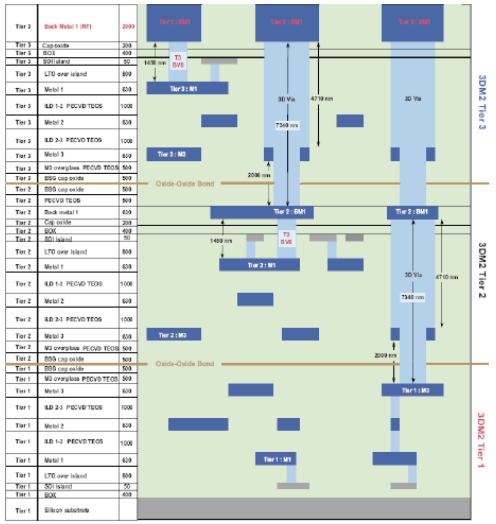


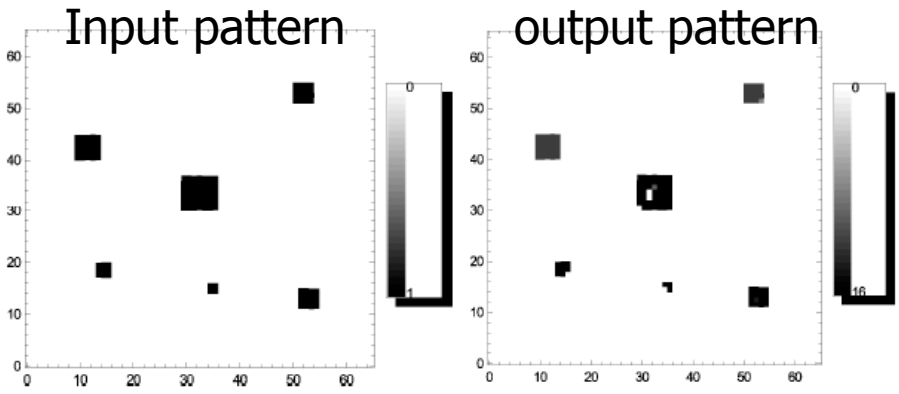


3-D Vertical Integration

R. Lipton
Z. Ye

- Fermilab VIP chip
  - 3 – Tiers
  - 22 micron thick
- Multiproject run being organized by Fermilab
  - Cost sharing
  - Synergy
- Special focus session on Tuesday

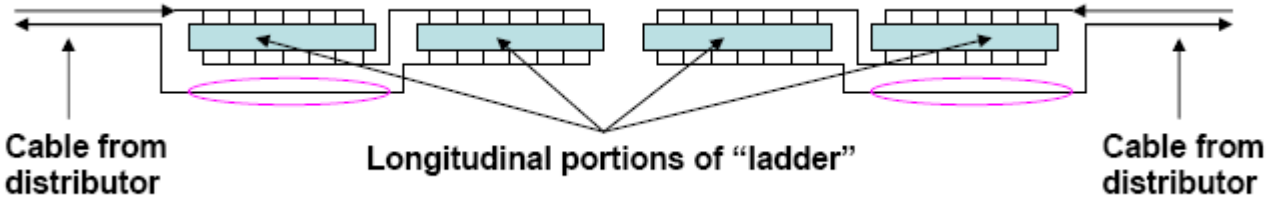




Preselected pattern of pixels for the injection of signal to the front-end amplifiers; pattern shifted into the matrix, than positive voltage step applied accross the injection capacitance; threshold levels for the discriminator adjusted according to the amplitude of the injected signal

Pattern of pixels from the preselected injection pattern that after injection of tests charge reported as hit (grey level represents number of repetition - 8 times injection)

Power Distribution to Vertex Detectors



- Cable

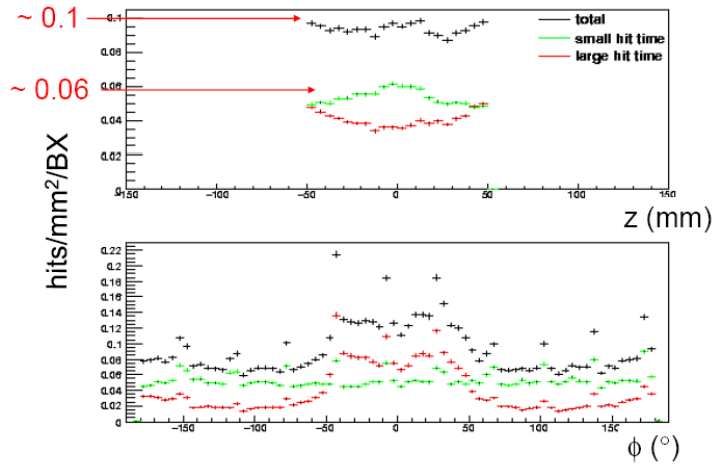
0.078 X_0

- Lorentz Forces: 0.72 N per cable
- Routing of cable has design implications

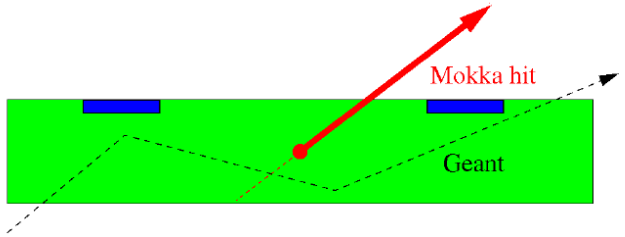
Backgrounds and Simulation

M. Winter
L. Maczewski
P. Luzniak
R. Walsh
W. Mitaroff

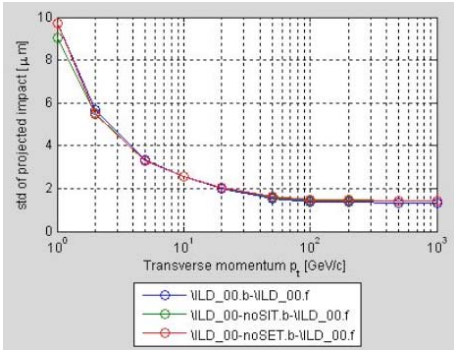
- Background in the first layer
  - large time hit
  - sensitive vol. thickness 50 μm



- Low angle tracks in simulation was not adequate
  - Option to store in new version

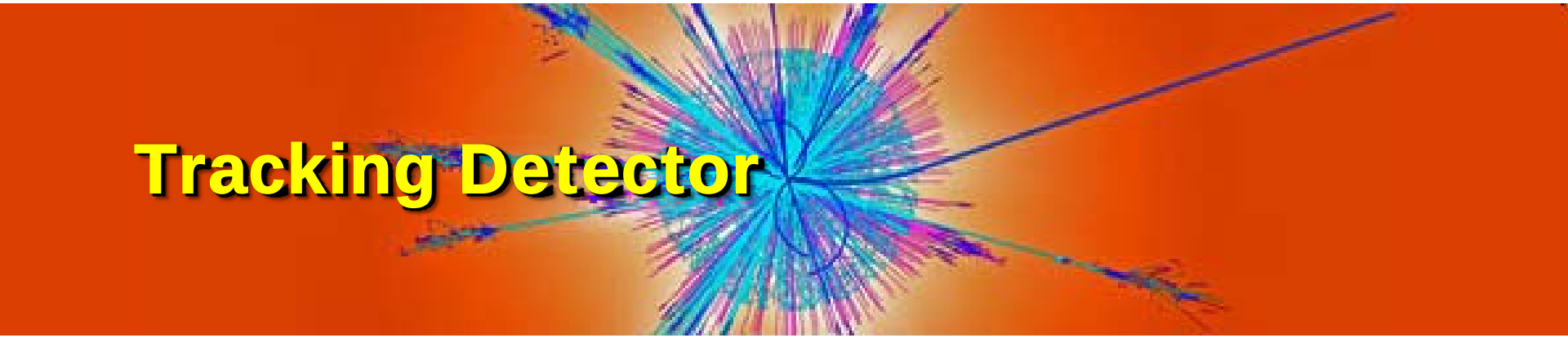


- Tagging studies for optimizations

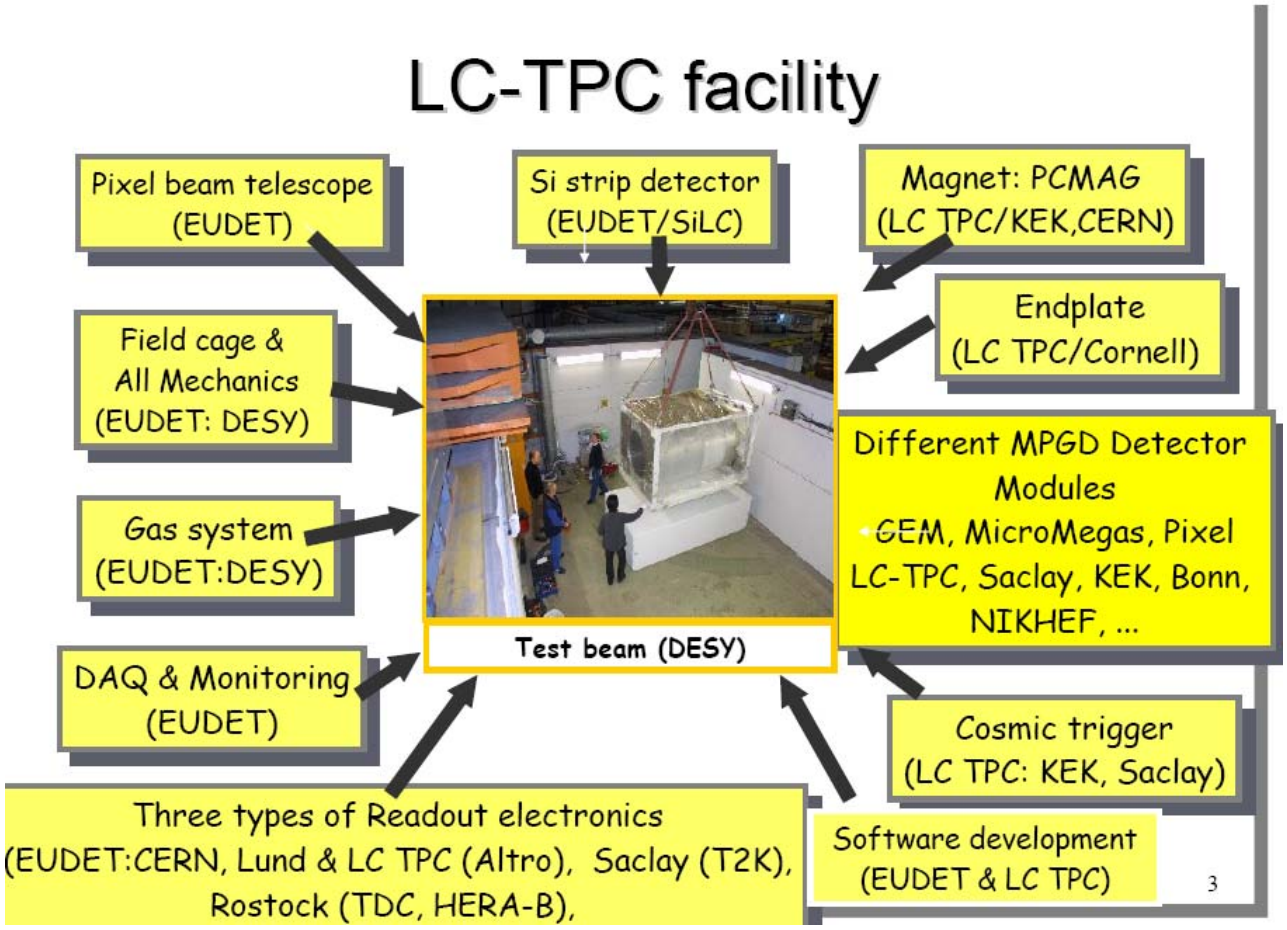


- LiC Detector Toy
  - allows quick study tracker perf.

Tracking Detector



LC TPC Large Prototype Test Beam

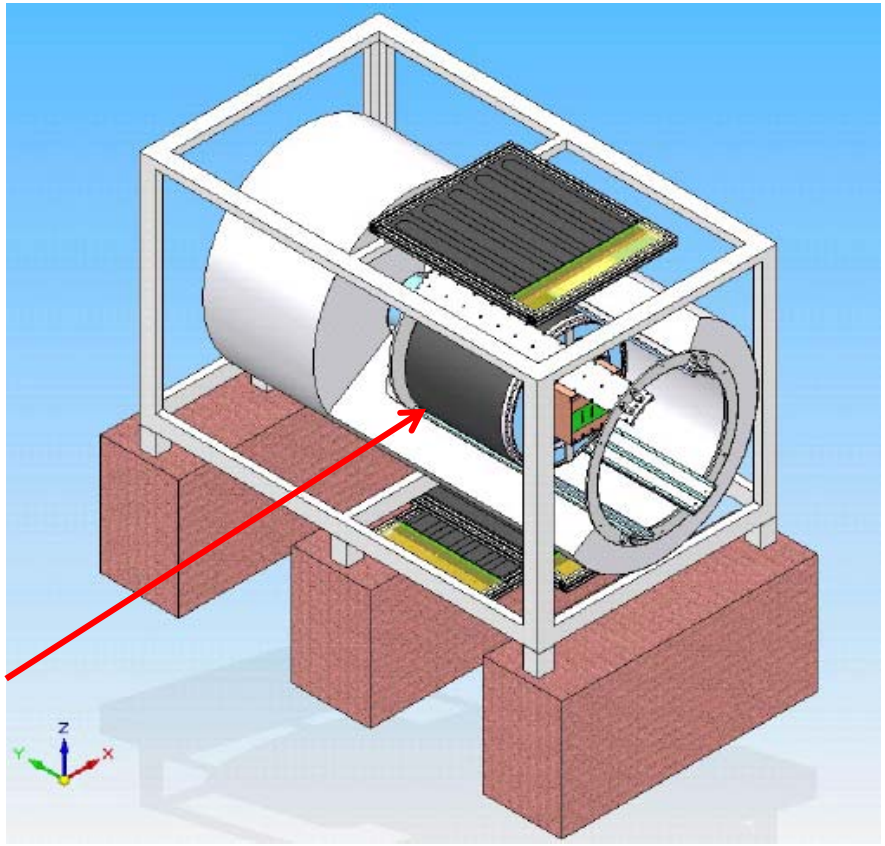


- Strong collaboration among many groups esp. EUDET
  - Talk by I. Gregor

LC TPC Large Prototype

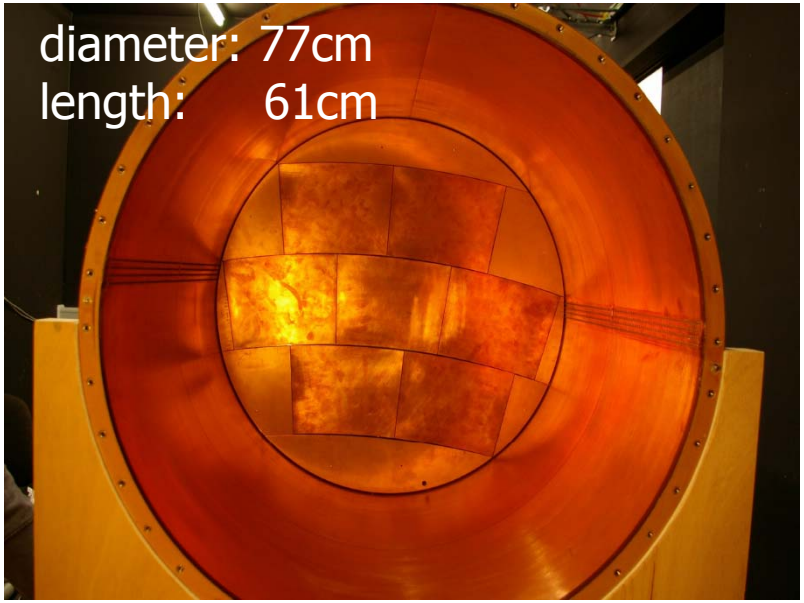
T. Behnke

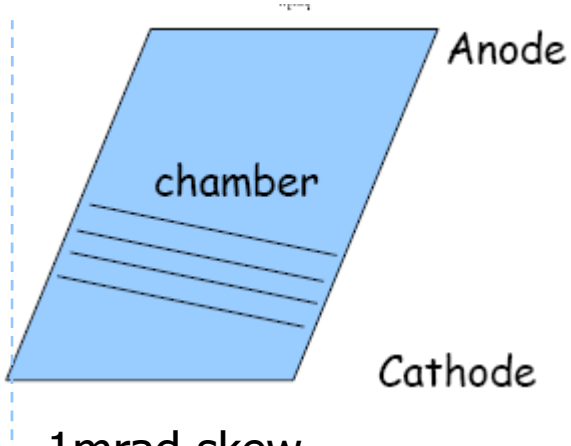
- SilC strip detector outside to monitor beam position
- Overall beam infrastructure ready
  - Movable stage expected early 2009
  - Beam will be available for most of 2009, but DESY cryo upgrade
- First cosmics with B field next week with micromegas



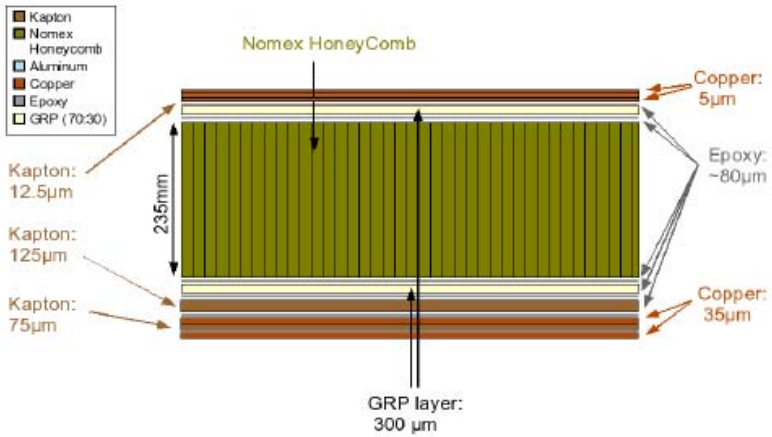
LC TPC Large Prototype

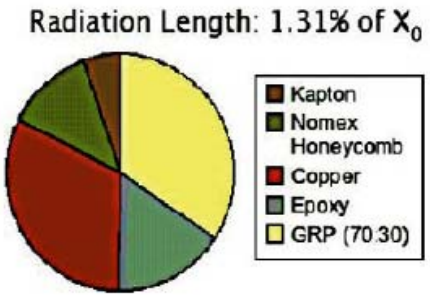
Ties Behnke





1mrad skew
$\rightarrow 10^{-3}$ variation in E-field



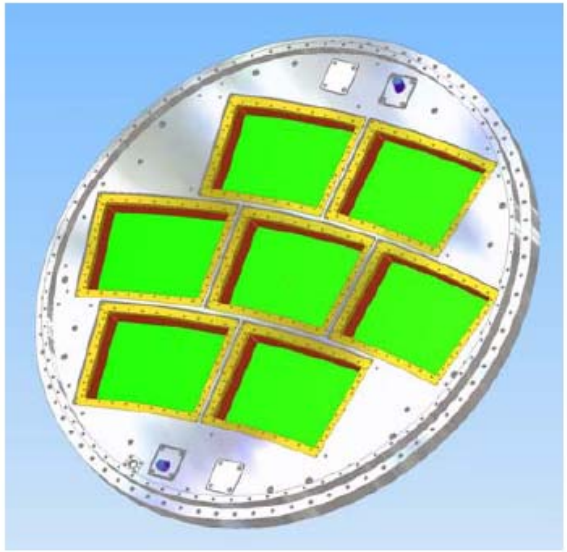


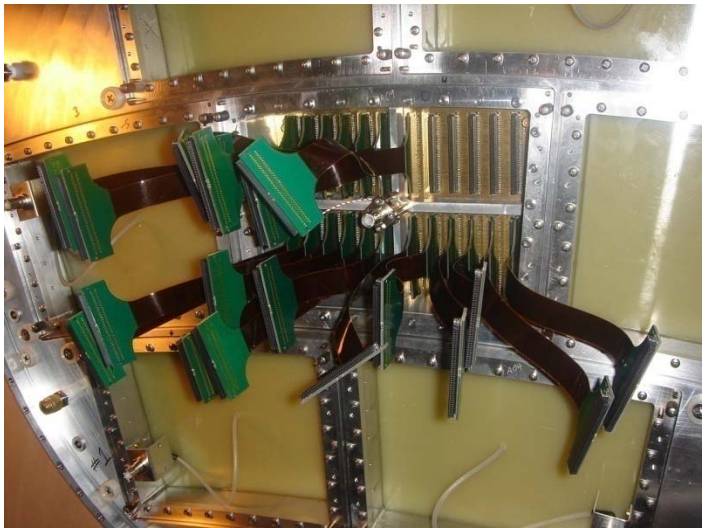
Material budget per wall

LC TPC Endplate

D. Peterson
M. Dixit

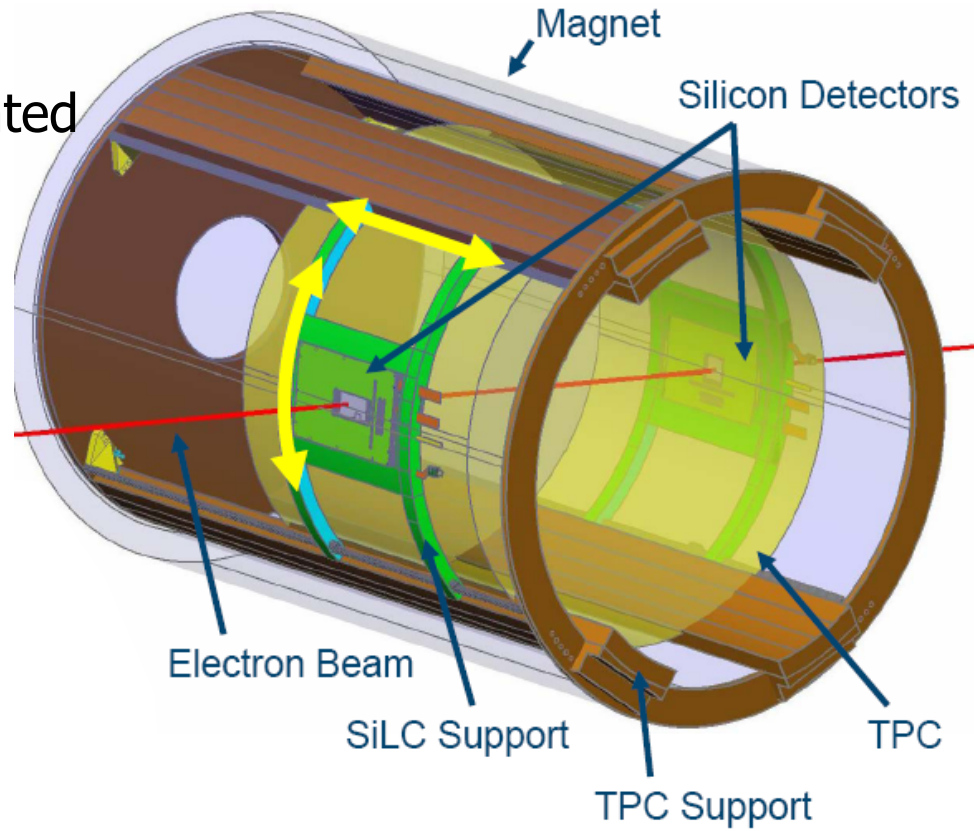
- provide framework to evaluate several readout technologies
  - 7 modules common radius of curvature
  - 25 micron tolerance
  - made of aluminum
  - 10/30/2008 endplate assembled with one micromegas module





LCTPC Large Prototype

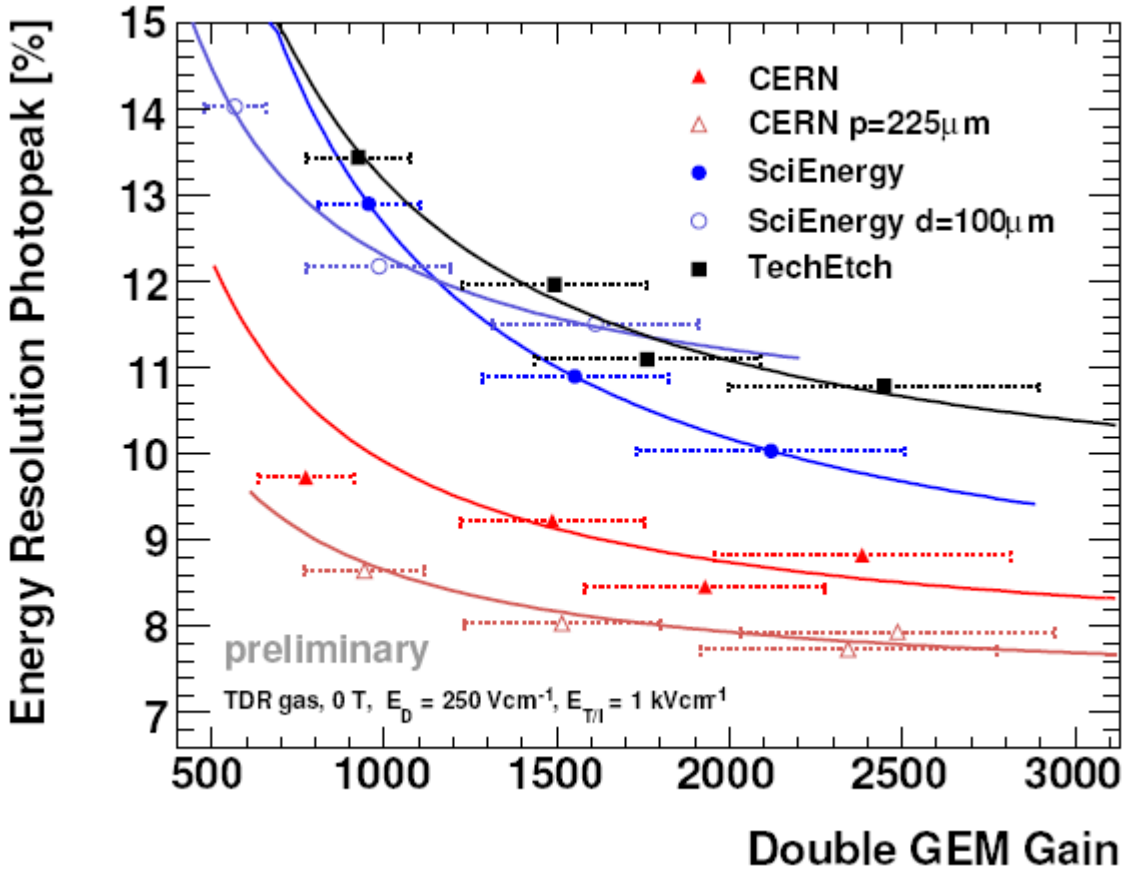
- Commissioning
  - End plate and cathode mounted
  - gas tightness confirmed
  - HV test undergoing
- Demonstrate
  - full volume tracking in non uniform B field
  - d(1/pt) ~ 10^{-4} (GeV^{-1})
  - 100 micron r-ϕ resolution 2-m drift
  - dE/dx capabilities



Silicon detectors in Feb. 2009

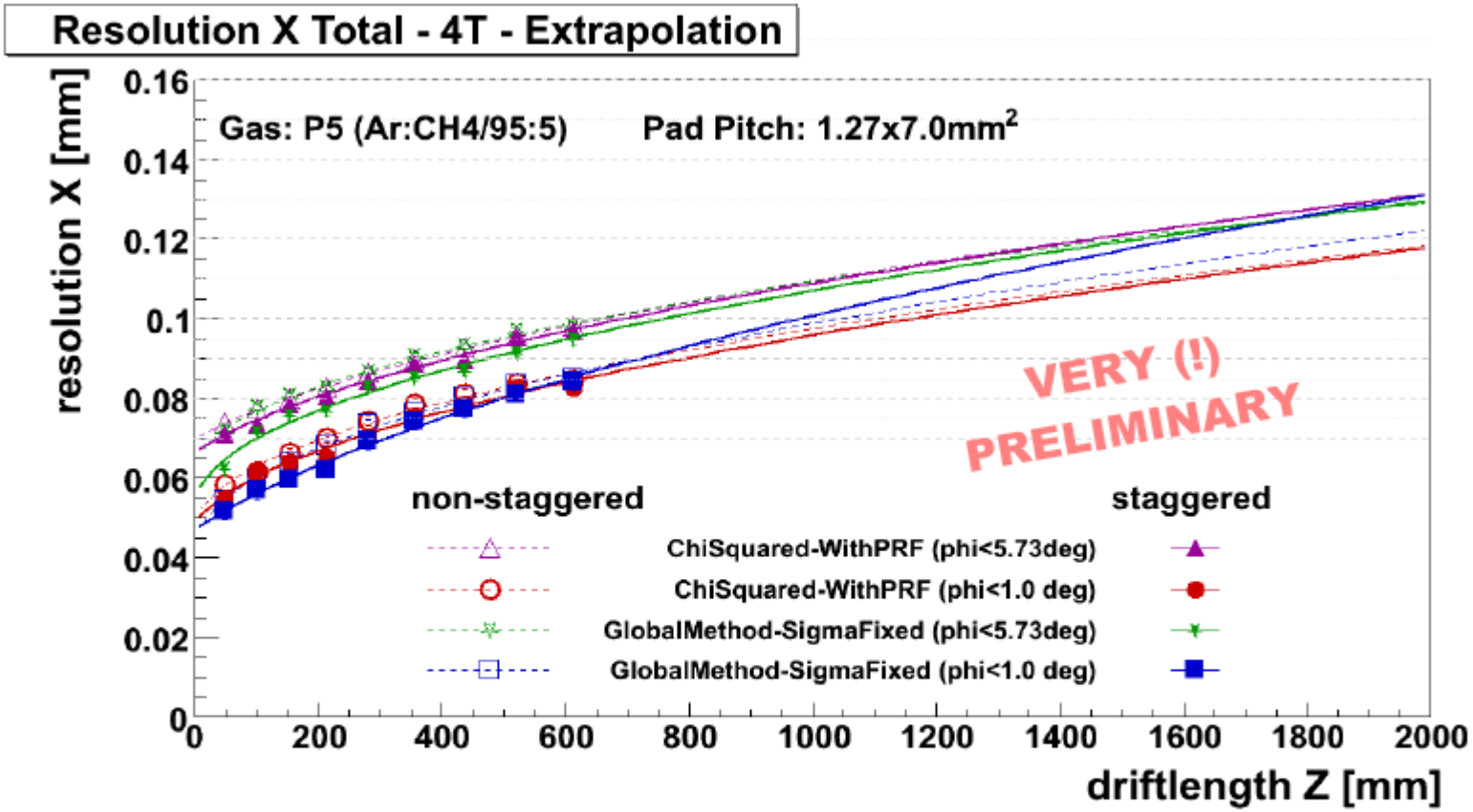
GEM R&D

L. Hallermann



Triple GEM in High B-field

R. Diener

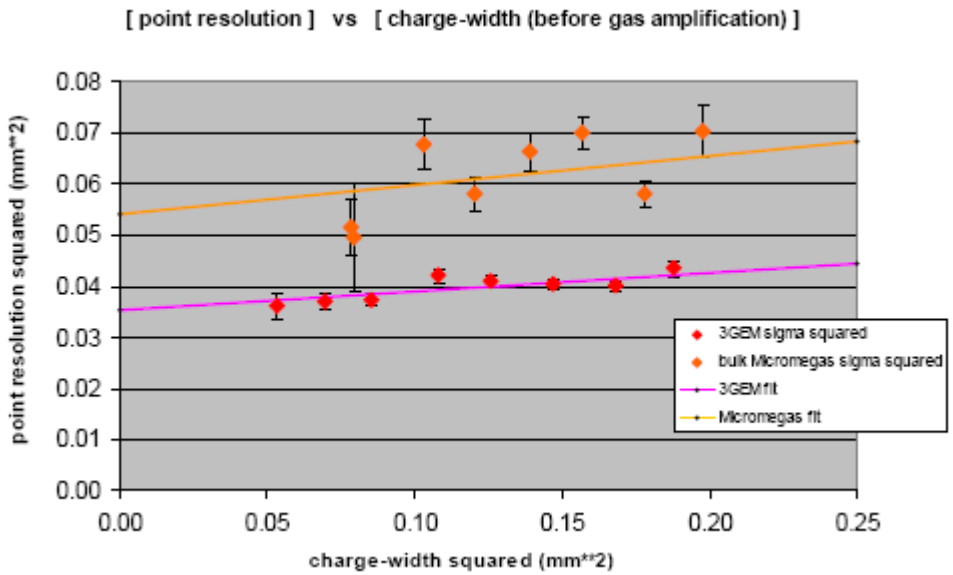


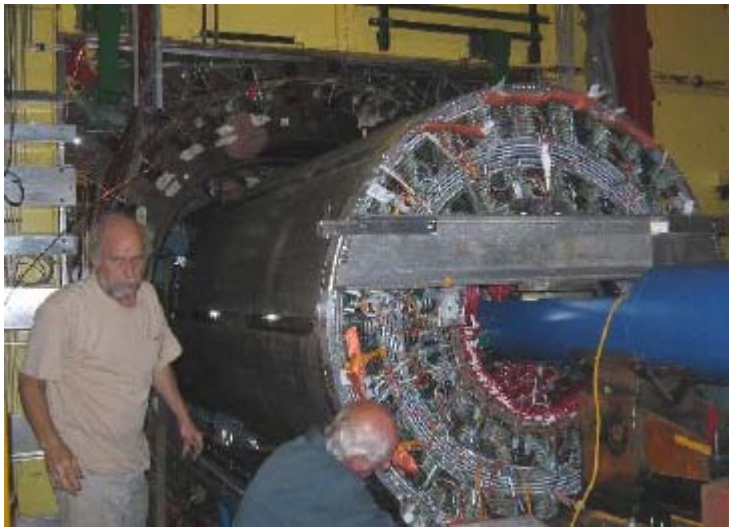
Angle Cut at |φ| <1.0° and |φ| < 0.1rad (5.73°)

GEM and Micromegas With Ar-CF_4-isobutane gas

D. Peterson

- small TPC prototype at Cornell in CLEO magnet





σ_0 ("corrected")

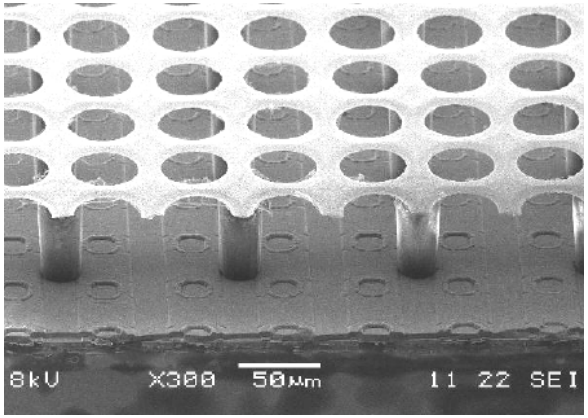
3GEM	158 μm
Micromegas	209 μm

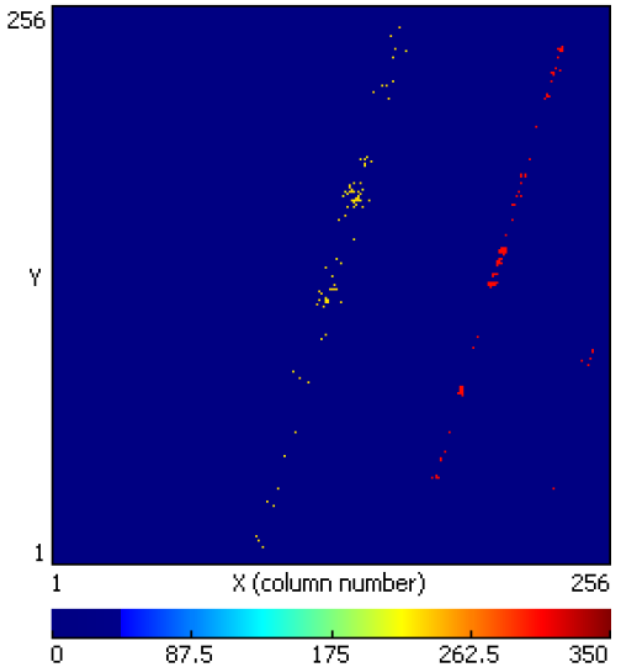
  - gain of micromegas half of 3GEM in this setup

Silicon Pixel Readout for TPC

J. Timmermans
R. Uwe

- Timepix chip with 20 micron Amorphous silicon protection
  - works stably even when discharge
  - CERN beam test
- In progress
  - Alternative grid structures: twin grid – separate high-gain region from anode
  - Optimize protection / signal
  - Scale up
- Studies of Triple GEM with timepix

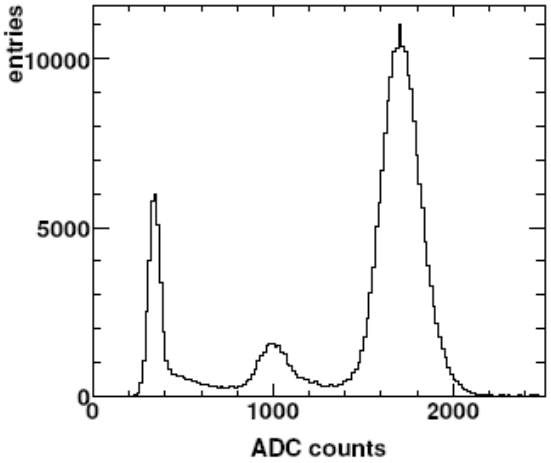




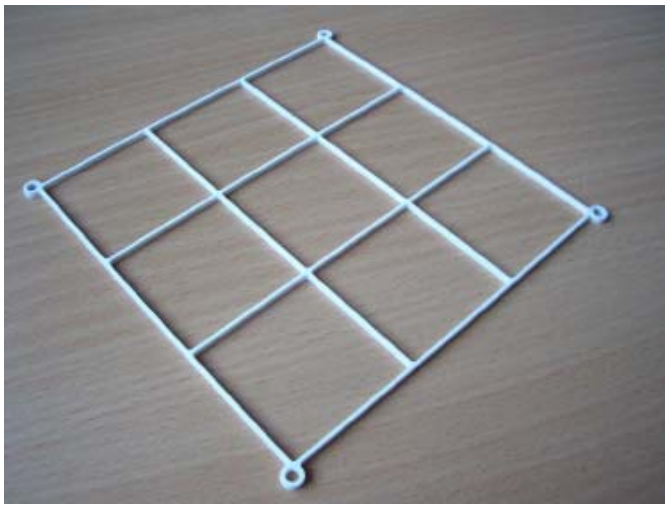
GEM Support

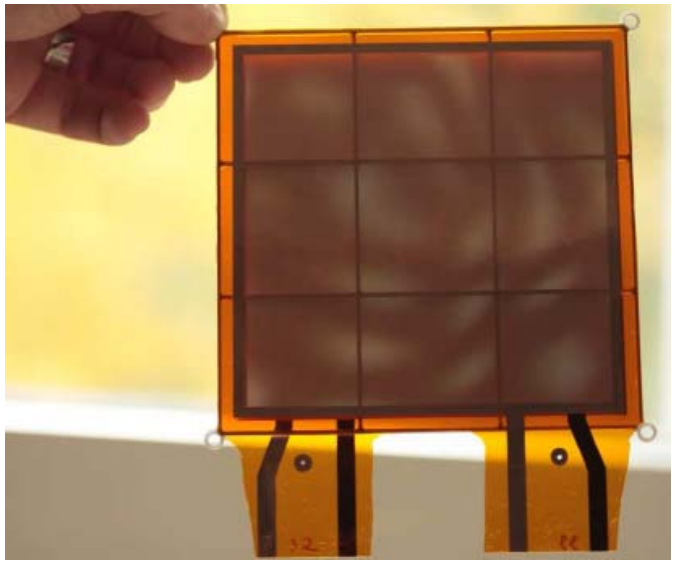
L. Hallermann

- Flatness affects gain variation
  - 380 μm variation in flatness ± 6% in gain
- GEM support
  - Ceramic material



370 V over both GEMs

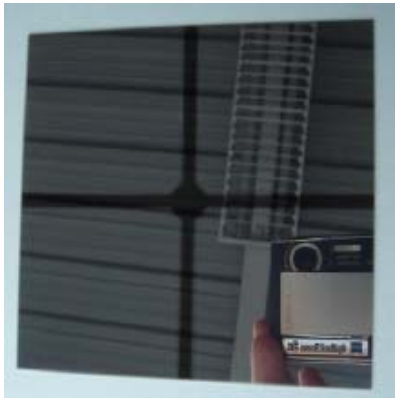




SiLC Tracker

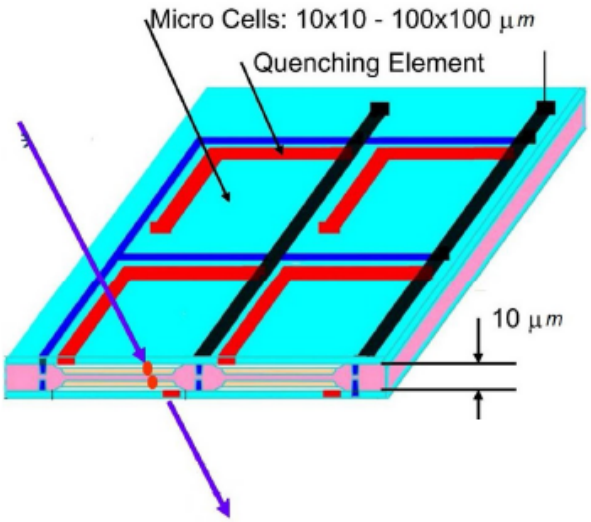
A. Navarro

- HPK 6” delivered end of 2007



- Short term
  - single sided sensor
  - edgeless detector from Canberra
  - thin detector with HPK
  - 3-D planar – started testing

- Longer term - pixel technology
  - DEPFET
  - Low material, high-gain 10^6
  - 3-D pixels and 3-D Vertical interconnect

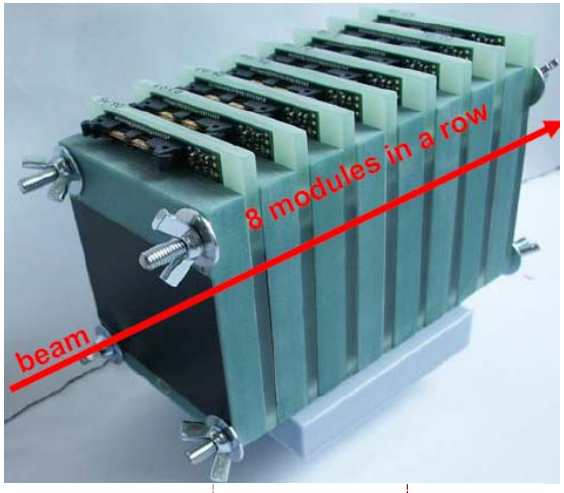


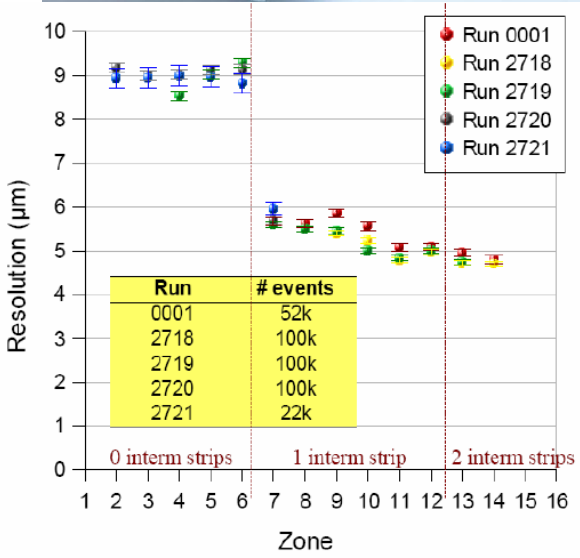
SiLC Tracker

A. Navarro
S. Haensel

- Sensors
  - HPK – 1 intermediate strip improves resolution from 9 → 5 micron
  - new 3D pixel – breakdown mode
- Electronics
  - FEE: 130nm -> 90 nm
  - FE chip direct connection to sensor by bump bonding
  - 3D Vertical integration

SiLC Beam Test

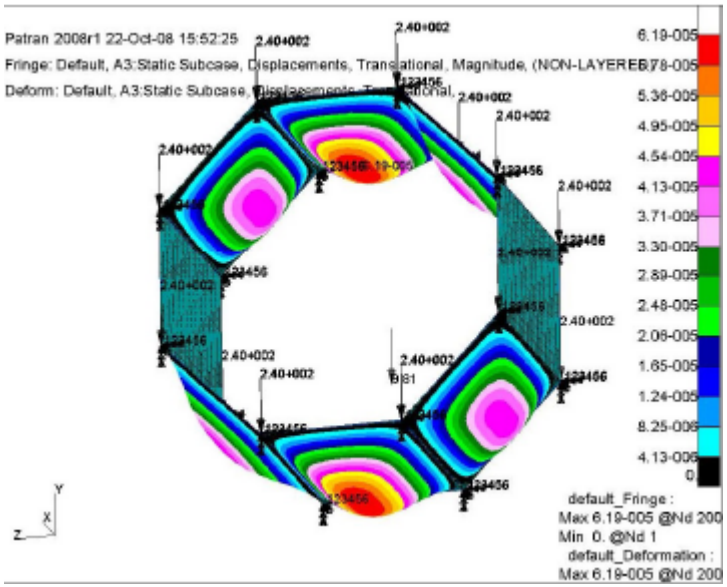




SiLC

A. Navarro

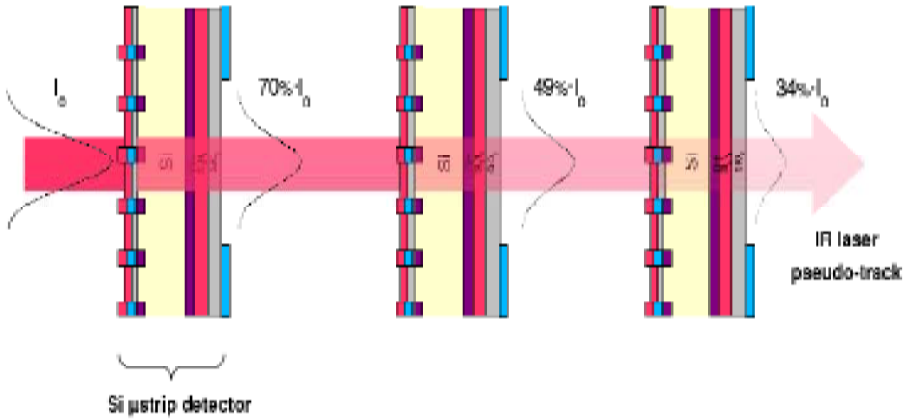
- Mechanics
  - Alignment – using silicon trackers, single layer
  - light support structure
  - test beam – 3-D table
- Integration
  - ILD integration of SiLC tracker
- Driving schedule
  - test beam
  - LOI
- Driving parameters
  - lightness and robustness
  - simplicity for construction

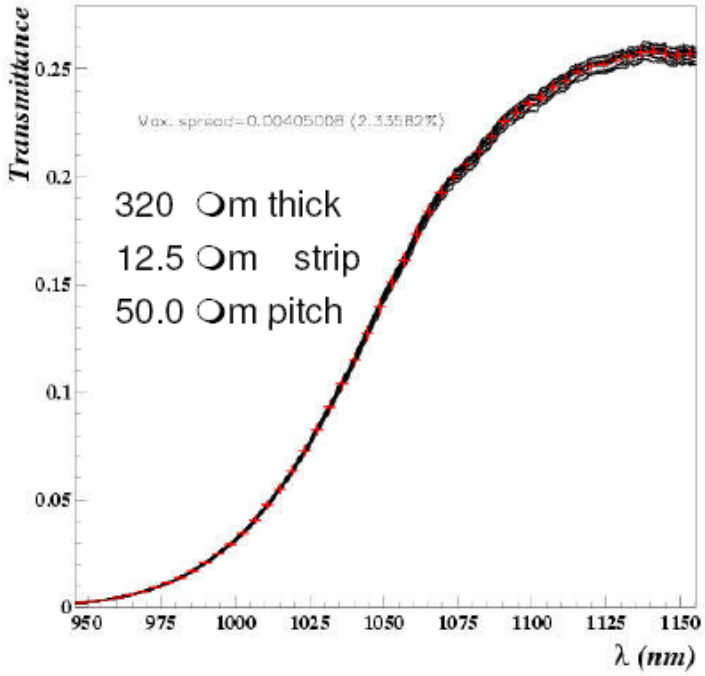


SiLC Tracker Alignment

A. Jimeno

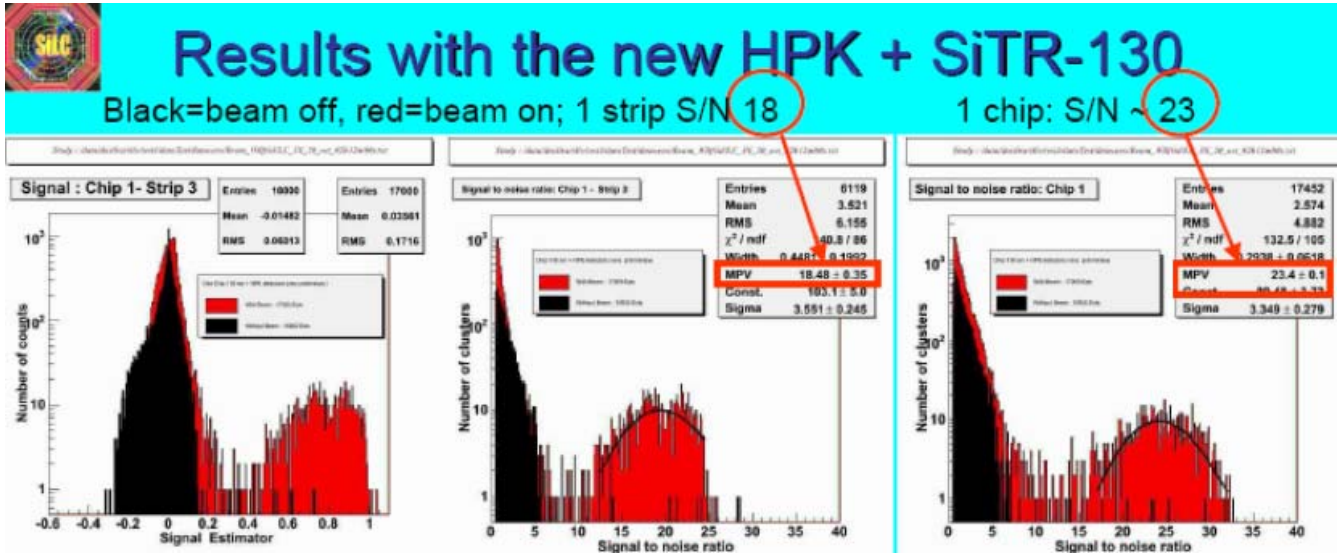
- Laser alignment
  - Used in AMS and CMS
- Problem is transmittance
  - strip width reduction
  - new transparent materials
- Accuracy currently 4 microns
  - Single layer





SiLC Tracker Readout Chip

A. Navarro



- 88 channel fully programmable version in hand
- Next steps
  - thin
  - 90 nm process
  - CLIC
  - bump bonding to sensor

Silicon Pixel Tracking

C. Damerell

- 5 layers, 5% X_0
  - 50 micron pixels
  - Occupancy: 10^{-4}
- 50 Gpixels
  - Integrate signals through 1 train or
  - Time slicing – integrate several bunches
  - ISIS technology – low power

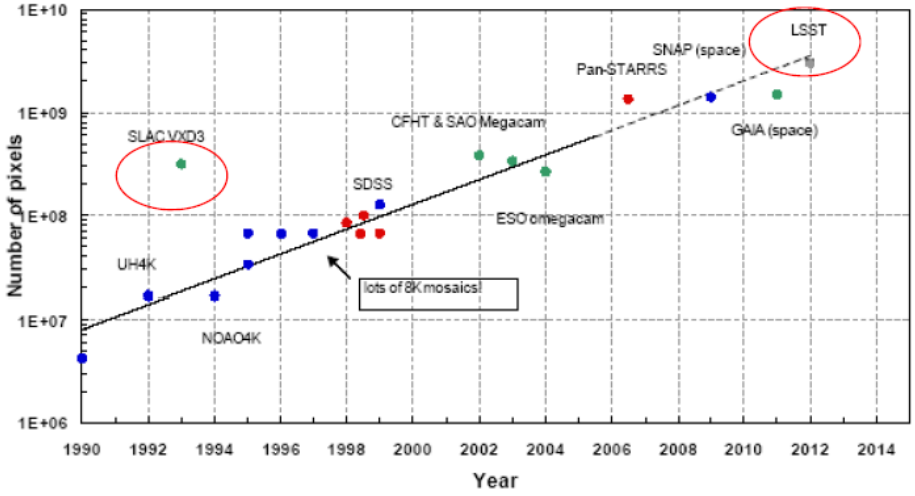


Illustration of focal plane sizes, from Luppino/Burke 'Moores' law

Focal plane size doubles every 2.5 years