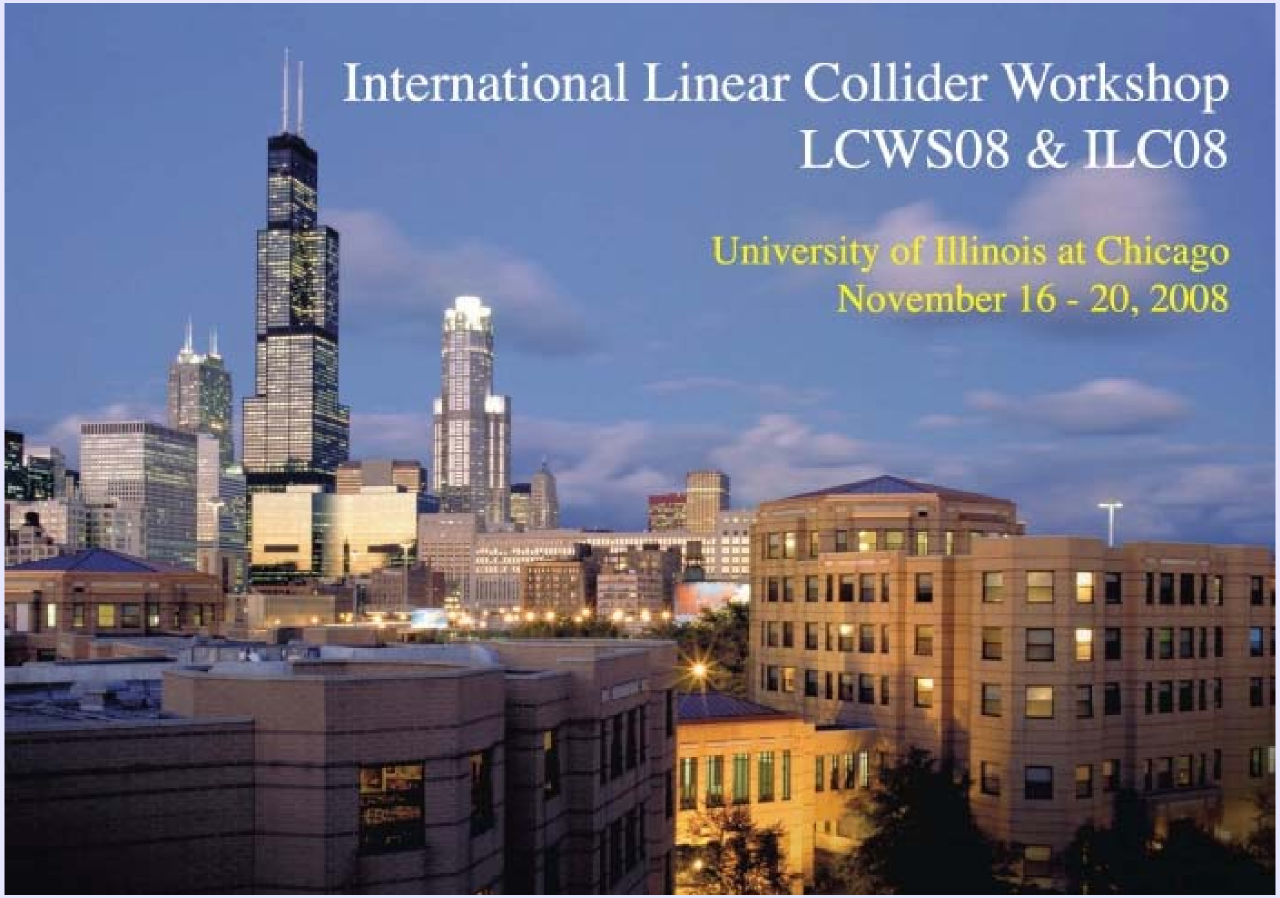
Report on the DAQ and GDN Activities



G. Eckerlin
November 20, 2008

Report on the DAQ and GDN Activities

- Activities on Front End Readout
  - Calorimeter readout à la CALICE
  - KPIX readout
  - Silicon readout (SiLC, Vertex)
- Activities on DAQ architecture
  - CALICE DAQ
  - SiD DAQ
  - SiLC DAQ
- GDN activities and experience
- ATCA for physics detectors and accelerators

Front End Readout Activities

Tuesday 18 November 2008

LCWS: Data Acquisition and Global Detector Network - SCE 613 (08:30-10:10)

- Conveners: Eckerlin, Gunter; Yasu, Yohsiji; Haller, Gunther

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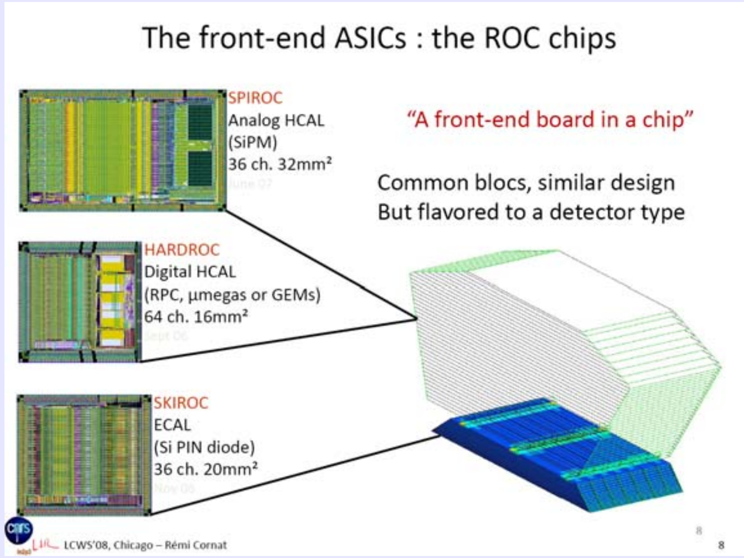
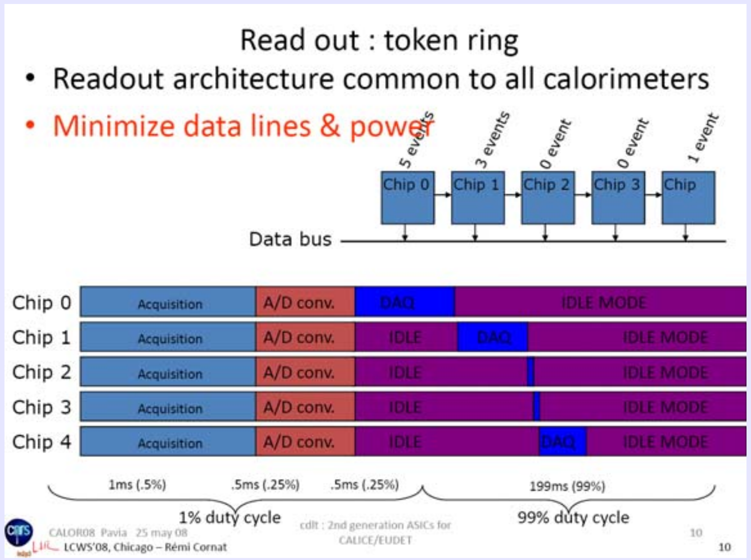
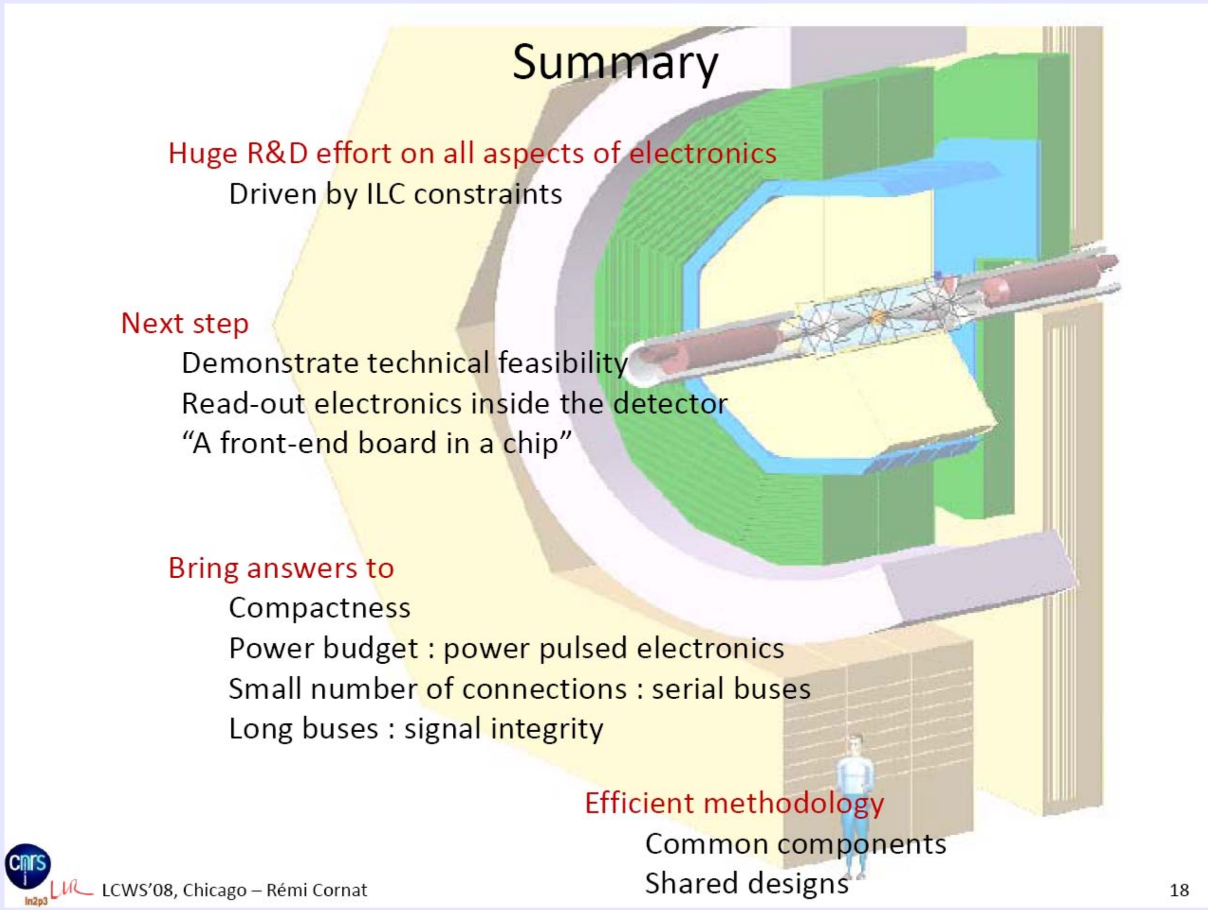
Front End Readout à la CALICE (Remi Cornat)





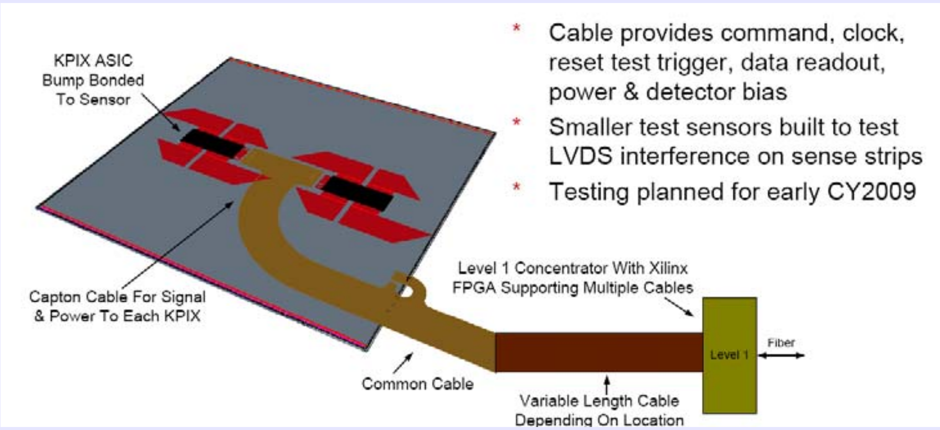
Getting very close to real design
3 different ROC designs for AHCAL, DHCAL, ECAL
Common readout architecture for all calorimeters



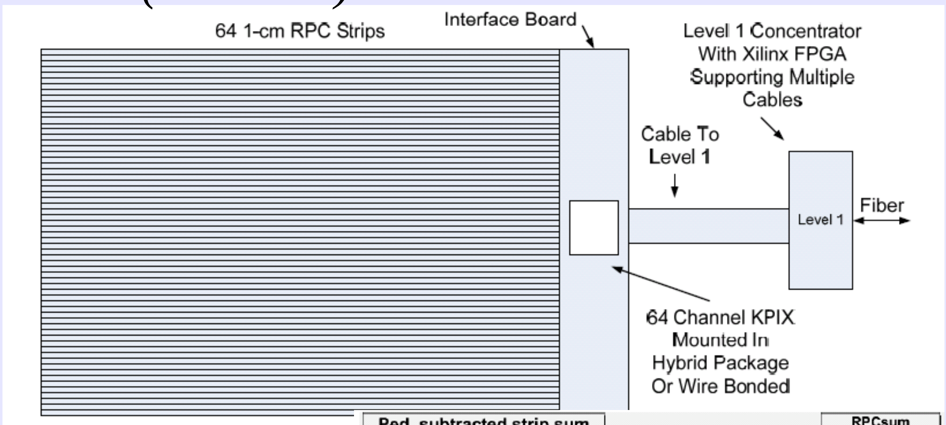
KPIX Readout for SiD (Rayn Herbst)

KPIX ASIC : multi channel chip for amplification, self triggering, digitizing and storage,
1024 channels, 2 gains, 2 thresholds, 4 hits per channel, 13 bit ADC, <20uW/ch (power cycling)
Applications for SiD ECAL, Tracker, HCAL and Muon detectors
Currently 64 channel prototype will go to 256 and then to 1024 channels

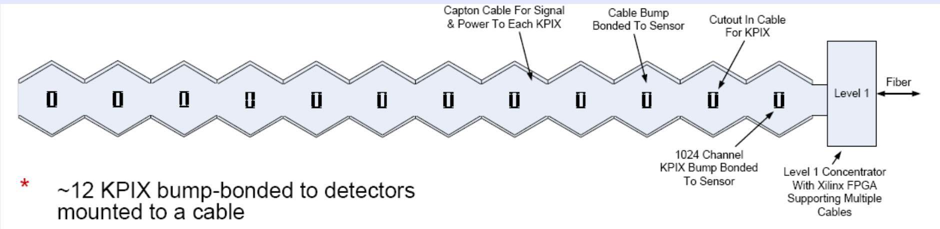
Tracker



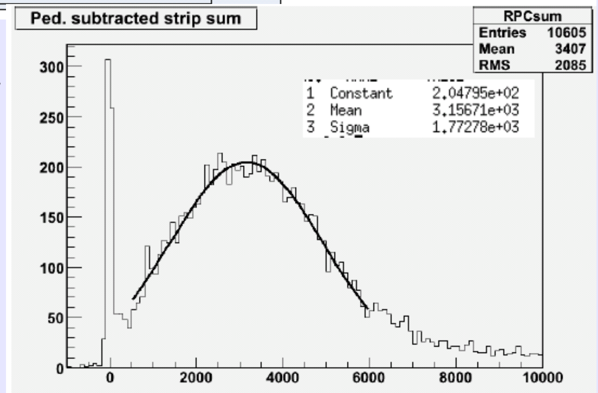
Muon (or HCAL)



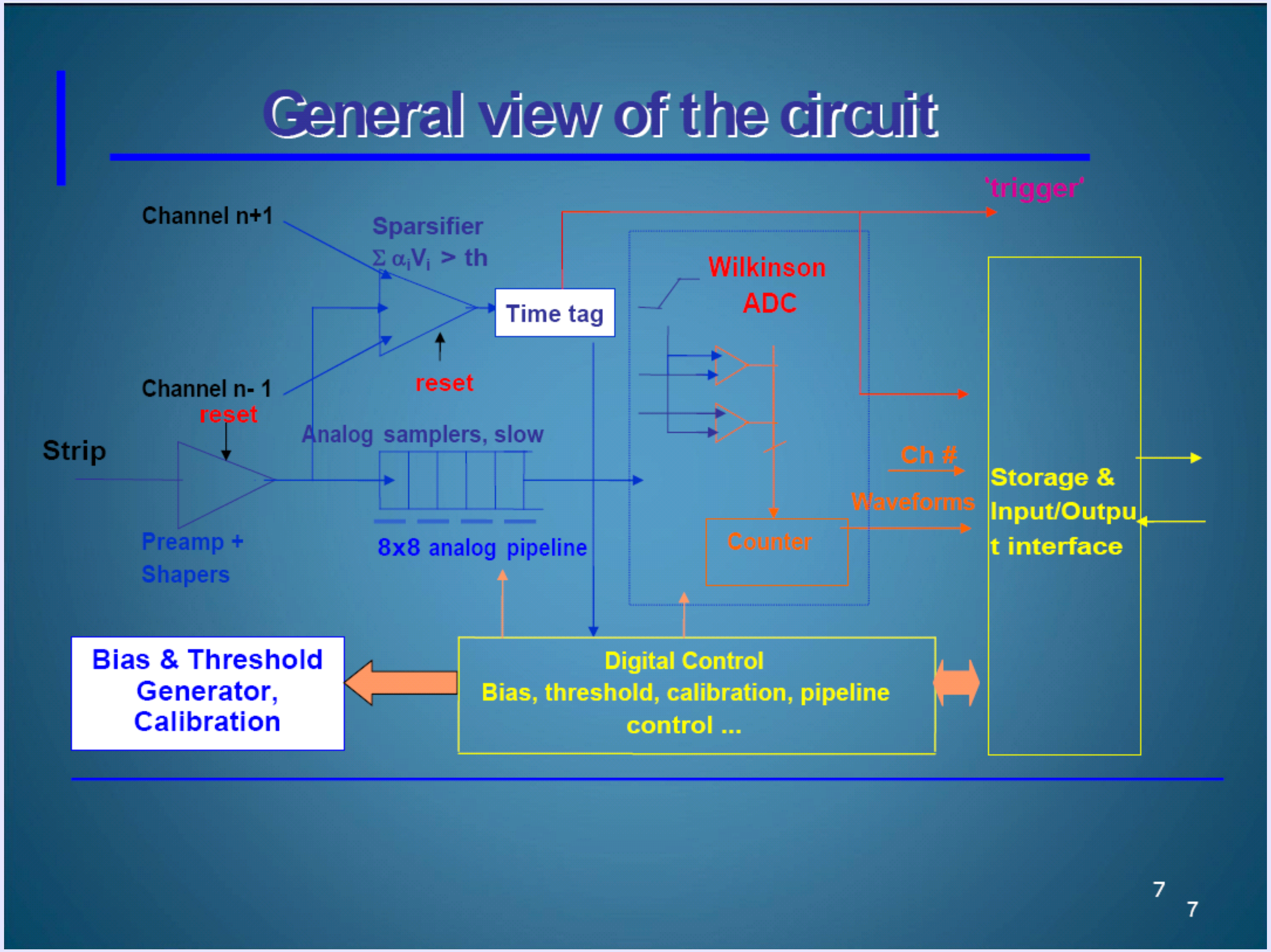
ECAL



cosmic data from RPCs



Silicon tracking Front End (Aurore Savoy-Navarro)



L1 : on sensor
full readout on chip

Preamp + shaper
Pipeline
Self triggering
ADC
Digital storage
Input/output interface

DAQ System Architectures

Tuesday 18 November 2008

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DAQ à la CALICE (Valeria Bartsch)

DAQ architecture

Detector Unit: ASICs

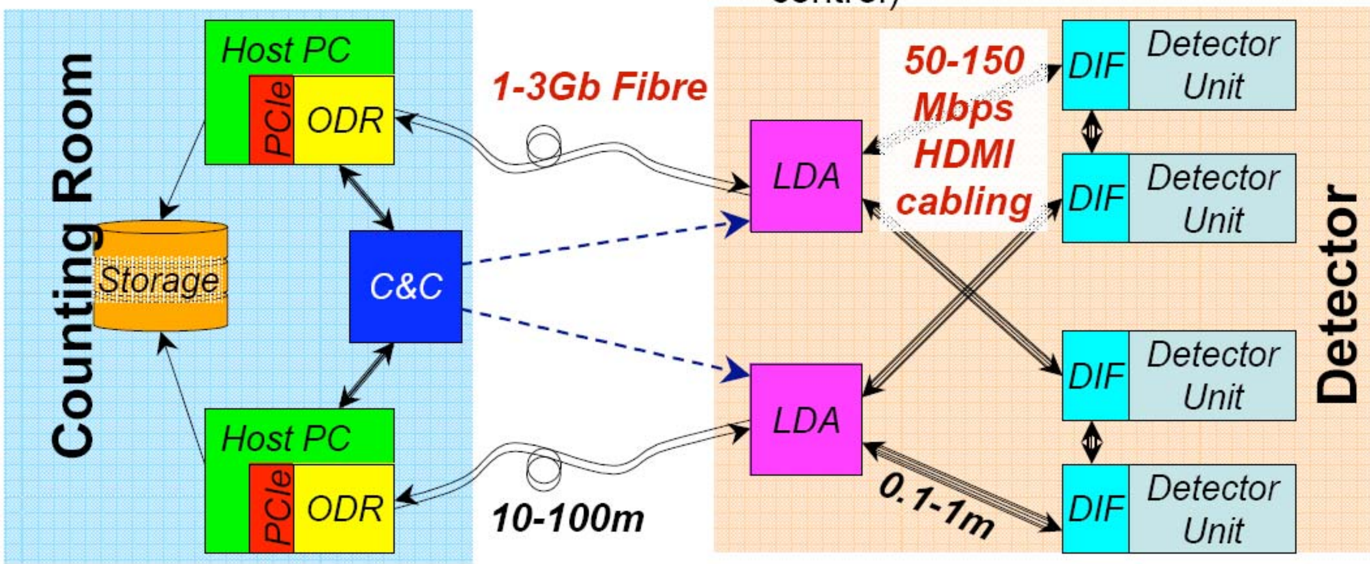
DIF: Detector InterFace connects Generic DAQ and services

LDA: Link/Data Aggregator – fanout/in DIFs and drives link to ODR

ODR: Off Detector Receiver – PC interface for system.

CCC: Clock & Control Card: Fanout to ODRs (or LDAs)

CONTROL PC: DOOCS GUI (run-control)

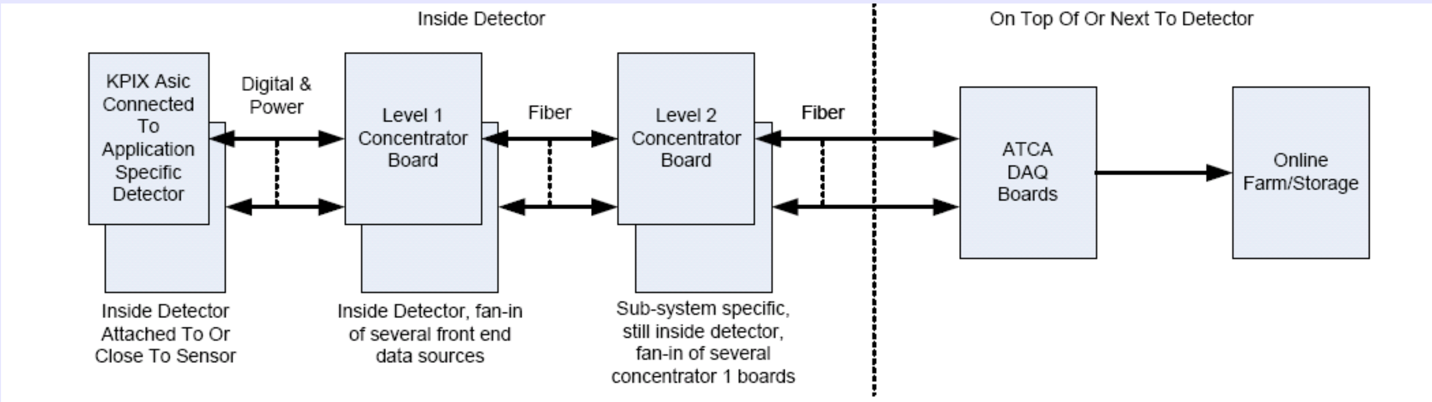


Full DAQ architecture from detector front end to storage

Objectives :
use commodity hardware
as generic as possible
standard protocols/interfaces
scalability
flexibility

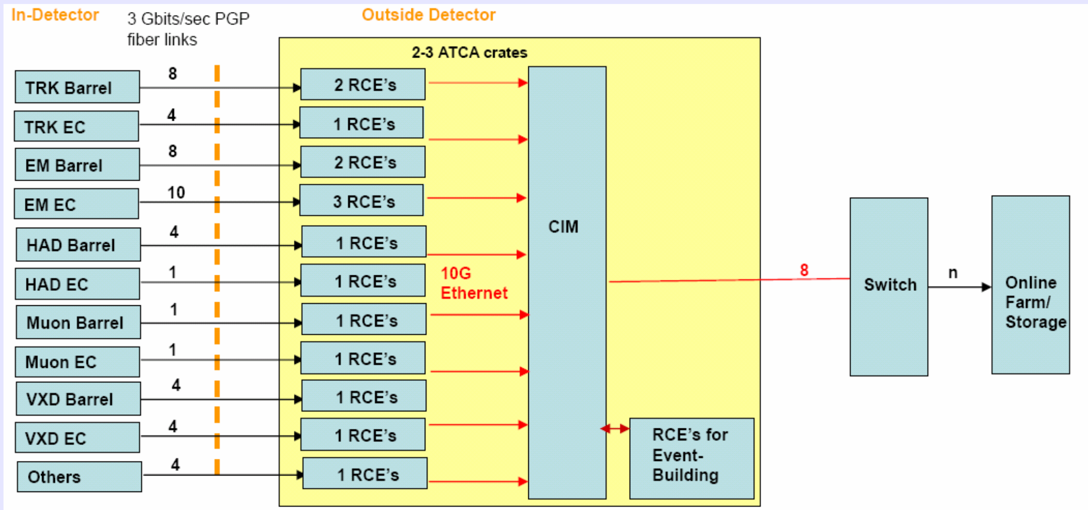
goal is to be ready by 2009

SiD DAQ Architecture (Gunther Haller)



XPIX on or close to sensor
L1 Control/Concentrator
L2 Concentrator if needed
ATCA based DAQ

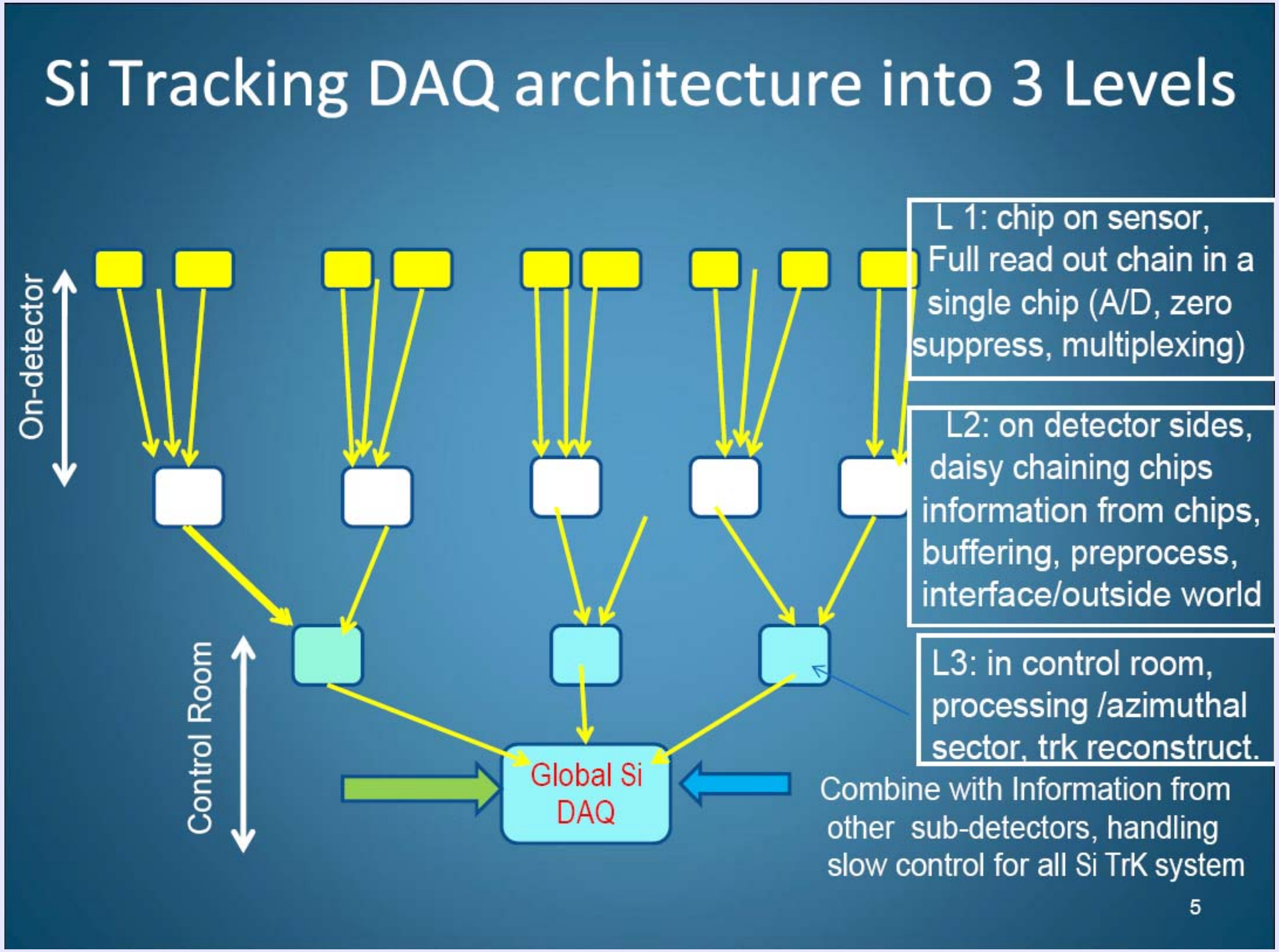
Sub-System	Mean # Hits/Train	#of bytes/hit at level 0	Bandwidth (bits/sec) (5 trains/sec)
Tracker Barrel	$2*10^7$	18*	15G
Tracker Endcap	$8*10^6$	18*	6G
EM Barrel	$4*10^7$	8	13G
EM Endcap	$6*10^7$	8	20G
HAD Barrel	$2*10^7$	8	6G
HAD Endcap	$4*10^6$	8	1.3G
Muon Barrel	$1*10^5$	8	32M
Muon Endcap	$1*10^5$	8	32M
Vertex			10M (dominated by layer 1)
LumCal/BeamCal	tbd		tbd
Total			~60G



total bandwidth : 60Gbit/sec

full readout into 2-3 ATCA crates
probably at least 1 per subsystem (partitioning)

Silicon tracking DAQ (Aurore Savoy-Navarro)



3 Level DAQ approach for silicon strip trackers

again same approach :

L1 : on sensor
full readout on chip

L2 : on/near detector
concentrating/processing

L3 : off detector
online tracking including combining with other detectors

GDN Activities and Experience

Tuesday 18 November 2008

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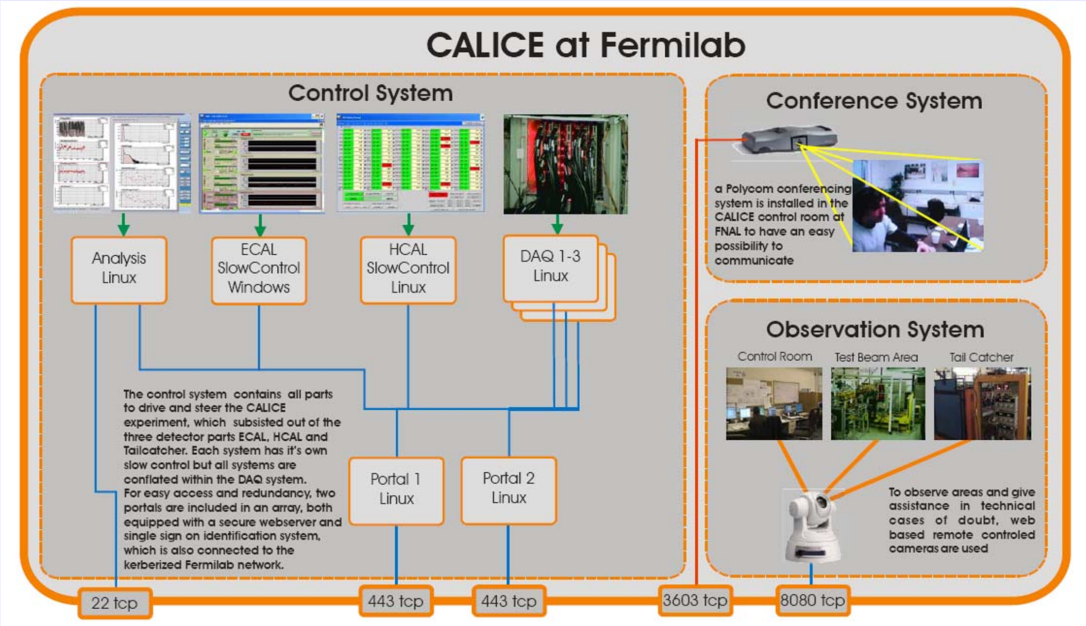
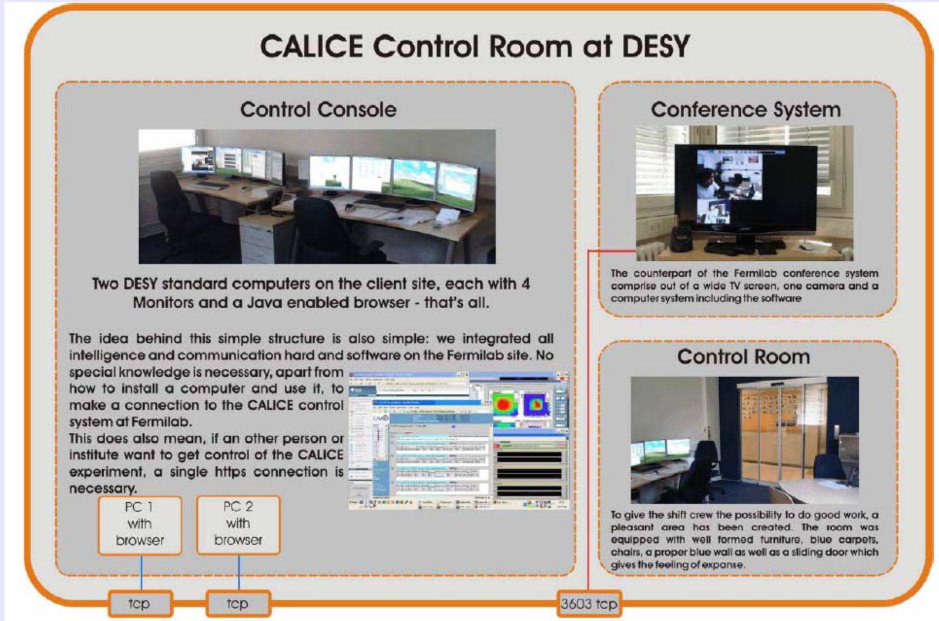
CALICE GDN experience (Sven Karstensen)





Remote operation of CALICE test beams at CERN and FNAL :
dedicated ROC at DESY with : 2 PCs 4 screens each and a Video Confernecing system
control via internet using : HTTP, Sun Secure Desktop
communication via internet using ESnet and WEBcams with HTTP interface (remote controlled)
Successfully used for Test beams
Not shown at this workshop (but worth to note):
CMS just finished 4 weeks of cosmic running with remote DQM shifts done from the CMS ROCs at CERN, FNAL and DESY

ATCA for Detectors and Accelerators

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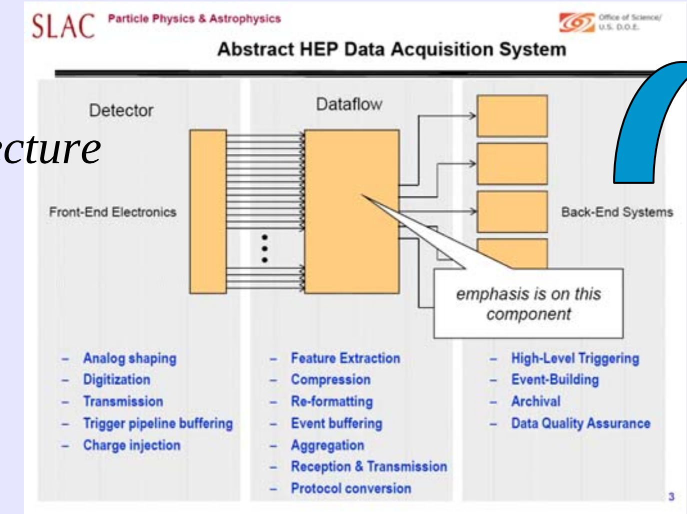
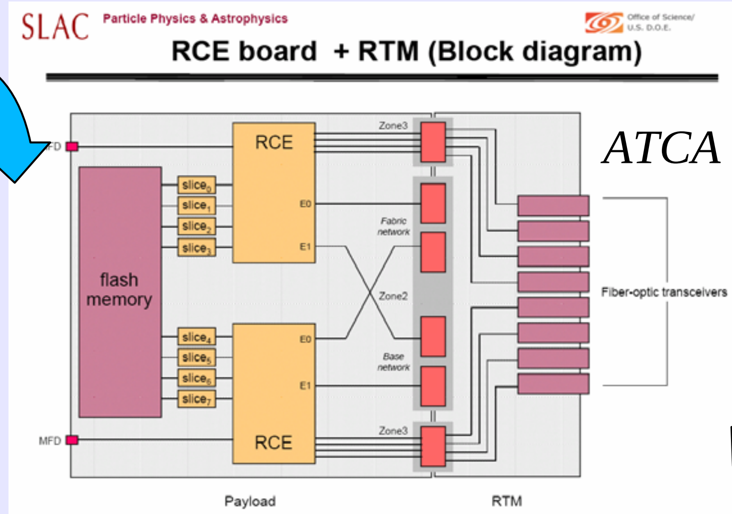
SiD ATCA DAQ System (Matt Weaver)

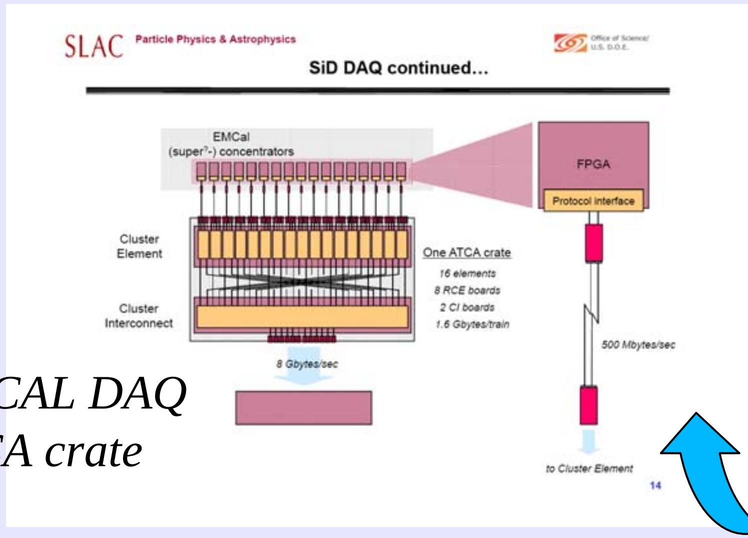
DAQ architecture

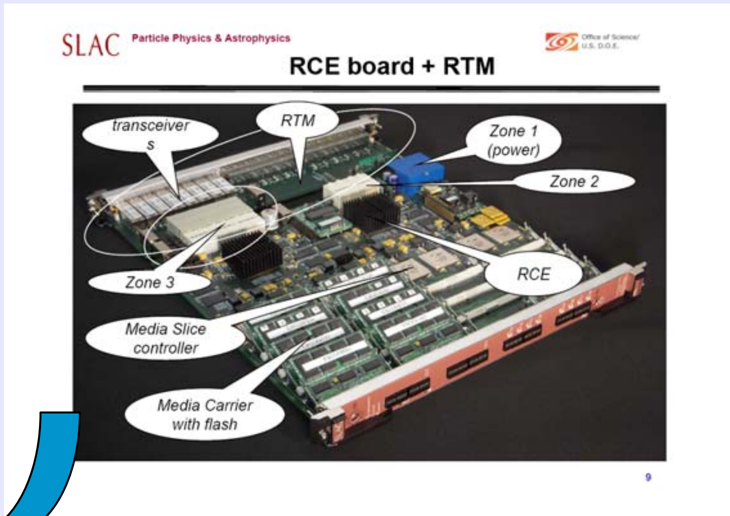


ATCA board diagram



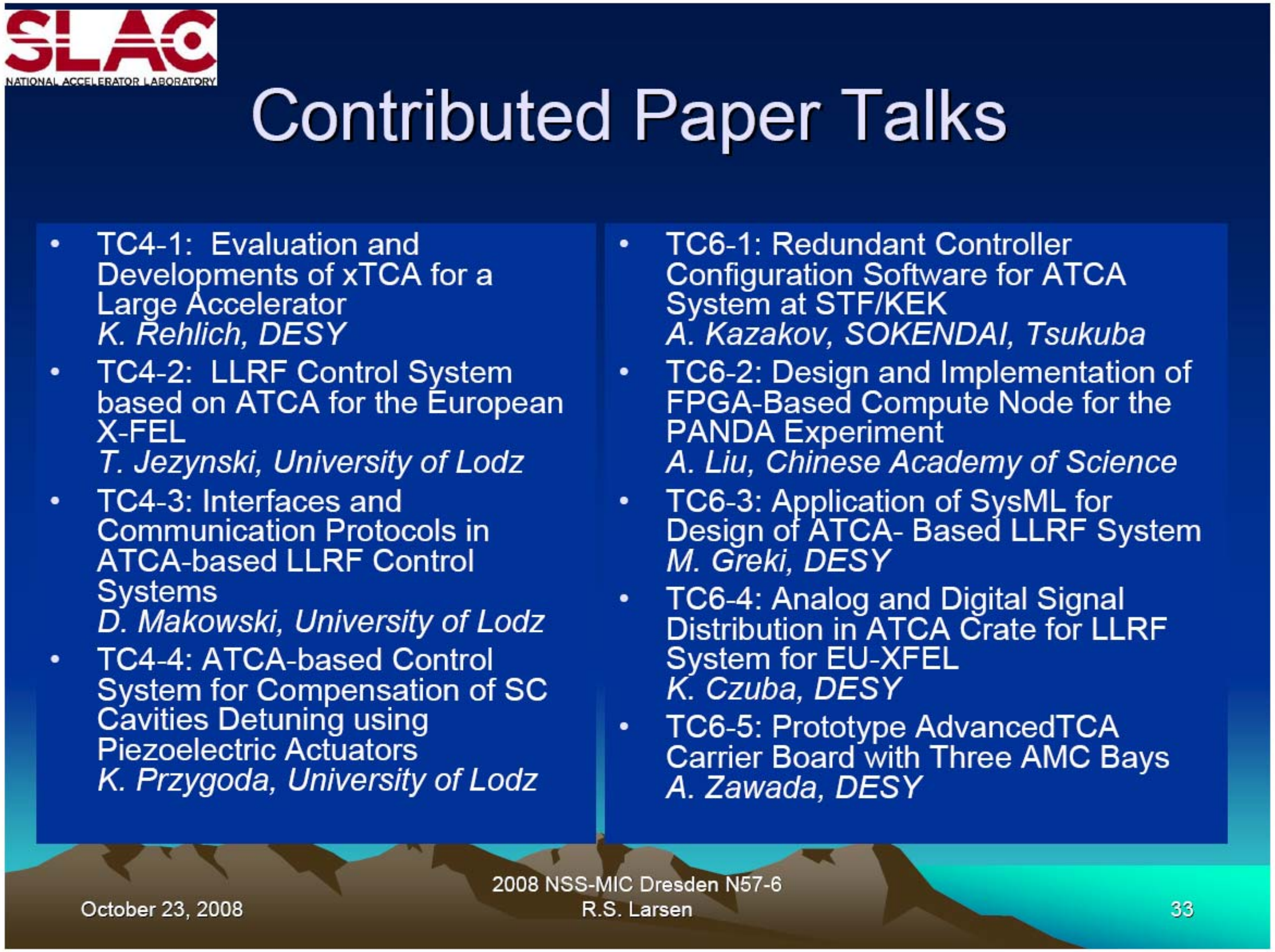
realization





Possible ECAL DAQ with 1 ATCA crate

2nd ATCA Workshop for Physics (Ray Larsen)



2 days workshop
IEEE NSS-MIC
Dresden Oct. 2008

Industry tutorials
Design experience
Physics Standards
Industry Demonstrations

Contributed papers
(from Labs and Industry)

7 industry presentations

8 talks on accelerator
and detector applications

2nd ATCA Workshop for Physics (Ray Larsen)

Physics Standards Requirements

- Hardware – Robert Downing
  - xTCA platform has many advantages for physics
  - Propose developing down selection options into an xTCA Physics Profile
  - Follow SCOPE methodology, Gap Analysis
  - Candidate areas to narrow choices:
    - Protocols – Ethernet & PCIe
    - Rear IO for ATCA, AMC; designate AMC extra lanes for IO; possible options with stacking connectors
    - Recommend IO connectors – copper, fiber, high BW
    - Recommend board interconnect, routing design rules
    - Cooling options for crates, rear transition area (RTM), racks
    - Redundancy options to optimize to application
      - High BW, throughput for concentrated DAQ vs. low BW, long distance controls networks

October 23, 2008 — 2008 NSS-MIC Dresden N57-6, R.S. Larsen — 20

Proposal to define a xTCA physics profile

Protocols
Read I/O
Connectors
Cooling (crates, racks)

Draft document available

2nd ATCA Workshop for Physics (Ray Larsen)

Worldwide Study of the Physics and Detectors for Future Linear e+ e- Colliders

SLAC NATIONAL ACCELERATOR LABORATORY

Standards Collaboration Discussion

- Possibility of forming xTCA for Physics Working Groups under PICMG, SAF and SCOPE presented (R. Larsen)
  - Many real issues identified, need addressing if labs to achieve useful level of *interoperable* hardware-software-firmware standard solutions
  - Standards participation by labs encouraged
  - Fees for lab modest to none
  - Draft xTCA Profile for Physics document reviewed
  - Audience encouraged to consider supporting, collaborating
  - Possible Physics WG Model block diagram is attached
- Follow-up
  - Develop interest group mailing list
  - Collaborate on planning future tutorials, workshops
  - Investigate web tools for meetings

October 23, 2008 — 2008 NSS-MIC Dresden N57-6 — R.S. Larsen — 37

ATCA considered by accelerator and detector for DAQ and controls

We may need to adjust or down select standard to our needs

If you are interested contact Ray Larsen or come to the next workshops :

May 09, IEEE RT Bejing
Summer 09, Europe (TBD)
Oct 09, NSS-MIC Orlando

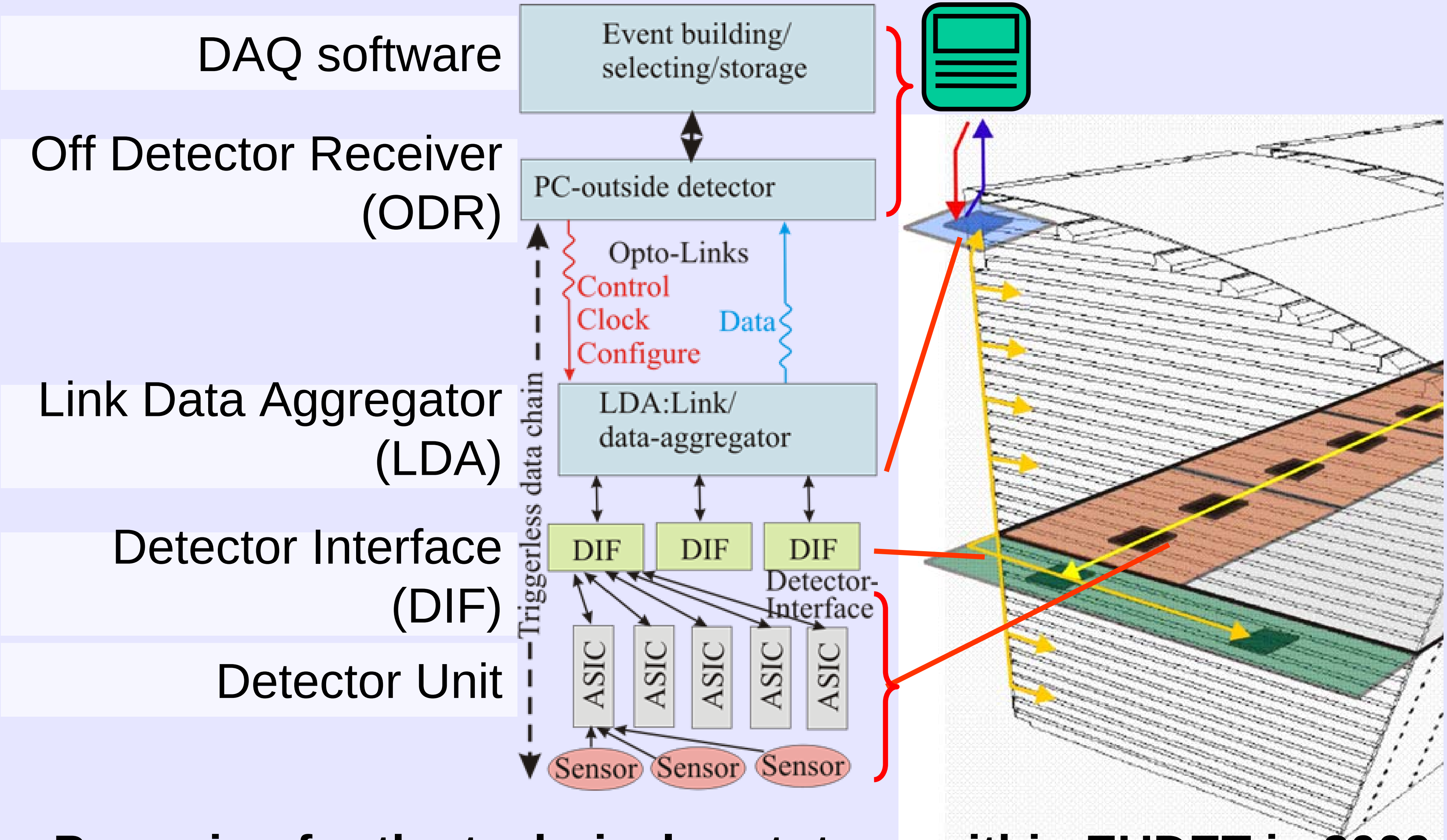
Personal Remark

- Front end of technical prototypes get closer to ILC design
  - Well advanced front end designs for CALICE/EUDET, SiD and SiLC
  - Encouraging to see common interfaces & standards for different detectors
- Well advanced DAQ architecture have been developed
  - All have similar approach : on/near sensor chips, on detector concentrator
  - Examples of ATCA based DAQ systems look promising
- Still to be done
  - address further common issues (calibration, commissioning, detector ctrl)
  - need to think about online data formats (offline software expects LCIO)

Thank you !

Backups

ILC Calorimeter DAQ (Valeria Bartsch)



Preparing for the technical prototype within EUDET in 2009

EUDET DAQ will use DOOCS (slide from ECFA WS, Tao Wu)

Application layer

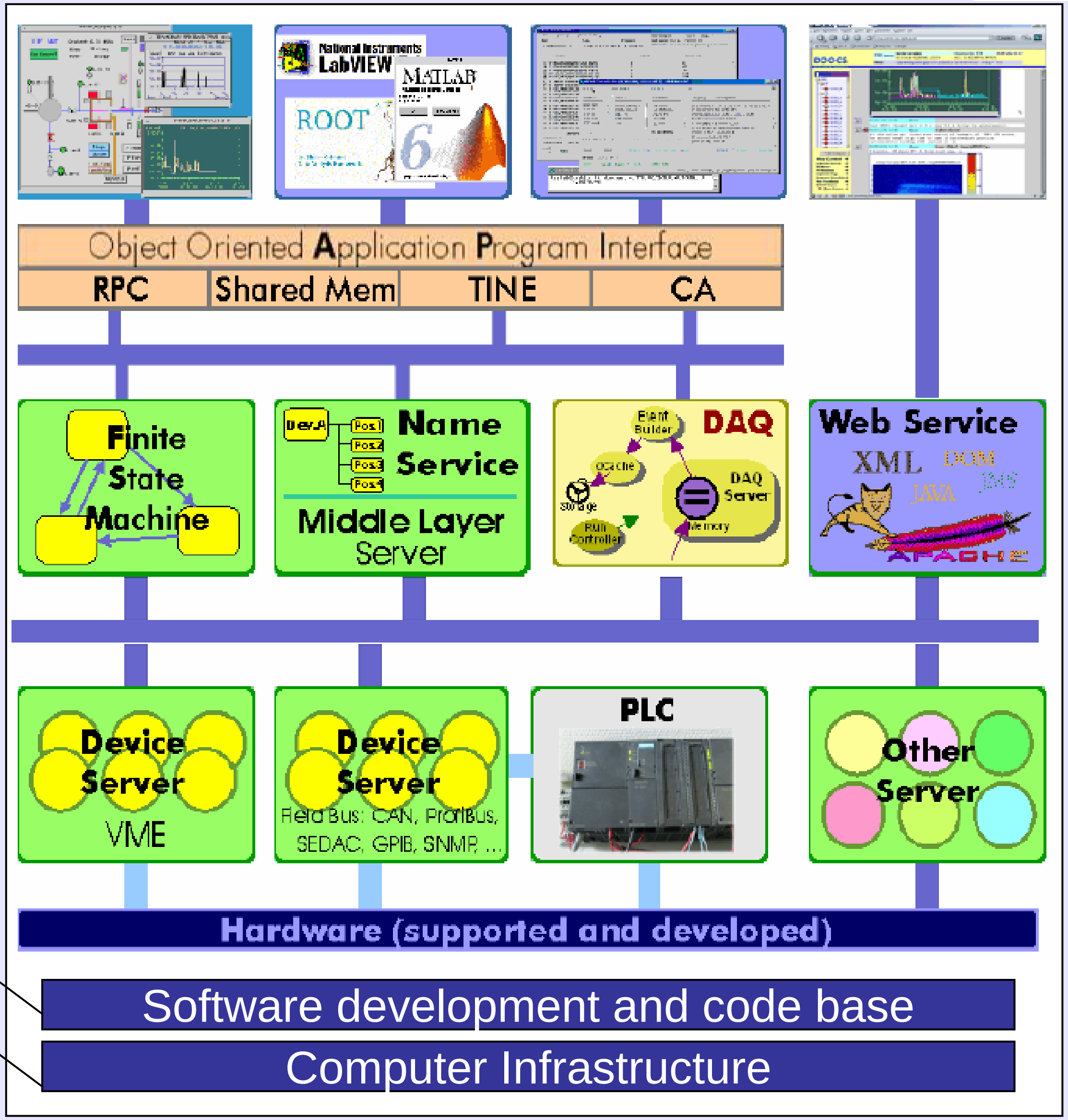
Communication

Middle layer

Device layer

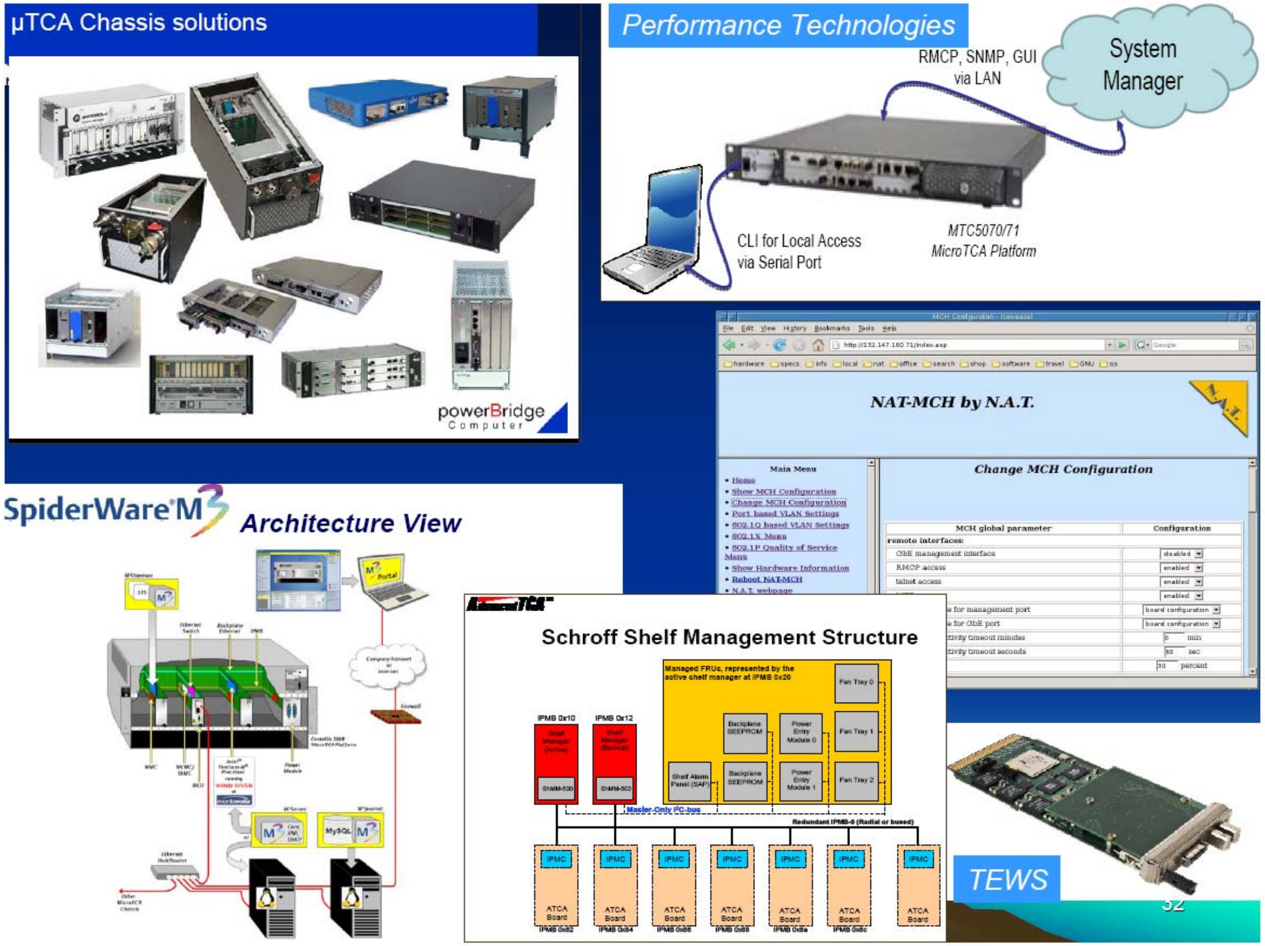
Software Libs

Sun/Linux Cluster



The Distributed Object Oriented Control System will also be used for XFEL Control and DAQ.

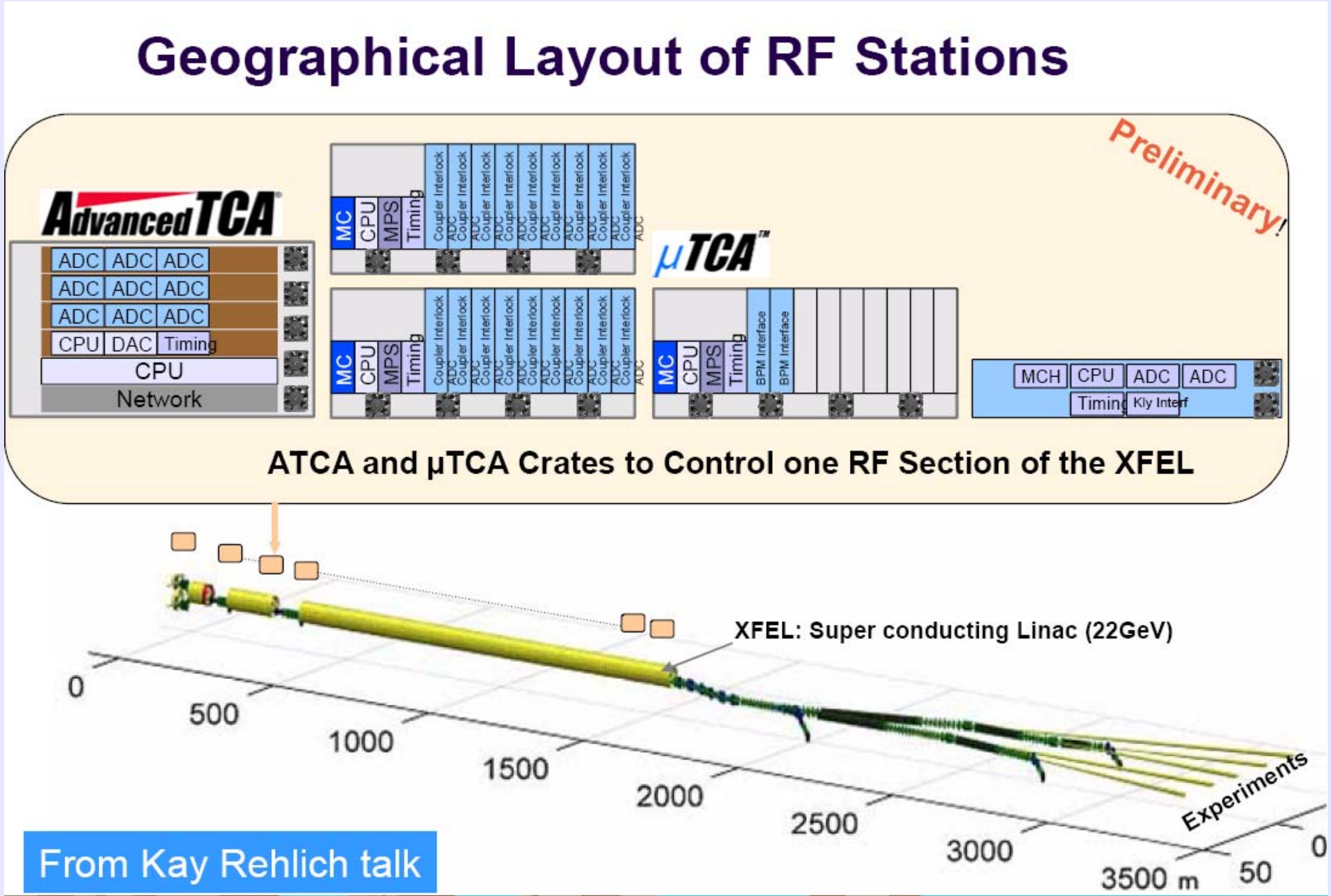
2nd ATCA Workshop for Physics (Ray Larsen)



Many ATCA solutions from Industry :

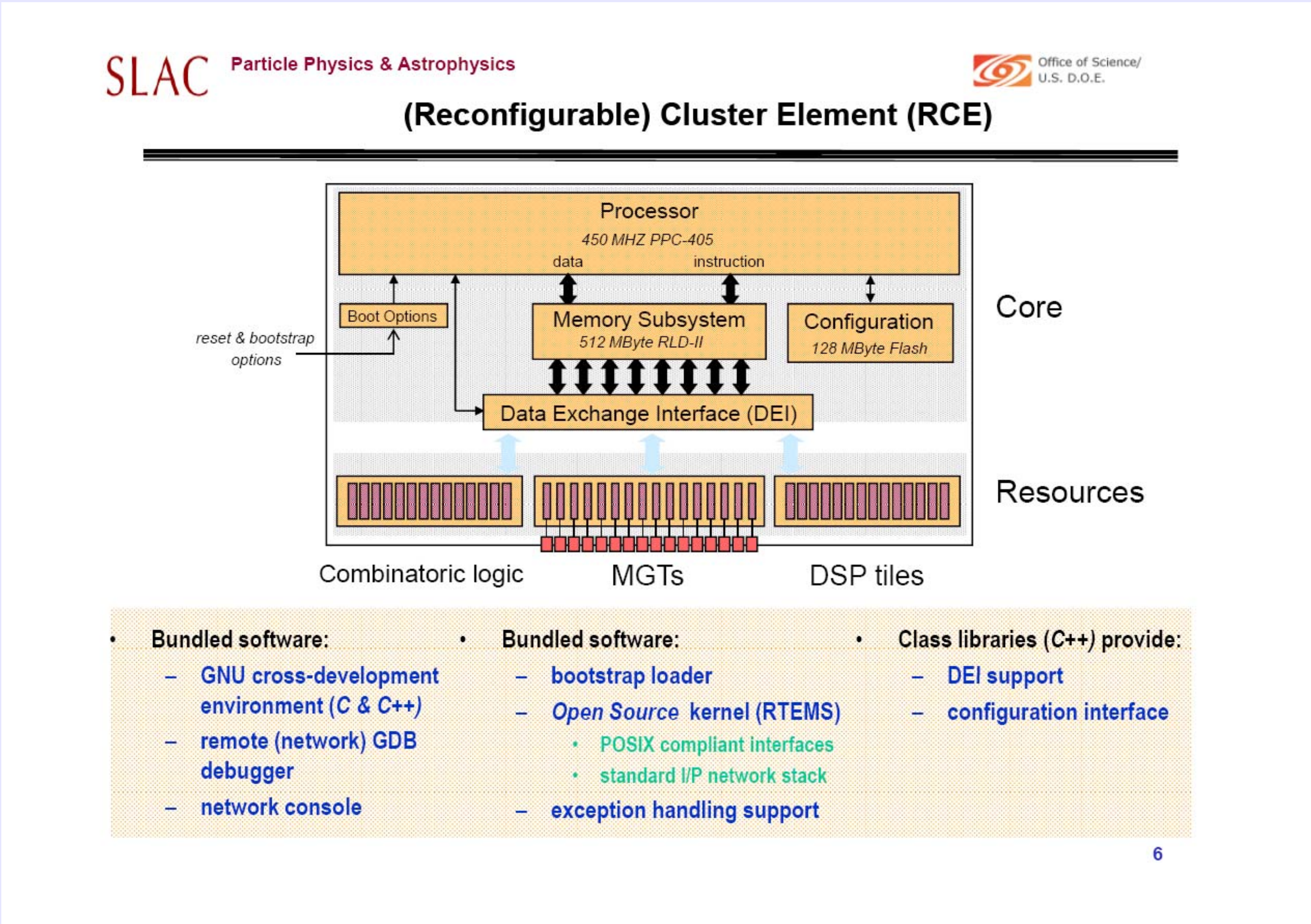
both hardware and software

2nd ATCA Workshop for Physics (Ray Larsen)



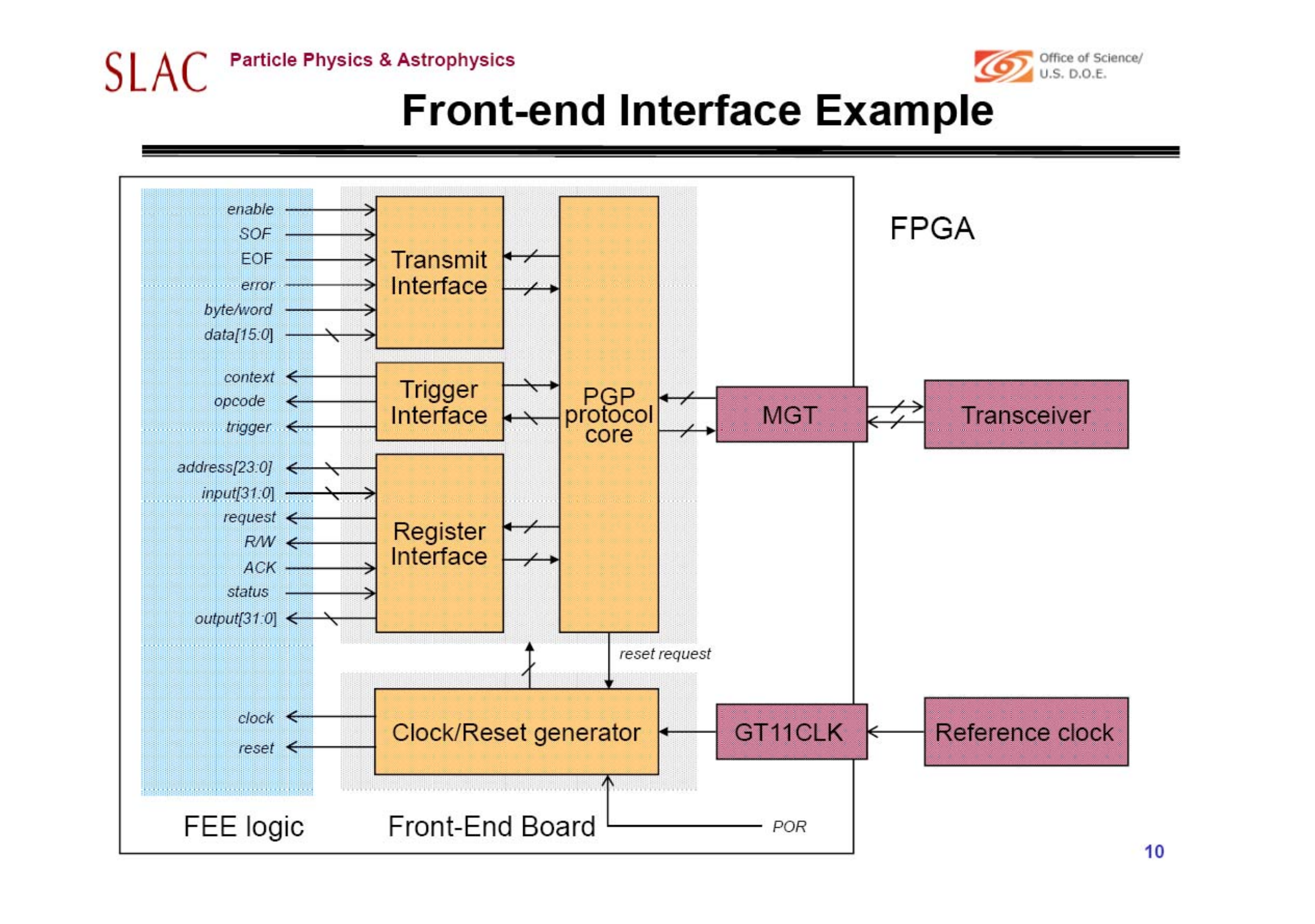
ATCA for XFEL

SiD ATCA DAQ System (Matt Weaver)



Block diagram of the RCE

SiD ATCA DAQ System (Matt Weaver)



Front End Interface for SiD ECAL