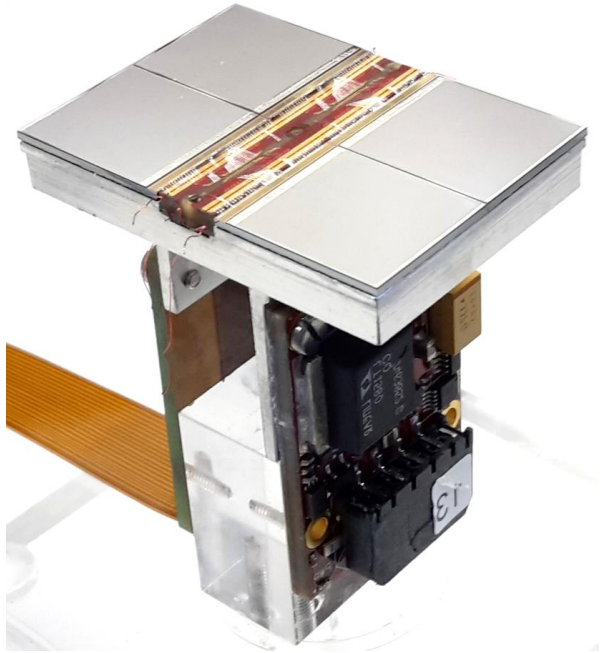
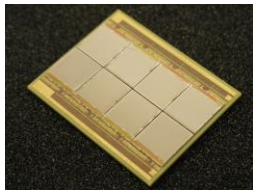
R&D for a Pixelated Time Projection Chamber

Yevgen Bilevych, Klaus Desch,
Harry van der Graaf, Fred Hartjes,
Jochen Kaminski, Peter Kluit,
Naomi van der Kolk,
Cornelis Ligtenberg,
Gerhard Raven, and
Jan Timmermans

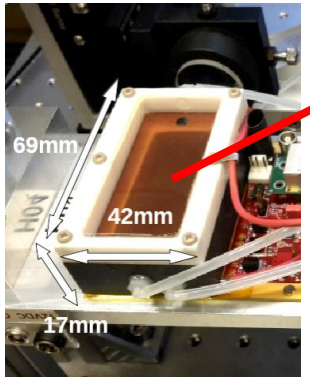


LCTPC workshop follow up

Pixel TPC

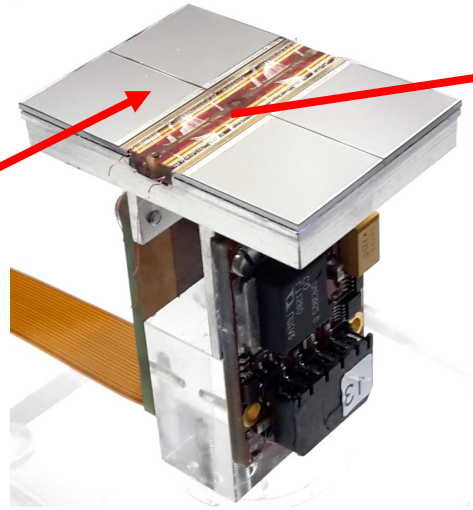


(Octopuce)



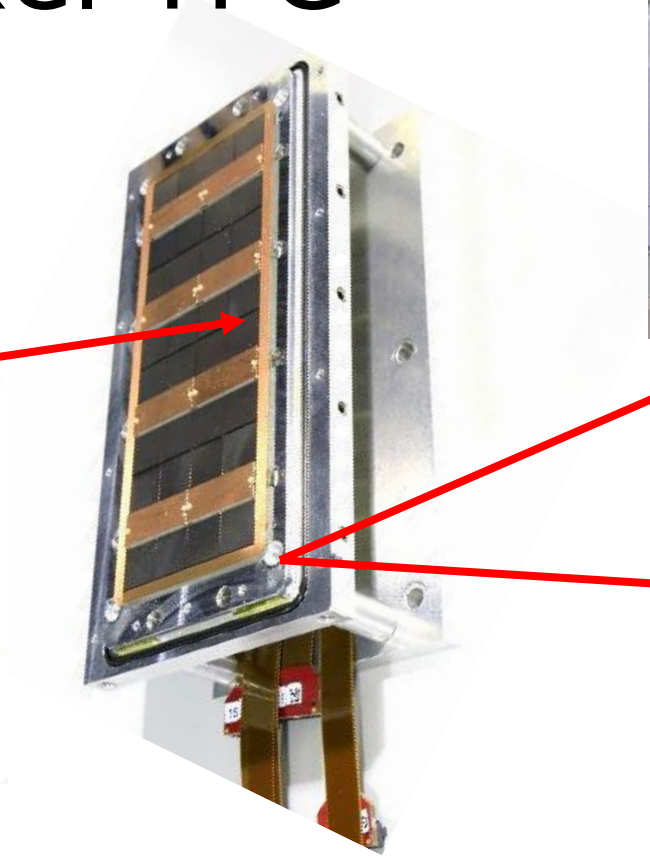
(TimePix1)

(2007-14)



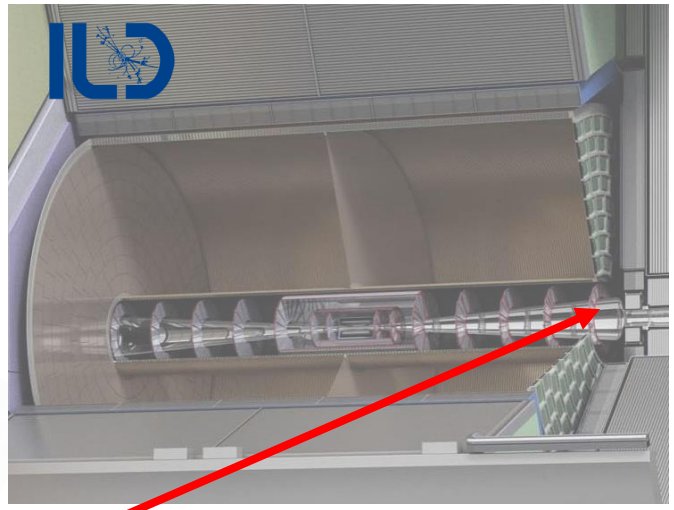
TPX3 chip

2017



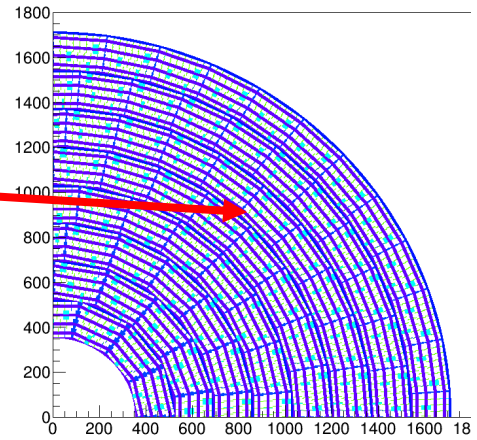
Quad

2018



Module

2019



TPC plane

R&D topics: power consumption

- Current TPX3 chip has 256x256 channels and a surface of 1.41 × 1.41 cm^2
- Power consumption ~2W/chip; this means 30 μW/channel
- A full pixel TPC in an ILD like detector will have a total surface 160 000 cm^2
- For full coverage one needs 80 000 chips
- With the current TPX3 chip one reaches about 60% coverage
- For the pixel TPC the total power is 160 kW (so 80 kW per endcap)

- R&D @ IHEP based on 0.5x0.5 mm^2 pixels and electronics uses a power of 2.4 mW/channel.
  - For a surface of 160 000 cm^2 one has 64 M channels and 153 kW power

power consumption for TPX4

- The most elegant solution to reduce the power consumption is - according to Nikhef electronics engineer V. Gromov - by
  - reducing the currents (gain) in the pre-amplifier and discriminator; this will affect (worsen) the time resolution. An option to reduce the digital power is to lower the clock frequency to e.g. 10-25 Mhz
  - Unfortunately, reducing the nr of channels does not help; increasing the nr of channels does help, because of the noise reduction (smaller pixels less noise).

- For the TPX4 chip the power in standard operation is 1 W/chip (0.5 W/cm^2)
- A special setting "low power mode" has been prepared for TPX4 reducing the power consumption by a factor of 5 (see next slide for the TPX4 settings).

R&D: low power mode TPX4

2. TestPulseCoarse and TestPulseFine: Refers to the TestPulse signal generated internally (see Section 20.2).
3. Dac_bits[4:0] (see Table 18.1): Bits to program the 5 bit threshold equalization DAC. All threshold adjustment bits and their inverted signals are programmed to logic 1 when the pixel is in the standby mode (PowerEnable=0).
4. DiscriminatorOutput : Discriminator output signal.

3.3. Digital to Analog Converters

Table 3.2 Table of DACs that control the analog front-end operation

BLOCK	DAC Name (type)	Bits	Flavour	Fast Timing Mode	High Flux Mode	Low Power Mode	Full Scale nominal
Preamplifier	VBiasPreamp (I)	8	I/N	500nA (85d)	500nA (85d)	100nA (17d)	1.45uA
Preamplifier	VCascPreamp (V)	8	V	750mV	750mV	750mV	1.2V
Preamplifier	VBiasLevelShift (I)	8	I/N	500nA (88d)	500nA (88d)	100nA (18d)	1.45uA
Preamplifier	VBiasIkrum (I)	8	I/N low I	1nA (3d)	20nA (60d)	1nA (3d)	100nA
Preamplifier	VFBK (V)	8	V	500mV (800mV)	500mV (800mV)	500mV (800mV)	1.2V
Test Pulse	VTpulseCoarse (V)	8	V	600mV	600mV	600mV	1.2V
Test Pulse	VTpulseFine (V)	14	V	600mV	600mV	600mV	1.2V
Discriminator	VBiasDiscTailNMOS (I)	8	I/N	1uA (83d)	500nA (41d)	200nA (17d)	3.1uA
Discriminator	VBiasDiscPMOS (I)	8	I/P	1.25uA (89d)	750nA (53d)	450nA (32d)	3.6uA
Discriminator	VBiasDiscTRAFF (I)	8	I/P	2uA (128d)	750nA (64d)	400nA (26d)	4uA
Discriminator	VCascDisc (V)	8	V	550mV	550mV	550mV	1.2V
Discriminator	VThreshold (V)	14	V	540mV (760mV)	540mV (760mV)	540mV (760mV)	1.2V
DAC	VBiasDAC (I)	8	I/N low I	30nA (47d)	15nA (24d)	7.5nA (12d)	160nA

Cells in the table:

1. Block : Analog circuit that is biased by the DAC.
2. DAC Name and Type : Type refers to the fact that a DAC is a Voltage (V) or a Current (I) DAC. It is recommended to bias the voltage DACs to the indicated value (by means of setting the DAC digital input code to the value that best approaches the indicated voltage value).
3. Bits : Number of bits of the DAC.
4. Flavour: For the current DACs there are three implementations "N", "N low I" and "P". The currents generated by these three DACs are adapted to the right levels in the Analog End of Column cells to match the target transistors in the pixels.
5. Fast Timing mode: Nominal operating point for fast timing applications.
6. High Flux mode: Nominal operating point for applications with high particle flux.
7. Low Power mode: Nominal operating point for applications that would like to operate at low power (with a penalty in the achievable time resolution).
8. Full scale: DAC full scale (nominal value (i.e. this value can change for technology corners)).

VBiasPreamp I

VBiasLevelShift (I)

VBiasIkrum

VBiasDiscTailNMOS

VBiasDiscPMOS

VBiasDAC

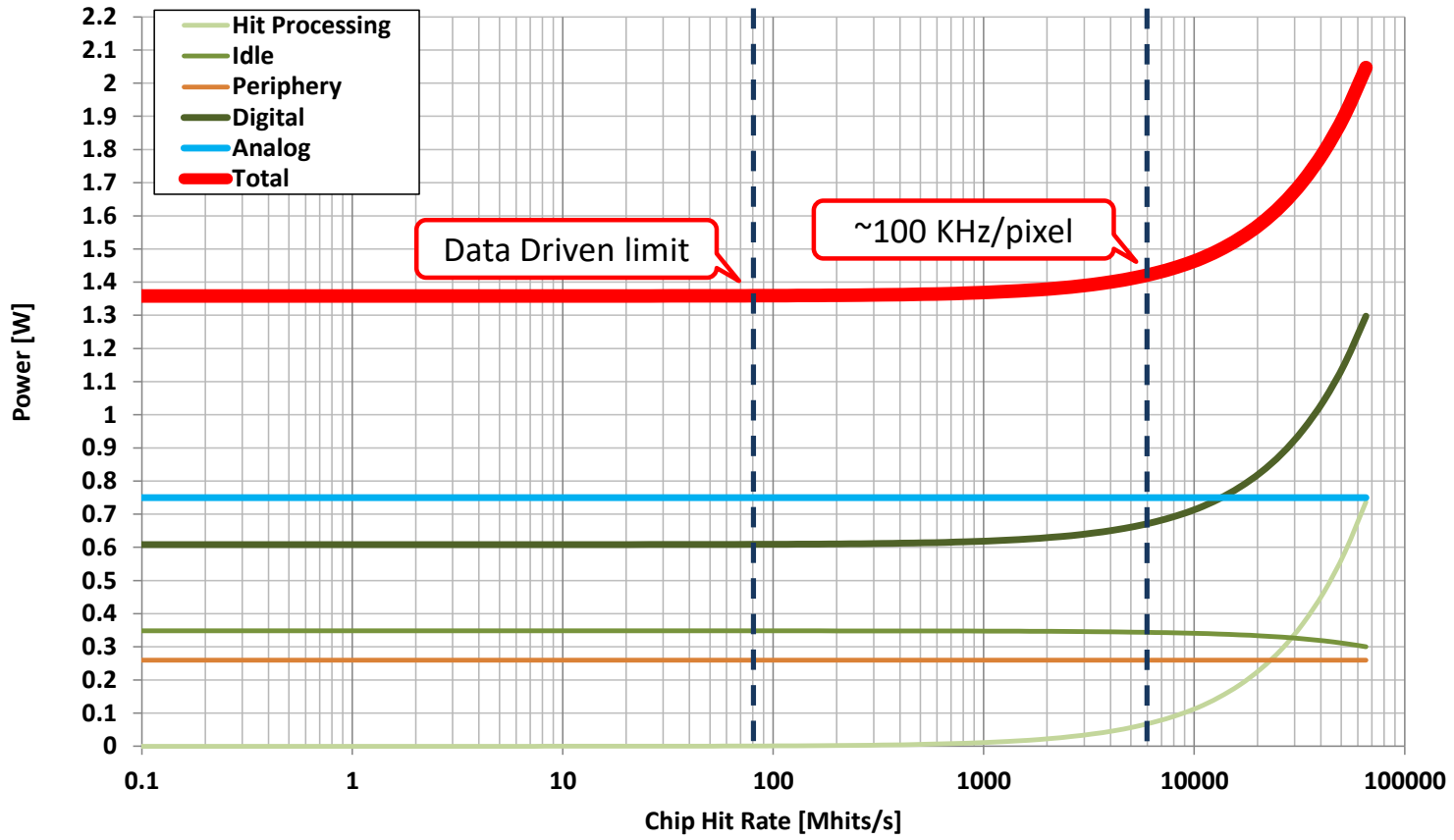
R&D: TPX3 power consumption

- The Medipix collaboration (CERN and Czech groups) carefully investigated the possibilities of the reduction of the power consumption for the TPX3 chip
- The results can be found at
  - Ref1 https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01024
  - Ref2 https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01001
- The analog power consumption can be reduced by a factor 10 [Ref1]
- If also the digital power consumption is reduced by lowering the clock frequency from 40MHz to 10 MHz, the total power consumption was show to be 0.216 W per chip [ref2]
- Standard settings uses 25 nsec bins and ‘low power’ 100 ns bins.
- So running at lower power will worsen the time resolution
- Note that this will bring down the power per endcap to 8 kW
- The low power dac settings can be found on slide 7

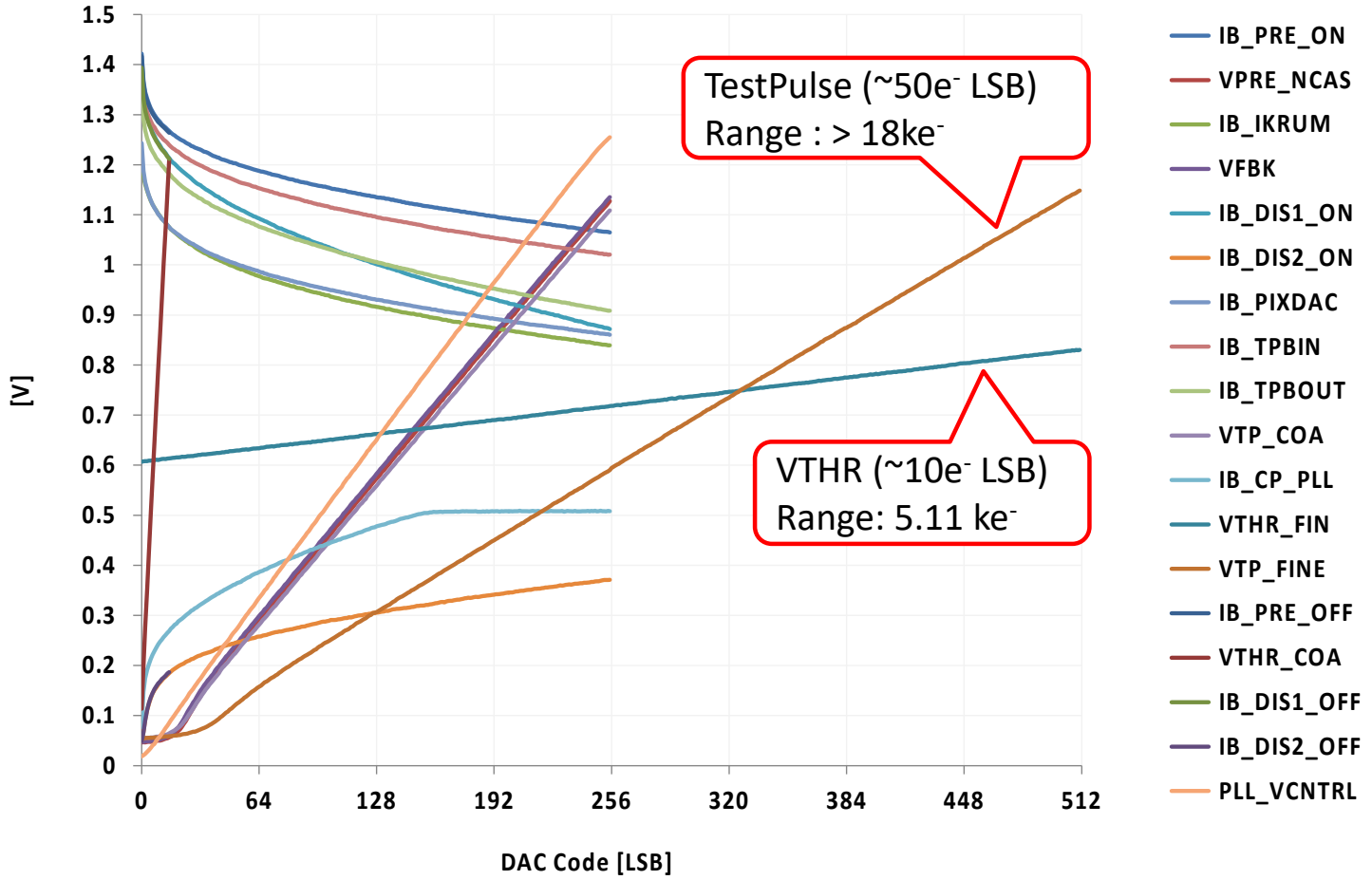
TPX3 power

Power Consumption PC Frame-based

[VDD=1.5V and VDDA=1.5V]



Timepix3 DACs



Low power dacs for TPX3

```
# TPX3 DAC settings
# lines starting with # are skipped
#
# reg_nr reg_value
#
   1      8     # TPX3_IBIAS_PREAMP_ON  [0-255]
   2      8     # TPX3_IBIAS_PREAMP_OFF [0-15]
   3    128      # TPX3_VPREAMP_NCAS     [0-255]
   4     10      # TPX3_IBIAS_IKRUM      [0-255]
   5    128      # TPX3_VFBK             [0-255]
   6    420      # TPX3_VTHRESH_FINE     [0-512]
   7      6     # TPX3_VTHRESH_COARSE   [0-15]
   8      8     # TPX3_IBIAS_DISCS1_ON  [0-255]
   9      8     # TPX3_IBIAS_DISCS1_OFF [0- 15]
  10      8      # TPX3_IBIAS_DISCS2_ON  [0-255]
  11      8      # TPX3_IBIAS_DISCS2_OFF [0-15]
  12     20      # TPX3_IBIAS_PIXELDAC   [0-255]
  13    128      # TPX3_IBIAS_TPBUFIN    [0-255]
  14    128      # TPX3_IBIAS_TPBUFOUT   [0-255]
  15    128      # TPX3_VTP_COARSE       [0-255]
  16    256      # TPX3_VTP_FINE         [0-512]
  17    128      # TPX3_IBIAS_CP_PLL     [0-255]
  18    128      # TPX3_PLL_VCNTRL       [0-255]
```

R&D: TPX3 power consumption

- For the GridPix it is possible to test the
  - Single chip new DAC settings plus lower clock frequency
  - Quad new DAC settings plus lower clock frequency
  - Module new DAC settings only

- The current design of the concentrators in the 32 chip module is based on a 40 MHz clock. This cannot be changed. So this will need a re-design of the concentrators. The concentrator combines the data streams and controls of 16 chips.
- For EIC I have prepared a set of low power dac settings

- Main conclusion is that running the TPX3 Gridpixes in low power mode reduces the power consumption for a pixel TPC to say 8 kW per endcap. Pretty good.