CALICE SiW ECAL – Status of Prototype

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On behalf of the SiW ECAL Groups in CALICE:

Virtual CALICE Collaboration Meeting – March 2021

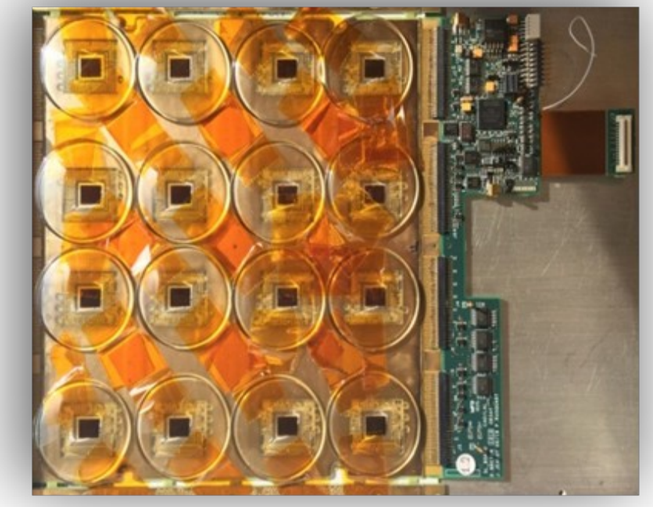
Prologue – “The FEV Zoo”

- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12

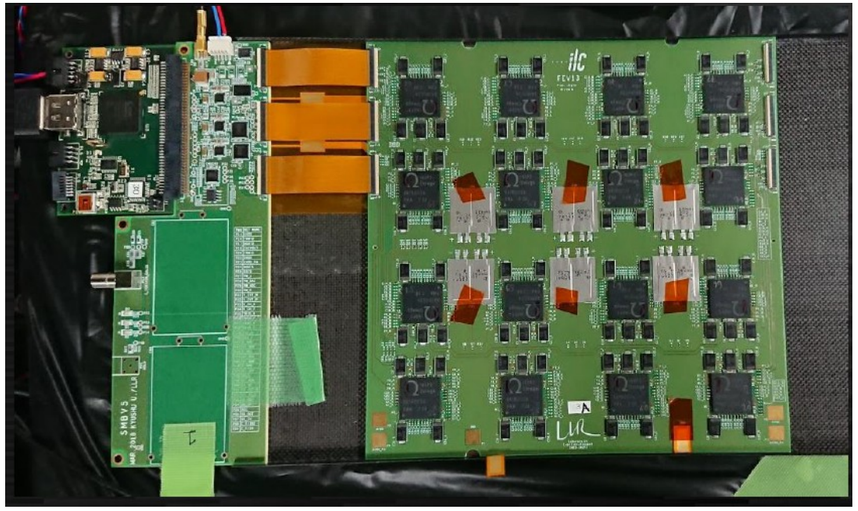
- ASICs in BGA Package
- Incremental modifications
  From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

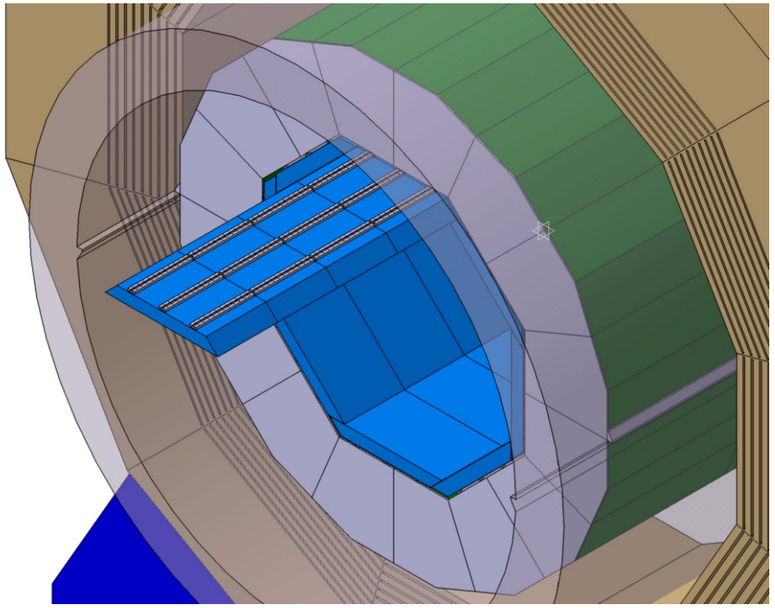
FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Silicon Tungsten electromagnetic calorimeter

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- $O(10^8)$ cells
- “No space”
=> Large integration effort

Basic Requirements:

- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

Basic Choices:

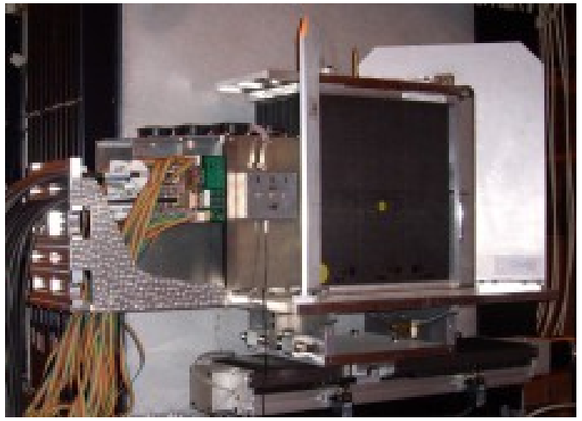
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisationRobust technology
  - Excellent signal/noise ratio: 10 as design value

- All future e+e- collider projects feature at least one detector concept with this technology
  - Decision for CMS HGCAL based on CALICE/ILD prototypes

Steps of R&D Program

Physics Prototype

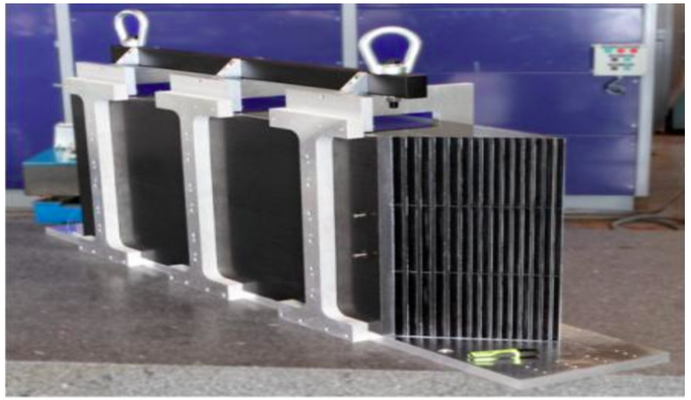
2003 - 2012



- Proof of principle of granular calorimeters
- Large scale combined beam tests

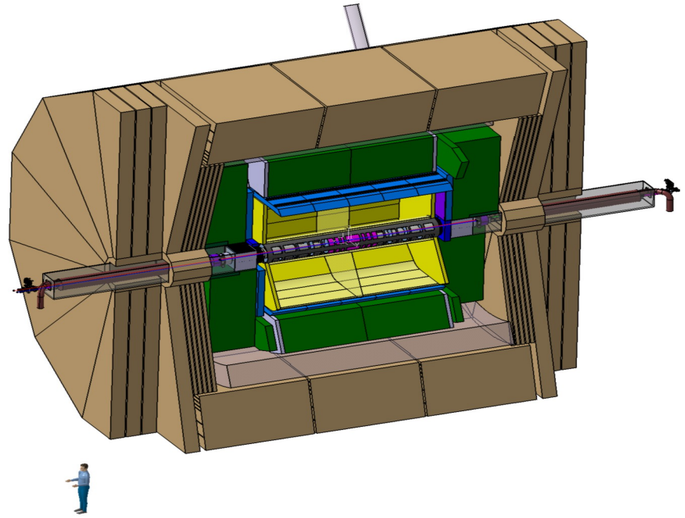
Technological Prototype

2010 - ...



- Engineering challenges
- Higher granularity
- Lower noise
  - **This talk**

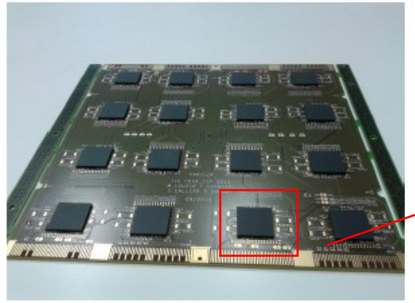
LC detector



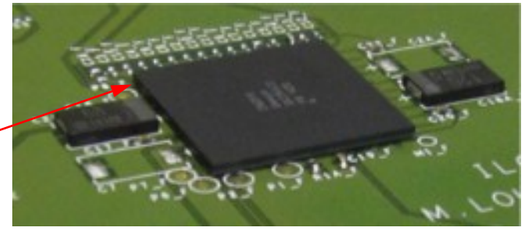
- The goal
  - Typically 10^8 calorimeter cells
- Compare:
  - ATLAS LAr ~10^5 cells
  - CMS HGCAL ~10^7 cells

SiW ECAL – Elements of (long) layer

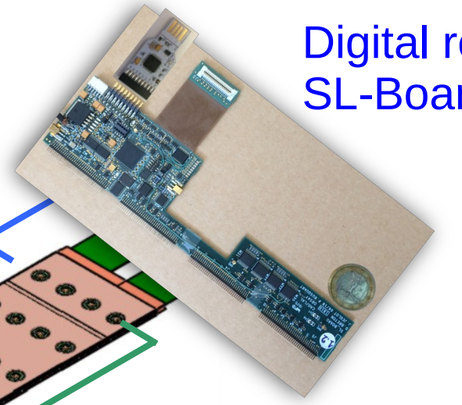
ASIC+PCB+SiWafer =ASU
Typcial size 18x18 cm²



ASIC SKIROC2a
Wire Bonded or
In BGA package



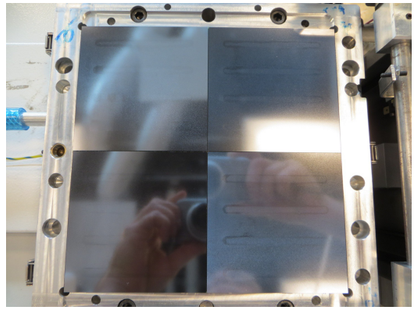
Interconnection



Digital readout
SL-Board

"end" PCB

SiWafers glued onto PCB
Pixel size
5.5x5.5 mm²



Some key numbers:
~10000 readout pads
~10000 interconnections
Power pulsing for 2ms

- This talk will report about a stack of short layers with one ASU plus readout card
  - Long layer -> See talk by J. Nanni

This talk

- First results of showers in technological SiW ECAL prototype
- Important feedback on operation of large scale system
- First tests of combined running

This talk

- First results of showers in technological SiW ECAL prototype
- Important feedback on operation of large scale system
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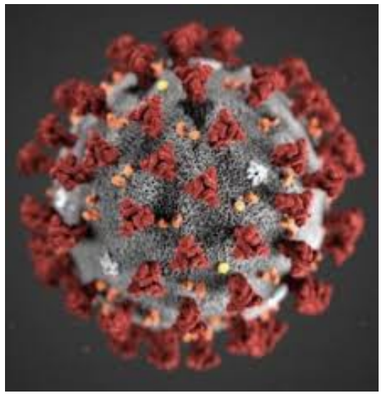
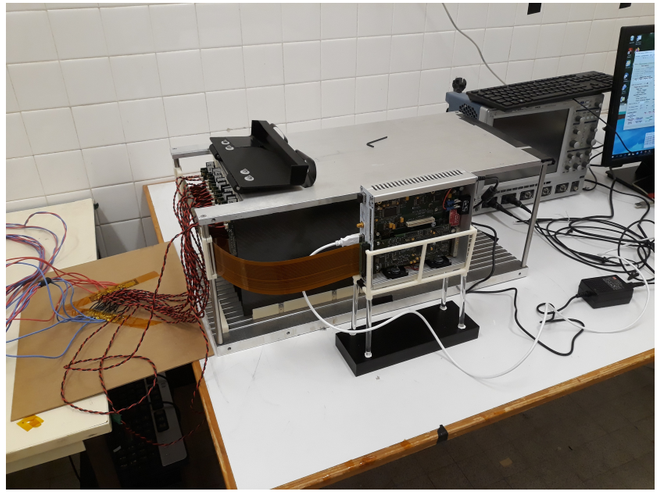
Well, No!

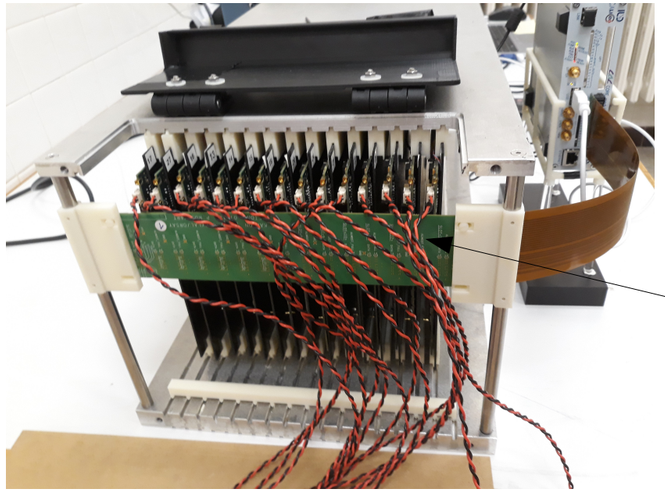


- Testbeam planned for November 2020 cancelled due to pandemic
- Testbeam planned for April 2021 also already cancelled due to pandemic
- This talk is a brief reminder and gives an overview on activities since last collaboration meeting

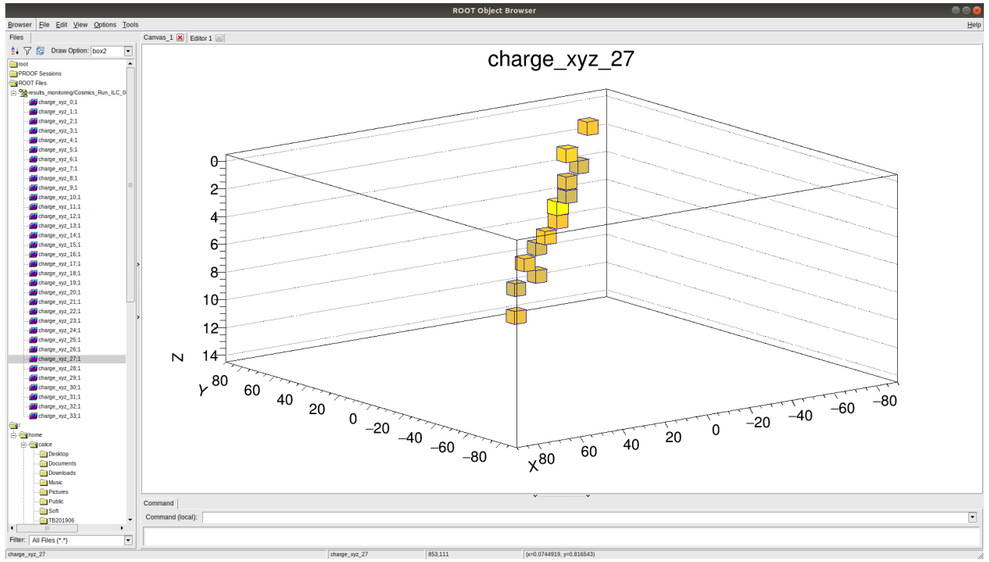
Beginning of June 2020

Running with 15 layers with 15360 channels (of which 13824 equipped with wafers !!!!)





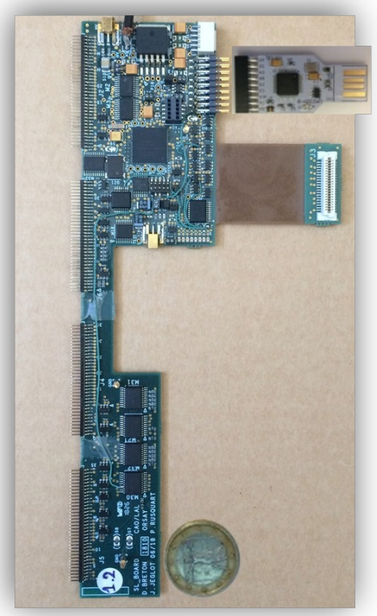
First cosmic (Adrian Irles)



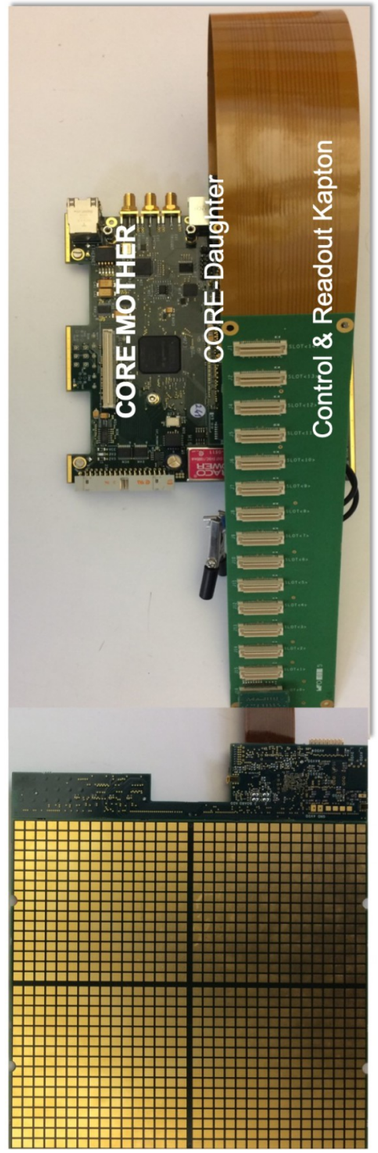
- Major breakthrough for the project
  - (Towards) the culmination of 10 years of work on Technological prototype
- Real size digital readout gives realistic impression of density at extremities of Ecal layers
- Revision and scrutinisation of setup
  - This talk

Reminder on compact readout

Current detector interface card (SL Board) and zoom into interface region



Complete readout system



- “Dead space free” granular calorimeters put tight demands on compactness
- Current developments in CALICE meet these requirements
- Can be applied/adapted wherever compactness is mandatory
- Components will/did already go through scrutiny phase in beam tests

Commissioning procedure

- A commissioning procedure has been prepared and carefully tested.
  - Based on the feature of the DAQ software of producing and reading ASCII configuration files
  - Hands-on done
  - Automatizable process (i.e. with EUDAQ)

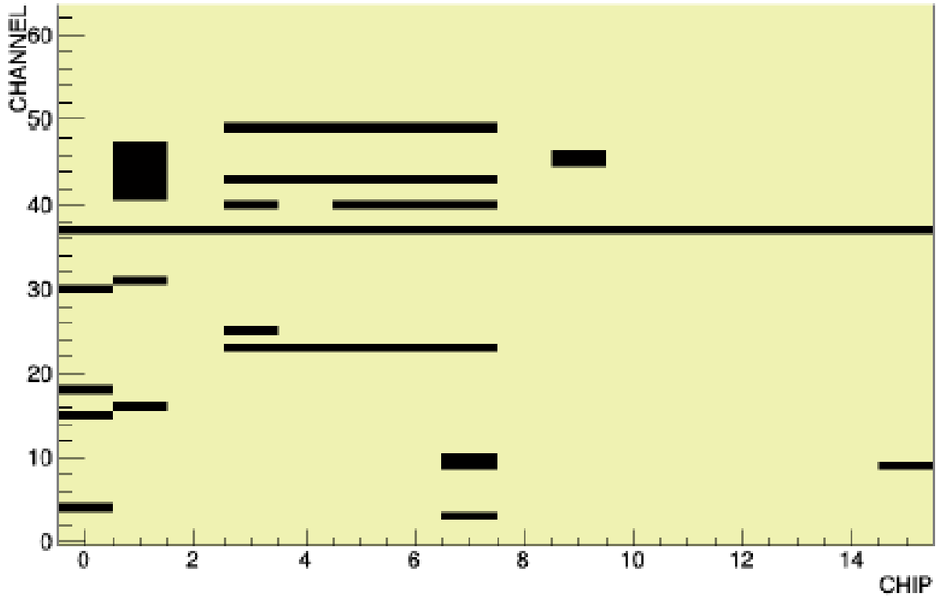
- Within ~3h we can tune up a system of 15000 cells and be ready for beam tests
  - For cosmics it takes one or two full days → since we need a much more dedicated masking procedure to cope wit the very low rates of signals.

- All material and tutorials to be uploaded here
  - https://twiki.cern.ch/twiki/bin/view/CALICE/SiWDESY202011
  - (work in progress!!)

Procedure setup by Adrian and successfully exercised by Vincent, Fabricio and R.P.

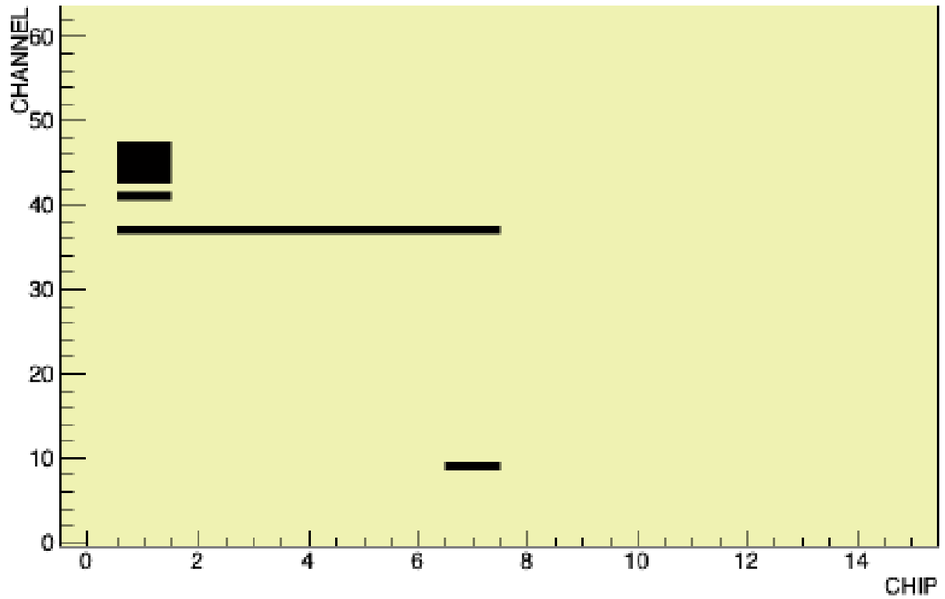
Effect of decoupling capacitances?

- 2017 configuration
  - We mask 5.7% of the cells



Standard FEV11 configuration

- Test configuration
  - Mask 1.36% of the cells

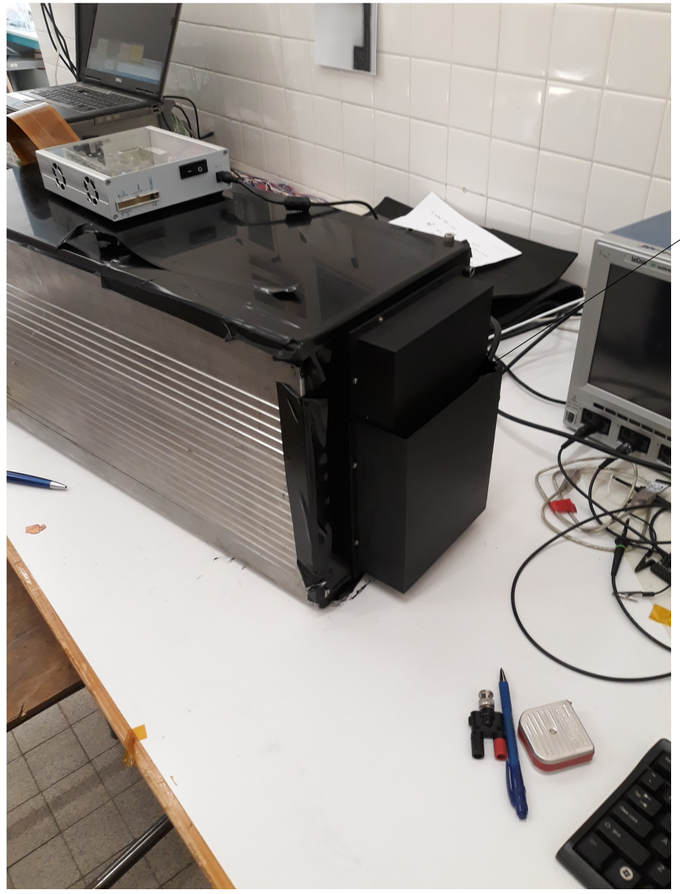


Adding 68muF to DVDD

- Remarkable improvement
  - All cards have been equipped with 68muF capacitances

All figures A. Irles

External infrastructure

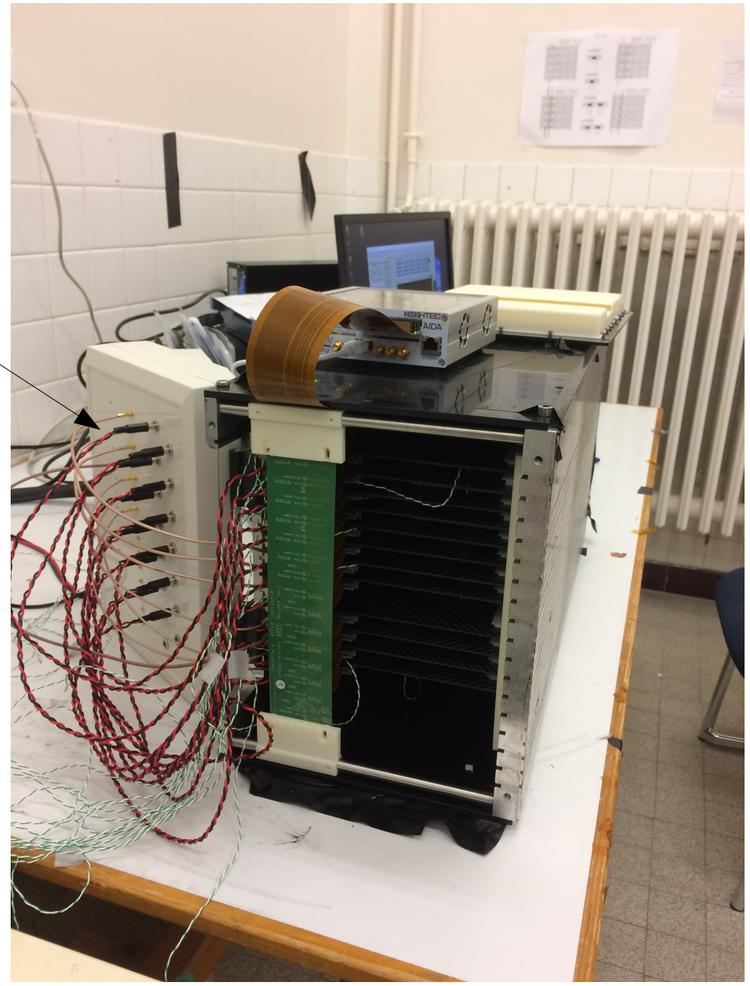


Ventilation system

- Needed since for the time being detector will be operated in continous mode
- Ensures laminar flux
- Ensures obscurity for layers

Patch panel

- New since last week
- Important piece to reduce noise sources



- With these two pieces (plus of course the readout system) the external infrastructure is complete

Recovery at slabs – Production of new slabs

- Two slabs are at LPNHE for repair work with the goal to recover them

- Two new FEV12 (Slabs 30+31) produced over Autumn/Winter 2020/21
  - Cabling at IJCLab
  - Wafers from LLR stock
  - Wafer gluing at LPNHE
  - About to be brought into operation at IJCLab

- COBs
  - Two COBs (Slabs 28+29) bonded at CERN
    (thanks to CERN team for helping with delivery and reception)
    - After return to IJCLab we have realised that the boards are bent
      - Honestly, we don't know when this occurred
      - They are operational but bending complicates the gluing of wafers
  - Have two more boards with complete metrology (see backup)
    - Will send these again for bonding to CERN and control each step
    - Out the four operational boards two will be equipped with full size wafers and two with our remaining baby wafers
  - The (thin) boards may be sensitive to temperature and humidity variation
    - The best is to get them delivered and “transform” them immediately into ASUs

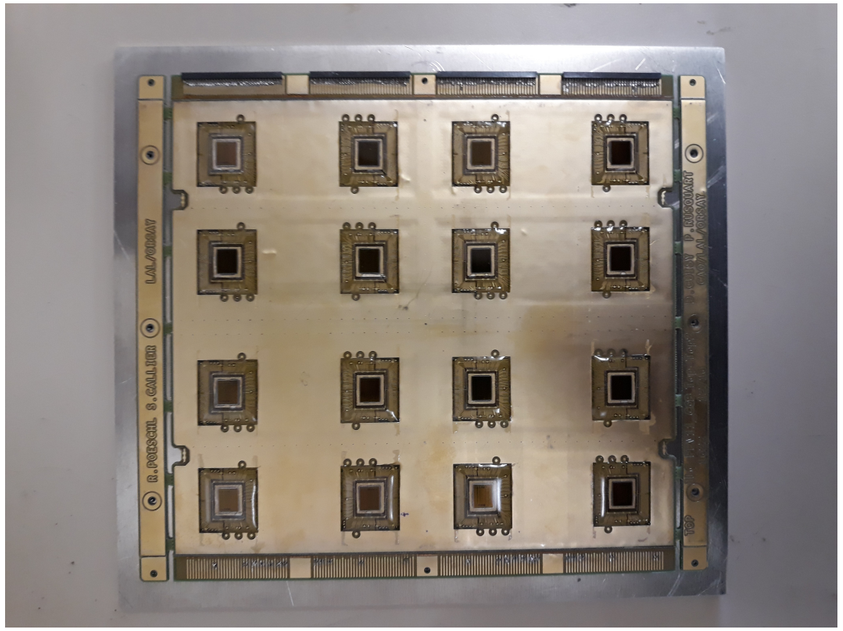
Status of Slabs – FEV10/11/12 + COBs

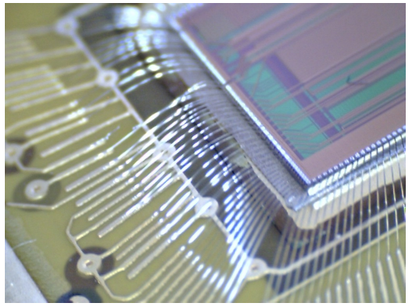
	DESY 2017		CERN 2018		
SLAB	status	calibrated cells	status	calibrated cells	Comments and 2020 status
13		0%		0%	Glue spilled in the SMBv. **Recovered for 2020**
14		0%		0%	Error in the SR return → fixed
15		0%		0%	Stopped working during the 2017 commissioning. **Being recovered for 2020 ?**
16		92%		?	Delaminated wafer
17		93%		95%	Delaminated wafer, about to be repaired at LPNHE
18		94%		?	At CERN : a pattern of lower MIP values is seen in the center of the ASU.
19		93%		93%	
20		94%		96%	
21		54%		0%	Stopped working at DESY 2018. **Fully recovered for 2020**
22		84%		87%	
23		0%		0%	FEV10 Never used → operational now.
24					FEV12 (Summer 2019)
25					FEV12 (Summer 2019)
26					Damaged COB with only one wafer
27					Damaged COB with only one wafer
28					COB : One Chip broken, operational and ready for gluing but bent
29					COB : Operational and ready for gluing but bent
30					FEV12 freshly produced in Autumn/Winter 2020/21, under test
31					FEV12 freshly produced in Autumn/Winter 2020/21, under test

Slabs < Slab23 are FEV11

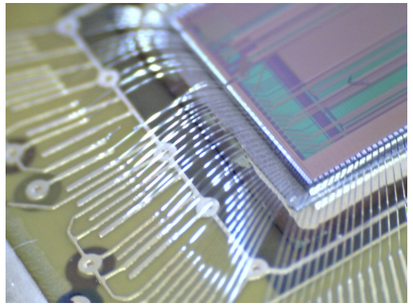
Encapsulation of FEV_COBs

ASICs on Chip-pn-Board version of PCB need to be protected





Before application of epoxy



After application of epoxy

- Successful “in house” application of Epoxy (Loctite Hysol) on several boards
- No degradation of performance observed
  - e.g. no ASIC damage, all ASICs fully operational after encapsulation
- Cooperation with Henkel/Loctite on hold due to pandemic
  - No access to French site since October
  - Plan is still to produce one board encapsulated at home and a second one at Loctite
  - NDA ready on CNRS side (thanks to services at IJCLab and CNRS-DR4)

Further News

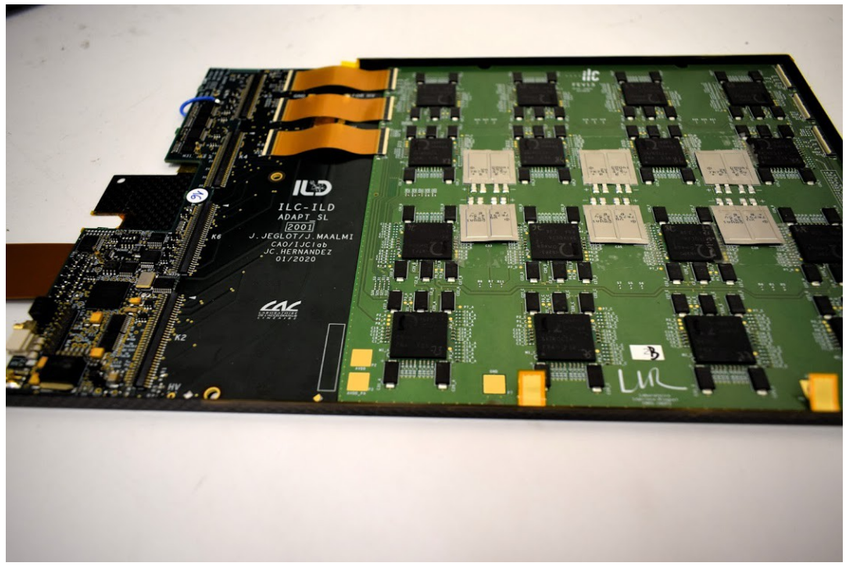
- Silicon Wafer purchase
  - Relics from 2020 budget allowed us purchasing Si-wafers at HPK
  - Organised by Kyushu
  - Quantitites: IFIC 8, IJCLab 12, LLR 22, KEK 10, Kyushu 8, Total: 60
    - + 4 wafers to Tel Aviv for tests for LUXW
  - Sensors from 6” wafers
    - No access to 8” wafers, production line blocked for CMS-HGCAL!?

- Tests at ALTO Facility IJCLab/Orsay???
  - IJCLab Director invited us to ponder possibility of tests at ALTO facility Orsay
  - Low energy electron beam (10 MeV)
  - Might be useful to test efficiently single elements
  - Plans in pre-embryonic state
  - Will check it out in coming weeks/months

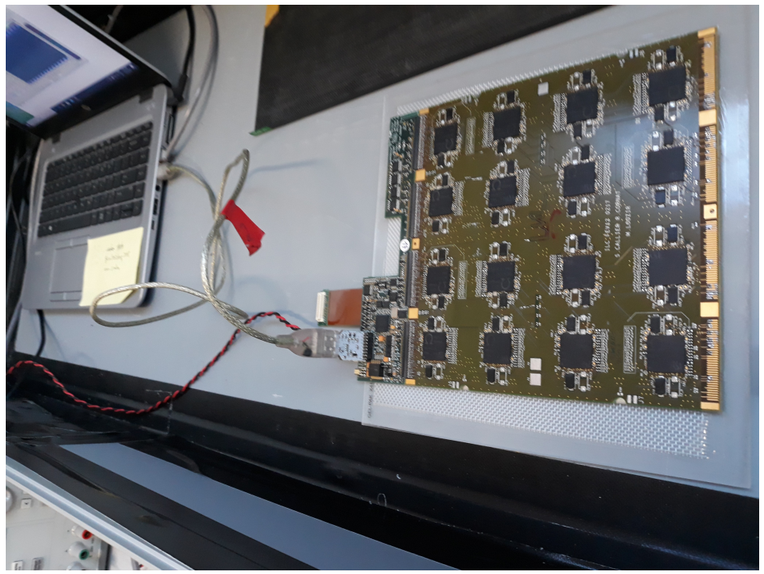
Towards beam test – Next steps

- The stack is a priori ready
  - However at the moment only 11 fully equipped layers
  - Three more during ~next week
  - COBs will complete the stack
- Completion of the stack with the goal to run with 15 ASUs/layers
  - Setup can be completed by FEV13 (See talk by Jihane in September meeting and next slide)
    - Would need (additional) mechanical housing
- Continuous commissioning in coming weeks with progressive increase of number of layers
- Setup of proper interlock and slow control systems

Interface to FEV13 and Deployment of hardware



FEV13 connected via interface card to SL-Board



New FEV12 on single slab test bench

- Interface card for allows for integration of FEV13 in stack
  - Successful technical tests in Autumn 2020
  - In total 7 FEV13 equipped with wafers are available in F and JP
- Started to deploy Hardware/software for digital readout (i.e. SL-Board and User Interface) to other Ecal groups
  - First “client” LLR
  - IFIC will follow soon (May/June, as soon as travel will be possible)
  - Deployment to Japan is planned

Summary and outlook

- SiW ECAL is waiting to be unleashed for beam test
  - First running with 15 layers in Summer 2020
  - Already three beam tests had to be cancelled due to pandemic
  - Let's cross fingers for Autumn 2021
  - Clearly the repetitive cancellations of beam tests are a penalty for our progress
  - Extremely important system test under real conditions that is lacking
  - Still, I would like to thank the extremely motivated team for continuation even under difficult circumstances
- Potential to run with 15+x layers
  - FEV13 have to be integrated into setup
- Re-commissioning in coming weeks
  - Benefit from new PhD student(s), internships and prolongation of postdoc contracts
- Software has to catch up with hardware

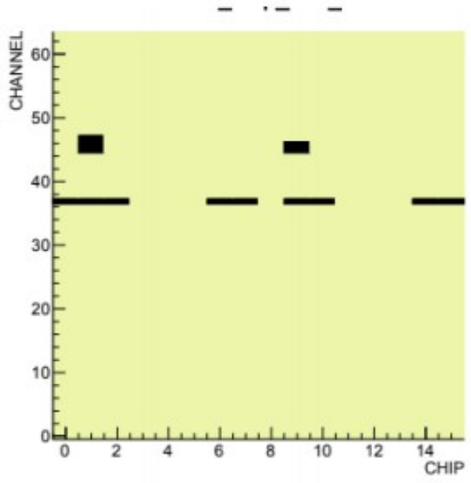
Backup

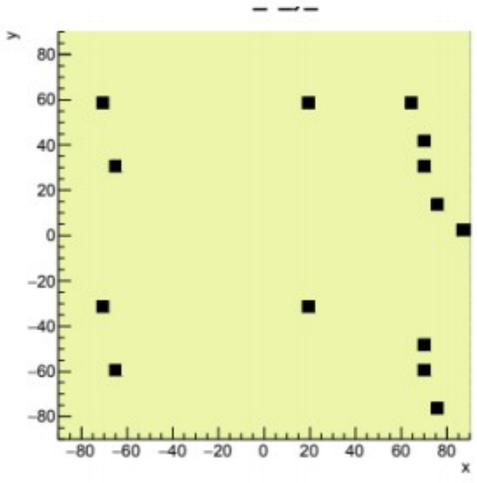
Towards beam test – Software

- Hardware preparation has to be accompanied by software development for the prototype
  - Upcoming data will go beyond pure technical tests
- Physics studies require proper implementation in simulation
  - See talk on progress by Fabricio on Friday
- Need to write proper reconstruction software
- Resuming of storing of relevant detector parameters in CALICE database
  - Need to refresh our memory on that
- Software and data analysis are clearly a point where the SiW ECAL has to make up its mind and is a nice entry point for new groups

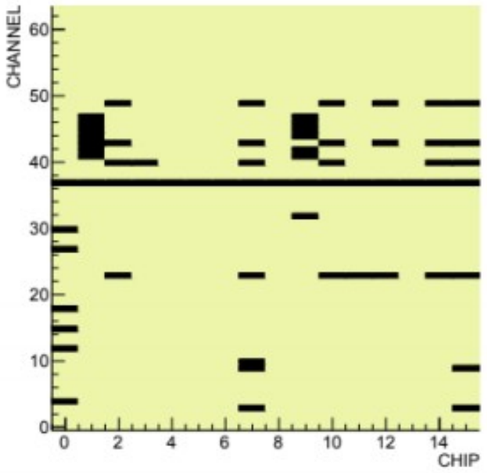
Some impressions from commissioning

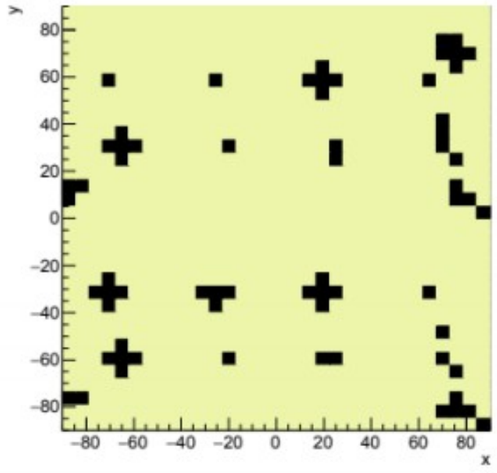
FEV10



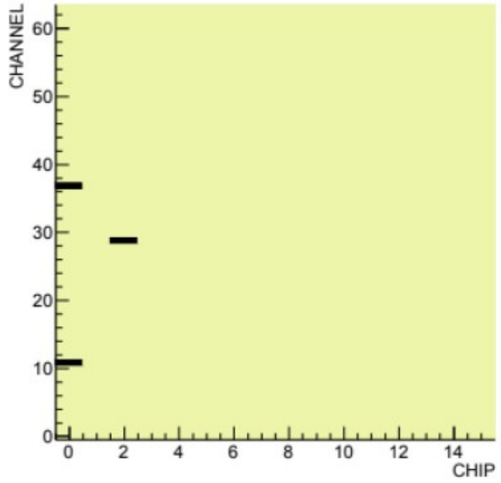


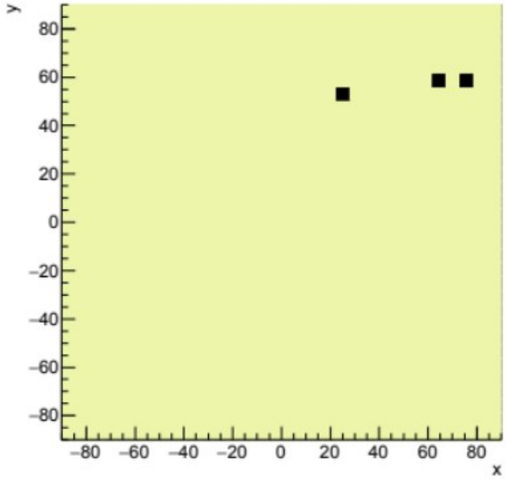
FEV11





FEV12





- Performance of FEV11 corresponds to performance in 2017 beam test
- FEV10 “surprisingly” good (different configuration of decoupling capacitances
- FEV12 looks excellent

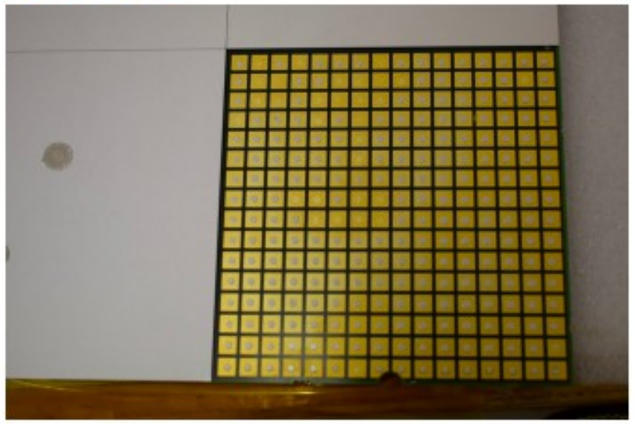
- Results are from June
- Need to be redone after manipulations over summer (see next slides)

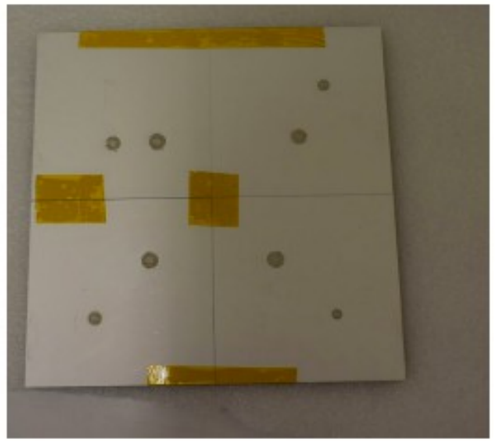
All figures A. Irles

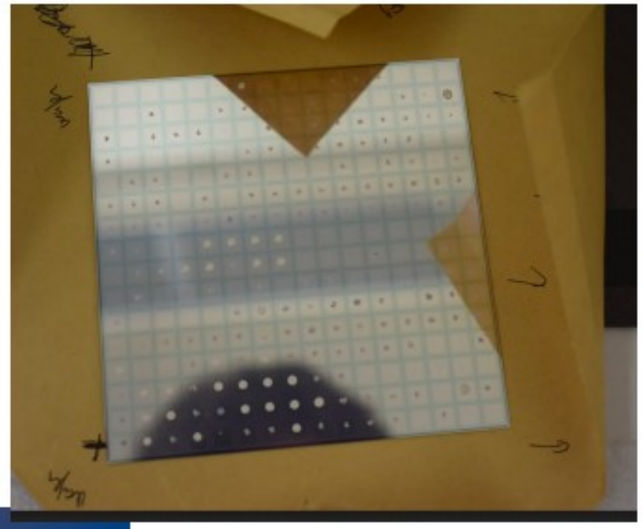
Slab 17 – Deliminated wafer

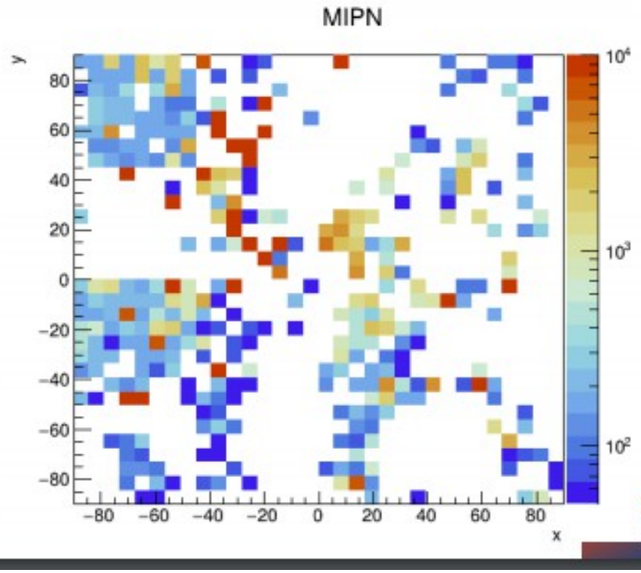
A very bad FEV11 → slab 17

- SLAB 17 (FEV11)
  - Travel Europe/Japan several times
  - Arrived to France just before the quarantine. After several days in customes it arrived to France very well packed and protected.
  - However… the wafers were simply partially dettached from the PCB. One of them was completely dettached.
- Some bricolage done trying to recover it…
  - It is not broken but only few channels are connected.

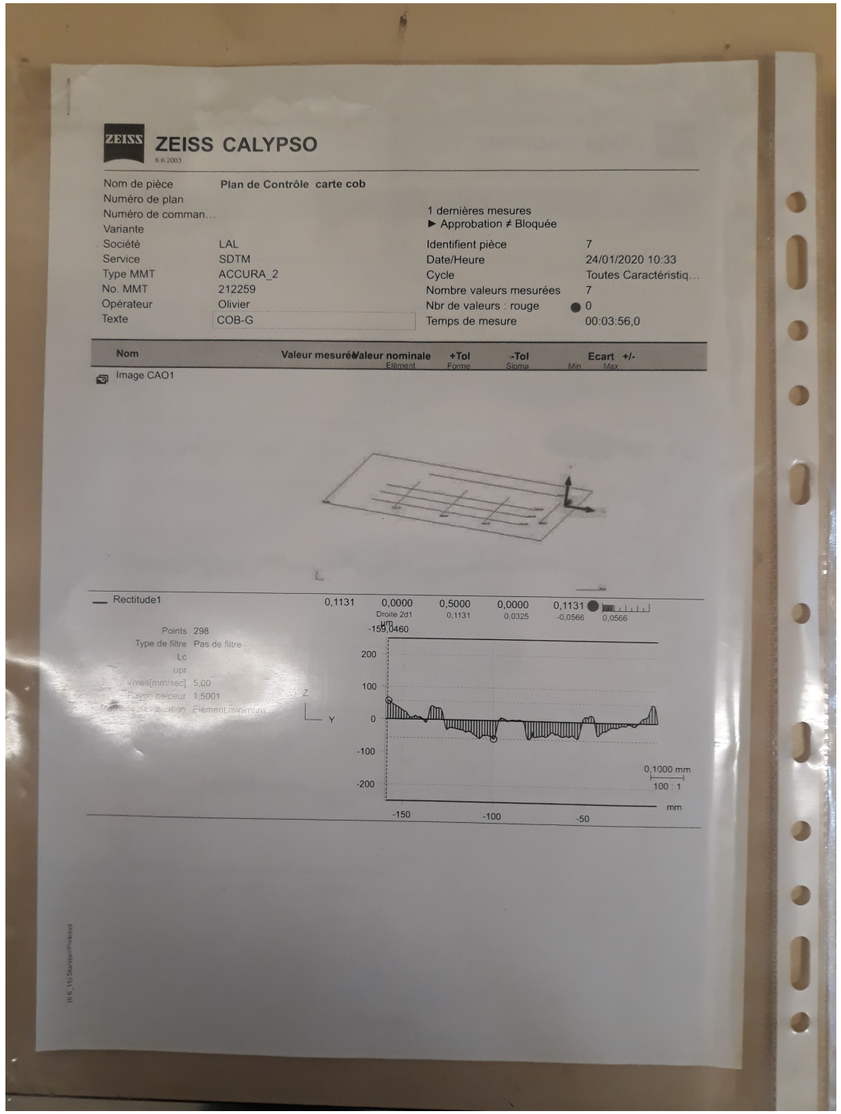








Metrology of two COBs still in stock

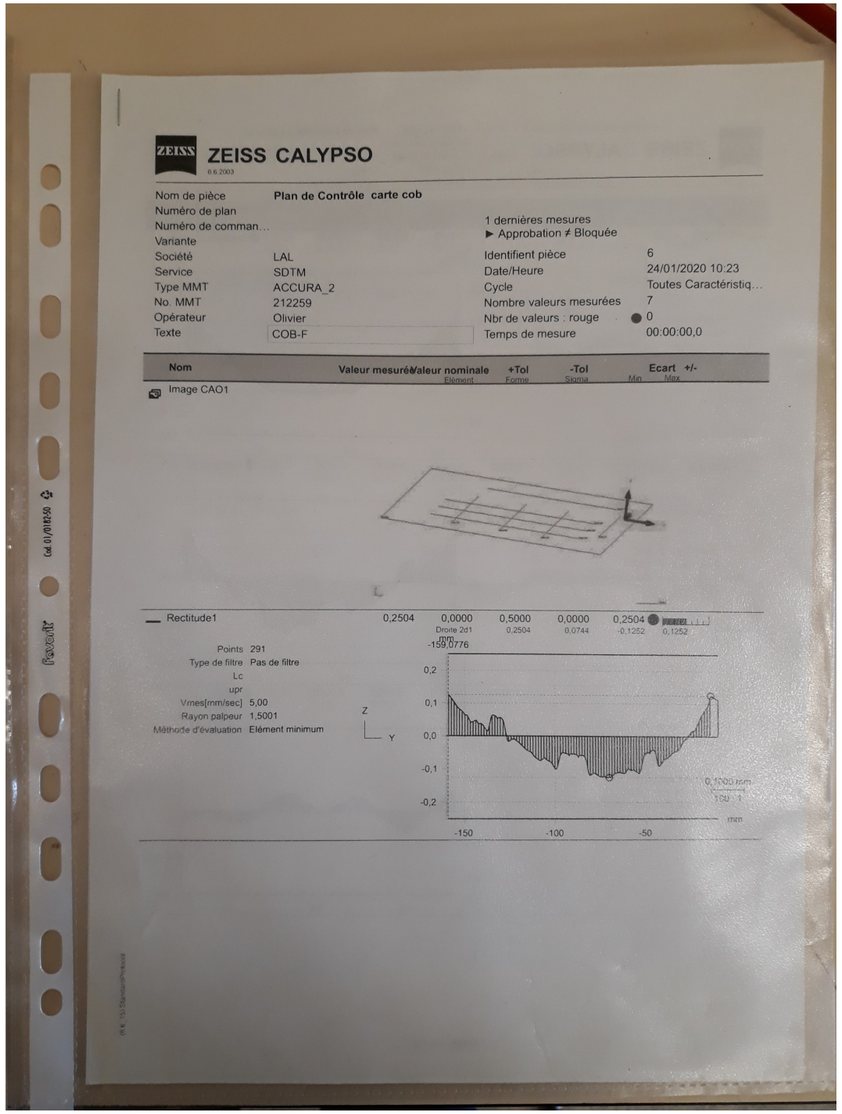


ZEISS CALYPSO
6.6.2003

Nom de pièce	Plan de Contrôle carte cob		
Numéro de plan		1 dernières mesures	
Numéro de comman…		► Approbation ≠ Bloquée	
Variante			
Société	LAL	Identifient pièce	7
Service	SDTM	Date/Heure	24/01/2020 10:33
Type MMT	ACCURA_2	Cycle	Toutes Caractéristiq…
No. MMT	212259	Nombre valeurs mesurées	7
Opérateur	Olivier	Nbr de valeurs : rouge	0
Texte	COB-G	Temps de mesure	00:03:56,0

Nom	Valeur mesurée	Valeur nominale	+Tol	-Tol	Ecart	+/-
		Elément	Forme	Sigma	Min	Max
Image CAO1						
Rectitude1	0,1131	0,0000	0,5000	0,0000	0,1131	
		Droite 2d1		0,0325	-0,0566	0,0566

Points 298
Type de filtre Pas de filtre
Lc
upr
Vmes[mm/sec] 5,00
Rayon palpeur 1,5001
Méthode d'évaluation Elément minimum



ZEISS CALYPSO
6.6.2003

Nom de pièce	Plan de Contrôle carte cob		
Numéro de plan		1 dernières mesures	
Numéro de comman…		► Approbation ≠ Bloquée	
Variante			
Société	LAL	Identifient pièce	6
Service	SDTM	Date/Heure	24/01/2020 10:23
Type MMT	ACCURA_2	Cycle	Toutes Caractéristiq…
No. MMT	212259	Nombre valeurs mesurées	7
Opérateur	Olivier	Nbr de valeurs : rouge	0
Texte	COB-F	Temps de mesure	00:00:00,0

Nom	Valeur mesurée	Valeur nominale	+Tol	-Tol	Ecart	+/-
		Elément	Forme	Sigma	Min	Max
Image CAO1						
Rectitude1	0,2504	0,0000	0,5000	0,0000	0,2504	
		Droite 2d1		0,0744	-0,1252	0,1252

Points 291
Type de filtre Pas de filtre
Lc
upr
Vmes[mm/sec] 5,00
Rayon palpeur 1,5001
Méthode d'évaluation Elément minimum